Intel® 915G/915GV/915GL/915P/ 915PL/910GL Express Chipset

Datasheet

For the Intel® 82915G/82915GV/82915GL/82910GL Graphics and Memory Controller Hub (GMCH) and the Intel® 82915P/82915PL Memory Controller Hub (MCH)

February 2005

Document Number: 301467-005

Contents

Figures

Tables

Revision History

Rev	Description	Date
-001	• Initial Release	June 2004
-002	• Added Intel® 82915GV GMCH • Minor edits throughout for clarity	September 2004
-003	• Added Intel® 82910GL GMCH	September 2004
-004	• Added Intel® 82915GL GMCH • Added Intel® 82915PL GMCH	January 2005
-005	• Minor edits throughout for clarity	February 2005

Intel® 82915G/82915GV/82915GL/ 82910GL/82915P/82915PL (G)MCH Features

- Processor Interface
  - One Intel® Pentium® 4 processor or Intel® Celeron® D processor including 775-Land package.
  - Supports Pentium 4 processor FSB interrupt delivery
  - 533 MT/s (133 MHz) FSB (82915G/82915GV/ 82915GL/82910GL/82915P/82915PL) and 800 MT/s (200 MHz) FSB (82915G/82915GV/ 82915GL/82915P/82915PL only)
  - FSB Dynamic Bus Inversion (DBI)
  - 32-bit host bus addressing for access to 4 GB of memory space
  - 12-deep In-Order Queue
  - 1-deep Defer Queue
  - GTL+ bus driver with integrated GTL termination resistors
  - Supports a Cache Line Size of 64 bytes
- System Memory
  - One or two 64-bit wide DDR/DDR2 SDRAM data channels (82915PL and 82910GL supports DDR 400 or DDR 333, 1 DIMM, 2 Channels only) (82915PL supports DDR only)
  - Bandwidth up to 8.5 GB/s (DDR/DDR2 533) in dual-channel interleaved mode.
  - Non-ECC memory only.
  - 256-Mb, 512-Mb and 1-Gb DDR/DDR2 technologies
  - Only x8, x16, DDR/DDR2 devices with four banks and also supports eight bank, 1-Gbit DDR2 devices.
  - Opportunistic refresh
  - Up to 64 simultaneously open pages (four ranks of eight bank devices* 2 channels)
  - SPD (Serial Presence Detect) scheme for DIMM detection support
  - Suspend-to-RAM support using CKE
  - Supports configurations defined in the JEDEC DDR/DDR2 DIMM specification only
- PCI Express* Graphics Interface (82915G/82915P/82915PL only)
  - One x16 PCI Express port
  - Compatible with the PCI Express Base Specification revision 1.0a
- Integrated Graphics Device (82915G/82915GV/82915GL/82910GL only)
  - Core frequency of 333 MHz
  - High-Quality 3D Setup and Render Engine
  - High-Quality Texture Engine
  - Video DVD/PC-VCR
  - 3D Graphics Rendering Enhancements
  - 2D Graphics
  - Video Overlay
  - Multiple Overlay Functionality
- Analog Display Support (82915G/82915GV/82915GL/82910GL only)
  - 400 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536@ 85 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Digital Display Support (82915G/82915GV/82915GL/82910GL only)
  - Two SDVO ports multiplexed with PCI Express Graphics Interface (82915G only)
  - 200 MHz dot clock on each 12-bit interface
  - Can combine two channels to form one larger interface (82915G only)
  - Flat panels up to 2048x1536@ 85Hz or digital CRT/HDTV at 1920x1080@ 85Hz
  - Dual Independent Display options with digital display. (82915G only)
  - Multiplexed Digital Display Channels (Supported with ADD2 Card). (82915G only)
  - Supports TMDS transmitters or TV-Out encoders
  - ADD2 card uses PCI Express Graphics x16 connector (82915G only)
- DMI Interface
  - A chip-to-chip connection interface to Intel® ICH6
  - 2 GB/s point-to-point DMI to ICH6 (1 GB/s each direction)
  - 100 MHz reference clock (shared with PCI Express Graphics Attach).
  - 32-bit downstream addressing
  - Messaging and Error Handling
- Package
  - 37.5 mm × 37.5 mm., 1210 balls, variable ball pitch

1 Introduction

The Intel® 91x Express chipset family is designed for use with the Intel® Pentium® 4 processor / Intel® Celeron® D processor (Intel® 915G/915GV/915GL/915P/915PL chipsets) or Intel® Celeron® processor (Intel® 910GL chipset) in desktop platforms. Each chipset in the family contains two components: GMCH (or MCH) for the host bridge and I/O Controller Hub 6 (ICH6) for the I/O subsystem. The 82915G GMCH is part of the 915G Express chipset, the 82915GV is part of the 915GV Express chipset, the 82915GL is part of the 915GL Express Chipset, the 82910GL is part of the 910GL Express chipset, the 82915P MCH is part of the 915P Express chipset, and the 82915PL is part of the 915PL Express chipset. The ICH6 is the sixth generation I/O Controller Hub and provides a multitude of I/O related functions. Figure 1-1 shows an example system block diagram for the 915G Express chipset, Figure 1-2 shows an example system block diagram for the 915P Express chipsets, Figure 1-3 shows an example system block diagram for the 915GV Express chipset, Figure 1-4 shows an example system block diagram for the 910GL Express chipsets, Figure 1-5 shows an example system block diagram for the 915PL Express chipsets, and Figure 1-6 shows an example system block diagram for the 915GL Express chipsets.

This document is the datasheet for the Intel® 82915G Graphics and Memory Controller Hub (GMCH), Intel® 82915GV Graphics and Memory Controller Hub (GMCH), Intel® 82915GL Graphics and Memory Controller Hub (GMCH), Intel® 82910GL Graphics and Memory Controller Hub (GMCH), Intel® 82915P Memory Controller Hub (MCH), and the Intel® 82915PL Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the (G)MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

The difference between the 82915G GMCH and 82915P MCH is that the 82915G GMCH contains an integrated graphics port (and associated SDVO and analog display ports) and the 82915P MCH does not contain these items. Both devices support PCI Express graphics. The 82915GV GMCH contains an integrated graphics port (and associated SDVO and analog display ports), but does not support PCI Express graphics. The 82915GL GMCH has the same features as the 82915GV GMCH, but only supports DDR memory. The 82915PL GMCH has the same features as the 82915P GMCH, but only supports 2 channels of DDR DIMM memory to a maximum of 1-DIMM per channel. The 82910GL GMCH supports only 533 MHz FSB, contains an integrated graphics port (and associated SDVO and analog display ports), does not support PCI Express graphics, and supports only 2 channels of DDR DIMM memory to a maximum of 1-DIMM per channel.

Note: Unless otherwise specified, the information in this document applies to the 82915G Graphics and Memory Controller Hub (GMCH), 82915GV Graphics and Memory Controller Hub (GMCH), 82915GV Graphics and Memory Controller Hub (GMCH), 82910GL Graphics and Memory Controller Hub (GMCH), 82915PL Memory Controller Hub (MCH), and the 82915P Memory Controller Hub (MCH).

Note: References in this document to PCI Express are for the 82915G, 82915P, and the 82915PL only.

Note: References in this document to the Integrated Graphics Device (IGD) are for the 82915G, 82915GV, 82915GL, and 82910GL only.

Note: References in this document to DDR2 memory are for the 82915G, 82915GV, and 82915P only.

Note: Unless otherwise specified, ICH6 refers to the Intel® 82801FB ICH6, 82801FR ICHR, 82801FW ICH6W, and 82801FRW ICH6RW I/O Controller Hub 6 components.

Figure 1-1. Intel® 915G Express Chipset System Block Diagram Example

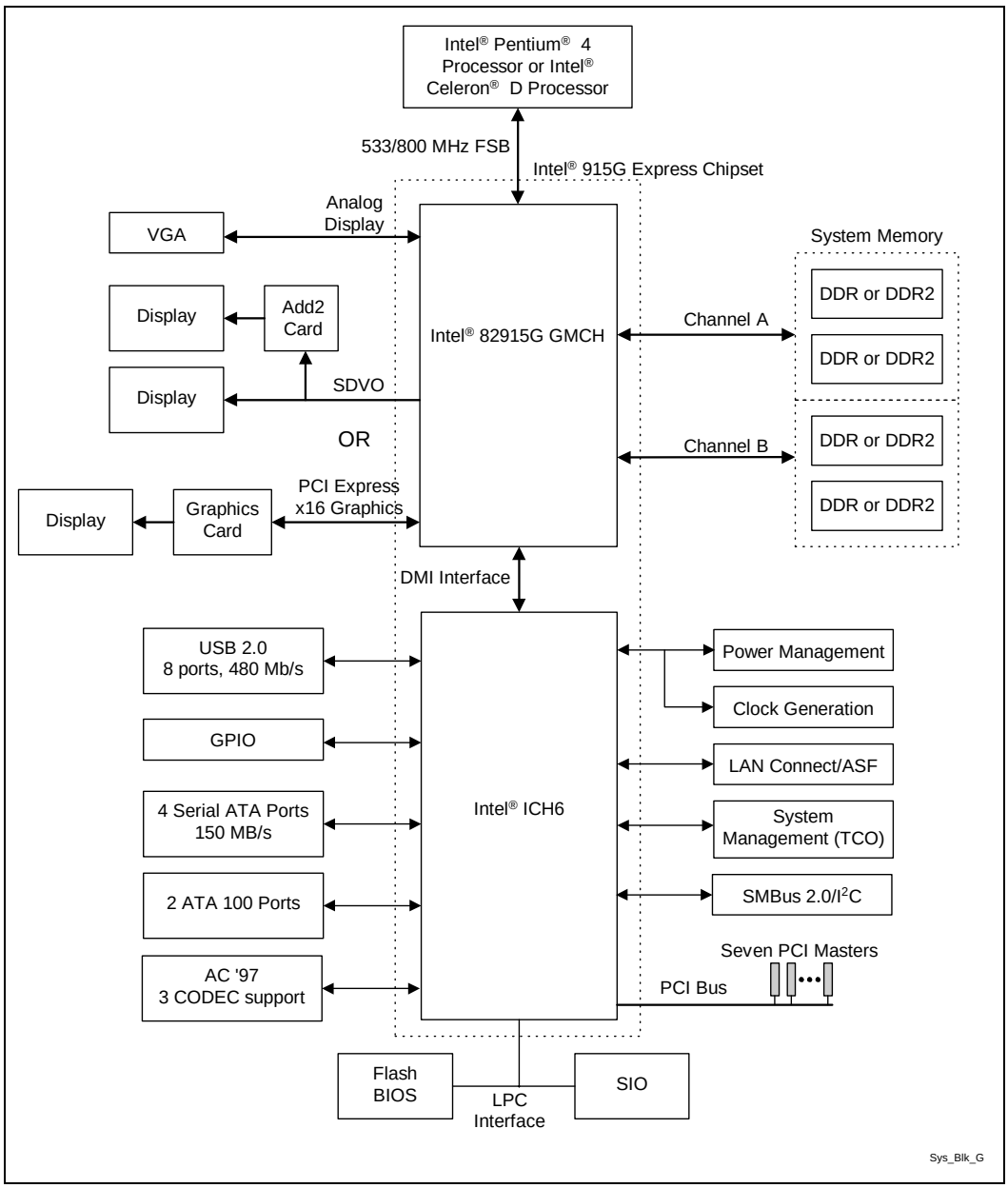


Figure 1-2. Intel® 915P Express Chipset System Block Diagram Example

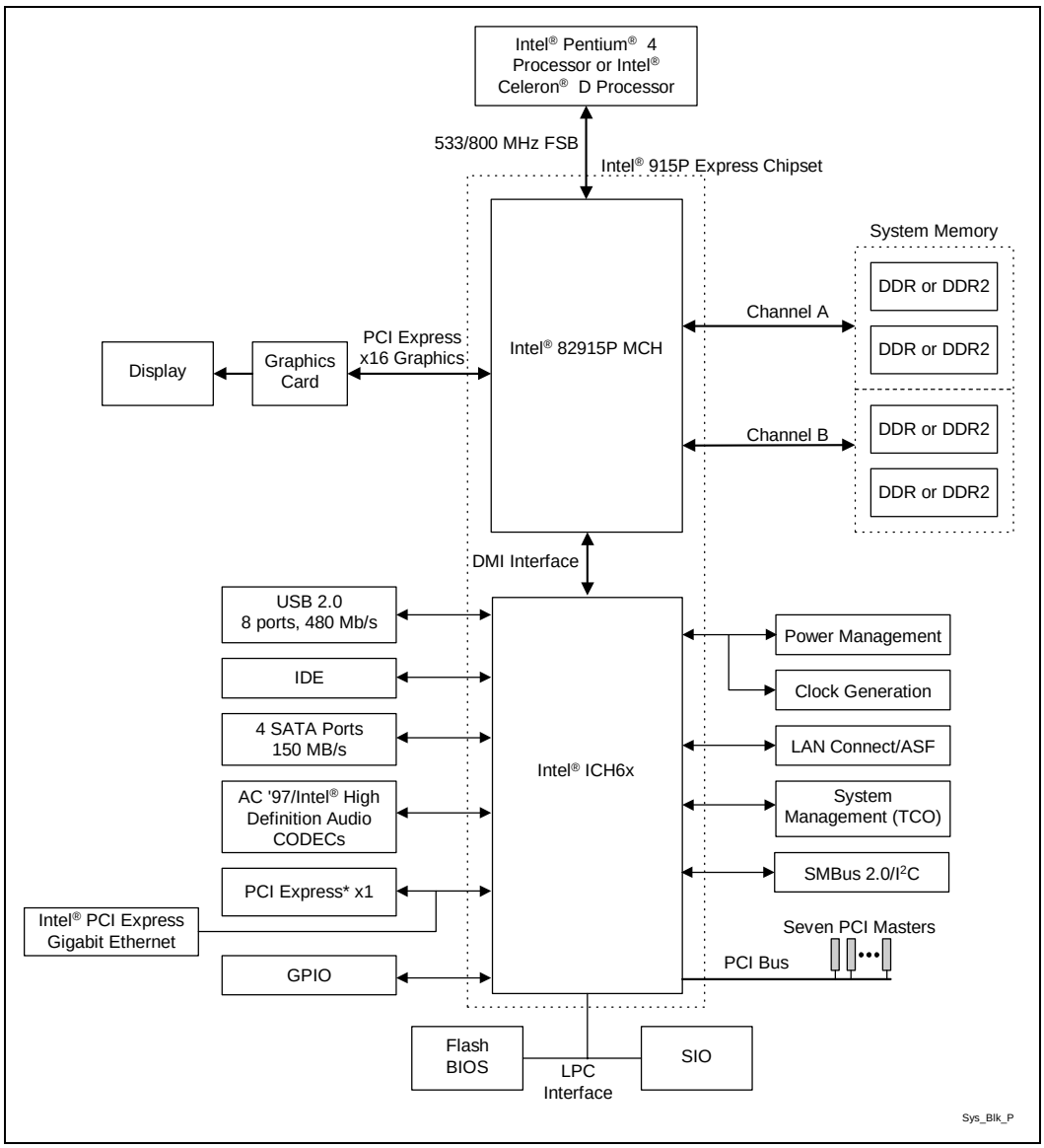


Figure 1-3. Intel® 915GV Express Chipset System Block Diagram Example

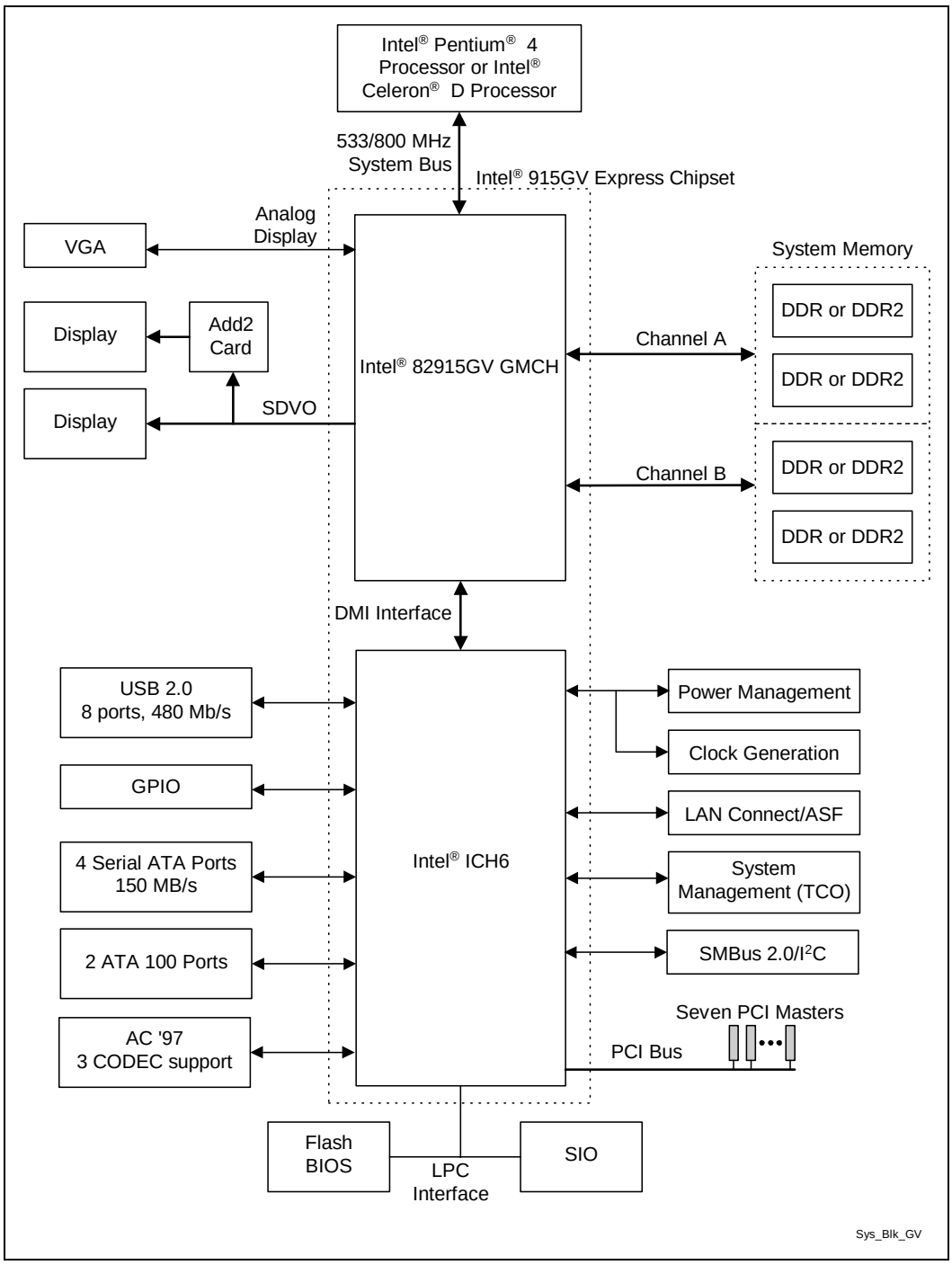


Figure 1-4. Intel® 910GL Express Chipset System Block Diagram Example

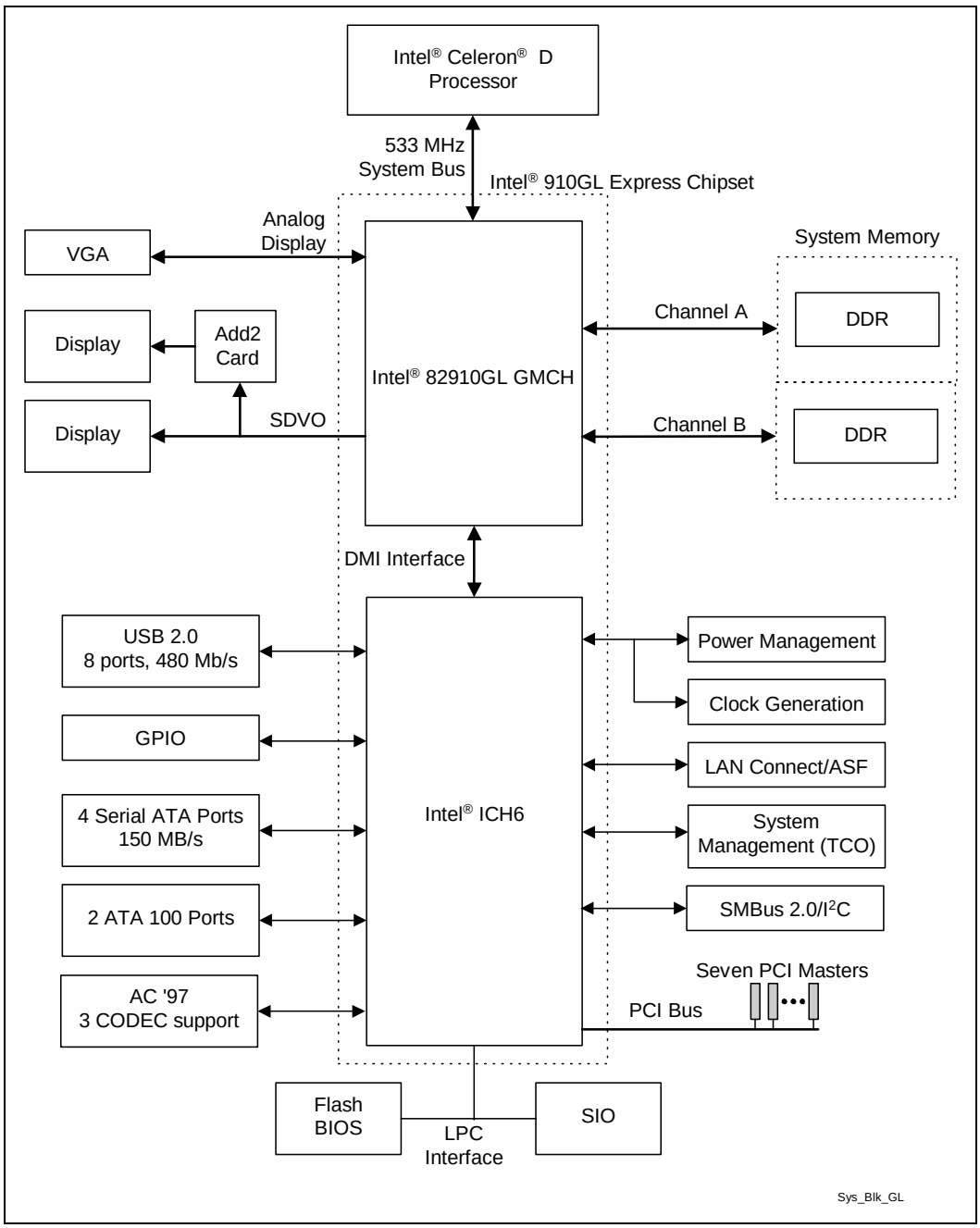


Figure 1-5. Intel® 915PL Express Chipset System Block Diagram Example

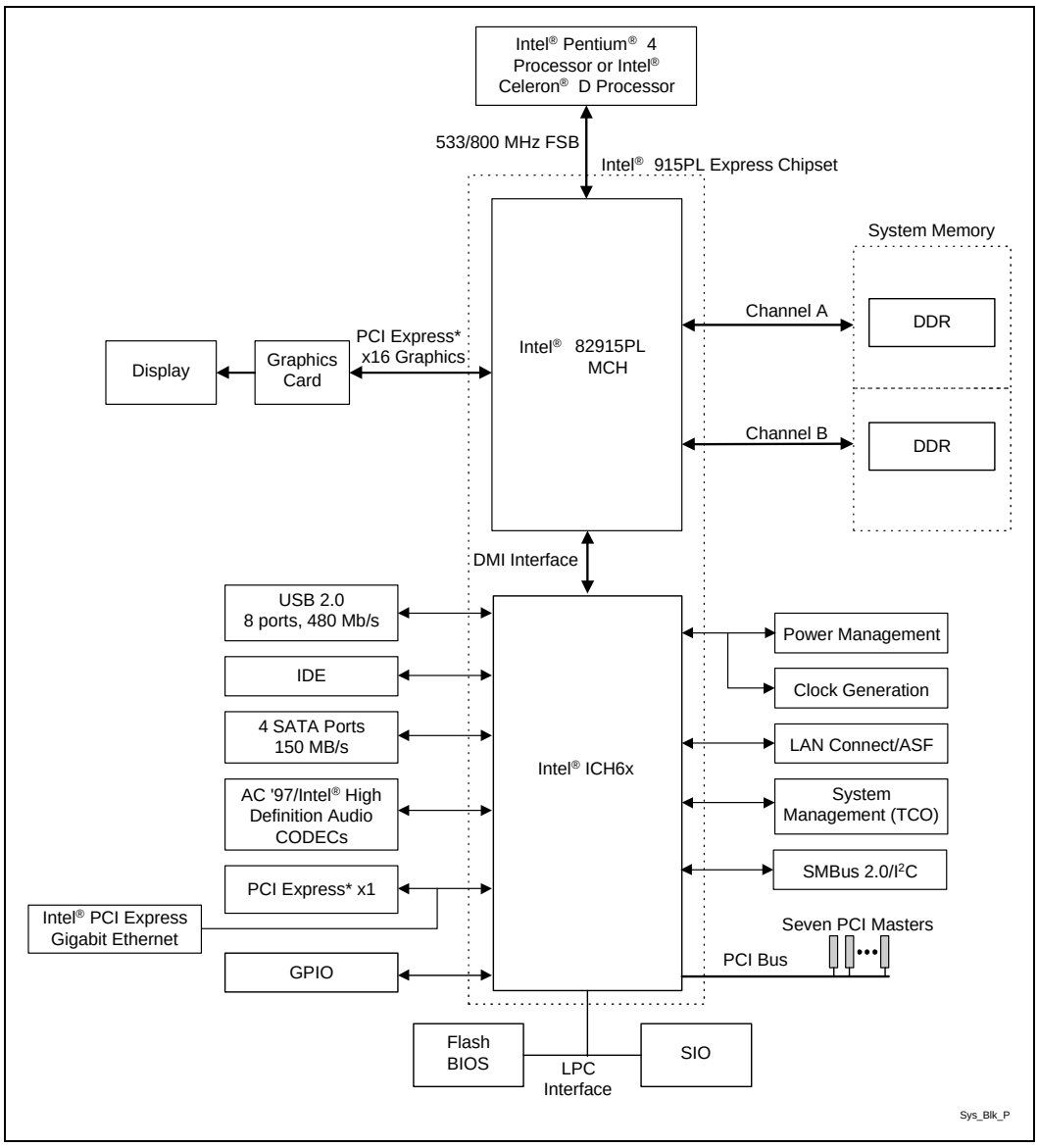
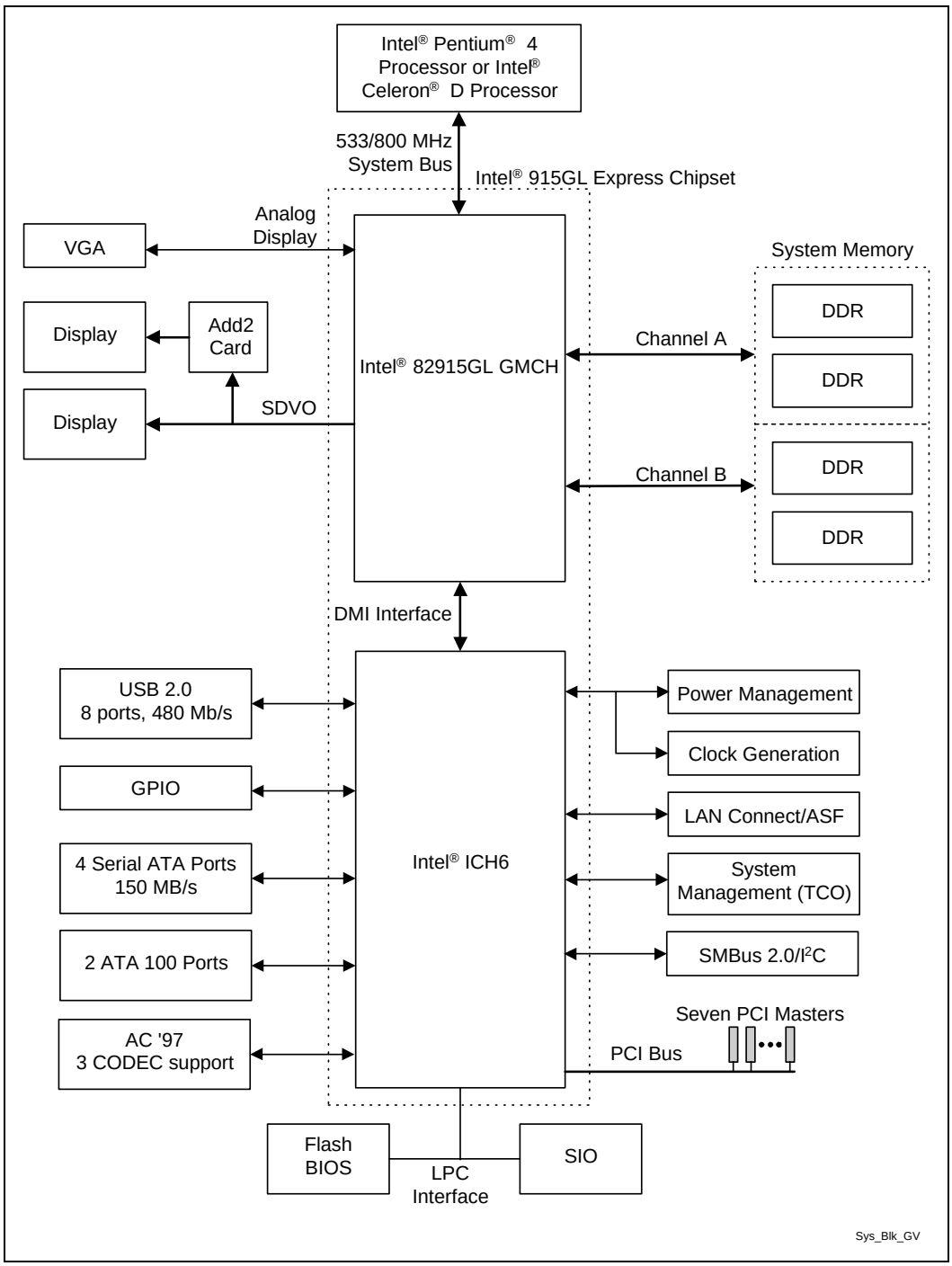


Figure 1-6. Intel® 915GL Express Chipset System Block Diagram Example



1.1 Terminology

Term	Description
ADD2 Card	Advanced Digital Display Card – **2**nd Generation. Provides digital display options for an Intel graphics controller that supports ADD2 cards. This card plugs into a x16 PCI Express connector but uses the multiplexed SDVO interface. Will **not** work with an Intel graphics controller that supports DVO and ADD cards.
Core	Core refers to the internal base logic in the (G)MCH.
CRT	Cathode Ray Tube.
DBI	Dynamic Bus Inversion.
DDR	Double Data Rate SDRAM memory technology.
DDR2	A second generation Double Data Rate SDRAM memory technology.
DMI	The Direct Media Interface is the connection between the (G)MCH and the Intel® ICH6.
DVI	Digital Video Interface. This is the specification that defines the connector and interface for digital displays.
FSB	Front Side Bus. The FSB is synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
GMCH	Graphics Memory Controller Hub component that contains the processor interface, DRAM controller, and integrated graphics device. It may also contain an x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (ICH6*) over the DMI interconnect. Throughout this document GMCH refers to the Intel® 82915G GMCH, 82915GV GMCH, 82915GL, and 82910GL, unless otherwise specified. Note that term (G)MCH is used when referring to both GMCH and MCH components.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. It transmits all ATSC HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details are available through www.HDMI.org)
Host	This term is used synonymously with processor.
INTx	An interrupt request signal where X stands for interrupts A,B,C, and D.
Intel® ICH6	Sixth generation I/O Controller Hub component that contains additional functionality compared to previous ICH6s. The Intel® I/O Controller Hub component contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the GMCH over a proprietary interconnect called DMI.
IGD	Internal Graphics Device.
LCD	Liquid Crystal Display.
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.

Term	Description
MCH	The Memory Controller Hub (MCH) component contains the processor interface and DRAM controller; however, it does not contain an internal graphics device like the GMCH. It may also contain an x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (ICH6*) and other I/O controller hubs over the DMI interconnect. Throughout this document the term MCH refers to the 82915P and 82915PL MCH. Note: (G)MCH is used when referring to both GMCH and MCH components.
MSI	Message Signaled Interrupt. A transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	Third Generation Input Output (PCI Express) Graphics Attach called PCI Express Graphics. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the GMCH to an external graphics controller is a x16 link and replaces AGP.
Primary PCI	The physical PCI bus that is driven directly by the ICH6 component. Communication between Primary PCI and the GMCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
SCI	System Control Interrupt. SCI is used in ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the Intel® 82915G GMCH, The SDVO interface is multiplexed on a portion of the x16 graphics PCI Express interface.
SDVO Device	Third party codec that uses SDVO as an input. An SDVO device may have a variety of output formats including: DVI, LVDS, HDMI, TV-Out, etc.
SERR	An indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. SMI is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
TMDS	Transition Minimized Differential Signaling. Signaling interface from Silicon Image that is used in DVI and HDMI.
TOLM	Top Of Low Memory. The highest address below 4 GB for which a processor-initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
VCO	Voltage Controlled Oscillator.
UMA	Unified Memory Architecture. UMA describes an IGD using system memory for its frame buffers.

1.2 Reference Documents

Document Title	Document Number/Location
Intel® 915G/915GV/910GL Express Chipset Thermal Design Guide	http://intel.com/design/chipsets/designex/301469.htm
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	http://developer.intel.com/design/chipsets/datashts/301473.htm
Advanced Configuration and Power Interface Specification, Version 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Version 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Version 2.3	http://www.pcisig.com/specifications
PCI Express Specification,* Version 1.0a	http://www.pcisig.com/specifications

1.3 GMCH (MCH) Overview

The (G)MCH connects to the processor as shown in Figure 1-1, Figure 1-2, Figure 1-3, Figure 1-4, Figure 1-5, and Figure 1-6. A major role of the (G)MCH in a system is to manage the flow of information between its interfaces: the processor interface (FSB), the System Memory interface (DRAM controller), the Integrated Graphics interface (82915G/82915GV/82915GL/82910GL GMCH only), the External Graphics interface via PCI Express (82915G/82915P/82915PL MCH only), and the I/O Controller Hub through the DMI interface. This includes arbitrating between the interfaces when each initiates transactions.

The (G)MCH supports one or two channels of DDR (82915G/82915GV/82915GL/82915P/82915PL/82910GL) or DDR2 (82915G/82915GV/82915P) SDRAM. The (G)MCH also supports the new PCI Express based external graphics attach. Thus, the 915G/915GV/915GL/910GL/915P and 915PL Express chipsets are NOT compatible with AGP (1X, 2X, 4X, or 8X).

To increase system performance, the (G)MCH incorporates several queues and a write cache. The (G)MCH also contains advanced desktop power management logic.

1.3.1 Host Interface

The (G)MCH is optimized for both the Pentium 4 processors in the LGA775 socket and the Celeron D processor in the FC-mPGA4 socket. The (G)MCH can use a single LGA 775 socket processor. The (G)MCH supports FSB frequency of 533/800 MT/s (133/200 MHz HCLK) using a scalable FSB Vcc_CPU (82910GL only supports 533 MT/s, 133 MHz HCLK). The (G)MCH supports the Pentium 4 processor subset of the Extended Mode Scaleable Bus Protocol. The primary enhancements over the Compatible Mode P6 bus protocol are: Source synchronous double-pumped (2) Address and Source synchronous quad-pumped (4x) Data.

The (G)MCH supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the (G)MCH

configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI, or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system memory will be snooped on the host bus.

1.3.2 System Memory Interface

The (G)MCH integrates a system memory DDR/DDR2 controller with two, 64-bit wide interfaces (82910GL, 82915PL, and 82915GL supports DDR only). Only Double Data Rate (DDR/DDR2) memory is supported; consequently, the buffers support only SSTL_2/1.8 V signal interfaces. The memory controller interface is fully configurable through a set of control registers. Features of the (G)MCH memory controller include:

- The (G)MCH System Memory Controller directly supports one or two channels of memory (each channel consisting of 64 data lines).
- Supports two memory addressing organization options:
  - The memory channels are asymmetric: "Stacked" channels are assigned addresses serially. Channel B addresses are assigned after all Channel A addresses.
  - The memory channels are interleaved: Addresses are ping-ponged between the channels after each cache line (64-B boundary).
- Available bandwidth up to:
  - 3.2 GB/s (DDR/DDR2 400) for single-channel mode
  - 6.4 GB/s in dual-channel interleaved mode assuming DDR or DDR2 400 MHz.
  - 8.5 GB/s in dual-channel interleaved mode assuming DDR2 533 MHz.
- Supports DDR memory DIMM frequencies of 333 MHz and 400 MHz or DDR2 memory DIMM frequencies of 400 MHz and 533 MHz. All DIMMs in a system must be of the same type (e.g., all DDR or all DDR2, not mixed). The speed used in all channels is the speed of the slowest DIMM in the system.
- 82910GL supports DDR memory only, DIMM frequencies of 333 MHz and 400 MHz, dual channel mode, 1-DIMM maximum per channel.
- I/O Voltage of 2.6 V for DDR, and 1.8 V for DDR2.
- Supports non-ECC memory only.
- Supports 256-Mb, 512-Mb and 1-Gb DDR/DDR2 technologies
- Supports only x8, x16, DDR/DDR2 devices with four banks and also supports eight bank, 1-Gbit DDR2 devices.
- Supports opportunistic refresh
- In dual channel mode the (G)MCH supports 64 simultaneously open pages (four ranks of eight bank devices* 2 channels)
- Supports Partial Writes to memory using Data Mask (DM) signals.
- Supports page sizes of 4 KB, 8 KB and 16 KB.
- Supports a burst length of 8 for single-channel and dual-channel interleaved and asymmetric operating modes.
- Supports unbuffered DIMMs.
- SPD (Serial Presence Detect) scheme for DIMM detection support
- Suspend-to-RAM support using CKE
- Supports configurations defined in the JEDEC DDR/DDR2 DIMM specification only

By using 256-Mb technology, the smallest memory capacity possible is 128 MB, assuming single-channel mode. (16M rows * 16b/(row*device) * 4 devices/DIMM-side * 1 DIMM-side/channel * 1 channel *1B/8b = 128 MB). By using 1-Gb technology in dual-channel interleaved mode, the largest memory capacity possible is 8 GB. (128M rows * 8b/(row*device) * 8 devices/DIMM-side * 4 DIMM-sides/channel * 2 channels * 1B/8b * 1G/1024M = 8 GB). This exceeds a 32-bit address limit of 4 GB. In a 32-bit system, only the first 4 GB of memory will be accessible.

The (G)MCH supports a memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered either by on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the (G)MCH and ICH6. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH6 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH6 and (G)MCH). Features of the DMI include:

- A chip-to-chip connection interface to ICH6
- 2 GB/s point-to-point DMI to ICH6 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express Graphics Attach).
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined “End Of Interrupt” broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.3.4 PCI Express* Graphics Interface (Intel® 82915G/82915P/ and 82915PL Only)

The (G)MCH (82915G, 82915P, and 82915PL only) contains a 16-lane (x16) PCI Express port intended for an external PCI Express graphics card. The PCI Express port is compatible with the *PCI Express Base Specification* revision 1.0a. The x16 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical bandwidth of 4 Gb/s each direction. The 82915G GMCH multiplexes the PCI Express interface with two Intel® SDVO ports.

Features of the PCI Express Interface include:

- One x16 PCI Express port intended for graphics attach, compatible with the PCI Express Base Specification revision 1.0a.
- Theoretical PCI Express transfer rate of 2.5 Gb/s.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a theoretical bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when (1)x16.
- PCI Express Graphics Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports “static” lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX15->TX0, RX15->RX0). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.

1.3.5 Integrated Graphics (Intel® 82915G/82915GV/82910GL/82915GL GMCH Only)

The 82915G/82915GV/82910GL/915GL GMCH provides an integrated graphics device (IGD) delivering cost competitive 3D, 2D and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, BLT and Stretch BLT operations, motion compensation, overlay, and display control. The GMCH’s video engines support video conferencing and other video applications. The GMCH does not support a dedicated local graphics memory interface, it may only be used in a UMA configuration. The GMCH also has the capability to support external graphics accelerators via the PCI Express Graphics port but cannot work concurrently with the integrated graphics devce. High bandwidth access to data is provided through the system memory port. The GMCH also provides 3D hardware acceleration for block level transfers of data (BLTs). 2D BLTs are considered a special case of 3D transfers and use the 3D acceleration. The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces processor load, and thus improves performance.

GMCH graphics support includes:

- Core Frequency of 333 MHz
- High Quality 3D Setup and Render Engine
  - —Setup matching processor geometry delivery rates
  - —Triangle lists, strips and fans
  - —Indexed vertex and flexible vertex formats
  - —Vertex cache
  - —Pixel accurate fast scissoring and clipping operation
  - —Backface culling
  - —Supports D3D and OpenGL pixelization rules
  - —Anti-aliased lines
  - —Sprite points
  - —Zone Rendering Technology 3
  - —Shadow maps
  - —Double-sided stencil
- High-Quality Texture Engine
  - —533 MegaTexel/Sec Performance – 266 Mpixel/Sec fill rate up to 2 bilinear textures
  - —Hardware Pixel Shader 2.0
  - —Per-pixel perspective corrected texture mapping
  - —2/10/10/10 texture format
  - —Bi-cubic filtering
  - —Single-pass quad texture compositing
  - —Enhanced texture blending functions
  - —12 levels of detail mip map sizes from 1x1 to 2Kx2K
  - —All texture formats including 32-bit RGBA and 8-bit palettes
  - —Alpha and luminance maps
  - —Texture color-keying/chromakeying
  - —Bilinear, trilinear and anisotropic mip-mapped filtering
  - —Cubic environment reflection mapping
  - —Embossed and DOT3 bump-mapping
  - —DXTn and FXT1 texture decompression
  - —Non-power of 2 texture
  - —Render to texture
- Video DVD/PC-VCR
  - —H/W Motion Compensation for MPEG2
  - —Dynamic Bob and Weave Support for Video Streams
  - —Source Resolution up to 1920x1080 with 2 vertical taps
  - —Software DVD At 30 fps, Full Screen
  - —Supports 720x480 DVD Quality Encoding at low processor Utilization for PC-VCR or home
  - —movie recording and editing
- 3D Graphics Rendering Enhancements
  - —1.3 Dual Texture GigaPixel/Sec Fill Rate
  - —Flat and Gouraud Shading
  - —Color Alpha Blending for Transparency
  - —Vertex and Programmable Pixel Fog and Atmospheric Effects
  - —Color Specular Lighting
  - —Z Bias Support
  - —Dithering
  - —Anti-Aliased Lines
  - —16- and 24-bit Z Buffering
  - —8-bit Stencil Buffering
  - —Double and Triple Render Buffer Support
  - —16- and 32-bit Color
  - —Destination Alpha
  - —Maximum 3D Resolution Supported: 1600x1200x32@85Hz
  - —Fast Clear Support
- 2D Graphics
  - —Optimized 256-bit BLT Engine
  - —Alpha Stretch Blitter
  - —Anti-aliased Lines
  - —32-bit Alpha Blended Cursor
  - —Color Space Conversion
  - —Programmable 3-Color Transparent Cursor
  - —8-, 16- and 32-bit Color
  - —ROP Support
- Video Overlay
  - —Advanced Deinterlacing
  - —Process Amplifier Color Control
  - —Single High Quality Scalable Overlay
- Multiple Overlay Functionality provided via Stretch Blitter (PIP, Video Conferencing, etc.)
  - —5-tap Horizontal, 2-tap Vertical Filtered Scaling
  - —Independent Gamma Correction
  - —Independent Brightness/Contrast/Saturation
  - —Independent Tint/Hue Support
  - —Destination Color-keying
  - —Source Chroma-keying
  - —Maximum Source Resolution: 720x480x32
  - —Maximum Overlay Display Resolution: 2048x1536x32
  - —Video Mixer Render (VMR)

1.3.6 Analog and Intel® SDVO Displays (Intel® 82915G/82915GV/82910GL/82915GL GMCH Only)

The GMCH provides interfaces to a progressive scan analog monitor and two SDVO ports (multiplexed with PCI Express x16 Graphics Port signals) capable of driving an ADD2 card. The digital display channels are capable of driving a variety of SDVO devices (e.g., TMDS, TV-Out). Note that SDVO only works with the Integrated Graphics Device (IGD). The GMCH provides two SDVO ports that are capable of driving up to a 200 MHz pixel clock each.

The GMCH SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data. Alternatively, the SDVO ports can combine to support dual channel devices, supporting higher resolutions and refresh rates. The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH Supports Hot-Plug and Display for PCI Express* x16 Graphics. This is not supported for ADD2 cards.

1.3.7 System Interrupts

The (G)MCH interrupt support includes:

- Supports both 8259 and Pentium 4 processor FSB interrupt delivery mechanisms.
- Supports interrupts signaled as upstream Memory Writes from PCI Express and DMI
  - MSIs routed directly to FSB
  - From I/OxAPICs

1.3.8 (G)MCH Clocking

The differential FSB clock (HCLKP/HCLKN) can be set to either 133 MHz or 200 MHz (82915G/82915GV/82915GL/82915P/82915PL only). This supports FSB transfer rates of 533 MT/s and 800 MT/s (82915G/82915GV/82915GL/82915P/82915PL only). The Host PLL generates 2X, 4X, and 8X versions of the host clock for internal optimizations. The (G)MCH core clock is synchronized to the host clock.

The internal and external memory clocks of 133 MHz and 200 MHz are generated from one of two (G)MCH PLLs that use the host clock as a reference. This includes 2X and 4X for internal optimizations.

For the 82915G/82915P/82915PL (G)MCH, the PCI Express core clock of 250 MHz is generated from a separate PCI Express PLL. This clock uses the fixed 100 MHz Serial Reference Clock (GCLKP/GCLKN) for reference.

For the 82915G/82915GV/82915GL/82910GL GMCH, display timings are generated from display PLLs that use a 96 MHz differential non-spread spectrum clock as a reference. Display PLLs can also use the SDVO_TVCLKIN[+/-] from an SDVO device as a reference.

All of the above mentioned clocks are capable of tolerating Spread Spectrum clocking as defined in the Clock Generator specification. Host, Memory, and PCI Express* x16 Graphics PLLs, and all associated internal clocks are disabled until PWROK is asserted.

1.3.9 Power Management

(G)MCH Power Management support includes:

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1-MB TSEG from the Base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Rev 1.0 compatible power management
- Supports processor states: C0, C1, C2, C3, and C4
- Supports System states: S0, S1, S3, S4, and S5
- Supports processor Thermal Management 2 (TM2)
- Microsoft Windows NT* Hardware Design Guide v1.0 compliant

§

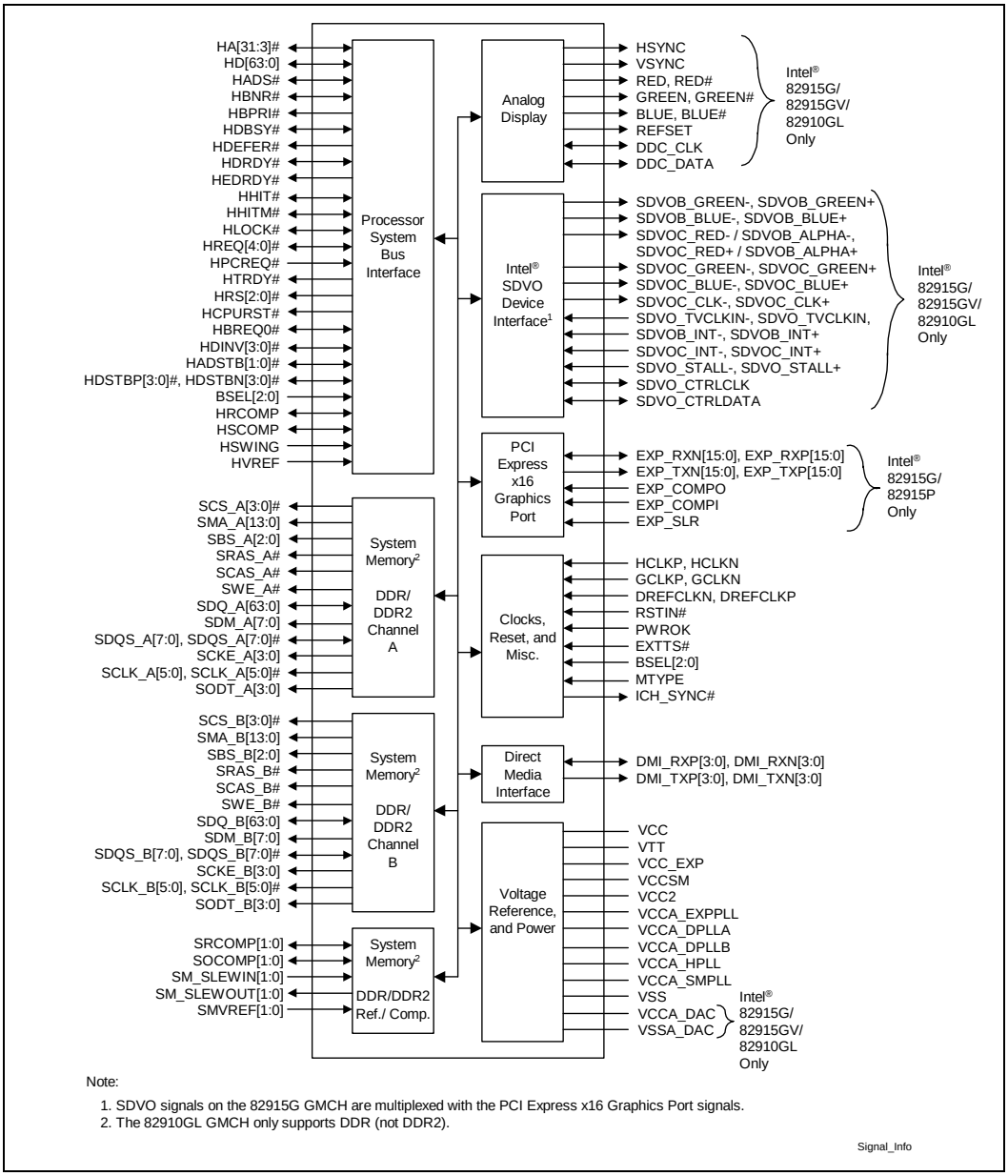
2 Signal Description

This chapter provides a detailed description of (G)MCH signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in Section 2.11.

The following notations are used to describe the signal type:

GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The (G)MCH integrates GTL+ termination resistors, and supports VTT of from 0.83 V to 1.65 V (including guardbanding).
PCIE	PCI-Express interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 V maximum. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification = (|D+ - D-|) * 2 = 1.2 V maximum. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 2.5 V tolerant.
HVCMOS	High Voltage CMOS buffers. 2.5 V tolerant.
HVIN	High Voltage CMOS input-only buffers. 3.3 V tolerant.
SSTL-2	Stub Series Termination Logic. These are 2.6 V output capable buffers. 2.6 V tolerant.
SSTL-1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

Figure 2-1. Intel® (G)MCH Signal Interface Diagram



Note:

1. SDVO signals on the 82915G GMCH are multiplexed with the PCI Express x16 Graphics Port signals.
2. The 82910GL GMCH only supports DDR (not DDR2).

2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (VTT).

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** This signal is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. HBREQ0# should be tristated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH6 must provide processor frequency select strap set-up and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the Intel® ICH6 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** Signals that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0] signals**.** Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **HDINVx# — Data Bits** HDINV3# — HD[63:48] HDINV2# — HD[47:32] HDINV1# — HD[31:16] HDINV0# — HD[15:0]

Signal Name	Type	Description
HDRDY#	I/O GTL+	**Data Ready**: This signal is asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready**: This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The (G)MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express Graphics initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0] and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobes** / **Data** / **Bits** HDSTBP3#, HDSTBN3# / HD[63:48] / HDINV3# HDSTBP2#, HDSTBN2# / HD[47:32] / HDINV2# HDSTBP1#, HDSTBN1# / HD[31:16] / HDINV1# HDSTBP0#, HDSTBN0# / HD[15:0] / HDINV0#
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HHITM# by the target to extend the snoop window.
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This signal is also driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express Graphics accesses to DRAM are allowed when HLOCK# is asserted by the processor).
HPCREQ#	I GTL+ 2x	**Precharge Request:** The processor provides a “hint” to the (G)MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The (G)MCH uses this information to schedule the read request to memory using the special “AutoPrecharge” attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. Asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.

Signal Name	Type	Description
HREQ[4:0]#	I/O GTL+ 2x	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the (G)MCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Response Signals:** These signals indicate the type of response as shown below: 000 = Response type 001 = Idle state 010 = Retry response 011 = Deferred response 100 = Reserved (not driven by (G)MCH) 101 = Hard Failure (not driven by (G)MCH) 110 = No data response 111 = Implicit Writeback 111 = Normal data response
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O CMOS	**Host RCOMP:** Used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (VTT).
HSCOMP	I/O CMOS	**Slew Rate Compensation:** Compensation for the Host Interface.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HVREF	I A	**Host Reference Voltage Reference:** Voltage input for the data, address, and common clock signals of the Host GTL interface.

2.2 DDR/DDR2 DRAM Channel A Interface

Note that the 82910GL, 82915GL, and 82915PL (G)MCH only supports DDR DRAM.

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-2/1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-2/1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary differential DDR/DDR2 clock signals.
SCS_A[3:0]#	O SSTL-2/1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-2/1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_A[2:0]	O SSTL-2/1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR2: 1-Gb technology is 8 banks. DDR: 1-Gb technology is 4 banks. SBS_A[2] is not used.
SRAS_A#	O SSTL-2/1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-2/1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-2/1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-2/1.8 2x	**Data Lines:** SDQ_A signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-2/1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax signal for every data byte lane.
SDQS_A[7:0]	I/O SSTL-2/1.8 2x	**Data Strobes:** For DDR, the rising and falling edges of SDQS_Ax are used for capturing data during read and write transactions. For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.
SDQS_A[7:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements (DDR2 only):** These signals are the complementary DDR2 strobe signals.

Signal Name	Type	Description
SCKE_A[3:0]	O SSTL-2/1.8	**Clock Enable:** (1 per Rank) SACKE is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination (DDR2 only):** Active On-die Termination Control signals for DDR2 devices.

2.3 DDR/DDR2 DRAM Channel B Interface

Note that the 82910GL, 82915GL, and 82915PL (G)MCH only supports DDR DRAM.

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-2/1.8	**SDRAM Differential Clock:** (3 per DIMM) SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-2/1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary differential DDR/DDR2 clock signals.
SCS_B[3:0]#	O SSTL-2/1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank
SMA_B[13:0]	O SSTL-2/1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_B[2:0]	O SSTL-2/1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR2: 1-Gb technology is 8 banks. DDR: 1-Gb technology is 4 banks. SBS_B[2] is not used
SRAS_B#	O SSTL-2/1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands
SCAS_B#	O SSTL-2/1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-2/1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-2/1.8 2x	**Data Lines:** SDQ_Bx signals interface to the SDRAM data bus
SDM_B[7:0]	O SSTL-2/1.8 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx signal for every data byte lane.

Signal Name	Type	Description
SDQS_B[7:0]	I/O SSTL-2/1.8 2x	**Data Strobes:** For DDR the rising and falling edges of SDQS_Bx are used for capturing data during read and write transactions. For DDR2, SDQS_Bx and its complement SDQS_Bx# make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements (DDR2 only):** These signals are the complementary DDR2 Strobe signals.
SCKE_B[3:0]	O SSTL-2/1.8	**Clock Enable:** (1 per Rank) SCKE_B is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination (DDR2 only):** Active On-die Termination Control signals for DDR2 devices.

2.4 DDR/DDR2 DRAM Reference and Compensation

Note that the 82910GL, 82915GL, and 82915PL (G)MCH only supports DDR DRAM.

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) driver compensation (DDR2 only)**
SM_SLEWIN[1:0]	I A	**Buffer Slew Rate Input:** Slew Rate characterization buffer input for X and Y orientation.
SM_SLEWOUT[1:0]	O A	**Buffer Slew Rate Output:** Slew Rate characterization buffer output for X and Y orientation
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DM, DQS, and DQS# input signals.

2.5 PCI Express* x16 Graphics Port Signals (Intel® 82915G, 82915P, 82915PL Only)

Unless otherwise specified, PCI Express Graphics signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	**PCI Express Graphics Receive Differential Pair**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	**PCI Express Graphics Transmit Differential Pair**
EXP_COMPO	I A	**PCI Express Graphics Output Current Compensation** **Note:** EXP_COMP0 is used for DMI current compensation.
EXP_COMPI	I A	**PCI Express Graphics Input Current Compensation** **Note:** EXP_COMPI is used for DMI current compensation.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal:** The (G)MCH's PCI Express lane numbers are reversed. For example, the (G)MCH PCI Express interface signals can be configured as follows: **Ball** / **Normal Operation** / **Lane Reversed** C10 / EXP_TXP0 / EXP_TXP15 A9 / EXP_TXP1 / EXP_TXP14 … / … / … N3 / EXP_TXP14… / EXP_TXP1… P1 / EXP_TXP15 / EXP_TXP0 0 = (G)MCH's PCI Express lane numbers are reversed 1 = Normal operation

2.6 Analog Display Signals (Intel® 82915G/82915GV/82915GL/82910GL GMCH Only)

Signal Name	Type	Description
RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
RED#	O A	**REDB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
GREEN#	O A	**GREENB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ω routing impedance; however, the terminating resistor to ground will be 75 Ω (e.g., 75 Ω resistor on the board, in parallel with a 75 Ω CRT load).
BLUE#	O A	**BLUEB Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 Ω 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 2.5 V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5 V output
VSYNC	O 2.5 V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5 V output.
DDC_CLK	I/O 2.5 V CMOS	**Monitor Control Clock.** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 2.5 V CMOS	**Monitor Control Data.** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

2.7 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain.
GCLKP GCLKN	I CMOS	**Differential PCI Express Graphics Clock In:** These pins receive a differential 100 MHz serial reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I CMOS	**Display PLL Differential Clock In**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PLTRST# output of the Intel® ICH6. All PCI Express Graphics Attach output signals will also tri-state compatible with *PCI Express* Specification* Rev 1.0a. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXTTS#	I HVCMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
MTYPE	I CMOS	**Memory Type Select Strap.** This signal is a strapping option that indicates the type of system memory. For the 82910GL GMCH, this signal must be tied to ground. 0 = DDR2 1 = DDR
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH6.

2.8 Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	**Direct Media Interface:** These signals are the receive differential pair (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** These signals are the transmit differential pair (Tx).

2.9 Intel® Serial DVO (SDVO) Interface (82915G/82915GV/82915GL/82910GL GMCH Only)

For the 82915G/82915GV/82915GL/82910GL GMCH, all but two of the pins in this section are multiplexed with the lower 8 lanes of the PCI Express interface.

Note: The SDVO interface does not support static lane reversal (e.g., SDVOB_CLK# will originate from the same ball whether the PCI Express interface is lane-reversed mode or not.

Signal Name	Type	Description
SDVOB_GREEN-	O PCIE	**Serial Digital Video Channel B Green Complement**. This signal is multiplexed with EXP_TXN1.
SDVOB_GREEN+	O PCIE	**Serial Digital Video Channel B Green**. This signal is multiplexed with EXP_TXP1.
SDVOB_BLUE-	O PCIE	**Serial Digital Video Channel B Blue Complement**. This signal is multiplexed with EXP_TXN2.
SDVOB_BLUE+	O PCIE	**Serial Digital Video Channel B Blue**. This signal is multiplexed with EXP_TXP2.
SDVOC_RED- / SDVOB_ALPHA-	O PCIE	**Serial Digital Video Channel C Red Complement Channel B Alpha Complement**. This signal is multiplexed with EXP_TXN4.
SDVOC_RED+ / SDVOB_ALPHA+	O PCIE	**Serial Digital Video Channel C Red Channel B Alpha**. This signal is multiplexed with EXP_TXP4.
SDVOC_GREEN-	O PCIE	**Serial Digital Video Channel C Green Complement**. This signal is multiplexed with EXP_TXN5.
SDVOC_GREEN+	O PCIE	**Serial Digital Video Channel C Green**. This signal is multiplexed with EXP_TXP5.
SDVOC_BLUE-	O PCIE	**Serial Digital Video Channel C Blue Complement**. This signal is multiplexed with EXP_TXN6.
SDVOC_BLUE+	O PCIE	**Serial Digital Video Channel C Blue**. This signal is multiplexed with EXP_TXP6.
SDVOC_CLK-	O PCIE	**Serial Digital Video Channel C Clock Complement**. This signal is multiplexed with EXP_TXN7.
SDVOC_CLK+	O PCIE	**Serial Digital Video Channel C Clock**. This signal is multiplexed with EXP_TXP7.
SDVO_TVCLKIN-	I PCIE	**Serial Digital Video TVOUT Synchronization Clock Complement**. This signal is multiplexed with EXP_RXN0.
SDVO_TVCLKIN+	I PCIE	**Serial Digital Video TVOUT Synchronization Clock**. This signal is multiplexed with EXP_RXP0.
SDVOB_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement.** This signal is multiplexed with EXP_RXN1.
SDVOB_INT+	I PCIE	**Serial Digital Video Input Interrupt.** This signal is multiplexed with EXP_RXP1.
SDVOC_INT+	I PCIE	**Serial Digital Video Input Interrupt.** This signal is multiplexed with EXP_RXP5.
SDVOC_INT-	I PCIE	**Serial Digital Video Input Interrupt Complement.** This signal is multiplexed with EXP_RXN5.

Signal Name	Type	Description
SDVO_STALL-	I PCIE	**Serial Digital Video Field Stall Complement.** This signal is multiplexed with EXP_RXN2.
SDVO_STALL+	I PCIE	**Serial Digital Video Field Stall..** This signal is multiplexed with EXP_RXP2.
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock.**
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data.** This signal also provides a strapping option. Device 1 (Host-PCI Express Bridge) is disabled on Reset when the SDVO Presence strap (SDVO_CTLRDATA) is sampled high, and is enabled when this signal is sampled low.

2.10 Power and Ground

Name	Voltage	Description
VCC	1.5 V	**Core Power.**
VTT	1.2 V	**Processor System Bus Power.**
VCC_EXP	1.5 V	**PCI Express* and DMI Power.**
VCCSM	1.8 V / 2.6 V	**System Memory Power.** DDR2: VCCSM = 1.8 V DDR: VCCSM = 2.6 V
VCC2	2.5 V	**2.5 V CMOS Power.**
VCCA_EXPPLL	1.5 V	**PCI Express PLL Analog Power.**
VCCA_DPLLA	1.5 V	**Display PLL A Analog Power.**
VCCA_DPLLB	1.5 V	**Display PLL B Analog Power.**
VCCA_HPLL	1.5 V	**Host PLL Analog Power.**
VCCA_SMPLL	1.5 V	**System Memory PLL Analog Power.**
VCCA_DAC	2.5 V	**Display DAC Analog Power.** This signal is on the 82915G/82915GV/82915GL/82910GL GMCH only.
VSS	0 V	**Ground.**
VSSA_DAC	0 V	**Ground.** This signal is on the 82915G/82915GV/82915GL/82910GL GMCH only.

2.11 Reset States and Pull-up/Pull-downs

This section describes the expected states of the (G)MCH I/O buffers during and immediately after the assertion of RSTIN#. This table only refers to the contributions on the interface from the (G)MCH and does **not** reflect any external influence (such as external pull-up/pull-down resistors or external drivers).

Legend:

CMCT: Common Mode Center Tapped. Differential signals are weakly driven to the common mode central voltage.
DRIVE: Strong drive (to normal value supplied by core logic if not otherwise stated)
TERM: Normal termination devices are turned on
LV: Low voltage
HV: High voltage
IN: Input buffer enabled
ISO: Isolate input buffer so that it doesn't oscillate if input left floating
TRI: Tri-state
PU: Weak internal pull-up
PD: Weak internal pull-down
STRAP: Strap input sampled during assertion or on the de-asserting edge of RSTIN#

Table 2-1. Host Interface Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Host I/F	HCPURST#	O	DRIVE LV	TERM HV after approximately 1ms	TRI (No VTT)	
	HADSTB[1:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HA[31:3]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HD[63:0]	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDSTBP[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDSTBN[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDINV[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HADS#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HBNR#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HBPRI#	O	TERM HV	TERM HV	TRI (No VTT)	
	HDBSY#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDEFER#	O	TERM HV	TERM HV	TRI (No VTT)	
	HDRDY#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HEDRDY#	O	TERM HV	TERM HV	TRI (No VTT)	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Host I/F	HHIT#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HHITM#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HLOCK#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HREQ[4:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HTRDY#	O	TERM HV	TERM HV	TRI (No VTT)	
	HRS[2:0]#	O	TERM HV	TERM HV	TRI (No VTT)	
	HBREQ0#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HPCREQ#	I	TERM HV	TERM HV	TRI (No VTT)	
	HVREF	I	IN	IN	TRI	
	HRCOMP	I/O	TRI	TRI after RCOMP	TRI	20 Ω resistor for board with target impedance of 60 Ω
	HSWING	I	IN	IN		
	HSCOMP	I/O	TRI	TRI	TRI	

Table 2-2. System Memory (DDR2) Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
System Memory (DDR2)	**Channel A**					
	SCLK_A[5:0]	O	TRI	TRI	TRI	
	SCLK_A[5:0]#	O	TRI	TRI	TRI	
	SCS_A[3:0]#	O	TRI	TRI	TRI	
	SMA_A[13:0]	O	TRI	TRI	TRI	
	SBS_A[2:0]	O	TRI	TRI	TRI	
	SRAS_A#	O	TRI	TRI	TRI	
	SCAS_A#	O	TRI	TRI	TRI	
	SWE_A#	O	TRI	TRI	TRI	
	SDQ_A[63:0]	I/O	TRI	TRI	TRI	
	SDM_A[7:0]	O	TRI	TRI	TRI	
	SDQS_A[7:0]	I/O	TRI	TRI	TRI	
	SDQS_A[7:0]#	I/O	TRI	TRI	TRI	
	SCKE_A[3:0]	O	LV	LV	LV	
	SODT_A[3:0]	O	LV	LV	LV	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
System Memory (DDR2)	**Channel B**					
	SCLK_B[5:0]	O	TRI	TRI	TRI	
	SCLK_B[5:0]#	O	TRI	TRI	TRI	
	SCS_B[3:0]#	O	TRI	TRI	TRI	
	SMA_B[13]	O	TRI	TRI	TRI	
	SMA_B[12:11]	O	LV	LV	LV	
	SMA_B[10:8]	O	TRI	TRI	TRI	
	SMA_B[7]	O	LV	LV	LV	
	SMA_B[6:0]	O	TRI	TRI	TRI	
	SBS_B[2]	O	LV	LV	LV	
	SBS_B[1:0]	O	TRI	TRI	TRI	
	SRAS_B#	O	TRI	TRI	TRI	
	SCAS_B#	O	TRI	TRI	TRI	
	SWE_B#	O	TRI	TRI	TRI	
	SDQ_B[63:0]	I/O	TRI	TRI	TRI	
	SDM_B[7:0]	O	TRI	TRI	TRI	
	SDQS_B[7:0]	I/O	TRI	TRI	TRI	
	SDQS_B[7:0]#	I/O	TRI	TRI	TRI	
	SCKE_B[3:0]	O	LV	LV	LV	
	SODT_B[3:0]	O	LV	LV	LV	
	SRCOMP0	I/O	TRI	TRI (after RCOMP)	TRI	
	SRCOMP1	I/O	TRI	TRI (after RCOMP)	TRI	
	SM_SLEWIN[1:0]	I	IN	IN	IN	
	SM_SLEWOU{1:0]	O	TRI	TRI (after RCOMP)	TRI	
	SMVREF[1:0]	I	IN	IN	IN	
	SOCOMP[1:0]	I/O	TRI	TRI	TRI	DDR2: 40 Ω resistor to ground

Table 2-3. System Memory (DDR) Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
System Memory (DDR)	**Channel A**					
	SCLK_A[5:0]	O	TRI	TRI	TRI	
	SCLK_A[5:0]#	O	TRI	TRI	TRI	
	SMA_A[13:9]	O	TRI	TRI	TRI	
	SMA_A[8]	O	LV	LV	LV	
	SMA_A[7:6]	O	TRI	TRI	TRI	
	SMA_A[5]	O	LV	LV	LV	
	SMA_A[4:0]	O	TRI	TRI	TRI	
	SBS_A[2:0]	O	TRI	TRI	TRI	
	SCS_A[3]#	O	TRI	TRI	TRI	
	SCS_A[2:1]#	O	LV	LV	LV	
	SCS_A[0]#	O	TRI	TRI	TRI	
	SRAS_A#	O	TRI	TRI	TRI	
	SCAS_A#	O	LV	LV	LV	
	SWE_A#	O	TRI	TRI	TRI	
	SDQ_A[63:0]	I/O	TRI	TRI	TRI	
	SDM_A[7:0]	O	TRI	TRI	TRI	
	SDQS_A[7:0]	I/O	TRI	TRI	TRI	
	SDQS_A[7:0]#	I/O	TRI	TRI	TRI	
	SCKE_A[3:0]	O	LV	LV	LV	
System Memory (DDR)	**Channel B**					
	SCLK_B[5:0]	O	TRI	TRI	TRI	
	SCLK_B[5:0]#	O	TRI	TRI	TRI	
	SMA_B[13:0]	O	TRI	TRI	TRI	
	SMA_B[0]	O	LV	LV	LV	
	SBS_B[2]	O	TRI	TRI	TRI	
	SBS_B[1]	O	LV	LV	LV	
	SBS_B[0]	O	TRI	TRI	TRI	
	SCS_B[3]#	O	LV	LV	LV	
	SCS_B[2:0]#	O	TRI	TRI	TRI	
	SRAS_B#	O	TRI	TRI	TRI	
	SCAS_B#	O	TRI	TRI	TRI	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
System Memory (DDR)	SWE_B#	O	TRI	TRI	TRI	
	SDQ_B[63:0]	I/O	TRI	TRI	TRI	
	SDM_B[7:0]	O	TRI	TRI	TRI	
	SDQS_B[7:0]	I/O	TRI	TRI	TRI	
	SDQS_B[7:0]#	I/O	TRI	TRI	TRI	
	SCKE_B[3:0]	O	LV	LV	LV	
	SRCOMP0	I/O	TRI	TRI (after RCOMP)	TRI	
	SRCOMP1	I/O	TRI	TRI (after RCOMP)	TRI	
	SM_SLEWIN[1:0]	I	IN	IN	IN	
	SM_SLEWOU[1:0]	O	TRI	TRI (after RCOMP)	TRI	
	SMVREF[1:0]	I	IN	IN	IN	
	SOCOMP[1:0]	I/O	TRI	TRI	TRI	DDR2: 40 Ω resistor to ground

Table 2-4. PCI Express* Graphics x16 Port Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
PCI Express*-Graphics	EXP_RXN[15:0]	I/O	CMCT	CMCT	CMCT	
	EXP_RXP[15:0]	I/O	CMCT	CMCT	CMCT	
	EXP_TXN[15:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	EXP_TXP[15:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	EXP_COMPO	I	TRI	TRI (after RCOMP)	TRI	
	EXP_COMPI	I	TRI	TRI (after RCOMP)	TRI	

Table 2-5. DMI Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
DMI	DMI_RXN[3:0]	I/O	CMCT	CMCT	CMCT	
	DMI_RXP[3:0]	I/O	CMCT	CMCT	CMCT	
	DMI_TXN[3:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	DMI_TXP[3:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	

Table 2-6. Clocking Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Clocks	HCLKN	I	IN	IN	IN	
	HCLKP	I	IN	IN	IN	
	GCLKN	I	IN	IN	IN	
	GCLKP	I	IN	IN	IN	
	DREFCLKN	I	IN	IN	IN	
	DREFCLKP	I	IN	IN	IN	

Table 2-7. MISC Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Misc.	RSTIN#	I	IN	IN	IN	
	PWROK	I	HV	HV	HV	
	EXTTS#	I	PU	PU	PU	
	BSEL[2:0]	I	TRI	TRI	TRI	
	MTYPE	I	TERM HV	TERM HV	TERM HV	
	EXP_SLR	I	TERM HV	TERM HV	TERM HV	
	ICH_SYNC#	O	PU	PU	PU	
	SDVO_CTRLCLK	O	TRI	TRI	TRI	
	SDVO_CTRLDATA	I/O	TERM PD	TRI	TERM PD	

Table 2-8. DAC Reset and S3 States (Intel® 82915G/82915GV/82915GL/82910GL GMCH only)

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# Deassertion	S3	Pull-up/ Pull-down
DAC	HSYNC	O	LV		LV	
	VSYNC	O	LV		LV	
	RED	O	TRI	TRI	TRI	
	RED#	O	TRI	TRI	TRI	
	GREEN	O	TRI	TRI	TRI	
	GREEN#	O	TRI	TRI	TRI	
	BLUE	O	TRI	TRI	TRI	
	BLUE#	O	TRI	TRI	TRI	
	REFSET	O	TRI	0.5* VCCA_DAC	TRI	255 Ω 1% Resistor to Ground
	DDC_CLK	I/O	IN	IN	IN	
	DDC_DATA	I/O	IN	IN	IN	

§

3 Register Description

The (G)MCH contains two sets of software accessible registers, accessed via the processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space that control access to PCI and PCI Express configuration space (see Section 3.4).
- Internal configuration registers residing within the (G)MCH are partitioned into three logical device register sets (“logical” since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e. DRAM configuration, other chipset operating parameters and optional features). The second register block is dedicated to the 82915G/82915P/82915PL (G)MCH Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). The third register block is for the 82915G/82915GV/82915GL/82910GL GMCH internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS that can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers that reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

3.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to ‘1’ when read and then will continue to remain set until written. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is “Power Good Reset” as defined in the *PCI Express* Specification*).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the *PCI Express* Specification*).

Item	Description
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent read could retrieve a ‘1’.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent read could retrieve a ‘1’. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WC	Read Write Clear bit(s). These bits can be read and written. However, a write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.
Reserved Bits	Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled "Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32-bits in size). Writes to “Reserved” registers have no effect on the (G)MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.
Default Value	Upon a Full Reset, the (G)MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

3.2 Platform Configuration

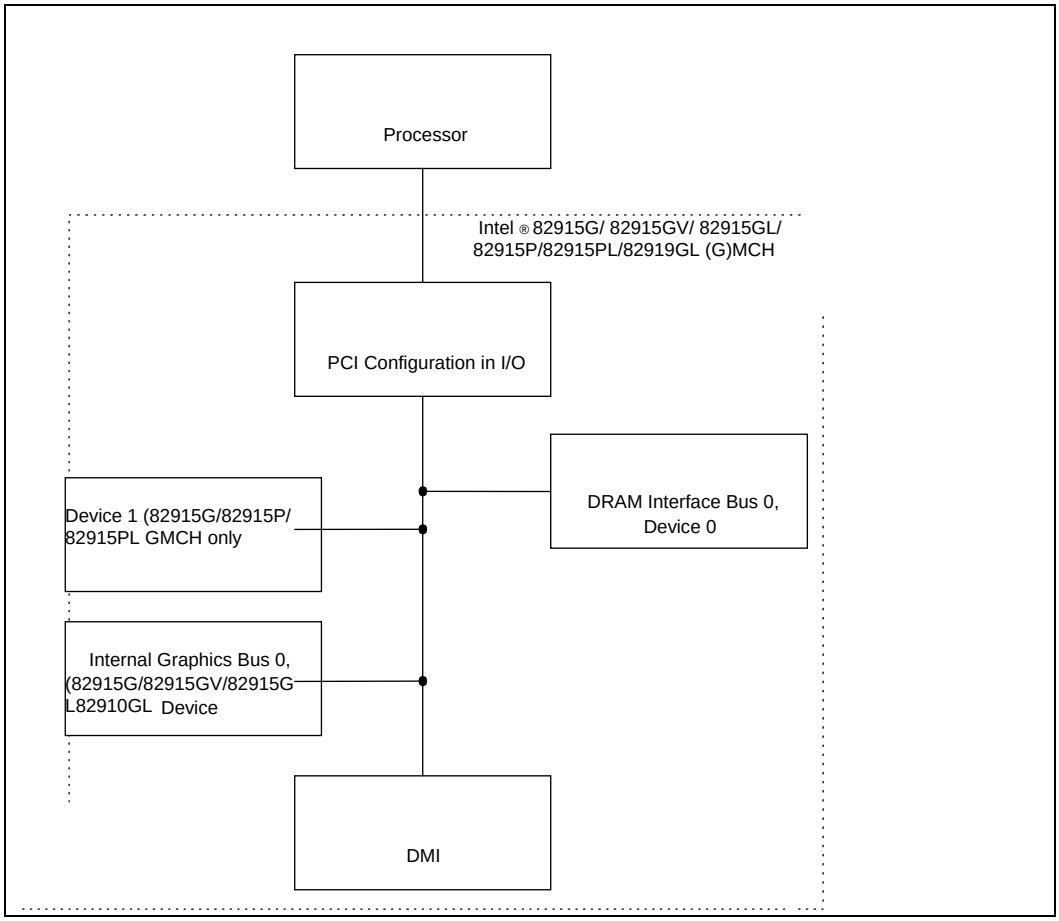
In platforms that support DMI (e.g. this (G)MCH) the configuration structure is significantly different from previous Hub architectures. The DMI physically connects the (G)MCH and the Intel ICH6; so, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the (G)MCH and the Intel ICH6 appear to be on PCI bus 0.

The ICH6 internal LAN controller does not appear on bus 0; it appears on the external PCI bus (whose number is configurable).

The system's primary PCI expansion bus is physically attached to the Intel ICH6 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist and that DMI and the internal devices in the (G)MCH and Intel ICH6 logically constitute PCI Bus 0 to configuration software. This is shown in Figure 3-1.

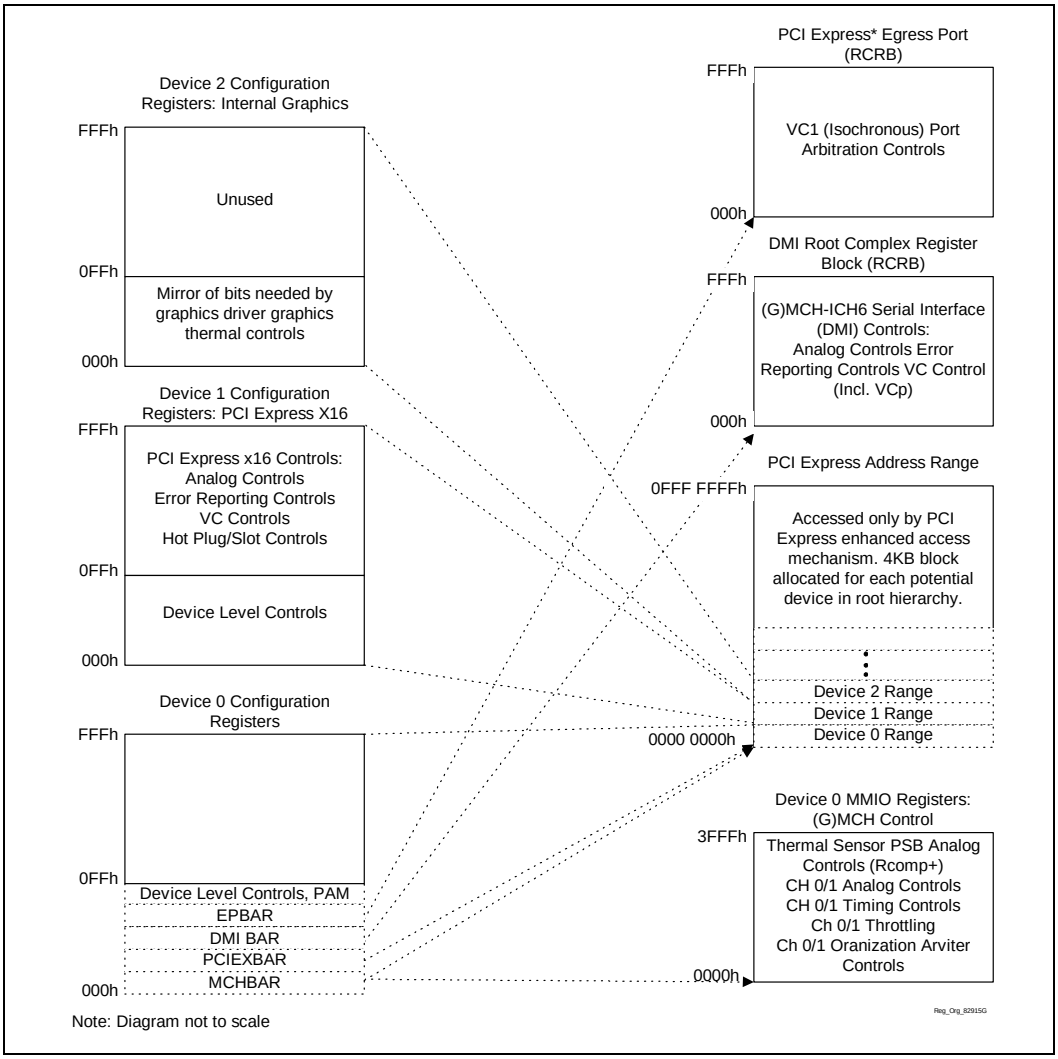
Figure 3-1. Conceptual Chipset PCI Configuration Diagram



The (G)MCH contains the following PCI devices within a single physical component. The configuration registers for the devices are mapped as devices residing on PCI bus 0.

- **Device 0 – Host Bridge/DRAM Controller**: Logically this appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other (G)MCH specific registers.
- **Device 1– Host-PCI Express Bridge (82915G/82915P/82915PL (G)MCH only)**. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express* Specification* Revision 1.0a. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2 – Internal Graphics Control (82915G/82915GV/82915GL/82910GL GMCH only)**. Logically, this appears as a PCI device residing on PCI bus 0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.

Figure 3-2. Register Organization (Representative of the Intel® 82915G GMCH)



NOTES:

1. Very high level representation. Many details omitted.
2. Inter graphics memory mapped registers are not shown.
3. Only Device 1 use PCI Express extended configuration space.
4. Device 0 and Device 2 use only standard PCI configuration space.
5. Hex numbers represent address range size and not actual locations.

Table 3-1. Device Number Assignment for Internal (G)MCH Devices

(G)MCH Function	Device#
Host Bridge / DRAM Controller	Device 0
Host-to-PCI Express* Bridge (virtual P2P) (Intel® 82915G/82915P/82915PL (G)MCH only)	Device 1
Internal Graphics Control (82915G/82915GV/82915GL/82910GL GMCH only)	Device 2

3.3 General Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express. PCI and PCI Express configuration cycles are selectively routed to one of these interfaces. The (G)MCH is responsible for routing configuration cycles to the proper interface. Configuration cycles to the Intel ICH6 internal devices and Primary PCI (including downstream devices) are routed to the Intel ICH6 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port.

A detailed description of the mechanism for translating processor I/O bus cycles to configuration cycles is described below.

3.3.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS [31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

3.3.2 Logical PCI Bus 0 Configuration Mechanism

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the (G)MCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the (G)MCH is hardwired as Device 1 on PCI Bus 0. The 82915G/82915GV/82915GL/82910GL GMCH's Device 2 contains the control registers for the Integrated Graphics Controller. The Intel ICH6 decodes the Type 0 access and generates a configuration access to the selected internal device.

3.3.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between upper bound in device's Subordinate Bus Number register and lower bound in device's Secondary Bus Number register), the (G)MCH would generate a Type 1 DMI Configuration Cycle. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the Intel ICH6 via the DMI, the Intel ICH6 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for ICH6 PCI Express ports one of the Intel ICH6's devices, the DMI, or a downstream PCI bus.

Figure 3-3. DMI Type 0 Configuration Address Translation

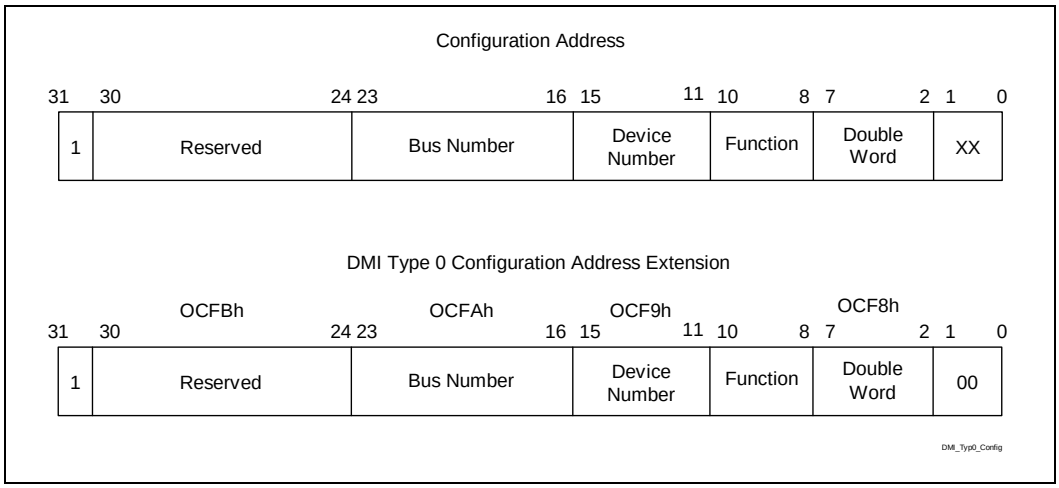
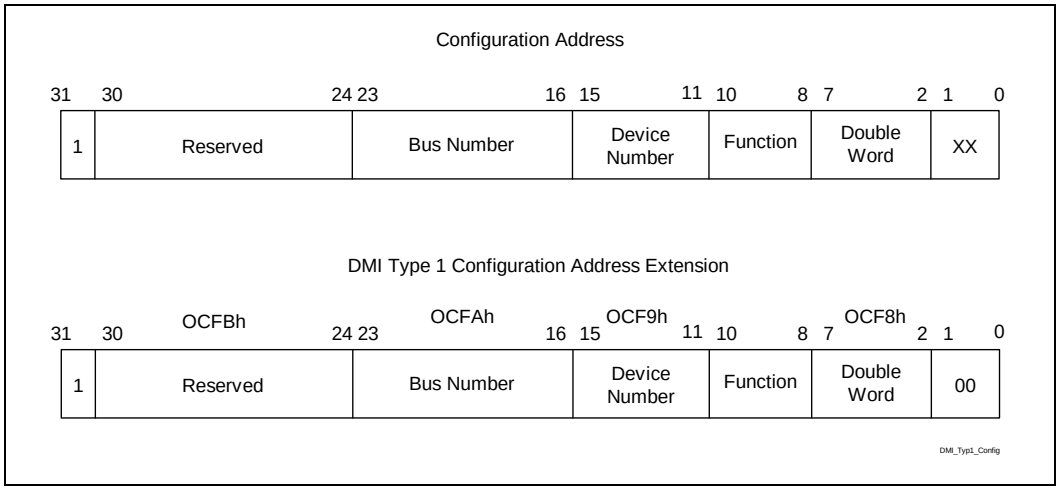


Figure 3-4. DMI Type 1 Configuration Address Translation

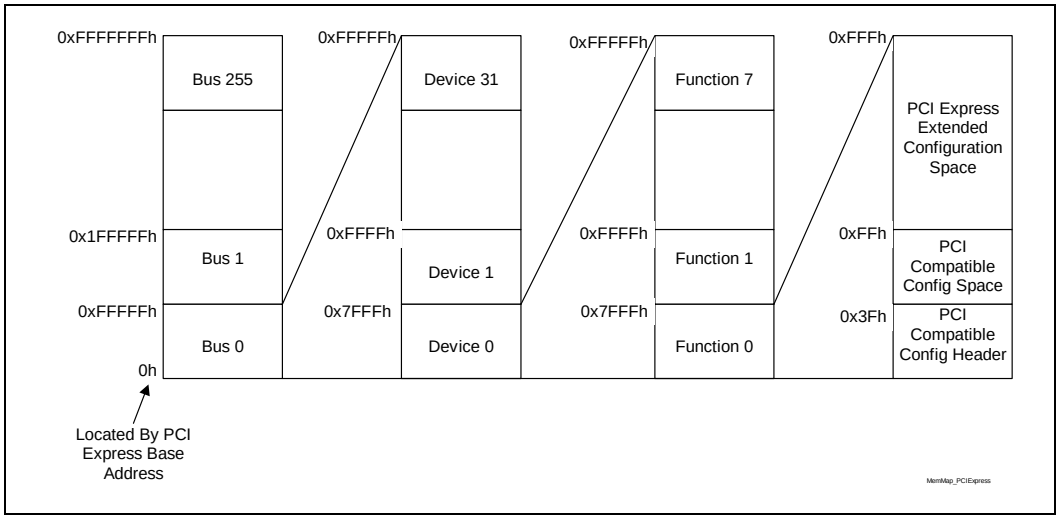


3.3.4 PCI Express* Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification, Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region that consists of the first 256B of a logical device's configuration space and a PCI Express extended region that consists of the remaining configuration space.

The PCI compatible region can be accessed using either the mechanism defined in the previous section or using the enhanced PCI Express configuration access mechanism described in this section. The extended configuration registers may only be accessed using the enhanced PCI Express configuration access mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent. The enhanced PCI Express configuration access mechanism uses a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. The PCIEXBAR register defines the base address for the 256-MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The PCI Express Configuration Transaction Header includes an additional 4 bits (Extended Register Address[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

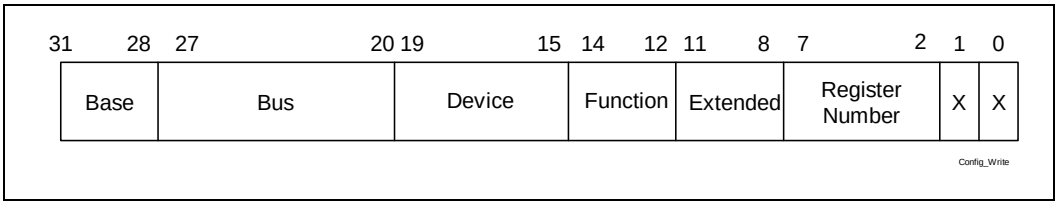
Figure 3-5. Memory Map to PCI Express* Device Configuration Space



Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function, and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are performed only once by BIOS)

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 31 of the DEVEN register.
2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write to or read from that register.



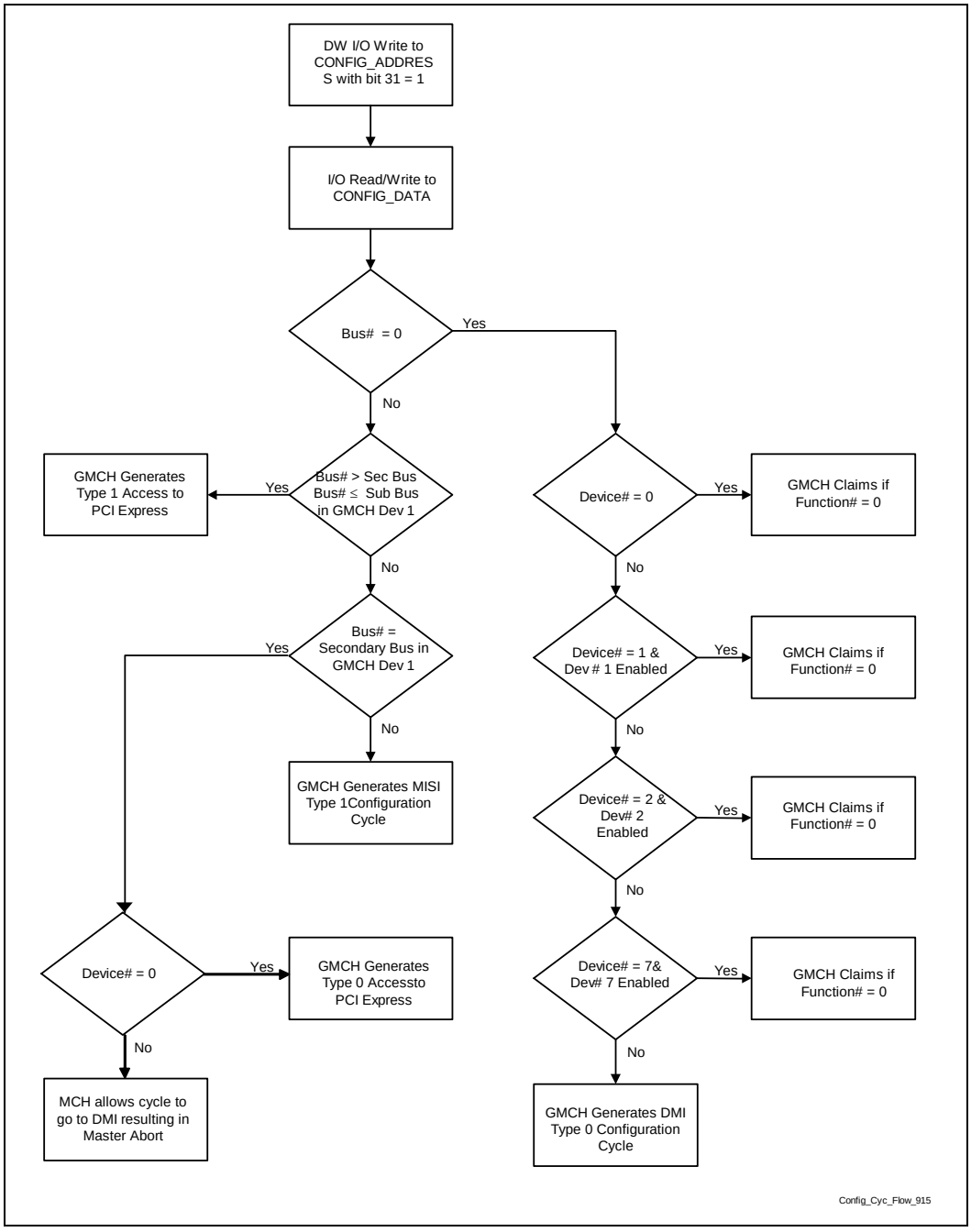
PCI Express Configuration Writes

Internally the host interface unit translates writes to PCI Express extended configuration space to configurations on the backbone. Writes to extended space are posted on the FSB, but non-posted on the PCI Express* x16 Graphics Interface or DMI pins (i.e., translated to configuration writes).

See the *PCI Express Specification* for more information on both the PCI 2.3 compatible and PCI Express enhanced configuration mechanism and transaction rules.

3.3.5 Intel® 915x GMCH Configuration Cycle Flowchart

Figure 3-6. Intel® 915x GMCH Configuration Cycle Flowchart



3.4 I/O Mapped Registers

The (G)MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DWord
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE):** 1 = Enable 0 = Disable
30:24		Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus #0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is ≥ 3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express Graphics. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1 a Type 1 PCI configuration cycle will be generated on PCI Express Graphics. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.

Bit	Access & Default	Description
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is “00”, the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2 the internal (G)MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

3.4.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

§

4 Host Bridge/DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

Warning: Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 4-1. Device 0 Function 0 Register Address Map Summary

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2580h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/W/C
08h	RID	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	060000h	RO
0Ch	—	**Reserved**	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0F–2Bh	—	**Reserved**	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/W/O
2E–2Fh	SID	Subsystem Identification	0000h	R/W/O
30–33h	—	**Reserved**	—	—
34h	CAPPTR	Capabilities Pointer	EOh	RO
35–3Fh	—	**Reserved**	—	—
40–43h	EPBAR	Egress Port Base Address	00000000h	RO
44–47h	MCHBAR	GMCH Memory Mapped Register Range Base Address	00000000h	R/W
48–4Bh	PCIEXBAR	PCI Express* Register Range Base Address	E0000000h	R/W
4C–4Fh	DMIBAR	Root Complex Register Range Base Address	00000000h	R/W

Address Offset	Register Symbol	Register Name	Default Value	Access
52–53h	GGC	GMCH Graphics Control Register (82915G GMCH only)	0030h	R/W/L
54–57h	DEVEN	Device Enable	00000019h	R/W
58–8Fh	—	**Reserved**	—	—
90h	PAM0	Programmable Attribute Map 0	00h	R/W
91h	PAM1	Programmable Attribute Map 1	00h	R/W
92h	PAM2	Programmable Attribute Map 2	00h	R/W
93h	PAM3	Programmable Attribute Map 3	00h	R/W
94h	PAM4	Programmable Attribute Map 4	00h	R/W
95h	PAM5	Programmable Attribute Map 5	00h	R/W
96h	PAM6	Programmable Attribute Map 6	00h	R/W
97h	LAC	Legacy Access Control	00h	R/W
98–9Bh	—	**Reserved**	—	—
9Ch	TOLUD	Top of Low Usable DRAM	08h	R/W
9Dh	SMRAM	System Management RAM Control	00h	RO, R/W/L
9Eh	ESMRAMC	Extended System Management RAM Control	00h	RO, R/W/L
9F–C7h	—	**Reserved**	—	—
C8–C9h	ERRSTS	Error Status	0000h	RO, R/W/L
CA–CBh	ERRCMD	Error Command	0000h	R/W
CC–DBh	—	**Reserved**	—	—
DC–DFh	SKPD	Scratchpad Data	00000000h	R/W
E0–E8h	CAPID0	Capability Identifier	0000000000 01090009h	RO
E9–FFh	—	**Reserved**	—	—
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
104–107h	—	**Reserved**	—	—
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	R/W
10A–10Bh	—	**Reserved**	—	—
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	R/W
10Dh	—	**Reserved**	—	—

Address Offset	Register Symbol	Register Name	Default Value	Access
10E–10F	C0BNKARC	Channel A DRAM Bank Architecture	0000h	R/W
110–113h	—	**Reserved**	—	—
114–117h	C0DRT1	Channel A DRAM Timing Register	900122h	R/W
118–11Fh	—	**Reserved**	—	—
120–123h	C0DRC0	Channel A DRAM Controller Mode 0	00000000h	R/W, RO
124–17Fh	—	**Reserved**	—	—
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
184–187h	—	**Reserved**	—	—
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	R/W
18A–18Bh	—	**Reserved**	—	—
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	R/W
18Dh	—	**Reserved**	—	—
18E–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	R/W
190–193h	—	**Reserved**	—	—
194h	C1DRT1	Channel B DRAM Timing Register 1	900122h	R/W, RO
195–19Fh	—	**Reserved**	—	—
1A0–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	00000000h	R/W, RO
1A4–F0Fh	—	**Reserved**	—	—
F10–F13h	PMCFG	Power Management Configuration	00000000h	R/W
F14h	PMSTS	Power Management Status	00000000h	R/W/C/S

4.1 Host Bridge/DRAM Controller PCI Register Details (D0:F0)

4.1.1 VID—Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

4.1.2 DID—Device Identification (D0:F0)

PCI Device: 0
Address Offset: 02h
Default Value: 2580h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2580h	**Device Identification Number (DID):** This field is an identifier assigned to the (G)MCH core/primary PCI device.

4.1.3 PCICMD—PCI Command (D0:F0)

PCI Device: 0
Address Offset: 04h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since (G)MCH Device 0 does not physically reside on Primary PCI bus, many of the bits are not implemented.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B).** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0.
8	R/W 0b	**SERR Enable (SERRE).** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have a SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over DMI to the ICH6. 1 = Enable. The (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS, and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the (G)MCH for Device 0. 0 = Disable **Note:** That this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP).** Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE).** PERR# is not implemented by the (G)MCH and this bit is hardwired to 0.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP).** Hardwired to a 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE).** The (G)MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0.
3	RO 0b	Reserved
2	RO 1b	**Bus Master Enable (BME).** The (G)MCH is always enabled as a master. This bit is hardwired to a "1".
1	RO 1b	**Memory Access Enable (MAE).** The (G)MCH always allows access to main memory. This bit is not implemented and is hardwired to 1.
0	RO 0b	**I/O Access Enable (IOAE).** Hardwired to a 0.

4.1.4 PCISTS—PCI Status (D0:F0)

PCI Device: 0
Address Offset: 06h
Default Value: 0090h
Access: RO, R/W/C
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the (G)MCH Device 0 does not physically reside on Primary PCI, many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to a 0.
14	R/W/C 0b	**Signaled System Error (SSE):** Software clears this bit by writing a 1 to it. 1 = The (G)MCH Device 0 generated an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS, or ERRSTS registers.
13	R/WC 0b	**Received Master Abort Status (RMAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives an Unsupported Request completion packet.
12	R/WC 0b	**Received Target Abort Status (RTAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives a Completer Abort completion packet.
11	RO 0b	**Signaled Target Abort Status (STAS):** The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the (G)MCH and is hardwired to a 0.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Device 0 does not physically connect to Primary PCI. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for Primary PCI is not limited by the (G)MCH.
8	RO 0b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the (G)MCH; therefore, this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. Device 0 does not physically connect to Primary PCI. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for Primary PCI is not limited by the (G)MCH.
6		Reserved
5	RO 0b	**66 MHz Capable:** Does not apply to PCI Express*. Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability standard register resides.
3:0		Reserved

4.1.5 RID—Revision Identification (D0:F0)

PCI Device: 0
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 0.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This field indicates the number of times that this device in this component has been "stepped" through the manufacturing process. Refer to the *Intel® 82915G/82915P/82915GV/82910GL Express Chipset Specification Update* for the value of the Revision ID Register.

4.1.6 CC—Class Code (D0:F0)

PCI Device: 0
Address Offset: 09h
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. 06h = Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the (G)MCH falls. 00h = Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

4.1.7 MLT—Master Latency Timer (D0:F0)

PCI Device: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the (G)MCH is not a PCI master. Therefore, this register is not implemented.

Bit	Access & Default	Description
7:0		Reserved

4.1.8 HDR—Header Type (D0:F0)

PCI Device: 0
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0 to indicate that the (G)MCH is a single function device with standard header layout.

4.1.9 SVID—Subsystem Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

4.1.10 SID—Subsystem Identification (D0:F0)

PCI Device: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/W/O
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

4.1.11 CAPPTR—Capabilities Pointer (D0:F0)

PCI Device: 0
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

4.1.12 EPBAR—Egress Port Base Address (D0:F0)

PCI Device: 0
Address Offset: 40h
Default Value: 00000000h
Access: RO
Size: 32 bits

This is the base address for the Egress Port MMIO configuration space. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to EPBAREN[Dev 0, offset 54h, bit 27]

Bit	Access & Default	Description
31:12	R/W 00000h	**Egress Port MMIO Base Address:** This field corresponds to bits 31 to 12 of the base address Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the (G)MCH MMIO register set.
11:0		Reserved

4.1.13 MCHBAR—(G)MCH Memory Mapped Register Range Base Address (D0:F0)

PCI Device:	0
Address Offset:	44h
Default Value:	00000000h
Access:	R/W
Size:	32 bits

This is the base address for the (G)MCH memory-mapped configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 54h, bit 28]

Bit	Access & Default	Description
31:14	R/W 00000h	**(G)MCH Memory Mapped Base Address:** This field corresponds to bits 31:14 of the base address (G)MCH memory-mapped configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the (G)MCH Memory-mapped register set.
13:0		Reserved

4.1.14 PCIEXBAR—PCI Express* Register Range Base Address (D0:F0) (Intel® 82915G/82915P/82915PL Only)

PCI Device: 0
Address Offset: 48h
Default Value: E0000000h
Access: R/W
Size: 32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express hierarchy associated with the (G)MCH. There is not actual physical memory within this 256-MB window that can be addressed. Each PCI Express hierarchies require a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy.

The 256 MB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space. For example, MCHBAR reserves a 16-KB space and reserves a 4-KB space both outside of PCIEXBAR space. They cannot be overlaid on the space reserved by PCIEXBAR for devices 0.

On reset, this register is disabled and must be enabled by writing a 1 to PCIEXBAREN [Dev 0, offset 54h, bit 31]

If the PCI Express Base Address [bits 31:28] were set to Fh, an overlap with the High BIOS area, APIC ranges would result. Software must guarantee that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). If a system is populated with more than 3.5 GB, either the PCI Express Enhanced Access mechanism must be disabled or the value in TOLUD must be reduced to report that only 3.5 GB are present in the system to allow a value of Eh for the PCI Express Base Address (assuming that all PCI 2.3 compatible configuration space fits above 3.75 GB).

Bit	Access & Default	Description
31:28	R/W Eh	**PCI Express* Base Address:** This field corresponds to bits 31 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a 256-MB block of contiguous memory address space. Having control of those particular 4 bits insures that this base address will be on a 256-MB boundary, above the lowest 256 MB and still within total addressable memory space, currently 4 GB. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB The address used to access the PCI Express configuration space for **Device 1** in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = **PCI Express Base Address + 32 KB**. Remember that this address is the beginning of the 4-KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27:0		Reserved

4.1.15 DMIBAR—Root Complex Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 4Ch
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express hierarchy associated with the (G)MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB that is reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to the DMIBAREN [Dev 0, offset 54h, bit 29].

Bit	Access & Default	Description
31:12	R/W 0000 0h	**DMI Base Address:** This field corresponds to bits 31 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the DMI register set.
11:0		Reserved

4.1.16 GGC—GMCH Graphics Control Register (D0:F0) (82915G/82915GV/82915GL/82910GL GMCH only)

PCI Device: 0
Address Offset: 52h
Default Value: 0030h
Access: R/W/L
Size: 16 bits

Bit	Access & Default	Descriptions
15:7		Reserved
6:4	R/W/L 011b	**Graphics Mode Select (GMS):** This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Device 2 (IGD) does not claim VGA cycles (memory and I/O), and the Sub-Class Code field within Device 2, Function 0 Class Code register is 80h. 000 = No memory pre-allocated 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved. 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100–111 = Reserved. **NOTES:** 1. This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. 2. If IGD is disabled, this field should be set to 000.
3:2		Reserved
1	R/W 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00h. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2, Function 0 Class Code register is 80h.
0		Reserved

4.1.17 DEVEN—Device Enable (D0:F0)

PCI Device: 0
Address Offset: 54h
Default Value: 00000019h
Access: R/W
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH.

Bit	Access & Default	Description
31	R/W 0b	**82915G/82915P/82915PL (G)MCH:** **PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 31:28 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the (G)MCH. These translated cycles are routed as shown in the table above. **82915GV/82915GL/82910GL GMCH:** Reserved.
30		Reserved
29	R/W 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory. 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately.
28	R/W 0b	**MCHBAR Enable (MCHBAREN):** 0 = MCHBAR is disabled and does not claim any memory. 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately.
27	R/W 0b	**EPBAR Enable (EPBAREN):** 0 = EPBAR is disabled and does not claim any memory. 1 = EPBAR memory mapped accesses are claimed and decoded appropriately.
26:5		Reserved

Bit	Access & Default	Description
4	R/W 1b	**82915G/82915GV/82915GL/82910GL GMCH:** **Internal Graphics Engine Function 1 (D2F1EN):** 0 = Bus 0 Device 2 Function 1 is disabled and hidden 1 = Bus 0 Device 2 Function 1 is enabled and visible **Note:** Setting this bit to enabled when bit 3 is 0 has no meaning. **82915P/82915PL MCH:** Reserved.
3	R/W 1b	**82915G/82915GV/82915GL/82910GL GMCH:** **Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0 Device 2 Function 0 is disabled and hidden 1 = Bus 0 Device 2 Function 0 is enabled and visible **82915P/82915PL MCH:** Reserved.
2		Reserved
1	R/W 1b Strap dependent	**82915G/82915P/82915PL (G)MCH:** **PCI Express* Port (D1EN):** 0 = Bus 0 Device 1 Function 0 is disabled and hidden. This also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstb). 1 = Bus 0 Device 1 Function 0 is enabled and visible. The SDVO Presence hardware strap determines default value. Device 1 is disabled on Reset when the SDVO Presence strap (SDVO_CTLRDATA signal) is sampled high, and is enabled otherwise. **82915GV/82915GL/82910GL GMCH:** Reserved.
0	RO 1b	**Host Bridge:** Bus 0 Device 0 Function 0 can not be disabled and is therefore hardwired to 1.

4.1.18 PAM0—Programmable Attribute Map 0 (D0:F0)

PCI Device: 0
Address Offset: 90h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFh

The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cache ability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE (Read Enable). When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to Primary PCI.
- WE (Write Enable). When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to Primary PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that addresses the BIOS area from 0F0000h to 0FFFFFh. 00 = DRAM Disabled: All accesses are directed to the DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0		Reserved

Warning: The (G)MCH may hang if a PCI Express graphics attach or DMI originated access to Read Disabled or Write Disabled PAM segments occurs (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express graphics attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

4.1.19 PAM1—Programmable Attribute Map 1 (D0:F0)

PCI Device: 0
Address Offset: 91h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h–0C7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C0000-0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.20 PAM2—Programmable Attribute Map 2 (D0:F0)

PCI Device: 0
Address Offset: 92h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h–0CFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0CC000h–0CFFFFh Attribute (HIENABLE):** 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C8000h–0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.21 PAM3—Programmable Attribute Map 3 (D0:F0)

PCI Device: 0
Address Offset: 93h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h–0D7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0D4000h–0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D0000h–0D3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.22 PAM4—Programmable Attribute Map 4 (D0:F0)

PCI Device: 0
Address Offset: 94h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0DC000h–0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D8000h–0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.23 PAM5—Programmable Attribute Map 5 (D0:F0)

PCI Device: 0
Address Offset: 95h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0E4000h–0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E0000h–0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.24 PAM6—Programmable Attribute Map 6 (D0:F0)

PCI Device: 0
Address Offset: 96h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0EC000h–0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E8000h–0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.25 LAC—Legacy Access Control (D0:F0)

PCI Device: 0
Address Offset: 97h
Default Value: 00h
Access: R/W
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

<table>
<tr><th>Bit</th><th>Access & Default</th><th>Description</th></tr>
<tr><td>7</td><td>R/W
0b</td><td>Hole Enable (HEN): This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped.

0 = No memory hole.

1 = Memory hole from 15 MB to 16 MB.</td></tr>
<tr><td>6:1</td><td></td><td>Reserved</td></tr>
<tr><td>0</td><td>R/W
0b</td><td>MDA Present (MDAP): This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set.

If device 1's VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are forwarded to the DMI.

If the VGA enable bit is set and MDA is not present, then accesses to I/O address range x3BCh–x3BFh are forwarded to PCI Express* if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to the DMI.

MDA resources are defined as the following:

Memory: 0B0000h – 0B7FFFh

I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh,
(Including ISA address aliases, A [15:10] are not used in decode)

Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above.

The following table shows the behavior for all combinations of MDA and VGA:
<table>
<tr><th>VGAEN</th><th>MDAP</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>All References to MDA and VGA space are routed to the DMI</td></tr>
<tr><td>0</td><td>1</td><td>Illegal combination</td></tr>
<tr><td>1</td><td>0</td><td>All VGA and MDA references are routed to PCI Express Graphics Attach.</td></tr>
<tr><td>1</td><td>1</td><td>All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the DMI</td></tr>
</table>
</td></tr>
</table>

4.1.26 TOLUD—Top of Low Usable DRAM (D0:F0)

PCI Device: 0
Address Offset: 9Ch
Default Value: 08h
Access: R/W
Size: 8 bits

This 8-bit register defines the Top of Low Usable DRAM. TSEG and Graphics Stolen Memory (82915G only) are within the DRAM space defined. From the top, the (G)MCH optionally claims 1 to 32 MB of DRAM for internal graphics if enabled (82915G/82915GV/82915GL/82910GL GMCH only), and 1, 2, or 8 MB of DRAM for TSEG if enabled. These bits are LT Lockable.

Bit	Access & Default	Description
7:3	R/W 01h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31:27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits 31:27 programmed to 01h implies a minimum memory size of 128 MBs. Configuration software must set this value to the smaller of the following 2 choices: • Maximum amount memory in the system plus one byte or the minimum address allocated for PCI memory. Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. If this register is set to 0000 0b, it implies 128 MBs of system memory. **Note:** The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory (82915G/82915GV/82915GL/82910GL only) and TSEG. The host interface determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by 1 MB to determine base of TSEG.
2:0		Reserved

Programming Example (82915G/82915GV/82915GL/82910GL GMCH only):

- C1DRB7 is set to 4 GB
- TSEG is enabled and TSEG size is set to 1 MB
- Internal Graphics is enabled and Graphics Mode Select is set to 32 MB
- BIOS knows the OS requires 1G of PCI space.

BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20-MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to: 4 GB = 1_0000_0000h

The system memory requirements are:

4 GB (max addressable space) – 1 GB (PCI space) – 20 MB (lost memory) =
3 GB – 128 MB (minimum granularity) = B800_0000h

Since B800_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to B8h.

4.1.27 SMRAM—System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Dh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7		Reserved
6	R/W/L 0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W/L 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

4.1.28 ESMRAMC—Extended System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Eh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W/L 0b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME is 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/W/C 0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the (G)MCH .
4	RO 1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the (G)MCH.
3	RO 1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the (G)MCH.
2:1	R/W/L 00b	**TSEG Size (TSEG_SZ):** This field selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to the DMI when the TSEG memory block is enabled. 00 = 1-MB Tseg. (TOLUD – Graphics Stolen Memory Size – 1M) to (TOLUD – Graphics Stolen Memory Size). 01 = 2-MB Tseg (TOLUD – Graphics Stolen Memory Size – 2M) to (TOLUD – Graphics Stolen Memory Size). 10 = 8-MB Tseg (TOLUD – Graphics Stolen Memory Size – 8M) to (TOLUD – Graphics Stolen Memory Size). 11 = Reserved. Once D_LCK has been set, these bits become read only. **NOTE:** References to Graphics Stolen Memory only apply to the 82915G/82915GV/82915GL/82910GL GMCH only.
0	R/W/L 0b	**TSEG Enable (T_EN):** This bit Enables SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

4.1.29 ERRSTS—Error Status (D0:F0)

PCI Device: 0
Address Offset: C8h
Default Value: 0000h
Access: R/WC/S, RO
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. A SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

0Bit	Access & Default	Description
15:13		Reserved
12	R/WC/S 0b	**(G)MCH Software Generated Event for SMI:** 1 = This bit indicates the source of the SMI was a Device 2 Software Event.
11	R/WC/S 0b	**(G)MCH Thermal Sensor Event for SMI/SCI/SERR:** This bit indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI, or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command, and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, an interrupt message will not be sent on a new thermal sensor event.
10		Reserved
9	R/WC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** 1 = (G)MCH detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S 0b	**Received Refresh Timeout Flag(RRTOF):** 1 = 1024 memory core refreshes are enqueued.
7:0		Reserved

4.1.30 ERRCMD—Error Command (D0:F0)

PCI Device: 0
Address Offset: CAh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the (G)MCH responses to various system errors. Since the (G)MCH does not have an SERR# signal, SERR messages are passed from the (G)MCH to the Intel ICH6 over DMI. When a bit in this register is set, a SERR message will be generated on DMI when the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access & Default	Description
15:12		Reserved
11	R/W 0b	**SERR on (G)MCH Thermal Sensor Event (TSESERR)** 1 = The (G)MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0 = Reporting of this condition via SERR messaging is disabled.
10		Reserved
9	R/W 0b	**SERR on LOCK to non-DRAM Memory (LCKERR)** 1 = The (G)MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Reporting of this condition via SERR messaging is disabled.
8	R/W 0b	**SERR on DRAM Refresh Timeout (DRTOERR)** 1 = The (G)MCH generates a DMI SERR special cycle when a DRAM Refresh timeout occurs. 0 = Reporting of this condition via SERR messaging is disabled.
7:0		Reserved

4.1.31 SKPD—Scratchpad Data (D0:F0)

PCI Device: 0
Address Offset: DCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**Scratchpad Data:** 1 DWord of data storage.

4.1.32 CAPID0—Capability Identifier (D0:F0)

PCI Device: 0
Address Offset: E0h
Default Value: 000000000001090009h
Access: RO
Size: 72 bits

Bit	Access & Default	Description
71:28		Reserved
27:24	RO 1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

§

5 MCHBAR Registers

These registers are offset from the MCHBAR base address.

Address Offset	Register Symbol	Register Name	Default Value	Access
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
104–107h	—	Reserved	—	—
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	R/W
10A–10Bh	—	Reserved	—	—
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	R/W
10Dh	—	Reserved	—	—
10E–10F	C0BNKARC	Channel A DRAM Bank Architecture	0000h	R/W
110–113h	—	Reserved	—	—
114–117h	C0DRT1	Channel A DRAM Timing Register	900122h	R/W
118–11Fh	—	Reserved	—	—
120–123h	C0DRC0	Channel A DRAM Controller Mode 0	00000000h	R/W, RO
124–17Fh	—	Reserved	—	—
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
184–187h	—	Reserved	—	—
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	R/W
18A–18Bh	—	Reserved	—	—
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	R/W
18Dh	—	Reserved	—	—
18E–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	R/W
190–193h	—	Reserved	—	—
194h	C1DRT1	Channel B DRAM Timing Register 1	900122h	R/W, RO

Address Offset	Register Symbol	Register Name	Default Value	Access
195–19Fh	—	Reserved	—	—
1A0–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	00000000h	R/W, RO
1A4–F0Fh	—	Reserved	—	—
F10–F13h	PMCFG	Power Management Configuration	00000000h	R/W
F14h	PMSTS	Power Management Status	00000000h	R/W/C/S

5.1 MCHBAR Register Details

5.1.1 C0DRB0—Channel A DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 100h
Default Value: 00h
Access: R/W
Size: 8 bits

The **DRAM Rank Boundary Register** defines the upper boundary address of each DRAM rank with a granularity of 32 MB. Each rank has its own single-byte **DRB** register. These registers are used to determine which chip select will be active for a given address.

Channel and Rank Map:

Channel A Rank 0: 100h
Channel A Rank 1: 101h
Channel A Rank 2: 102h
Channel A Rank 3: 103h
Channel B Rank 0: 180h
Channel B Rank 1: 181h
Channel B Rank 2: 182h
Channel B Rank 3: 183h

Single Channel or Asymmetric Channels Example

If the channels are independent, addresses in Channel B should begin where addresses in Channel A left off, and the address of the first rank of Channel A can be calculated from the technology (256 Mbit, 512 Mbit, or 1 Gbit) and the x8 or x16 configuration. With independent channels, a value of 01h in **C0DRB0** indicates that 32 MB of DRAM has been populated in the first rank, and the top address in that rank is 32 MB.

Programming guide

If Channel A is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

———

C1DRB0 = Total memory in chA rank0 + chA rank1 + chA rank2 + chA rank3 + chB rank0 (in 32-MB increments)

If Channel B is empty, all of the C1DRBs are programmed with the same value as C0DRB3.

Interleaved Channels Example

If channels are interleaved, corresponding ranks in opposing channels will contain the same value, and the value programmed takes into account the fact that twice as many addresses are spanned by this rank compared to the single channel case. With interleaved channels, a value of 01h in **C0DRB0** and a value of 01h in **C1DRB0** indicate that 32 MB of DRAM has been populated in the first rank of each channel and the top address in that rank of either channel is 64 MB.

Programming guide:

C0DRB0 = C1DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = C1DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

———

C0DRB3 = C1DRB3 = Total memory in chA rank0 + chA rank1+ chA rank2 + chA rank3 (in 32-MB increments)

Note: Channel A DRB3 and Channel B DRB3 must be equal for this mode, but the other DRBs may be different.

In all modes, if a DIMM is single sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Each Rank is represented by a byte. Each byte has the following format.

Bit	Access & Default	Description
7:0	R/W 00h	**Channel A DRAM Rank Boundary Address:** This 8 bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0s. Bit 7 may be programmed to a 1 in the highest DRB (DRB3) if 4 GBs of memory is present.

5.1.2 C0DRB1—Channel A DRAM Rank Boundary Address 1

MMIO Range:	MCHBAR
Address Offset:	101h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.3 C0DRB2—Channel A DRAM Rank Boundary Address 2

MMIO Range:	MCHBAR
Address Offset:	102h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.4 C0DRB3—Channel A DRAM Rank Boundary Address 3

MMIO Range:	MCHBAR
Address Offset:	103h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.5 C0DRA0—Channel A DRAM Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 108h
Default Value: 00h
Access: R/W
Size: 8 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the **CxDRA** registers describes the page size of a pair of ranks.

Channel and Rank Map:

Channel A Rank 0, 1: 108h
Channel A Rank 2, 3: 109h
Channel B Rank 0, 1: 188h
Channel B Rank 2, 3: 189h

Bit	Access & Default	Description
7		Reserved
6:4	R/W 000b	**Channel A DRAM odd Rank Attribute:** This 3 bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved
3		Reserved
2:0	R/W 000b	**Channel A DRAM even Rank Attribute:** This 3 bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved

5.1.6 C0DRA2—Channel A DRAM Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 109h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.7 C0DCLKDIS—Channel A DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 10Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register can be used to disable the system memory clock signals to each DIMM slot. This can significantly reduce EMI and Power concerns for clocks that go to unpopulated DIMMs. Clocks should be enabled based on whether a slot is populated, and what kind of DIMM is present.

Bit	Access & Default	Description
7:6		Reserved
5	R/W 0b	**DIMM Clock Gate Enable Pair 5** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
4	R/W 0b	**DIMM Clock Gate Enable Pair 4** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
3	R/W 0b	**DIMM Clock Gate Enable Pair 3** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
2	R/W 0b	**DIMM Clock Gate Enable Pair 2** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
1	R/W 0b	**DIMM Clock Gate Enable Pair 1** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
0	R/W 0b	**DIMM Clock Gate Enable Pair 0** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.

Note: Since there are multiple clock signals assigned to each Rank of a DIMM, it is important to clarify exactly which Rank width field affects which clock signal:

Channel	Rank	Clocks Affected
0	0 or 1	SCLK_A[2:0]/ SCLK_A[2:0]#
0	2 or 3	SCLK_A[5:3]/ SCLK_A[5:3]#
1	0 or 1	SCLK_B[2:0]/ SCLK_B[2:0]#
1	2 or 3	SCLK_B[5:3]/ SCLK_B[5:3]#

5.1.8 C0BNKARC—Channel A DRAM Bank Architecture

MMIO Range: MCHBAR
Address Offset: 10Eh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register is used to program the bank architecture for each Rank.

Bit	Access & Default	Description
15:8		Reserved
7:6	R/W 00b	Rank 3 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
5:4	R/W 00b	Rank 2 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
3:2	R/W 00b	Rank 1 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
1:0	R/W 00b	Rank 0 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved

5.1.9 C0DRT1—Channel A DRAM Timing Register

MMIO Range: MCHBAR
Address Offset: 114h
Default Value: 900122hh
Access: R/W, RO
Size: 32 bits

Bit	Access & Default	Description
31:24		Reserved
23:20	R/W 9h	**Activate to Precharge delay (t_{RAS}).** This bit controls the number of DRAM clocks for t_{RAS}. Minimum recommendations are beside their corresponding encodings. 0h – 3h = Reserved 4h – Fh = Four to Fifteen Clocks respectively.
19	RO 0b	**Reserved for Activate to Precharge Delay (t_{RAS}) MAX:** It is required that the Panic Refresh timer be set to a value less than the t_{RAS} maximum. Based on this setting, a Panic Refresh occurs before T_{RAS} maximum expiration and closes all the banks. This bit controls the maximum number of clocks that a DRAM bank can remain open. After this time period, the DRAM controller will guarantee to pre-charge the bank. This time period may or may not be set to overlap with time period that requires a refresh to happen. The DRAM controller includes a separate $t_{RAS-MAX}$ counter for every supported bank. With a maximum of four ranks, and four banks per rank, there are 16 counters per channel. 0 = 120 microseconds 1 = Reserved **Note:** This register will become Read Only with a value of 0 if the design does not implement these counters. $t_{RAS-MAX}$ is not required because a panic refresh will close all banks in a rank before $t_{RAS-MAX}$ expires.
18:10		Reserved
9:8	R/W 01b	**CASB Latency (tCL).** This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system. **Encoding** / **DDR CL** / **DDR2 CL** 00 / 3 / 5 01 / 2.5 / 4 10 / 2 / 3 11 / Reserved / Reserved
7		Reserved

Bit	Access & Default	Description
6:4	R/W 010b	**DRAM RAS to CAS Delay (t_{RCD}).** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. 000 = 2 DRAM clocks 001 = 3 DRAM clocks 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 – 111 = Reserved
3		Reserved
2:0	R/W 010b	**DRAM RAS Precharge (t_{RP}).** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. 000 = 2 DRAM clocks 001 = 3 DRAM clocks 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 – 111 = Reserved

5.1.10 C0DRC0—Channel A DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 120h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:30		Reserved
29	R/W 0b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28:11		Reserved
10:8	R/W 000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Refresh disabled 001 = Refresh enabled. Refresh interval 15.6 µsec 010 = Refresh enabled. Refresh interval 7.8 µsec 011 = Refresh enabled. Refresh interval 3.9 µsec 100 = Refresh enabled. Refresh interval 1.95 µsec 111 = Refresh enabled. Refresh interval 64 clocks (fast refresh mode) Other = Reserved
7	RO 0b	Reserved

Bit	Access & Default	Description
6:4	R/W 000 b	**Mode Select (SMS).** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000 = Post Reset state – When the (G)MCH exits reset (power-up or otherwise), the mode select field is cleared to “000”. During any reset sequence, while power is applied and reset is active, the (G)MCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During suspend, (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, (G)MCH will be reset – which will clear this bit field to “000” and maintain CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), (G)MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, (G)MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. 001 = NOP Command Enable – All processor cycles to DRAM result in a NOP command on the DRAM interface. 010 = All Banks Pre-charge Enable – All processor cycles to DRAM result in an “all banks precharge” command on the DRAM interface. 011 = Mode Register Set Enable – All processor cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. 101 = Reserved 110 = CBR Refresh Enable – In this mode all processor cycles to DRAM result in a CBR cycle on the DRAM interface 111 = Normal operation
3:2		Reserved
1:0	RO	**DRAM Type (DT).** This field is used to select between supported SDRAM types. This bit is controlled by the MTYPE strap signal. 00 = Reserved 01 = Dual Data Rate (DDR) SDRAM 10 = Second Revision Dual Data Rate (DDR2) SDRAM 11 = Reserved

5.1.11 C1DRB0—Channel B DRAM Rank Boundary Address 0

MMIO Range:	MCHBAR
Address Offset:	180h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.12 C1DRB1—Channel B DRAM Rank Boundary Address 1

MMIO Range:	MCHBAR
Address Offset:	181h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.13 C1DRB2—Channel B DRAM Rank Boundary Address 2

MMIO Range:	MCHBAR
Address Offset:	182h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.14 C1DRB3—Channel B DRAM Rank Boundary Address 3

MMIO Range:	MCHBAR
Address Offset:	183h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.15 C1DRA0—Channel B DRAM Rank 0,1 Attribute

MMIO Range:	MCHBAR
Address Offset:	188h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.16 C1DRA2—Channel B DRAM Rank 2,3 Attribute

MMIO Range:	MCHBAR
Address Offset:	189h
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.17 C1DCLKDIS—Channel B DRAM Clock Disable

MMIO Range:	MCHBAR
Address Offset:	18Ch
Default Value:	00h
Access:	R/W
Size:	8 bits

The operation of this register is detailed in the description for register C0DCLKDIS.

5.1.18 C1BNKARC—Channel B Bank Architecture

MMIO Range:	MCHBAR
Address Offset:	18Eh
Default Value:	0000h
Access:	R/W
Size:	16 bits

The operation of this register is detailed in the description for register C0BNKARC.

5.1.19 C1DRT1—Channel B DRAM Timing Register 1

MMIO Range:	MCHBAR
Address Offset:	194h
Default Value:	900122h
Access:	R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT1.

5.1.20 C1DRC0—Channel B DRAM Controller Mode 0

MMIO Range:	MCHBAR
Address Offset:	1A0h
Default Value:	00000000h
Access:	R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC0.

5.1.21 PMCFG—Power Management Configuration

MMIO Range: MCHBAR
Address Offset: F10h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:5		Reserved
4	R/W 0b	**Enhanced Power Management Features Enable** 0 = Legacy power management mode 1 = Reserved.
3:0		Reserved

5.1.22 PMSTS—Power Management Status

MMIO Range: MCHBAR
Address Offset: F14h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register is Reset by PWROK only.

Bit	Access & Default	Description
31:2		Reserved
1	R/WC/S 0b	**Channel B in self-refresh.** This bit is set by power management hardware after Channel B is placed in self refresh as a result of a Power State or a Reset Warn sequence. It is cleared by power management hardware before starting Channel B self refresh exit sequence initiated by a power management exit. It is cleared by BIOS in a warm reset (Reset# asserted while pwrok is asserted) exit sequence. 0 = Channel B not guaranteed to be in self-refresh. 1 = Channel B in Self-Refresh.
0	R/WC/S 0b	**Channel A in Self-refresh.** Set by power management hardware after Channel A is placed in self refresh as a result of a Power State or a Reset Warn sequence. It is cleared by power management hardware before starting Channel A self refresh exit sequence initiated by a power management exit. It is cleared by the BIOS in a warm reset (Reset# asserted while PWOK is asserted) exit sequence. 0 = Channel A not guaranteed to be in self-refresh. 1 = Channel A in Self-Refresh.

§

6 EPBAR Registers—Egress Port Register Summary

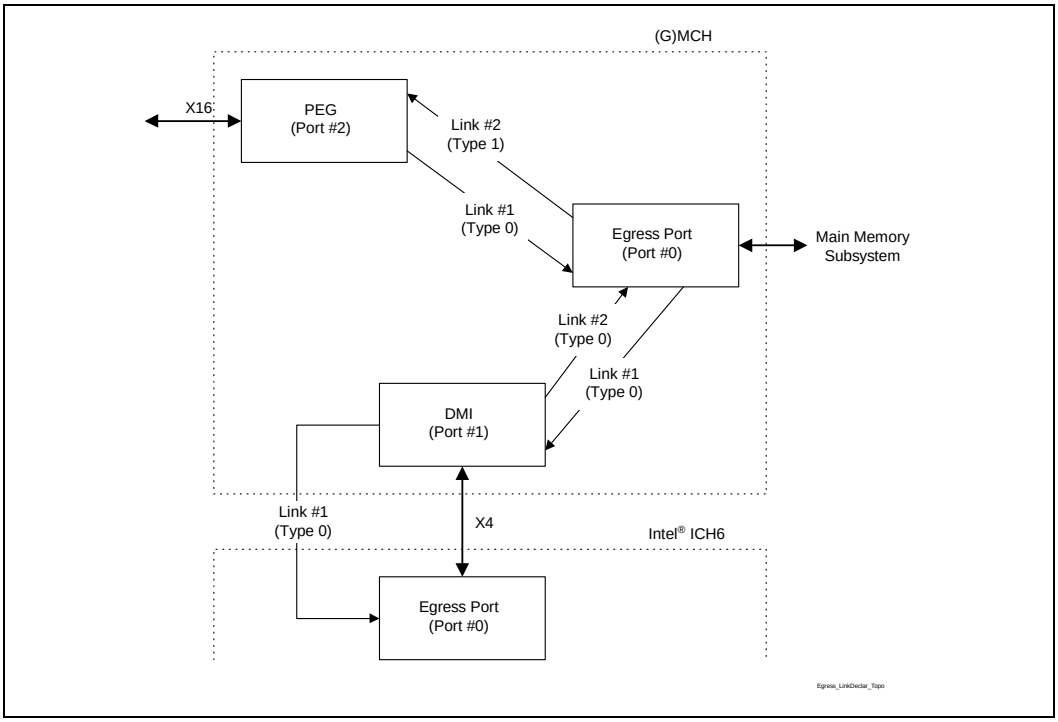
These registers are offset from the EPBAR base address.

Table 6-1. Egress Port Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
044h–047h	EPESD	EP Element Self Description	0000h	R/WO, RO
050h–053h	EPLE1D	EP Link Entry 1 Description	0100h	R/WO, RO
058h–05Fh	EPLE1A	EP Link Entry 1 Address	0000000000000000h	R/WO, RO
060h–063h	EPLE2D	EP Link Entry 2 Description	02000002h	R/WO, RO
068h–06Fh	EPLE2A	EP Link Entry 2 Address	0000000000080000h	RO

6.1 EP RCRB Configuration Register Details

Figure 6-1. Link Declaration Topology



6.1.1 EPESD—EP Element Self Description

MMIO Range: EPBAR
Address Offset: 044h
Default Value: 00000201h
Access: R/WO, RO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. A value of 00h indicates to configuration software that this is the default egress port.
23:16	R/WO 00h	**Component ID:** This field identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 02h	**Number of Link Entries:** This field indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express* x16 interface and DMI).
7:4		Reserved
3:0	RO 1h	**Element Type:** This field Indicates the type of the Root Complex Element. 1h = Port to system memory

6.1.2 EPLE1D—EP Link Entry 1 Description

MMIO Range: EPBAR
Address Offset: 050h
Default Value: 0100h
Access: R/WO, RO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** This bit indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.3 EPLE1A—EP Link Entry 1 Address

MMIO Range: EPBAR
Address Offset: 058h
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

This register provides the second part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field provides the memory-mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0		Reserved

6.1.4 EPLE2D—EP Link Entry 2 Description

MMIO Range: EPBAR
Address Offset: 060h
Default Value: 02000002h
Access: R/WO, RO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (PCI Express* x16 interface). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 1b	**Link Type:** 1 = Link points to configuration space of the integrated device that controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0b	**Link Valid** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.5 EPLE2A—EP Link Entry 2 Address

MMIO Range: EPBAR
Address Offset: 068h
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register provides the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28		Reserved
27:20	RO 00h	**Bus Number**
19:15	RO 0 0001b	**Device Number:** Target for this link is PCI Express* x16 port (Device 1).
14:12	RO 000b	**Function Number**
11:0		Reserved

§

7 DMIBAR Registers—Direct Media Interface (DMI) RCRB

This Root Complex Register Block (RCRB) controls the (G)MCH-Intel ICH6 serial interconnect. The base address of this space is programmed in DMIBAR in device 0 configuration space. These registers are offset from the DMIBAR base address

Table 7-1. DMI Register Address Map Summary

Address offset	Register Symbol	Register Name	PCI Dev #
000–003h	DMIVCECH	DMI Virtual Channel Enhanced Capability Header	DMIBAR
004–007h	DMIPVCCAP1	DMI Port VC Capability Register 1	DMIBAR
008–00Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	DMIBAR
00C–00Dh	DMIPVCCTL	DMI Port VC Control	DMIBAR
00E–00Fh	—	**Reserved**	DMIBAR
010–013h	DMIVC0RCAP	DMI VC0 Resource Capability	DMIBAR
014–017h	DMIVC0RCTL	DMI VC0 Resource Control	DMIBAR
018–019h	—	**Reserved**	DMIBAR
01A–01Bh	DMIVC0RSTS	DMI VC0 Resource Status	DMIBAR
01C–01Fh	DMIVC1RCAP	DMI VC1 Resource Capability	DMIBAR
020–023h	DMIVC1RCTL	DMI VC1 Resource Control	DMIBAR
024–025h	—	**Reserved**	DMIBAR
026–027h	DMIVC1RSTS	DMI VC1 Resource Status	DMIBAR
028–083h	—	**Reserved**	DMIBAR
084–087h	DMILCAP	DMI Link Capabilities	DMIBAR
088–089h	DMILCTL	DMI Link Control	DMIBAR
08A–08Bh	DMILSTS	DMI Link Status	DMIBAR
08C–FFFh	—	**Reserved**	DMIBAR

7.1 Direct Media Interface (DMI) RCRB Register Details

7.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability Header

MMIO Range: DMIBAR
Address Offset: 000h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability:** This field indicates the next item in the list.
19:16	RO 1h	**Capability Version:** This field indicates support as a version 1 capability structure.
15:0	RO 0002h	**Capability ID:** This field indicates this is the Virtual Channel capability item.

7.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

MMIO Range: DMIBAR
Address Offset: 004h
Default Value: 00000001h
Access: R/WO, RO
Size: 32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:12		Reserved
11:10	RO 00b	**Port Arbitration Table Entry Size (PATS):** This field indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports).
9:8	RO 00b	**Reference Clock (RC)** Fixed at 10 ns.
7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVC):** This field indicates that there are no additional VCs of low priority with extended capabilities.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates that there is one additional VC (VC1) that exists with extended capabilities.

7.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

MMIO Range: DMIBAR
Address Offset: 008h
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (ATO):** This field indicates that no table is present for VC arbitration since it is fixed.
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the VC arbitration is fixed in the root complex. VC1 is highest priority and VC0 is lowest priority.

7.1.4 DMIPVCCTL—DMI Port VC Control

MMIO Range: DMIBAR
Address Offset: 00Ch
Default Value: 00000000h
Access: R/W, RO
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	RO 0b	**Load VC Arbitration Table (LAT):** This field indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

7.1.5 DMIVC0RCAP—DMI VC0 Resource Capability

MMIO Range: DMIBAR
Address Offset: 010h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** This VC implements no port arbitration table since the arbitration is fixed.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This VC implements fixed arbitration, and therefore this field is not used.
15	RO 0b	**Reject Snoop Transactions (RTS):** This VC must be able to take snoopable transactions.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates that this VC uses fixed port arbitration.

7.1.6 DMIVC0RCTL0—DMI VC0 Resource Control

MMIO Range: DMIBAR
Address Offset: 014h
Default Value: 8000007Fh
Access: R/W, RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27		Reserved
26:24	RO 000b	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	RO 0b	**Load Port Arbitration Table (LAT):** The root complex does not implement an arbitration table for this virtual channel.
15:8		Reserved
7:1	R/W 7Fh	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

7.1.7 DMIVC0RSTS—DMI VC0 Resource Status

MMIO Range: DMIBAR
Address Offset: 01Ah
Default Value: 00000002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC Negotiation Pending (NP):** 0 = Virtual channel is Not being negotiated with ingress ports. 1 = Virtual channel is still being negotiated with ingress ports.
0	RO 0b	**Port Arbitration Tables Status (ATS):** There is no port arbitration table for this VC, so this bit is reserved at 0.

7.1.8 DMIVC1RCAP—DMI VC1 Resource Capability

MMIO Range: DMIBAR
Address Offset: 01Ch
Default Value: 00008001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** This field indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	RO 1b	**Reject Snoop Transactions (RTS):** All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates the port arbitration capability is time-based WRR of 128 phases.

7.1.9 DMIVC1RCTL1—DMI VC1 Resource Control

MMIO Range: DMIBAR
Address Offset: 020h
Default Value: 00100000h
Access: R/W, RO
Size: 32 bits

This register controls the resources associated with Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**Virtual Channel Enable (EN):** 0 = Disable. 1 = Enable.
30:27	RO 0h	Reserved
26:24	R/W 001b	**Virtual Channel Identifier (ID):** This field indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** This field indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16:8		Reserved
7:1	R/W 00h	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

7.1.10 DMIVC1RSTS—DMI VC1 Resource Status

MMIO Range: DMIBAR
Address Offset: 026h
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC Negotiation Pending (NP):** 0 = Virtual channel is Not being negotiated with ingress ports. 1 = Virtual channel is still being negotiated with ingress ports.
0		Reserved

7.1.11 DMILCAP—DMI Link Capabilities

MMIO Range: DMIBAR
Address Offset: 084h
Default Value: 00012C41h
Access: R/WO, RO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency (EL1).** L1 not supported on DMI.
14:12	R/WO 010b	**L0s Exit Latency (EL0):** This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	RO 11b	**Active State Link PM Support (APMS):** This field indicates that L0s is supported on DMI.
9:4	RO 4h	**Maximum Link Width (MLW):** This field indicates the maximum link width is 4 ports.
3:0	RO 1h	**Maximum Link Speed (MLS):** This field indicates the link speed is 2.5 Gb/s.

7.1.12 DMILCTL—DMI Link Control

MMIO Range: DMIBAR
Address Offset: 088h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of DMI.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	**Extended Synch (ES):** 1 = Forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 prior to entering L0.
6:2		Reserved
1:0	R/W 00b	**Active State Link PM Control (APMC):** Indicates whether DMI should enter L0s. 00 = Disabled 01 = L0s entry enabled 10 = Reserved 11 = Reserved

7.1.13 DMILSTS—DMI Link Status

MMIO Range: DMIBAR
Address Offset: 08Ah
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access & Default	Description
15:10		Reserved
9:4	RO 00h	**Negotiated Link Width (NLW):** This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). Negotiated link width is x4 (000100b). All other encodings are reserved.
3:0	RO 1h	**Link Speed (LS)** Link is 2.5 Gb/s.

§

8 Host-PCI Express* Bridge Registers (D1:F0) (Intel® 82915G/82915P/82915PL Only)

Device 1contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It is typically referred to as PCI Express* x16 Graphics Interface port. In addition, it also functions as the virtual PCI-to-PCI bridge.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits: Reserved and Preserved:

- Reserved for future R/W implementations; software must preserve value read for writes to bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type that have historically been the typical definition for Reserved.

It is important to note that most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 8-1. Host-PCI Express* Graphics Bridge Register Address Map (D1:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2581h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, R/W
06–07h	PCISTS1	PCI Status	0000h	RO, R/W
08h	RID1	Revision Identification	See register description	RO
09–0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W
0Dh	—	**Reserved**	—	—
0Eh	HDR1	Header Type	01h	RO

Address Offset	Register Symbol	Register Name	Default Value	Access
0F–17h	—	Reserved	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RO
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	—	**Reserved**	—	—
1Ch	IOBASE1	I/O Base Address	F0h	RO
1Dh	IOLIMIT1	I/O Limit Address	00h	R/W
1Eh–1Fh	SSTS1	Secondary Status	00h	RO, R/W/C
20–21h	MBASE1	Memory Base Address	FFF0h	R/W
22–23h	MLIMIT1	Memory Limit Address	0000h	R/W
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28–33h	—	**Reserved**	—	—
34h	CAPPTR1	Capabilities Pointer	88h	RO
35–3Bh	—	Reserved	—	—
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	00h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
40–7Fh	—	**Reserved**	—	—
80–83h	PM_CAPID1	Power Management Capabilities	19029001h or 1902A001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RO, R/W
94–97h	MA	Message Address	00000000h	RO, R/W
98–99h	MD	Message Data	0000h	R/W
9A–9Fh	—	**Reserved**	—	—
A0–A1h	PEG_CAPL	PCI Express* Capability List	0010h	RO
A2–A3h	PEG_CAP	PCI Express Capabilities	0141h	RO
A4–A7h	DCAP	Device Capabilities	00000000h	RO
A8–A9h	DCTL	Device Control	0000h	R/W
AA–ABh	DSTS	Device Status	0000h	RO
AC–AFh	LCAP	Link Capabilities	02012E01h	R/WO
B0–B1h	LCTL	Link Control	0000h	RO, R/W

Address Offset	Register Symbol	Register Name	Default Value	Access
B2–B3h	LSTS	Link Status	1001h	RO
B4–B7h	SLOTCAP	Slot Capabilities	00000000h	R/WO
B8–B9h	SLOTCTL	Slot Control	01C0h	R/W
BA–BBh	SLOTSTS	Slot Status	0X00h	RO, R/W/C
BC–BDh	RCTL	Root Control	0000h	R/W
BE–BFh	—	**Reserved**	—	—
C0–C3h	RSTS	Root Status	00000000h	RO, R/W/C
C4–EBh	—	Reserved	—	—
EC–EFh	PEGLC	PCI Express*-Graphics Legacy Control	00000000h	R/W, RO
F0–FFh	—	**Reserved**	—	—
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO, R/WO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000001h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	R/W
10E–10Fh	—	**Reserved**	—	—
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	8000007Fh	RO, R/W
118–119h	—	**Reserved**	—	—
11A–11Bh	VC0RSTS	VC0 Resource Status	0000h	RO
11C–11Fh	VC1RCAP	VC1 Resource Capability	00008000h	RO
120–123h	VC1RCTL	VC1 Resource Control	01000000h	RO, R/W
124–125h	—	**Reserved**	—	—
126–127h	VC1RSTS	VC1 Resource Status	0000h	RO
128–13Fh	—	**Reserved**	—	—
140–143h	RCLDECH	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, R/WO
148–14Fh	—	**Reserved**	—	—
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
154–157h	—	**Reserved**	—	—
158–15Fh	LE1A	Link Entry 1 Address	000000000 0000000h	R/WO
160–217h	—	**Reserved**	—	—
218–21Fh	PEGSSTS	PCI Express*-Graphics Sequence Status	000000000 0000FFFh	RO
220–FFFh	—	**Reserved**	—	—

8.1 Host-PCI Express* Bridge PCI Register Details (D1:F0)

8.1.1 VID1—Vendor Identification (D1:F0)

PCI Device: 1
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

8.1.2 DID1—Device Identification (D1:F0)

PCI Device: 1
Address Offset: 02h
Default Value: 2581h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2581h	**Device Identification Number (DID1):** This field is an identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express* Graphics port).

8.1.3 PCICMD1—PCI Command (D1:F0)

PCI Device: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**INTA Assertion Disable:** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD asserts and de-assert messages.
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.
8	R/W 0b	**SERR Message Enable (SERRE1):** This bit is an enable bit for Device 1 SERR messaging. The (G)MCH communicates the SERR# condition by sending a SERR message to the Intel® ICH6. This bit, when set, enables reporting of non-fatal and fatal errors to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express* specific bits in the Device Control Register 0 = The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1 = The (G)MCH is enabled to generate SERR messages which will be sent to the ICH6 for specific Device 1 error conditions that are individually enabled in the BCTRL1 register and for all non-fatal and fatal errors generated on the primary side of the virtual PCI to PCI Express bridge (not those received by the secondary side). The error status is reported in the PCISTS1 register.
7		Reserved
6	R/WO 0b	**Parity Error Enable (PERRE):** This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register **cannot** be set. 1 = Master Data Parity Error bit in PCI Status register **can** be set.
5	RO 0b	**VGA Palette Snoop:** Hardwired to 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0.

Bit	Access & Default	Description
2	R/W 0b	**Bus Master Enable (BME):** This bit does not affect forwarding of completions from the primary interface to the secondary interface. 0 = This device is prevented from making memory or I/O requests to its primary bus. Note that according to the PCI specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, I/O writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0h with byte enables de-asserted. Reads will be forwarded to memory address 0h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.
1	R/W 0b	**Memory Access Enable (MAE)** 0 = All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0b	**IO Access Enable (IOAE)** 0 = All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1 and IOLIMIT1 registers.

8.1.4 PCISTS1—PCI Status (D1:F0)

PCI Device: 1
Address Offset: 06h
Default Value: 0000h
Access: RO, R/W/C
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge in the (G)MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device.
14	R/WC 0b	**Signaled System Error (SSE):** 1 = This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is '1'. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.

Bit	Access & Default	Description
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00b	**DEVSELB Timing (DEVT):** This device is not the subtractive decoded device on bus 0. This bit field is therefore hardwired to 00b to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express* x16 Graphics Interface's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality, there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC; however, for this implementation, an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6		Reserved
5	RO 0b	**66/60MHz capability (CAP66):** Hardwired to 0.
4	RO 1b	**Capabilities List:** This bit indicates that a capabilities list is present. Hardwired to 1.
3	RO 0b	**INTA Status:** This field indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0		Reserved

8.1.5 RID1—Revision Identification (D1:F0)

PCI Device: 1
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH device 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID1):** This field indicates the number of times that this device in this component has been "stepped" through the manufacturing process. Refer to the *Intel® 82915G/82915P/82915PL/82915GV/82915GL/82910GL Express Chipset Specification Update* for the value of the Revision ID Register.

8.1.6 CC1—Class Code (D1:F0)

PCI Device: 1
Address Offset: 09h
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This field indicates the base class code for this device. 06h = Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** This field indicates the sub-class code for this device. 04h = PCI-to-PCI Bridge.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

8.1.7 CL1—Cache Line Size (D1:F0)

PCI Device: 1
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Cache Line Size (Scratch pad):** This field is implemented by PCI Express* devices as a read/write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

8.1.8 HDR1—Header Type (D1:F0)

PCI Device: 1
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** This field returns 01h to indicate that this is a single function device with bridge header layout.

8.1.9 PBUSN1—Primary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

8.1.10 SBUSN1—Secondary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 19h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge i.e. to PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express*-G.

8.1.11 SUBUSN1—Subordinate Bus Number (D1:F0)

PCI Device: 1
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the PCI Express*-G segment, this register will contain the same value as the SBUSN1 register.

8.1.12 IOBASE1—I/O Base Address (D1:F0)

PCI Device: 1
Address Offset: 1Ch
Default Value: F0h
Access: RO
Size: 8 bits

This register controls the processor-to-PCI Express Graphics I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access & Default	Description
7:4	R/W Fh	**I/O Address Base (IOBASE):** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express*-G. BIOS must not set this register to 00h; otherwise, 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0		Reserved

8.1.13 IOLIMIT1—I/O Limit Address (D1:F0)

PCI Device: 1
Address Offset: 1Dh
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the processor-to-PCI Express Graphics I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purposes of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0h	**I/O Address Limit (IOLIMIT):** This field corresponds to A[15:12] of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express* hierarchy associated with this device.
3:0		Reserved

8.1.14 SSTS1—Secondary Status (D1:F0)

PCI Device: 1
Address Offset: 1Eh
Default Value: 00h
Access: RO, R/W/C
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express Graphics side) of the "virtual" PCI-PCI Bridge in the (G)MCH.

Bit	Access & Default	Description
15	R/WC 0b	**Detected Parity Error (DPE):** 1 = The MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC 0b	**Received System Error (RSE):** 1 = Secondary side sends an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC 0b	**Received Master Abort (RMA):** 1 = Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a completion with **Unsupported Request** Completion Status.
12	R/WC 0b	**Received Target Abort (RTA):** 1 = Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a completion with **Completer Abort** Completion Status.
11	RO 0b	**Signaled Target Abort (STA):** Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00b	**DEVSELB Timing (DEVT):** Hardwired to 0.
8	R/WC 0b	**Master Data Parity Error (SMDPE).** 1 = The MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). Note: This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6		Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Hardwired to 0.
4:0		Reserved

8.1.15 MBASE1—Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 20h
Default Value: FFF0h
Access: R/W
Size: 16 bits

This register controls the processor to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Memory Address Base (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0		Reserved

8.1.16 MLIMIT1—Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 22h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the processor-to-PCI Express Graphics non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. Configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express Graphics address ranges (typically, where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically, graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor-PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access & Default	Description
15:4	R/W 000h	**Memory Address Limit (MLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express*.
3:0		Reserved

8.1.17 PMBASE1—Prefetchable Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 24h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register, in conjunction with the corresponding Upper Base Address register, controls the processor-to-PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Prefetchable Memory Base Address (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** This field indicates that the bridge supports only 32 bit addresses.

8.1.18 PMLIMIT1—Prefetchable Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 26h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register, in conjunction with the corresponding Upper Limit Address register, controls the processor-to-PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	R/W 000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** This field indicates the bridge supports only 32 bit addresses.

8.1.19 CAPPTR1—Capabilities Pointer (D1:F0)

PCI Device: 1
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

8.1.20 INTRLINE1—Interrupt Line (D1:F0)

PCI Device: 1
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather device drivers and operating systems use it to determine priority and vector information.

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller this device's interrupt pin is connected to.

8.1.21 INTRPIN1—Interrupt Pin (D1:F0)

PCI Device: 1
Address Offset: 3Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a single function device, the PCI Express* device specifies INTA as its interrupt pin. 01h = INTA

8.1.22 BCTRL1—Bridge Control (D1:F0)

PCI Device: 1
Address Offset: 3Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within (G)MCH (e.g., VGA compatible address ranges mapping).

Bit	Access & Default	Description
15:12		Reserved
11	RO 0b	**Discard Timer SERR Enable:** Hardwired to 0.
10	RO 0b	**Discard Timer Status:** Hardwired to 0.
9	RO 0b	**Secondary Discard Timer:** Hardwired to 0.
8	RO 0b	**Primary Discard Timer:** Hardwired to 0.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Hardwired to 0.
6	R/W 0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express* Port.
5	RO 0b	**Master Abort Mode (MAMODE):** When acting as a master, unclaimed reads that experience a master abort returns all 1s and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W 0b	**VGA 16-bit Decode:** This bit enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	R/W 0b	**VGA Enable (VGAEN):** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].

Bit	Access & Default	Description
2	R/W 0b	**ISA Enable (ISAEN):** This bit is needed to exclude legacy resource decode to route ISA resources to legacy decode path. This bit modifies the response by the (G)MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express Graphics. 1 = (G)MCH will not forward to PCI Express Graphics any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express Graphics, these cycles are forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W 0b	**SERR Enable (SERREN)** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RO 0b	**Parity Error Response Enable (PEREN):** This bit controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP. 0 = Master Data Parity Error bit in Secondary Status register **cannot** be set. 1 = Master Data Parity Error bit in Secondary Status register **can** be set..

8.1.23 PM_CAPID1—Power Management Capabilities (D1:F0)

PCI Device: 1
Address Offset: 80h
Default Value: 1902 9001h or 1902 A001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support:** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot, and D3cold. This device is not required to do anything to support D3hot and D3cold; it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0b	**D2:** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current:** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0 b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock:** Hardwired to 0 to indicate this device does NOT support PME# generation.
18:16	RO 010b	**PCI PM CAP Version:** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the *PCI Power Management Interface Specification*.
15:8	RO 90h or A0h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express* capability at A0h.
7:0	RO 01h	**Capability ID:** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

8.1.24 PM_CS1—Power Management Control/Status (D1:F0)

PCI Device: 1
Address Offset: 84h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**PME Status:** This bit indicates that this device does not support PME# generation from $D3_{cold}$.
14:13	RO 00b	**Data Scale:** This field indicates that this device does not support the power management data register.
12:9	RO 0h	**Data Select:** This field indicates that this device does not support the power management data register.
8	R/W/S 0b	**PME Enable:** This bit indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state to be fully functional. There is no hardware functionality required to support these power states.

8.1.25 SS_CAPID—Subsystem ID and Vendor ID Capabilities (D1:F0)

PCI Device: 1
Address Offset: 88h
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16		Reserved
15:8	RO 80h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0D h	**Capability ID:** A value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

8.1.26 SS—Subsystem ID and Subsystem Vendor ID (D1:F0)

PCI Device: 1
Address Offset: 8Ch
Default Value: 00008086h
Access: RO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field identifies the manufacturer of the subsystem and is the same as the vendor ID that is assigned by the PCI Special Interest Group.

8.1.27 MSI_CAPID—Message Signaled Interrupts Capability ID (D1:F0)

PCI Device: 1
Address Offset: 90h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL [0] at 7Fh). In that case walking this linked list will skip this capability and, instead, go directly from the PCI PM capability to the PCI Express capability.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list that is the PCI Express* capability.
7:0	RO 05h	**Capability ID:** 05h = Identifies this linked list item (capability structure) as being for MSI registers.

8.1.28 MC—Message Control (D1:F0)

PCI Device: 1
Address Offset: 92h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8		Reserved
7	RO 0b	**64-bit Address Capable:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. 000 = 1 message allocated 001–111 = Reserved
3:1	RO 000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. 000 = 1 message requested 001–111 = Reserved
0	R/W 0b	**MSI Enable (MSIEN)** Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

8.1.29 MA—Message Address (D1:F0)

PCI Device: 1
Address Offset: 94h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Message Address:** This field is used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align:** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

8.1.30 MD—Message Data (D1:F0)

PCI Device: 1
Address Offset: 98h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data:** This field provides a base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. This register supplies the lower 16 bits.

8.1.31 PEG_CAPL—PCI Express* Capability List (D1:F0)

PCI Device: 1
Address Offset: A0h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability:** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express* specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express extended configuration space.
7:0	RO 10h	**Capability ID:** This field identifies this linked list item (capability structure) as being for PCI Express registers.

8.1.32 PEG_CAP—PCI Express*-G Capabilities (D1:F0)

PCI Device: 1
Address Offset: A2h
Default Value: 0141h
Access: RO
Size: 16 bits

Indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14		Reserved
13:9	RO 00h	**Interrupt Message Number:** Hardwired to 0.
8	R/WO 1b	**Slot Implemented** 0 = The PCI Express* Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. BIOS must initialize this field appropriately if a slot connection is not implemented.
7:4	RO 4h	**Device/Port Type:** Hardwired to 0100 to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version:** Hardwired to 1 as it is the first version.

8.1.33 DCAP—Device Capabilities (D1:F0)

PCI Device: 1
Address Offset: A4h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register indicates PCI Express link capabilities.

Bit	Access & Default	Description
31:6		Reserved
5	RO 0b	**Extended Tag Field Supported:** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO 00b	**Phantom Functions Supported:** Hardwired to 0.
2:0	RO 000b	**Max Payload Size:** Hardwired to indicate 128B maximum supported payload for Transaction Layer Packets (TLP).

8.1.34 DCTL—Device Control (D1:F0)

PCI Device: 1
Address Offset: A8h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8		Reserved
7:5	R/W 000b	**Max Payload Size** 000 = 128B maximum supported payload for Transaction Layer Packets (TLP). As a receiver, the device must handle TLPs as large as the set value; as transmitter, the device must not generate TLPs exceeding the set value. **Note:** All other encodings are reserved.
4		Reserved
3	R/W 0b	**Unsupported Request Reporting Enable:** 0 = Disable. 1 = Enable. Unsupported Requests will be reported. Note that reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W 0b	**Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W 0b	**Non-Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W 0b	**Correctable Error Reporting Enable:** 0 = Disable. 1 = Enable. Correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

8.1.35 DSTS—Device Status (D1:F0)

PCI Device: 1
Address Offset: AAh
Default Value: 0000h
Access: RO
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register.

Note: The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6		Reserved
5	RO 0b	**Transactions Pending** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4		Reserved
3	R/WC 0b	**Unsupported Request Detected:** 1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
2	R/WC 0b	**Fatal Error Detected:** 1 = Fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	R/WC 0b	**Non-Fatal Error Detected:** 1 = Non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	R/WC 0b	**Correctable Error Detected:** 1 = Correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. **Note:** The (G)MCH may report a false 8B/10B Receiver Error when exiting L0s. This is reported thru the Correctable Error Detected bit CESTS device 1, offset 1D0h, Bit [0]. This will reduce the value of Receiver Error detection when L0s is enabled. Disable L0s for accurate Receiver Error reporting.

8.1.36 LCAP—Link Capabilities (D1:F0)

PCI Device: 1
Address Offset: ACh
Default Value: 02012E01h
Access: R/WO
Size: 16 bits

This register indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field indicates the PCI Express* port number for the given PCI Express link. This field matches the value in Element Self Description [31:24].
23:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency:** This field indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	R/WO 010b	**L0s Exit Latency:** This field indicates the length of time this Port requires to complete the transition from L0s to L0. The value 010 b indicates the range of 128 ns to less than 256 ns. If this field is required to be any value other than the default, BIOS must initialize it accordingly. **Note:** When PCI Express* is operating with separate reference clocks, L0s exit latency may be greater than the setting in the L0s Exit Latency Register. Expect longer exit latency then setting in L0s Exit Latency Register. The link may enter Recovery state before reaching L0. System BIOS can program the appropriate Exit Latency and advertised N_FTS value if it detects that the downstream device is not using the common reference clock (indicated in the Slot Clock Configuration bit 12 of the device's Link Status Register)
11:10	R/WO 11b	**Active State Link PM Support:** L0s & L1 entry supported.
9:4	RO 10h	**Max Link Width:** Hardwired to indicate X16. When Force X1 mode is enabled on this PCI Express* x16 Graphics Interface device, this field reflects X1 (01h).
3:0	RO 1h	**Max Link Speed:** Hardwired to indicate 2.5 Gb/s.

8.1.37 LCTL—Link Control (D1:F0)

PCI Device: 1
Address Offset: B0h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register allows control of PCI Express link.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	**Reserved.** Must be 0 when writing this register.
6	R/W 0b	**Common Clock Configuration** 0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock. Components use this common clock configuration information to report the correct L0s and L1 Exit Latencies.
5	R/W 0b	**Retrain Link** 0 = Normal operation 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	R/W 0b	**Link Disable** 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 0 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO 0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2		Reserved
1:0	R/W 00b	**Active State PM:** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

8.1.38 LSTS—Link Status (D1:F0)

PCI Device: 1
Address Offset: B2h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access & Default	Description
15:13		Reserved
12	RO 1b	**Slot Clock Configuration** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training:** 1 = Link training is in progress. Hardware clears this bit once Link training is complete.
10	RO 0b	**Training Error:** 1 = This bit is set by hardware upon detection of unsuccessful training of the Link to the L0 Link state.
9:4	RO 00h	**Negotiated Width:** This field indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h = Reserved 01h = X1 04h = Reserved 08h = Reserved 10h = X16 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed:** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

8.1.39 SLOTCAP—Slot Capabilities (D1:F0)

PCI Device: 1
Address Offset: B4h
Default Value: 00000000h
Access: R/WO
Size: 32 bits

PCI Express slot-related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
31:19	R/WO 0000h	**Physical Slot Number:** This field indicates the physical slot number attached to this Port. This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18:17		Reserved
16:15	R/WO 00b	**Slot Power Limit Scale:** This field specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO 00h	**Slot Power Limit Value:** In combination with the Slot Power Limit Scale value, this field specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO 0b	**Hot-plug Capable:** This field indicates that this slot is capable of supporting Hot-plug operations.
5	R/WO 0b	**Hot-plug Surprise:** This field indicates that a device present in this slot might be removed from the system without any prior notification.
4	R/WO 0b	**Power Indicator Present:** This field indicates that a Power Indicator is implemented on the chassis for this slot.
3	R/WO 0b	**Attention Indicator Present:** This field indicates that an Attention Indicator is implemented on the chassis for this slot.
2:1		Reserved
0	R/WO 0b	**Attention Button Present:** This field indicates that an Attention Button is implemented on the chassis for this slot. The Attention Button allows the user to request hot-plug operations.

8.1.40 SLOTCTL—Slot Control (D1:F0)

PCI Device: 1
Address Offset: B8h
Default Value: 01C0h
Access: R/W
Size: 16 bits

PCI Express slot related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
15:10		Reserved
9:8	R/W 01b	**Power Indicator Control:** Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator and cause the Port to send the appropriate POWER_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
7:6	R/W 11b	**Attention Indicator Control:** Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator and cause the Port to send the appropriate ATTENTION_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
5	R/W 0b	**Hot plug Interrupt Enable:** 0 = Disable. 1 = Enables generation of hot plug interrupt on enabled hot plug events.
4	R/W 0b	**Command Completed Interrupt Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt when the Hot plug controller completes a command.
3	R/W 0b	**Presence Detect Changed Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt or wake message on a presence detect changed event.
2:1		Reserved
0	R/W 0b	**Attention Button Pressed Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt or wake message on an attention button pressed event.

8.1.41 SLOTSTS—Slot Status (D1:F0)

PCI Device: 1
Address Offset: BAh
Default Value: 0X00h
Access: RO, R/W/C
Size: 16 bits

PCI Express slot-related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
15:7		Reserved
6	RO Xb	**Presence Detect State:** This bit indicates the presence of a card in the slot. 0 = Slot Empty 1 = Card Present in slot.
5		Reserved
4	R/WC 0b	**Command Completed:** 1 = Hot plug controller completed an issued command.
3	R/WC 0b	**Presence Detect Changed:** 1 = Presence Detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2:1		Reserved
0	R/WC 0b	**Attention Button Pressed:** 1 = Attention Button is pressed.

8.1.42 RCTL—Root Control (D1:F0)

PCI Device: 1
Address Offset: BCh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4		Reserved
3	R/W 0b	**PME Interrupt Enable** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W 0b	**System Error on Fatal Error Enable:** This bit controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W 0b	**System Error on Non-Fatal Uncorrectable Error Enable:** This bit controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0b	**System Error on Correctable Error Enable:** This bit controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

8.1.43 RSTS—Root Status (D1:F0)

PCI Device: 1
Address Offset: C0h
Default Value: 00000000h
Access: RO, R/W/C
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18		Reserved
17	RO 0b	**PME Pending:** This bit indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/W/C 0b	**PME Status:** This bit indicates that the requestor ID indicated in the PME Requestor ID field asserted PME. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID:** This field indicates the PCI requestor ID of the last PME requestor.

8.1.44 PEGLC—PCI Express*-G Legacy Control

PCI Device: 1
Address Offset: ECh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

Bit	Access & Default	Description
31:3	RO 0000 0000h	Reserved
2	R/W 0b	**PME GPE Enable (PMEGPE):** 0 = Do not generate GPE PME message when PME is received. 1 = Enable. Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PCI Express* x16 Graphics Interface port under legacy OSs.
1	R/W 0b	**Hot-Plug GPE Enable (HPGPE)** 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Enable. Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PCI Express* x16 Graphics Interface port under legacy OSs.
0	R/W 0b	**General Message GPE Enable (GENGPE)** 0 = Do not forward received GPE assert/deassert messages. 1 = Enable. Forward received GPE assert/deassert messages. These general GPE message can be received via the PCI Express* x16 Graphics Interface port from an external Intel device and will be subsequently forwarded to the Intel® ICH6 (via Assert_GPE and Deassert_GPE messages on DMI).

8.1.45 VCECH—Virtual Channel Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 100h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities.

Note: Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability:** The Link Declaration Capability is the next in the PCI Express* extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version:** Hardwired to 1 to indicate compliances with the 1.0a version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID:** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

8.1.46 PVCCAP1—Port VC Capability Register 1 (D1:F0)

PCI Device: 1
Address Offset: 104h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

8.1.47 PVCCAP2—Port VC Capability Register 2 (D1:F0)

PCI Device: 1
Address Offset: 108h
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset:** This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority, VC0 is the lowest priority.

8.1.48 PVCCTL—Port VC Control (D1:F0)

PCI Device: 1
Address Offset: 10Ch
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0		Reserved

8.1.49 VC0RCAP—VC0 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 110h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.50 VC0RCTL—VC0 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 114h
Default Value: 8000007Fh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable:** For VC0, this is hardwired to 1 and read only as VC0 can never be disabled.
30:27		Reserved
26:24	RO 000b	**VC0 ID:** This field assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8		Reserved
7:1	R/W 7Fh	**TC/VC0 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map:** Traffic Class 0 is always routed to VC0.

8.1.51 VC0RSTS—VC0 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 11Ah
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC0 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.52 VC1RCAP—VC1 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 11Ch
Default Value: 00008000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 1b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.53 VC1RCTL—VC1 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 120h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**VC1 Enable** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express* port); a 0 read from this bit indicates that the Virtual Channel is currently disabled. **Notes:** • To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. • To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. • Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. • Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27		Reserved
26:24	R/W 001b	**VC1 ID:** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:8		Reserved
7:1	R/W 00h	**TC/VC1 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b	**TC0/VC1 Map:** Traffic Class 0 is always routed to VC0.

8.1.54 VC1RSTS—VC1 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 126h
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC1 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as when the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.55 RCLDECH—Root Complex Link Declaration Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 140h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PCI Express* x16 Graphics Interface) to other elements of the root complex component to which it belongs. See the PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability:** This is the last capability in the PCI Express* extended capabilities list.
19:16	RO 1h	**Link Declaration Capability Version:** Hardwired to 1 to indicate compliances with the 1.0a version of the PCI Express specification.
15:0	RO 0005h	**Extended Capability ID:** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

Note: See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

8.1.56 ESD—Element Self Description (D1:F0)

PCI Device: 1
Address Offset: 144h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. The egress port of the component to provide arbitration to this Root Complex Element uses this port number value.
23:16	R/WO 00h	**Component ID:** This field indicates the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 01h	**Number of Link Entries:** This field indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as peer-to-peer capabilities in this topology are not reported).
7:4		Reserved
3:0	RO 0h	**Element Type:** This field indicates the type of the Root Complex Element. 0h = root port.

8.1.57 LE1D—Link Entry 1 Description (D1:F0)

PCI Device: 1
Address Offset: 150h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field indicates the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

8.1.58 LE1A—Link Entry 1 Address (D1:F0)

PCI Device: 1
Address Offset: 158h
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

This register provides the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field indicates memory-mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0		Reserved

8.1.59 PEGSSTS—PCI Express*-G Sequence Status (D1:F0)

PCI Device: 1
Address Offset: 218h
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60		Reserved
59:48	RO 000h	**Next Transmit Sequence Number:** Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44		Reserved
43:32	RO 000h	**Next Packet Sequence Number:** Packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28		Reserved
27:16	RO 000h	**Next Receive Sequence Number:** This is the sequence number associated with the TLP that is expected to be received next.
15:12		Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number:** This is the sequence number associated with the last acknowledged TLP.

§

9 Integrated Graphics Device Registers (D2:F0) (Intel® 82915G/82915GV/82915GL/ 82910GL GMCH Only)

Device 2 contains registers for the internal graphics functions. Table 9-1 lists the PCI configuration registers in order of ascending offset address. Function 0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device 0, offset 52h). The following sections describe Device 2 PCI configuration registers only.

Table 9-1. Integrated Graphics Device Register Address Map (D2:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2582h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
0Fh	—	**Reserved**	—	—
10–13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14–17h	IOBAR	I/O Base Address	00000001h	RO, R/W
18–1Bh	GMADR	Graphics Memory Range Address	00000008h	RO, R/W/L
1C–1Fh	GTTADR	Graphics Translation Table Range Address	00000000h	RO, R/W
20–2Bh	—	**Reserved**	—	—
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35–3Bh	—	**Reserved**	—	—

Address Offset	Register Symbol	Register Name	Default Value	Access
3Ch	INTRLINE	Interrupt Line	00h	R/W
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–43h	—	**Reserved**	—	—
44h	MCAPPTR	Mirror of Dev0 Capability Pointer	D0h	RO
45–47h	—	Reserved	—	—
48–50h	MCAPID	Mirror of Dev0 Capability Identification	0000000000 01090009h	RO
51h	—	**Reserved**	—	—
52–53h	MGGC	Mirror of Dev0 GMCH Graphics Control	0030h	RO
54–57h	MDEVENdev0F0	Mirror of Dev0 Device Enable	00000019h	RO
58–5Bh	—	**Reserved**	—	—
5C–5Fh	BSM	Base of Stolen Memory	07800000h	RO
60–61h	—	**Reserved**	—	—
62h	MSAC	Multi size Aperture Control	00h	R/W
63–CFh	—	**Reserved**	—	—
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6–D7h	—	**Reserved**	—	—
E0–E1h	SWSMI	Software SMI	0000h	R/W
E2–E3h	—	**Reserved**	—	—
E4–E7	ASLE	System Display Event	00000000h	R/W
E8h–FBh	—	**Reserved**	—	—
FC–FFh	ASLS	ASL Storage	00000000h	R/W

9.1 Integrated Graphics Device PCI Register Details (D2:F0)

9.1.1 VID2—Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

9.1.2 DID2—Device Identification (D2:F0)

PCI Device: 2
Address Offset: 02h
Default Value: 2582h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2582h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device

9.1.3 PCICMD2—PCI Command (D2:F0)

PCI Device: 2
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0 = Enable the assertion of this device's INTx# signal. 1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to the DMI.
9	RO 0b	**Fast Back-to-Back (FB2B)**: Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE)**: This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0 b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

9.1.4 PCISTS2—PCI Status (D2:F0)

PCI Device: 2
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity; this bit is always hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore, this bit is hardwired to 0.
12	RO 0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF).** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C).** N/A; Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0		Reserved

9.1.5 RID2—Revision Identification (D2:F0)

PCI Device: 2
Address Offset: 08h
Default Value: See bit description
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This field indicates the number of times that this device in this component has been "stepped" through the manufacturing process. Refer to the *Intel® 82915G/82915P/82915GV/82910GL Express Chipset Specification Update* for the value of the Revision ID Register.

9.1.6 CC—Class Code (D2:F0)

PCI Device: 2
Address Offset: 09h
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC).** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display Controller.
15:8	RO 00h	**Sub-Class Code (SUBCC):** Value will be determined based on Device 0 GGC register, bit 1. 00h = VGA compatible 80h = Non VGA
7:0	RO 00 h	**Programming Interface (PI)** 00h = Hardwired as a Display controller.

9.1.7 CLS—Cache Line Size (D2:F0)

PCI Device: 2
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD, as a PCI compliant master, does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

9.1.8 MLT2—Master Latency Timer (D2:F0)

PCI Device: 2
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value:** Hardwired to 0s.

9.1.9 HDR2—Header Type (D2:F0)

PCI Device: 2
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFunc):** This bit indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the Mfunc bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

9.1.10 MMADR—Memory Mapped Range Address (D2:F0)

PCI Device: 2
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO 0000h	**Address Mask:** Hardwired to 0s to indicate 512 KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

9.1.11 IOBAR—I/O Base Address (D2:F0)

PCI Device: 2
Address Offset: 14h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16 bit I/O address space. Bits 2:1 are fixed and return 0s; bit 0 is hardwired to a 1 indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of I/O space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1–D3 or if IO Enable is clear or if Device 2 is turned off. Note that access to this I/O BAR is independent of VGA functionality within Device 2. Also note that this mechanism in available only through function 0 of Device 2 and is not duplicated in Function 1.

If accesses to this I/O bar are allowed, the GMCH claims all 8, 16, or 32 bit I/O cycles from the processor that falls within the 8B claimed.

Bit	Access & Default	Description
31:16		Reserved
15:3	R/W 0000h	**IO Base Address:** Set by the OS, these bits correspond to address signals [15:3].
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 1b	**Memory / I/O Space:** Hardwired to 1 to indicate I/O space.

9.1.12 GMADR—Graphics Memory Range Address (D2:F0)

PCI Device: 2
Address Offset: 18h
Default Value: 00000008h
Access: RO, R/W/L
Size: 16 bits

IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
31:28	R/W 0h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:28].
27	R/W/L 0b	**256-MB Address Mask:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1]. See MSAC (Dev 2, Func 0, offset 62) for details.
26:4	RO 000000h	**Address Mask:** Hardwired to 0s to indicate at least 128-MB address range
3	RO 1b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching
2:1	RO 00b	**Memory Type:** Hardwired to 0 to indicate 32-bit address.
0	RO 0b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

9.1.13 GTTADR—Graphics Translation Table Range Address (D2:F0)

PCI Device: 2
Address Offset: 1Ch
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for Graphics Translation Table Range. The allocation is for 256 KB and the base address is defined by bits [31:18].

Bit	Access & Default	Description
31:18	R/W 0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:18].
17:4	RO 0000h	**Address Mask:** Hardwired to 0s to indicate 256-KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

9.1.14 SVID2—Subsystem Vendor Identification (D2:F0)

PCI Device: 2
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID.** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read-Only. This register can only be cleared by a Reset.

9.1.15 SID2—Subsystem Identification (D2:F0)

PCI Device: 2
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

9.1.16 ROMADR—Video BIOS ROM Base Address (D2:F0)

PCI Device: 2
Address Offset: 30h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore, this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address:** Hardwired to 0s.
17:11	RO 00h	**Address Mask:** Hardwired to 0s to indicate 256-KB address range.
10:1		Reserved
0	RO 0b	**ROM BIOS Enable:** 0 = ROM not accessible.

9.1.17 CAPPOINT—Capabilities Pointer (D2:F0)

PCI Device: 2
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0h	**Capabilities Pointer Value:** This field contains an offset into the function's PCI configuration space for the first item in the New Capabilities Linked List; the Power Management Capabilities ID registers at address D0h.

9.1.18 INTRLINE—Interrupt Line (D2:F0)

PCI Device: 2
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

9.1.19 INTRPIN—Interrupt Pin (D2:F0)

PCI Device: 2
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a device that only has interrupts associated with a single function, the IGD specifies INTA# as its interrupt pin. 01h = INTA#.

9.1.20 MINGNT—Minimum Grant (D2:F0)

PCI Device: 2
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value:** The IGD does not burst as a PCI compliant master.

9.1.21 MAXLAT—Maximum Latency (D2:F0)

PCI Device: 2
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value:** The IGD has no specific requirements for how often it needs to access the PCI bus.

9.1.22 MCAPPTR—Mirror of Dev0 Capability Pointer (D2:F0) (Mirrored_D0_34)

PCI Device: 2
Function: 0
Address Offset: 44h
Size: 8 bits

This register is a **Read-Only copy of Device 0**, Offset 34h register.

9.1.23 MCAPID—Mirror of Dev0 Capability Identification (D2:F0) (Mirrored_D0_E0)

PCI Device: 2
Function: 0
Address Offset: 48h
Size: 72 bits

This register is a **Read-Only copy of Device 0**, Offset E0h register.

9.1.24 MGGC—Mirror of Dev0 GMCH Graphics Control (D2:F0) (Mirrored_D0_52)

PCI Device: 2
Function: 0
Address Offset: 52h
Size: 16 bits

This register is a **Read-Only copy of Device 0**, Offset 52h register.

9.1.25 MDEVENdev0f0—Mirror of Dev0 Device Enable (D2:F0) (Mirrored_D0_54)

PCI Device: 2
Function: 0
Address Offset: 54h
Size: 32 bits

This register is a **Read-Only copy of Device 0**, Offset 54h register.

9.1.26 BSM—Base of Stolen Memory (D2:F0)

PCI Device: 2
Address Offset: 5Ch
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MBs of DRAM for internal graphics, if enabled.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0		Reserved

9.1.27 MSAC—Multi Size Aperture Control (D2:F0)

PCI Device: 2
Address Offset: 62h
Default Value: 00h
Access: R/W
Size: 8 bits

This register determines the size of the graphics memory aperture in function 0 and in the trusted space. By default, the aperture size is 256 MB (bit 27 read only). If bit 1 is set to a 1, then the aperture size is limited to 128 MB. Only the system BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access & Default	Description
7:4	R/W 0h	**Scratch Bits Only.** These bits have no physical effect on hardware.
3:2		Reserved
1	R/W 0b	**256-MB Aperture Disable** 0 = Bit 27 of GMADR and the equivalent trusted memory aperture is read-only, allowing 256 MB of address space to be mapped. 1 = Bit 27 of GMADR and the equivalent trusted memory aperture is read-write, limiting the address space to 128 MB.
0		Reserved

9.1.28 PMCAPID—Power Management Capabilities ID (D2:F0)

PCI Device: 2
Address Offset: D0h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**NEXT_PTR:** This field contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**CAP_ID:** SIG defines this ID is 01h for power management.

9.1.29 PMCAP—Power Management Capabilities (D2:F0)

PCI Device: 2
Address Offset: D2h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2:** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6		Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	**Auxiliary Power Source:** Hardwired to 0.
3	RO 0b	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification

9.1.30 PMCS—Power Management Control/Status (D2:F0)

PCI Device: 2
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		Reserved
8	RO 0b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, the write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

9.1.31 SWSMI—Software SMI (D2:F0)

PCI Device: 2
Address Offset: E0h
Default Value: 0000h
Access: R/W
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist that expect this register at this address, Dev2, F0, address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	R/W 00h	**SW scratch bits**
7:1	R/W 00h	**Software Flag:** This field is used to indicate caller and SMI function desired, as well as return result.
0	R/W 0b	**GMCH Software SMI Event:** When Set, this bit will trigger an SMI. Software must write a 0 to clear this bit

9.1.32 ASLE—System Display Event Register (D2:F0)

PCI Device: 2
Address Offset: E4h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Byte, Word, or Double Word PCI configuration cycles can access this register.

Bit	Access & Default	Description
31:8	R/W 00h	**ASLE Scratch Trigger 3:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	R/W 00h	**ASLE Scratch Trigger 2:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	R/W 00h	**ASLE Scratch Trigger 1:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	R/W 00h	**ASLE Scratch Trigger 0:** When written, this scratch byte triggers an interrupt when IER bit 0 is enabled and IMR bit 0 is unmasked. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

9.1.33 ASLS—ASL Storage (D2:F0)

PCI Device: 2
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This SW scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/Non VGA); one bit for _DGS (enable/disable requested) and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000 h	RW according to a software controlled usage to support device switching

10 Device 2 Function 1 (D2:F1) Configuration Registers (Intel® 82915G/82915GV/82915GL/ 82910GL Only)

Table 10-1. Device 2 Function 1 Register Address Map Summary

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2780h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code Register	03800h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type Register	80h	RO
0Fh	—	Reserved	—	—
10–13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14–2Bh	—	Reserved	—	—
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35–3Dh	—	Reserved	—	—
3Eh	MINGNT	Minimum Grant Register	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–43h	—	Reserved	—	—
44h	MCAPPTR	Mirror of Dev0 Capability Pointer		
45–47h	—	Reserved	—	—

Address Offset	Register Symbol	Register Name	Default Value	Access
48–50h	MCAPID	Mirror of Dev0 Capability Identification		
51h	—	Reserved	—	—
52–53h	MGGC	Mirror of Dev0 GMCH Graphics Control		
54–57h	MDEVENdev0f0	Mirror of Dev0 Device Enable		
58–5Bh	—	Reserved	—	—
5C–5Fh	BSM	Base of Stolen Memory Register	07800000h	RO
60–CFh	—	Reserved	0000h	—
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6–DFh	—	Reserved	—	—
E0–E1h	SWSMI	Software SMI	0000h	R/W
E2–FBh	—	Reserved	—	—
FC–FFh	ASLS	ASL Storage	00000000h	R/W

10.1 Device 2 Function 1 Configuration Register Details (D2:F1)

10.1.1 VID2—Vendor Identification (D2:F1)

PCI Device: 2
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.2 DID2—Device Identification (D2:F1)

PCI Device: 2
Address Offset: 02h
Default Value: 2782h
Access: RO
Size: 16 bits

This register is unique in Device 2, Function 1 (the Device 2, Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of function 1 when both function 0 and function 1 have the same class code.

10.1.3 PCICMD2—PCI Command (D2:F1)

PCI Device: 2
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back (FB2B)**: Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

10.1.4 PCISTS2—PCI Status (D2:F1)

PCI Device: 2
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity; this bit is always hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** The IGD never asserts SERR#; therefore, this bit is hardwired to 0.
13	RO 0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0**.**
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF).** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C).** Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status:** Hardwired to 0.
2:0		Reserved

10.1.5 RID2—Revision Identification (D2:F1)

PCI Device: 2
Address Offset: 08h
Default Value: See description below
Access: RO
Size: 8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.6 CC—Class Code Register (D2:F1)

PCI Device: 2
Address Offset: 09h
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display Controller.
15:8	RO 80h	**Sub-Class Code (SUBCC)** 80h = Non VGA
7:0	RO 00h	**Programming Interface (PI)** 00h = Hardwired as a Display controller.

10.1.7 CLS—Cache Line Size (D2:F1)

PCI Device: 2
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.8 MLT2—Master Latency Timer (D2:F1)

PCI Device: 2
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.9 HDR2—Header Type Register (D2:F1)

PCI Device: 2
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.10 MMADR—Memory Mapped Range Address (D2:F1)

PCI Device: 2
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO 0000h	**Address Mask:** Hardwired to 0s to indicate 512-KB address range.
3	RO 0b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

10.1.11 SVID2—Subsystem Vendor Identification (D2:F1)

PCI Device:	2
Address Offset:	2Ch
Default Value:	0000h
Access:	R/WO
Size:	16 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.12 SID2—Subsystem Identification (D2:F1)

PCI Device:	2
Address Offset:	2Eh
Default Value:	0000h
Access:	R/WO
Size:	16 bits

This register is a Read Only copy of Device 2, Function 0.

10.1.13 ROMADR—Video BIOS ROM Base Address (D2:F1)

PCI Device:	2
Address Offset:	30h
Default Value:	00000000h
Access:	RO
Size:	32 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.14 CAPPOINT—Capabilities Pointer (D2:F1)

PCI Device:	2
Address Offset:	34h
Default Value:	D0h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.15 MINGNT—Minimum Grant Register (D2:F1)

PCI Device:	2
Address Offset:	3Eh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.16 MAXLAT—Maximum Latency (D2:F1)

PCI Device:	2
Address Offset:	3Fh
Default Value:	00h
Access:	RO
Size:	8 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.17 MCAPPTR—Mirror of Dev0 Capability Pointer (D2:F1) (Mirrored_D0_34)

PCI Device:	2
Function:	1
Address Offset:	44h
Size:	8 bits

This register is a Read Only copy of Device 0, Offset 34h register.

10.1.18 MCAPID—Mirror of Dev0 Capability Identification (D2:F1) (Mirrored_D0_E0)

PCI Device:	2
Function:	1
Address Offset:	48h
Size:	72 bits

This register is a Read-Only copy of Device 0, Offset E0h register.

10.1.19 MGGC—Mirror of Dev0 GMCH Graphics Control (D2:F1) (Mirrored_D0_52)

PCI Device:	2
Address Offset:	52h
Size:	16 bits

This register is a Read Only copy of Device 0, Offset 52h register.

10.1.20 MDEVENdev0f0—Mirror of Dev0 Device Enable (D2:F1) (Mirrored_D0_54)

PCI Device:	2
Function:	1
Address Offset:	54h
Size:	32 bits

This register is a Read Only copy of Device 0, Offset 54h register.

10.1.21 BSM—Base of Stolen Memory Register (D2:F1)

PCI Device:	2
Address Offset:	5Ch
Default Value:	07800000h
Access:	RO
Size:	32 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.22 PMCAPID—Power Management Capabilities ID (D2:F1)

PCI Device:	2
Address Offset:	D0h
Default Value:	0001h
Access:	RO
Size:	16 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.23 PMCAP—Power Management Capabilities (D2:F1)

PCI Device:	2
Address Offset:	D2h
Default Value:	0022h
Access:	RO
Size:	16 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.24 PMCS—Power Management Control/Status (D2:F1)

PCI Device: 2
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		Reserved
8	RO 0 b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		Reserved
1:0	R/W 00 b	**Power State:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

10.1.25 SWSMI—Software SMI (D2:F1)

PCI Device: 2
Address Offset: E0h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register is a copy of Device 2, Function 0. It has the same Read, Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

10.1.26 ASLS—ASL Storage (D2:F1)

PCI Device: 2
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000 h	R/W according to a software controlled usage to support device switching

10.2 Device 2 – PCI I/O Registers

The following are not PCI configurations registers; they are I/O registers.

10.2.1 MMIO_INDEX—MMIO Address Register

I/O Address: IOBAR + 0h
Size: 32 bits

MMIO_INDEX: A 32 bit I/O write to this port loads the **offset** of the memory-mapped I/O (MMIO) register that needs to be accessed. An I/O Read returns the current value of this register. An 8/16-bit I/O write to this register is completed by the GMCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA I/O registers that are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Register Offset**: This field selects any one of the DWord registers within the MMIO register space of Device 2.
1:0		Reserved

10.2.2 MMIO_DATA—MMIO Data Register

I/O Address: IOBAR + 4h
Size: 32 bits

MMIO_DATA: A 32 bit I/O write to this port is re-directed to the MMIO register pointed to by the MMIO-index register. A 32 bit I/O read to this port is re-directed to the MMIO register pointed to by the MMIO-index register. 8 or 16 bit I/O writes are completed by the GMCH and may have un-intended side effects; hence, they must not be used to access the data port. 8 or 16 bit I/O reads are completed normally.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**MMIO Data Window**

§

11 System Address Map

The (G)MCH supports 4 GB of addressable memory space (see Figure 11-1) and 64 KB+3 bytes of addressable I/O space. A programmable memory address space under the 1-MB region is divided into regions that can be individually controlled with programmable attributes such as disable, read/write, write only, or read only. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

Note: Address mapping information for the Integrated Graphics Device applies to the 82915G/82915GV/82915GL/82910GL GMCH only. The 82915P/82915PL MCH does not have an IGD.

Note: Address mapping information for the PCI Express Device applies to the 82915G/82915P/82915PL (G)MCH only. The 82915GV/82915GL/82910GL GMCH does not support PCI Express.

Addressing of memory ranges larger than 4 GB is **not** supported. The HREQ[4:3] FSB pins are decoded to determine whether the access is above or below 4 GB.

The (G)MCH does not support the PCI Dual Address Cycle (DAC) Mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI or PCI Express interface. The (G)MCH does not limit system memory space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges that may be mapped to PCI Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

- Device 0
  - EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4-KB window)
  - MCHBAR – Memory mapped range for internal (G)MCH registers. For example, memory buffer register controls. (16-KB window)
  - PCIEXBAR – Flat memory-mapped address space to access device configuration registers. This mechanism can be used to access PCI configuration space (0h–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (256-MB window)
  - DMIBAR –This window is used to access registers associated with the (G)MCH/ICH6 (DMI) register memory range. (4-KB window)

  - IFPBAR – Any write to this window will trigger a flush of the (G)MCH's Global Write Buffer to let software guarantee coherency between writes from an isochronous agent and writes from the processor (4-KB window).
  - GGC – 82915G/82915GV/82910GL GMCH graphics control register. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes (0–64-MB options).

- Device 1: Function 0:
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - IOBASE1/IOLIMIT1 – PCI Express port I/O access window.

- Device 2: Function 0 (82915G/82915GV/82915GL/82910GL GMCH only)
  - MMADR – IGD registers and internal graphics instruction port. (512-KB window)
  - IOBAR – I/O access window for the GMCH internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
  - GMADR – Internal graphics translation window. (256-MB window)
  - GTTADR – Internal graphics translation table location. (256-KB window). Note that the PGTBL_CTL register (MMIO 2020) indicates the physical address base which is 4 KB aligned.

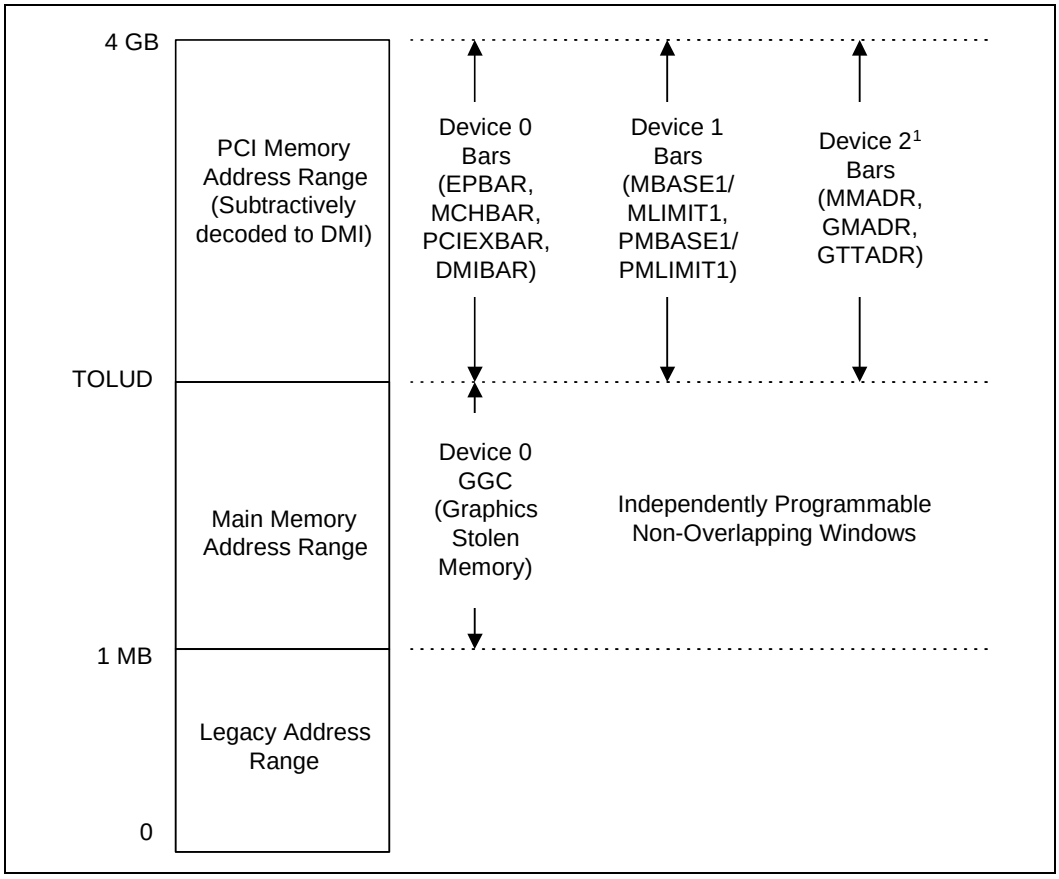
- Device 2: Function 1 (82915G/82915GV/82915GL/82910GL GMCH only)
  - MMADR – Function 1 IGD registers and internal graphics instruction port. (512-KB window)

The rules for the above programmable ranges are:

- ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
- In the case of overlapping ranges with memory, the memory decode will be given priority.
- There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
- Accesses to overlapped ranges may produce indeterminate results.
- The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 11-1 shows the system memory address map in a simplified form.

Figure 11-1. System Address Ranges



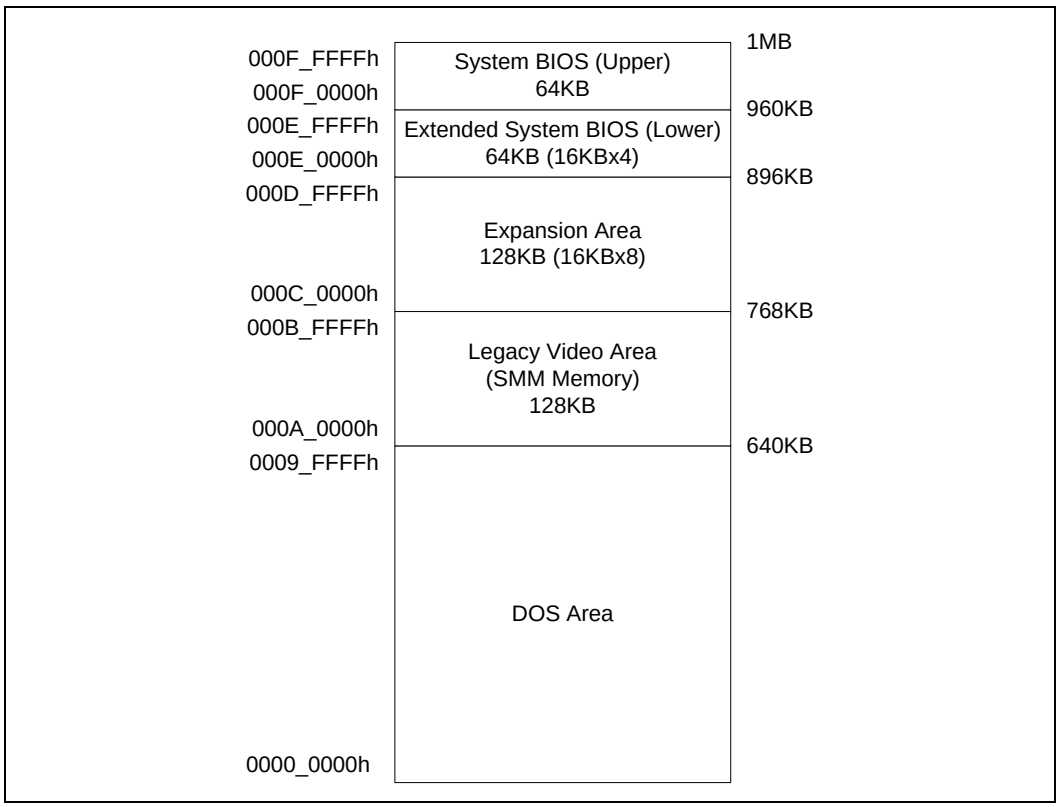
NOTES:
1. Device 2 is not on the 82915P/82915PL MCH.
2. Device 1 is not on the 82915GV/82910GL/82915GL GMCH.

11.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB: DOS Area
- 640 – 768 KB: Legacy Video Buffer Area
- 768 – 896 KB in 16-KB sections (total of 8 sections): Expansion Area
- 896 – 960 KB in 16-KB sections (total of 4 sections): Extended System BIOS Area
- 960-KB – 1-MB Memory: System BIOS Area

Figure 11-2. Microsoft MS-DOS* Legacy Address Range



11.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

11.1.2 Legacy Video Area (A_0000h–B_FFFFh)

The legacy 128-KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD, to PCI Express, and/or to the DMI. The appropriate mapping is programmable. Based on the programming, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the 82915G/82915GV/82915GL/82910GL GMCH, decode precedence is always given to the IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD (82915G/82915GV/82915GL/82910GL only) and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the programming. This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h–B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A 0000h–000B FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD (82915G/82915GV/82915GL/82910GL GMCH only) is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h–B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on the programming of the on-chip registers). Since the monochrome adapter may be mapped to any one of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h – 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

11.1.3 Expansion Area (C_0000h–D_FFFFh)

This 128-KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight, 16-KB segments. Each segment can be assigned one of four read/write states: read only, write only, read/write, or disabled. Typically, these blocks are mapped through the (G)MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 11-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h–0C3FFFh	W/R	Add-on BIOS
0C4000h–0C7FFFh	W/R	Add-on BIOS
0C8000h–0CBFFFh	W/R	Add-on BIOS
0CC000h –0CFFFFh	W/R	Add-on BIOS
0D0000h–0D3FFFh	W/R	Add-on BIOS
0D4000h–0D7FFFh	W/R	Add-on BIOS
0D8000h–0DBFFFh	W/R	Add-on BIOS
0DC000h–0DFFFFh	W/R	Add-on BIOS

11.1.4 Extended System BIOS Area (E_0000h–E_FFFFh)

This 64-KB area (000E_0000h – 000E_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to the DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 11-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h–0E3FFFh	W/R	BIOS Extension
0E4000h–0E7FFFh	W/R	BIOS Extension
0E8000h–0EBFFFh	W/R	BIOS Extension
0EC000h–0EFFFFh	W/R	BIOS Extension

11.1.5 System BIOS Area (F_0000h–F_FFFFh)

This area is a single, 64-KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the DMI. By programming the read/write attributes, the (G)MCH can “shadow” BIOS into main memory. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 11-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h–0FFFFFh	WE RE	BIOS Area

11.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM memory area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI.

However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC, it is possible to get IWB cycles targeting DMI. This may occur for DMI-originated cycles to disabled PAM regions.

Warning: For example, assume that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled”, the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

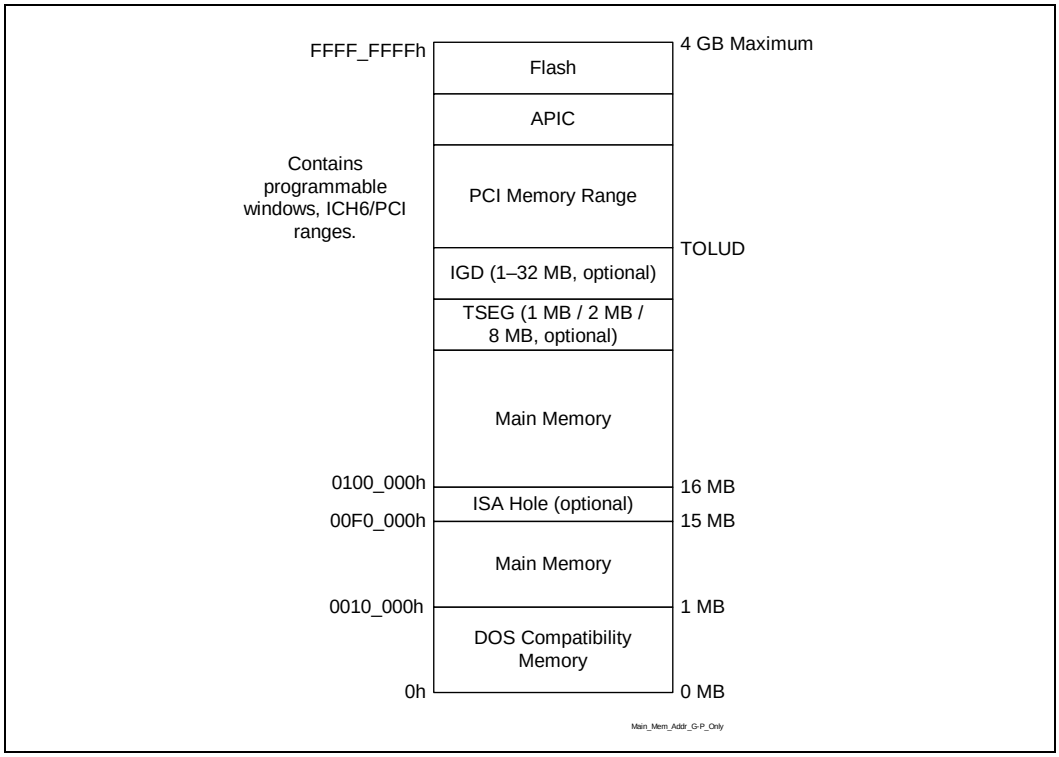
11.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the (G)MCH (as programmed by in the TOLUD register). All accesses to addresses within this range will be forwarded by the (G)MCH to the main memory unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

The (G)MCH provides a maximum main memory address decode space of 4 GB. The (G)MCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4 GB, there will be physical memory that exists, yet non-addressable; therefore, this memory is unusable by the system.

The (G)MCH does not limit main memory address space in hardware.

Figure 11-3. Main Memory Address Range



11.2.1 ISA Hole (15 MB–16 MB)

BIOS can create a hole at 15 MB–16 MB. Accesses within this hole are forwarded to the DMI. The range of physical main memory disabled by opening the hole is not remapped to the top of the memory; that physical main memory space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

11.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode write-back cycles that target TSEG space are completed to main memory for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical main memory minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

11.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 11-4 details the location and attributes of the regions.

Table 11-4. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available system memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - processor reads	TSEG Address Range and Pre-allocated memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 4/8/16/32/64 MB) when IGD is enabled.

11.3 PCI Memory Address Range (TOLUD – 4 GB)

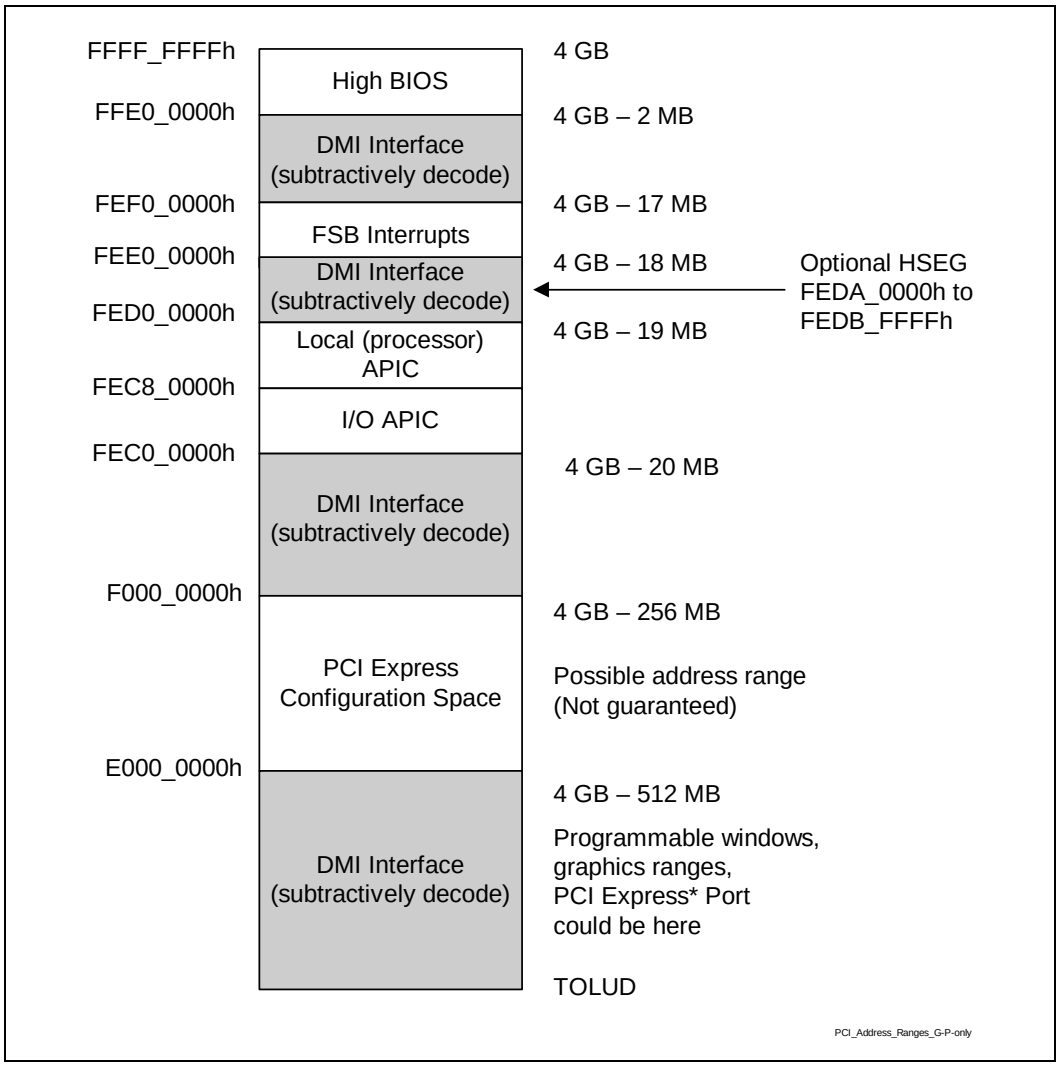
This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the (G)MCH) is normally mapped via the DMI to PCI. Exceptions to this mapping include BAR memory mapped regions that include:

- EPBAR, MCHBAR, DMIBAR.
- The second exception to the mapping rule deals with the PCI Express port:
  - Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
  - Addresses decoded to PCI Express configuration space are mapped based on Bus, Device, and Function number. (PCIEXBAR range).
- The third exception to the mapping rule occurs in an internal graphics configuration (82915G GMCH only):
  - Addresses decoded to the Graphics Memory Range. (GMADR range)
  - Addresses decoded to the Graphics Translation Table range (GTTADR range).

— Addresses decoded to the Memory Mapped Range of the Internal Graphics Device (MMADR range). There is a MMADR range for device 2 function 0 and a MMADR range for device 2 function 1. Both ranges are forwarded to the Internal Graphics Device.

The exceptions listed above for internal graphics and the PCI Express ports **MUST NOT** overlap with APCI Configuration, FSB Interrupt Space and High BIOS Address Range.

Figure 11-4. PCI Memory Address Range



11.3.1 APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH6 portion of the chipset, but may also exist as stand-alone components.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

11.3.2 HSEG (FEDA_0000h–FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode write-back cycles that are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical main memory behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

11.3.3 FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a memory write to 0FEEx_xxxxh. The (G)MCH will forward this memory write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDY#. This memory write cycle does not go to DRAM.

11.3.4 High BIOS Area

The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI memory address range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to the DMI so that the upper subset of this region aliases to the 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB, but the minimum processor MTRR range for this region is 2 MB; thus, that full 2 MB must be considered.

11.3.5 PCI Express* Configuration Address Space (Intel® 82915G/82915P Only)

A configuration register defines the base address for the 256-MB block of addresses below top of addressable memory (4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This range will be aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

11.3.6 PCI Express* Graphics Attach (Intel® 82915G/82915P Only)

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two programmed ranges specified via registers in the (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

It is essential to support a separate Prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note: The programmable ranges are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

11.3.7 AGP DRAM Graphics Aperture

Unlike AGP4x, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the (G)MCH has no APBASE and APSIZE registers.

11.3.8 Graphics Memory Address Ranges (Intel® 82915G/82915GV/82915GL/82910GL GMCH Only)

The GMCH can be programmed to direct memory accesses to IGD when addresses are within any of three programmable ranges.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Main-DRAM and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so that physical DRAM memory space is not allocate to them.

The memory allocated via the graphics translation table is a Prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

11.4 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. (G)MCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. For the 82915G/82915GV/82915GL/82910GL GMCH, the TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handler's code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

11.4.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped; therefore, the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped, the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. The following table describes three unique address ranges:

- Compatible Transaction Address
- High Transaction Address
- TSEG Transaction Address

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

11.4.2 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system main memory, or to any “PCI” devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE capability **must not** be enabled at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available main memory. This is a BIOS responsibility.
- Any address translated through the internal graphics device’s TLB must not target main memory from A_0000-F_FFFF.

11.4.3 SMM Space Combinations

When High SMM is enabled, the Compatible SMM space is effectively disabled. Processor originated accesses to the Compatible SMM space are forwarded to PCI Express if this VGA capability is enabled; otherwise, they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 11-5. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

11.4.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 11-6. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

11.4.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

11.4.6 Processor WB Transaction to an Enabled SMM Address Space

Processor write-back transactions (HREQ1# = 0) to enabled SMM address space must be written to the associated SMM DRAM, even though the space is not open and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

11.4.7 SMM Access through GTT TLB (Intel® 82915G/82915GV/82910GL GMCH Only)

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to memory address 0h with byte enables de-asserted and reads will be routed to memory address 0h. If a GTT TLB translated address hits enabled SMM DRAM space, an Invalid Translation Table Entry Flag is reported to BIOS.

PCI Express and DMI originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an Invalid Translation Table Entry Flag is reported to BIOS.

PCI Express and DMI write accesses through graphics memory range set up by BIOS will be snooped. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 0h with de-asserted byte enables.

PCI Express and DMI read accesses to the graphics memory range set up by BIOS are not supported; therefore, users/systems will have no address translation concerns. PCI Express and DMI reads to the graphics memory range will be remapped to address 0h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure they are not in SMM (actually, anything above base of TSEG or 640 KB – 1 MB). Thus, they will be invalid and go to address 0h. This is not specific to PCI Express or DMI; it applies to the processor or internal graphics engines. Also, since the graphics memory range snoop would not be directly to SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and goes to address 0h.

11.4.8 Memory Shadowing

Any block of memory that can be designated as “read only” or “write only” can be “shadowed” into (G)MCH main memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM memory. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

11.4.9 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the (G)MCH contains two internal registers in the processor I/O space. These locations are used to implement a configuration space access mechanism.

The processor allows 64 KB+3 bytes to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus; therefore, providing addressability for 64 KB+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HA16# address signal is asserted. HA16# is asserted on the processor bus when an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

For the 828915G GMCH, a set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control are explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are **not** posted. Memory writes to the ICH6 or PCI Express are posted.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

11.4.10 PCI Express* I/O Address Mapping (Intel® 82915G/82915P/82915PL Only)

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor-initiated I/O cycle addresses are within the PCI Express I/O address range.

11.4.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

The following are (G)MCH decode rules and cross-bridge address mapping used in this chipset:

- VGAA = 000A_0000h – 000A_FFFFh
- MDA = 000B_0000h – 000B_7FFFh
- VGAB = 000B_8000h – 000B_FFFFh
- MAINMEM = 0100_0000 to TOLUD

11.4.12 Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to IGD (82915G/82915GV/82915GL/82910GL GMCH only), to PCI Express (Device #1), and/or to the DMI depending on BIOS programming. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI Express.

§

12 Functional Description

This chapter describes the (G)MCH interfaces and major functional units.

12.1 Host Interface

The (G)MCH supports the Pentium 4 processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped, and a new address can be generated every other bus clock. At 133/200 MHz bus clock, the address signals run at 266/400 MT/s for a maximum address queue rate of 66/100 million addresses/sec. The data is quad pumped and an entire 64 byte cache line can be transferred in two bus clocks. At 133/200 MHz bus clock the data signals run at 533/800 MT/s for a maximum bandwidth of 4.2 GB/s or 6.4 GB/s.

Note: The host interface on the 82910GL GMCH runs at 133 MHz only.

The FSB interface supports up to 12 simultaneous outstanding transactions. The (G)MCH supports only one outstanding deferred transaction on the FSB.

12.1.1 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die. Also, approximately 2.8 pf (fast) – 3.3 pf (slow) per pad of on die capacitance will be implemented to provide better FSB electrical performance.

12.1.2 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV0#	HD[15:0]
HDINV1#	HD[31:16]
HDINV2#	HD[47:32]
HDINV3#	HD[63:48]

When the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINVx# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the (G)MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

12.1.3 APIC Cluster Mode Support

This is required for backwards compatibility with existing software, including various operating systems. As one example, beginning with Microsoft Windows 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

The (G)MCH supports three types of interrupt re-direction:

- Physical
- Flat-Logical
- Clustered-Logical

12.2 System Memory Controller

This section describes the (G)MCH system memory interface for both DDR memory and DDR2 memory. The (G)MCH supports both DDR and DDR2 memory and either one or two DIMMs per channel.

Note: The 82915G/82915GV GMCH and 82915P MCH support both DDR memory and DDR2 memory, and either one or two DIMMs per channel. The 82910GL only supports DDR memory and a maximum of one DIMM per channel. The 82915PL and 82915GL support only DDR and either one or two DIMMs per channel.

12.2.1 Memory Organization Modes

The system memory controller supports two styles of memory organization (Interleaved and Asymmetric) and two modes of operation (DDR and DDR2). Rules for populating DIMM slots are included in this chapter.

Interleaved Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64 byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawbacks of Interleaved Mode are that the system designer must populate both channels of memory such that they have equal capacity, but the technology and device width may vary from one channel to the other. Refer to Figure 12-1 for further clarification.

Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A; then, addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case. Refer to Figure 12-1 for further clarification.

Figure 12-1. System Memory Styles

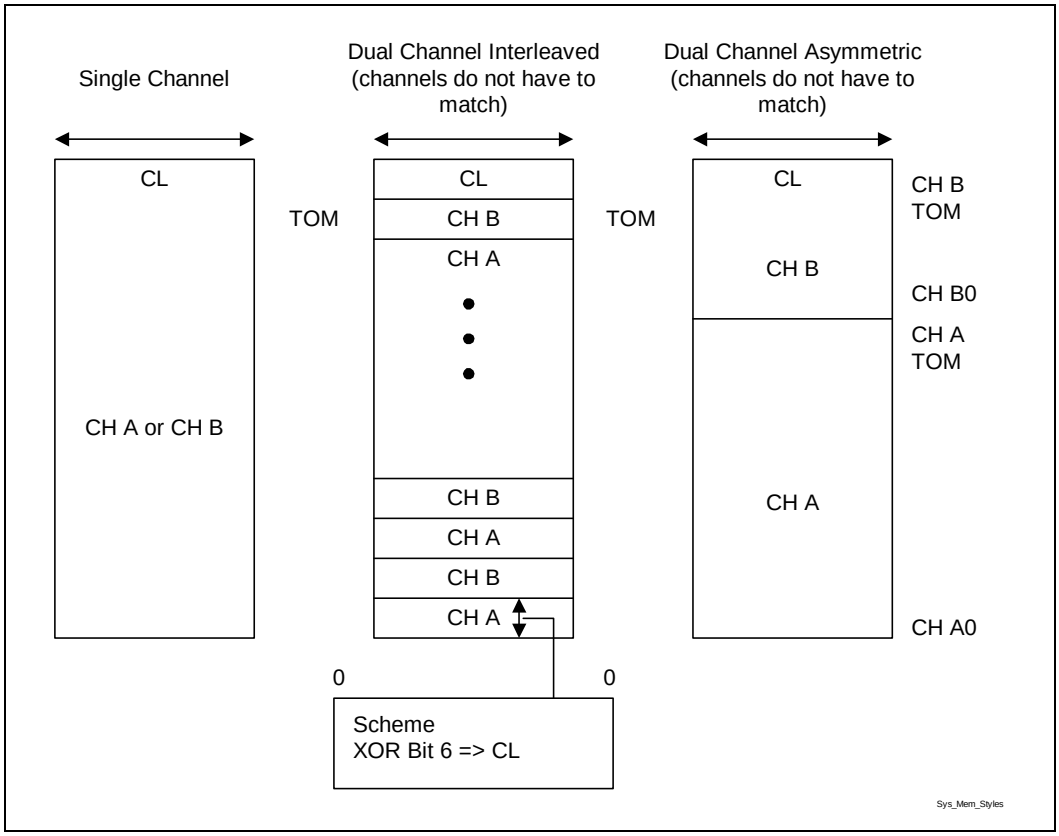


Table 12-1. Sample System Memory Organization with Interleaved Channels

Rank	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
3	0 MB	2560 MB	0 MB	2560 MB
2	256 MB	2560 MB	256 MB	2560 MB
1	512 MB	2048 MB	512 MB	2048 MB
0	512 MB	1024 MB	512 MB	1024 MB

Table 12-2. Sample System Memory Organization with Asymmetric Channels

Rank	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
3	0 MB	1280 MB	0 MB	2560 MB
2	256 MB	1280 MB	256 MB	2560 MB
1	512 MB	1024 MB	512 MB	2304 MB
0	512 MB	512 MB	512 MB	1792 MB

12.3 System Memory Configuration Registers Overview

The configuration registers located in the PCI configuration space of the (G)MCH control the system memory operation. Following is a brief description of configuration registers.

- **DRAM Rank Boundary (CxDRBy):** The x represents a channel, either A (where x = 0) or B (where x = 1). The y represents a rank, 0 through 3. DRB registers define the upper addresses for a rank of DRAM devices in a channel. When the (G)MCH is configured in asymmetric mode, each register represents a single rank. When the (G)MCH is configured in a dual interleaved mode, each register represents a pair of corresponding ranks in opposing channels. There are 4 DRB registers for each channel.
- **DRAM Rank Architecture (CxDRAy):** The x represents a channel, either A (where x = 0) or B (where x = 1). The y represents a rank, 0 through 3. DRA registers specify the architecture features of each rank of devices in a channel. The only architecture feature specified is page size. When the (G)MCH is configured in asymmetric mode, each DRA represents a single rank in a single channel. When the (G)MCH is configured in a dual-channel lock-step or interleaved mode, each DRA represents a pair of corresponding ranks in opposing channels. There are 4 DRA registers per channel. Each requires only 3 bits, so there are two DRAs packed into a byte.
- **Clock Configuration (CLKCFG):** Specifies DRAM frequency. The same clock frequency will be driven to all DIMMs.
- **DRAM Timing (CxDRTy):** The x represents a channel, A (where x = 0) or B (where x = 1). A second register for a channel is differentiated by y, A or B. The DRT registers define the timing parameters for all devices in a channel. The BIOS programs this register with “least common denominator” values after reading the SPD registers of each DIMM in the channel.
- **DRAM Control (CxDRCy):** The x represents a channel, A (where x = 0) or B (where x = 1). A second register for a channel is differentiated by y, A or B. DRAM refresh mode, rate, and other controls are selected here.

12.3.1 DRAM Technologies and Organization

All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices.

- All supported DDR devices have 4 banks; all supported DDR2 devices have 4 or 8 banks.
- The (G)MCH supports various page sizes. Page size is individually selected for every rank.
- 4 KB, 8 KB, and 16 KB for asymmetric, interleaved, or single-channel modes.
- The DRAM sub-system supports single or dual channels, 64-b wide per channel.
- There can be a maximum of four ranks populated (two double-sided DIMMs) per channel.
- Mixed mode double-sided DIMMs (x8 and x16 on the same DIMM) are not supported
- By using 1-Gb technology, the largest memory capacity is 8 GB

  32M rows/bank * 4 banks/device * 8 columns * 8 devices/rank * 4 ranks/channel * 2 channel * 1b/(row*column) * 1G/1024M * 1B/8b = 8 GB.

  Though it is possible to put 8 GB in system by stuffing both channels this way, the (G)MCH is still limited to 4 GB of addressable space due to the number of address pins on the FSB.
- By using 256-Mb technology, the smallest memory capacity is 128 MB
  (4M rows/bank * 4banks/device * 16 columns * 4 devices/rank * 1 rank * 1B/8b =128 MB)

12.3.1.1 Rules for Populating DIMM Slots

- In all modes, the frequency of system memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs.
- In the Single Channel mode, any DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, do not populate the unused channel.
- In Dual-Channel Asymmetric mode, any DIMM slot may be populated in any order.
- In Dual-Channel Interleaved mode, any DIMM slot may be populated in any order, but the total memory in each channel must be the same.

12.3.1.2 System Memory Supported Configurations

The (G)MCH supports the 256-Mbit, 512-Mbit and 1-Gbit technology based DIMMs from Table 12-3.

Table 12-3. DDR / DDR2 DIMM Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256Mbit	16M X 16	13	9	2	4K	128 MB
256Mbit	32M X 8	13	10	2	8K	256 MB
512Mbit	32M X 16	13	10	2	8K	256 MB
512Mbit	64M X 8	13	11	2	16K	512 MB
512Mbit	64M X 8	14	10	2	8K	512 MB
1Gbit	64M X 16	14	10	2	8K	512 MB
1Gbit	128M X 8	14	11	2	16K	1 GB
1Gbit	64M X 16	13	10	3	8K	512 MB
1Gbit	128M X 8	14	10	3	8K	1 GB

12.3.1.3 Main Memory DRAM Address Translation and Decoding

Table 12-4 and Table 12-5 specify the host interface to memory interface address multiplex for the (G)MCH. Refer to the details of the various DIMM configurations as described in Table 12-3. The address lines specified in the column header refer to the host (processor) address lines.

Table 12-4. DRAM Address Translation (Single Channel/Dual Asymmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB						r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x8	4i	16 KB	512 MB				r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB				r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x16	4i	8 KB	512 MB				r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x8	4i	16 KB	1 GB			r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x16	8i	8 KB	512 MB				r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB			r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. r – 'row' address bit

Table 12-5. DRAM Address Translation (Dual Channel Symmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB					r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x8	4i	16 KB	512 MB			r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x16	4i	4 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB			r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x16	4i	8 KB	512 MB			r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x8	4i	16 KB	1 GB		r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x16	8i	4 KB	512 MB			r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB		r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. h – channel select bit
4. r – 'row' address bit

12.3.2 DRAM Clock Generation

The (G)MCH generates three differential clock pairs for every supported DIMM. There are a total of 6 clock pairs driven directly by the (G)MCH to 2 DIMMs per channel (82915G/82915GV/82915GL and 82915P) and to 1 DIMM per channel (82910GL/82915PL).

12.3.3 Suspend-to-RAM and Resume

When entering the Suspend-to-RAM (STR) state, the SDRAM controller will flush pending cycles and then enter all SDRAM rows into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.n

12.3.4 DDR2 On-Die Termination

On-die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DM, DQS, and DQS# signal for x8 and x16 configurations via the ODT control signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves, instead of on the motherboard. The (G)MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM rank to enable or disable their termination resistance.

12.3.5 DDR2 Off-Chip Driver Impedance Calibration

The OCD impedance adjustment mode allows the (G)MCH to measure and adjust the pull-up and pull-down strength of the DRAM devices. It uses a series of EMRS commands to guide the DRAM through measurement and calibration cycles. This feature is described in more detail in the JEDEC DDR2 device specification.

The algorithm and sequence of the adjustment cycles is handled by software. The (G)MCH adjusts the DRAM driver impedance by issuing OCD commands to the DIMM and looking at the analog voltage on the DQ lines.

12.4 PCI Express* (Intel® 82915G/82915P82915PL Only)

Refer to Chapter 0 a for list of PCI Express features, and the PCI Express specification for further details. The (G)MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy.

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 Gb/s/direction that provides a 250 MB/s communications channel in each direction (500 MB/s total) per lane that is close to twice the data rate of classic PCI.

Note: The PCI Express graphics port will operate in x1 mode if a non-graphics card is plugged in.

12.4.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions (such as read and write as well as certain types of events). The Transaction Layer also manages flow control of TLPs.

Note: If the (G)MCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged. The (G)MCH will not log or identify the second malformed packet. However, the 1st malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2nd malformed TLP is detected or not.

12.4.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

12.4.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

12.5 Intel® Serial Digital Video Output (SDVO) (Intel® 82915G/82915GV/82915GL/82910GL GMCH Only)

The 82915G/82915GV/82915GL/82910GL GMCH SDVO ports are multiplexed with the PCI Express x16 interface. PCI Express and SDVO simultaneous operation is NOT supported, even though SDVO does not require all of the PCI Express lanes.

The Intel® SDVO port is the second generation of digital video output from compliant GMCH. The electrical interface is based on the PCI Express interface, although the protocol and timings are completely unique. Where PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an SDVO port will transmit display data in a high speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

12.5.1 Intel® SDVO Capabilities

SDVO ports can support a variety of display types including LVDS, DVI, Analog CRT, TV-Out and external CE type devices. The GMCH uses an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

The Internal Graphics Device on the 82915G/82915GV/82915GL/82910GL GMCH can have one or two SDVO ports multiplexed on the x16 PCI Express interface. When an external x16 PCI Express graphics accelerator is not in use, an ADD2 card may be plugged into the x16 connector or if a x16 slot is not present, the SDVO(s) may be located ‘down’ on the motherboard to access the multiplexed SDVO ports and provide a variety of digital display options.

The ADD2 card is designed to fit in a x16 PCI Express connector. The ADD2 card can support one or two devices. If a single channel SDVO device is used, it should be attached to the channel B SDVO pins. The ADD2 card can support two separate SDVO devices when the interface is in Dual Independent (82915G only) or Dual Simultaneous Standard modes.

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and GMCH. The SDVO control clock and data provide similar functionality to I^2C. However, unlike I^2C, this interface is intended to be point-to-point (from the GMCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface would.

12.5.2 Intel® SDVO Modes

The port can be dynamically configured in several modes:

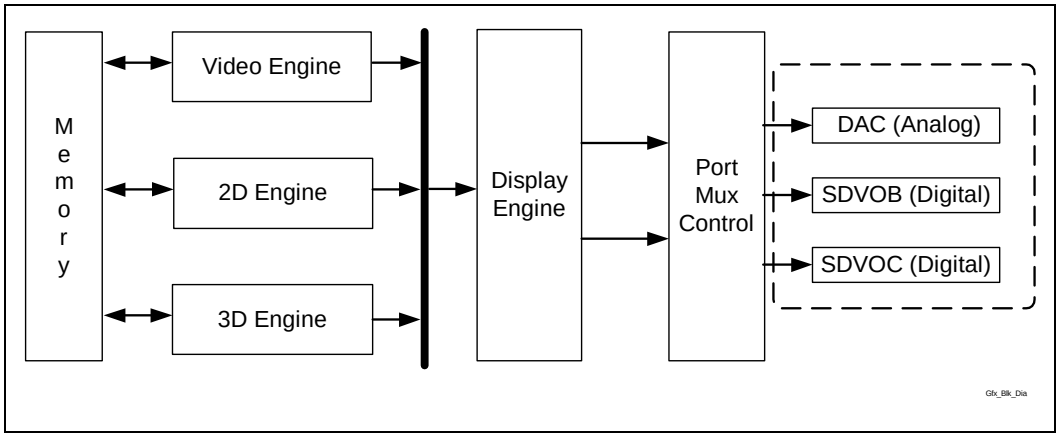
- **Standard.** This mode provides baseline SDVO functionality. Supports Pixel Rates between 25 and 200 MP/s. Utilizes three data pairs to transfer RGB data.
- **Extended.** This mode adds Alpha support to data stream. Extended mode supports Pixel rates between 25 MP/s and 200 MP/s. The mode uses four data channels and is only supported on SDVOB. Leverages channel C (SDVOC) Red pair as the Alpha pair for channel B (SDVOB).

  Note: Operating in extended SDVO mode is mutually exclusive to the use of a second display on SDVO.
- **Dual Standard.** This mode uses Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 and 200 MP/s.
  - Dual Independent Standard (82915G only). In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVOB will not be the same as the data stream across SDVOC.
  - Dual Simultaneous Standard. In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVOB will be the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this mode uses just a single data stream, it uses a single pixel pipeline within the GMCH.

12.6 Integrated Graphics Device (Intel® 82915G/82915GV/82915GL/82910GL GMCH Only)

The GMCH provides a highly integrated graphics accelerator and chipset while allowing a flexible integrated system graphics solution. Figure 12-2 shows a simplified block diagram of the IGD in the GMCH.

Figure 12-2. Integrated Graphics Device Block Diagram



High bandwidth access to data is provided through the graphics and system memory ports. The GMCH can access graphics data located in system memory at 4.2 GB/s – 8.5 GB/s (depending on memory configuration). The GMCH uses Intel's Direct Memory Execution model to fetch textures from system memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

The GMCH is able to drive an integrated DAC, and/or two SDVO ports (multiplexed with PCI Express) capable of driving an ADD2 card. External SDVO devices are capable of driving a standard progressive scan analog monitor with resolutions up to 2048x1536 @ 75 Hz. The SDVO ports are capable of driving a variety of TV-Out, TMDS, and LVDS transmitters.

The GMCH's Internal Graphics Device (IGD) contains several types of components. The major components in the IGD are the engines, planes, pipes and ports. The GMCH has a 3D/2D Instruction Processing unit to control the 3D and 2D engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to memory, which are then retrieved and processed by the GMCH planes.

The GMCH contains a variety of planes (such as display, overlay, cursor and VGA). A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The GMCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe. The GMCH contains three display ports, 1 analog (DAC)

and two digital (SDVO ports B and C). The ports will be explained in more detail later in the chapter.

The entire IGD is fed with data from its memory controller. The GMCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR333), the rest of the IGD will also be affected.

The rest of this chapter will focus on explaining the IGD components, their limitations and dependencies.

12.6.1 3D Engine

The 3D engine of GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. GMCH supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipline are the Setup Engine, Scan Converter, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engine's performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engine's performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

12.6.2 Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH maintains sub-pixel accuracy.

12.6.2.1 3D Primitives and Data Formats Support

The 3D primitives rendered by GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans and polygons. In addition to this, GMCH supports the Microsoft DirectX* Flexible Vertex Format (FVF), which enables the application to specify a variable length of parameter list obviating the need for sending unused information to the hardware. Strips, Fans and Indexed Vertices as well as FVF, improve the vertex rate delivered to the setup engine significantly.

12.6.2.2 Pixel Accurate “Fast” Scissoring and Clipping Operation

The GMCH supports 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the scissor rectangle, avoiding processing pixels that fall outside the rectangle. The GMCH’s clipping and scissoring in hardware reduce the need for software to clip objects, and thus improve performance. During the setup stage, GMCH clips objects to the scissor window.

A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle needs to be pixel accurate, and independent of line and point width. The GMCH will support a single scissor box rectangle that can be enabled or disabled. The rectangle is defined as an Inclusive box. Inclusive is defined as “draw the pixel if it is inside the scissor rectangle”.

12.6.2.3 Depth Bias

The GMCH supports source Depth Biasing in the Setup Engine. The Depth Bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The Depth Bias value is added to the z or w value of the vertices. This is used for coplanar polygon priority. If two polygons are to be rendered that are coplanar, due to the inherent precision differences induced by unique x, y and z values, there is no guarantee which polygon will be closer or farther. By using Depth Bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

12.6.2.4 Backface Culling

As part of the setup, the GMCH discards polygons from further processing, if they are facing away from or towards the user’s viewpoint. This operation, referred to as “Back Face Culling” is accomplished based on the “clockwise” or “counter-clockwise” orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

12.6.2.5 Scan Converter

Working on a per-polygon basis, the Scan Converter uses the vertex and edge information is used to identify all pixels affected by features being rendered.

12.6.2.6 Pixel Rasterization Rules

The GMCH supports both OpenGL and D3D pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry will be used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

12.6.2.7 2D Functionality

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

12.6.3 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon.

The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, and bilinear interpolation), and YUV to RGB conversions.

12.6.3.1 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

12.6.3.2 Texture Formats and Storage

The GMCH supports up to 32 bits of color for textures.

12.6.3.3 Texture Decompression

DirectX supports Texture Compression to reduce the bandwidth required to deliver textures. As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism for compressing textures. Texture decompression formats supported include DXT1, DXT2, DXT3, DXT4, DXT5 and FXT1.

12.6.3.4 Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For "linear" texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

12.6.3.5 Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns that occur as a result of a very small number of pixels available on screen to contain the data of a high resolution texture map. More subtle effects are observed in animation, where very small primitives blink in and out of view.

12.6.3.6 Texture Map Filtering

The GMCH supports many texture mapping modes. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. Textures need not be square. Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The GMCH supports 7 types of texture filtering:

- Nearest (aka Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present).
- Linear (aka Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present).
- Nearest MIP Nearest (aka Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel is used.
- Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
- Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel is selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.
- Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used minimize the visibility of LOD transitions across the polygon.
- Anisotropic MIP Nearest (Anisotropic Filtering): This is used if many LODs are present. The nearest LOD-1 level will be determined for each of four sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.

Both D3D (DirectX 6.0 and later) and OpenGL (Revision 1.1) allow support for all these filtering modes.

12.6.3.7 Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP Maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

12.6.3.8 Bi-Cubic Filter (4x4 Programmable Texture Filter)

A bi-cubic texture filter can be selected instead of the bilinear filter. The implementation is of a 4x4 separable filter with loadable coefficients. A 4x4 filter can be used for providing high-quality up/ down scaling of 2D or 3D rendered images.

12.6.3.9 Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing processor load. There are several methods to generate environment maps (such as, spherical, circular and cubic). The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping requires a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

12.6.4 Raster Engine

The Raster Engine is where the color data (such as fogging, specular RGB, texture map blending, etc.) is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the Texture Engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha and depth buffer tests are conducted which will determine whether the Frame and Depth Buffers will be updated with the new pixel values.

12.6.4.1 Texture Map Blending

Multiple Textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports using a texture coordinate set to access multiple texture maps. State variables in multiple texture are bound to texture coordinates, texture map or texture blending.

12.6.4.2 Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated “specular RGB” attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high-quality reflective colored lighting effect not available in devices which apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, RGB values from the output of the map blending are added to values for RS, GS, BS on a component by component basis.

12.6.4.3 Color Shading Modes

The Raster Engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular Highlights(R,G,B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex’s attribute values for the other

two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

OpenGL and D3D use a different vertex to select the flat shaded color. This vertex is defined as the “provoking vertex”. In the case of strips/fans, after the first triangle, attributes on every vertex that define a primitive are used to select the flat color of the primitive. A state variable is used to select the “flat color” prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has a different value.

All the attributes can be selected independently from one of the shading modes by setting the appropriate value state variables.

12.6.4.4 Color Dithering

Color Dithering helps to hide color quantization errors. Color Dithering takes advantage of the human eye’s propensity to “average” the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5- or 6- bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed on the components

12.6.4.5 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects (such as low visibility conditions in flight simulator-type games). It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (fewer polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance. Higher fog density produces lower visibility for distant objects. There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit.

12.6.4.6 Alpha Blending (Frame Buffer)

Alpha Blending adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color ($R_SG_SB_S$) and alpha (A_S) component with a destination pixel color ($R_DG_DB_D$) and alpha (A_D) component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.

12.6.4.7 Microsoft DirectX* API and SGI OpenGL* API Logic Ops

Both APIs provide a mode to use bitwise ops in place of alpha blending. This is used for rubber-banding (i.e., draw a rubber band outline over the scene using an XOR operation). Drawing it again restores the original image without having to do a potentially expensive redraw.

12.6.4.8 Color Buffer Formats: 8-, 16-, or 32-bits per Pixel (Destination Alpha)

The Raster Engine supports 8-bit, 16-bit, and 32-bit Color Buffer Formats. The 8-bit format is used to support planar YUV420 format, which used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z will be allowed to mix.

The GMCH supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer of the GMCH contains at least two hardware buffers: the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing. This also speeds up the display process over a single buffer. Additionally, triple back buffering is also supported. The instruction set of the GMCH provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

12.6.4.9 Depth Buffer

The Raster Engine can read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values, as opposed to only 64 K with a 16-bit Z buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when W (or eye-relative Z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, allowing applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point.

The GMCH supports a flexible format for the floating-point W buffer, wherein the number of exponent bits is programmable. This allows the driver to determine variable precision as a function of the dynamic range of the W (screen-space Z) parameter.

The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

12.6.4.10 Stencil Buffer

The Raster Engine provides 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows and constructive solid geometry rendering.

12.6.4.11 Projective Textures

The GMCH supports two simultaneous projective textures at full rate processing, and four textures at half rate. These textures require three floating point texture coordinates to be included in the Flexible Vertex Format (FVF). Projective textures enable special effects (such as projecting spot light textures obliquely onto walls, etc.).

12.6.5 2D Engine

The GMCH contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions (such as Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs) make use of the 3D renderer.

12.6.5.1 GMCH VGA Registers

The 2D registers are a combination of registers defined by IBM when the Video Graphics Array (VGA) was first introduced and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

12.6.5.2 Logical 128-bit Fixed BLT and 256 Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the

destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The GMCH can perform hardware clipping during BLTs.

12.6.6 Video Engine

12.6.6.1 Hardware Motion Compensation

The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward, or bi-directionally) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The Motion Compensation functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally support the YUV420 planar input formats.

12.6.6.2 Sub-Picture Support

Sub-picture is used for two purposes; one is Subtitles for movie captions, etc. (that are superimposed on a main picture), and the other is Menus used to provide some visual operation environments the user of a content player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called "Subtitle" because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications, for example, as Subtitles in different languages or other information to be displayed.

There are two kinds of Menus; the System Menus and other In-Title Menus. First, the System Menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can use four methods when dealing with sub-pictures. The flexibility enables the GMCH to work with all sub- picture formats.

12.6.7 Planes

A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

12.6.7.1 Cursor Plane

The cursor planes are one of the simplest display planes. With a few exceptions, the cursor plane has a fixed size of 64x64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.

12.6.7.2 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the processor, with the graphics data on the screen. The source data can be mirrored horizontally or vertically or both.

Source/Destination Color Keying/ChromaKeying

Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color keying/ChromaKeying can be used to handle occluded portions of the overlay window on a pixel by pixel basis that is actually an underlay. Destination ChromaKeying would only be used for YUV passthrough to TV. Destination color keying supports a specific color (8- or 15-bit) mode as well as 32-bit alpha blending.

Source color keying/ChromaKeying is used to handle transparency based on the overlay window on a pixel by pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

Gamma Correction

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

YUV to RGB Conversion

The format conversion can be bypassed in the case of RGB source data. The format conversion assumes that the YUV data is input in the 4:4:4 format and uses the full range scale.

Maximum Resolution and Frequency

The maximum frequency supported by the overlay logic is 180 MHz. The maximum resolution is dependent on a number of variables (e.g., memory speed, memory latency, port selected, pipe selected, mode definition).

Deinterlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV) needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.

12.6.7.3 Advanced Deinterlacing and Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to deinterlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame; this is known as Weaving. This is the best solution for images with little motion however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or “Bob” interpolates adjacent lines rather than replicating the nearest neighbor. This is the best solution for images with motion; however, it will have reduced spatial resolution in areas that have no motion and introduces aliasing. In the absence of any other deinterlacing, these form the baseline and are supported by the GMCH.

Scaling Filter and Control

The scaling filter has three vertical taps and five horizontal taps. Arbitrary scaling (per pixel granularity) for any video source (YUV422 or YUV420) format is supported.

The overlay logic can scale an input image up to 1600X1200with no major degradation in the filter used as long as the maximum frequency limitation is met. Display resolution and refresh rate combinations where the dot clock is greater than the maximum frequency require the overlay to use pixel replication.

12.6.8 Pipes

The display consists of two pipes. The Pipes can operate in a single-wide or “double-wide” mode at 2x graphics core clock though they are effectively limited by the respective display port. The display planes and the cursor plane will provide a “double wide” mode to feed the pipe.

12.6.8.1 Clock Generator Units (DPLL)

The clock generator units provide a stable frequency for driving display devices. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25–400 MHz. Accuracy for VESA timing modes is required to be within ± 0.5%.

The DPLL can take a reference frequency from the external reference input (DREFCLKINN/P), the TV clock input (TVCLKIN).

12.7 Display Interfaces (Intel® 82915G/82915GV/82915GL/ 82910GL GMCH Only)

The GMCH has three display ports; one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The analog port is a dedicated port (not multiplexed) on the 82915GV/82915GL/82910GL GMCH. For the 82915G GMCH, the SDVO ports B and C are multiplexed with the PCI Express graphics interface and are not available if an external PCI Express graphics device is in use. When a 915G Express chipset system uses a PCI Express graphics connector, SDVO ports B and C can be used via an ADD2 (Advanced Digital Display 2) card. Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

- The GMCH's analog port uses an integrated 400 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 85 Hz.
- The GMCH's SDVO ports are each capable of driving a 200-MP pixel rate. Each port is capable of driving a digital display up to 1600x1200 @ 60Hz. When in dual-channel mode, the GMCH can drive a flat panel up to 2048x1536 @ 85 Hz or dCRT/HDTV up to 1920x1080 @ 85 Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

Table 12-6. Display Port Characteristics

Interface Protocol		Analog	Digital Port B	Digital Port C
		RGB DAC	DVO 1.0	DVO 1.0
Signals	HSYNC	Yes Enable/Polarity		
	VSYNC	Yes Enable/Polarity		
	BLANK	No	Yes[1]	Yes[1]
	STALL	No	Yes	Yes
	Field	No	Yes	Yes
	Display_Enable	No		No[1]
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1		
Pixel Aspect Ratio		Square		
Voltage		RGB 0.7 V p-p	PCI Express*	PCI Express*
Clock		NA	Differential	
Max Rate		400 Mpixel	200/400 Mpixel	
Format		Analog RGB	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1/DDC2B	DDC2B	
External Device		No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-I	DVI/CVBS/S-Video/Component/SCART	

NOTES:
1. Single signal software selectable between display enable and Blank#.

12.7.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices (such as LCD panels) with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 12-7. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
	Voltage	2.5 V
	Enable/Disable	Port control
HSYNC	Polarity adjust	VGA or port control
VSYNC	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5V
	Control	Through GPIO interface

12.7.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. The GMCH's integrated 400 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 85Hz. Three 8-bit DACs provide the RED, GREEN, and BLUE signals to the monitor.

12.7.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals power up disabled in the high state. No composite sync or special flat panel sync support is included.

12.7.1.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

12.7.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDC_CLK and DDC_DATA signals to communicate with the analog monitor. The GMCH generates these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

12.7.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two SDVO ports that are multiplexed on the PCI Express* x16 Graphics Interface. When an external PCI Express* x16 Graphics Interface graphics accelerator is not present, the GMCH can use the multiplexed SDVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD2 card that is designed to plug in to a PCI Express connector.

12.7.2.1 Digital Display Channels – SDVOB and SDVOC

The GMCH has the capability to support digital display devices through two SDVO ports. When an external graphics accelerator is used via the PCI Express* x16 Graphics Interface port, these SDVO ports are not available.

The shared SDVO ports each support a pixel clock up to 200 MHz and can support a variety of transmission devices. When using a dual-channel external transmitter, it will be possible to pair the two SDVO ports in dual-channel mode to support a single digital display with higher resolutions and refresh rates. In this mode, GMCH is capable of driving pixel clock up to 400 MHz.

SDVO_CTRLDATA is an open-drain signal that will act as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an SDVO interface. When implementing SDVO, either via ADD2 cards or with a down device, a pull-up is placed on this line to signal to the GMCH to run in SDVO mode and for proper GMBus operation.

12.7.2.2 ADD2 Card

When a 915G Express chipset platform uses a PCI Express* x16 Graphics Interface connector, the multiplexed SDVO ports may be used via an ADD2 card. The ADD2 card will be designed to fit a standard PCI Express (x16) connector.

12.7.2.2.1 TMDS Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT). When combining the two multiplexed SDVO ports, the GMCH can drive a flat panel up to 2048x1536 or a dCRT/HDTV up to 1920x1080. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external

device, but has no native panel fitting capabilities. The GMCH will, however, provide unscaled mode where the display is centered on the panel.

12.7.2.2.2 LVDS Capabilities

The GMCH may use the multiplexed SDVO ports to drive a LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will, however, provide unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the SDVO stall input pair.

12.7.2.2.3 TV-Out Capabilities

Although traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. GMCH supports NTSC and PAL standard definition formats. The GMCH generates the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed SDVO interface is a NTSC/PAL/SECAM display on the TV-Out port , it can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided. If EasyLink is supported in the GMCH, then this mechanism could be used to interrogate the display device.

The TV-Out interface on the GMCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation will be that the overlay source data is in the YUV format and will bypass the conversion to RBG as it is sent to the TV port directly.

Sync Lock Support

Sync lock to the TV will be done using the external encoders PLL combined with the display phase detector mechanism. The availability of this feature will be used to determine which external encoder is in use.

Analog Content Protection

Analog content protection is provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

Connectors

Target TV connectors support includes the CVBS, S-Video, Component, and SCART connectors. The external TV encoder in use will determine the method of support.

12.7.2.2.4 Control Bus

Communication to SDVO registers and if utilized, ADD2 PROMs and monitor DDCs, are accomplished by using the SDVO_CTRLDATA and SDVO_CTRLCLK signals through the SDVO device. These signals run up to 1 MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device datasheets for level shifting requirements of these signals.

Intel® SDVO Modes

The port can be dynamically configured in several modes:

- Standard – This mode provides baseline SDVO functionality. The mode supports pixel rates between 25 and 200 MP/s. It uses three data pairs to transfer RGB data.
- Extended (82915G only) – This mode adds Alpha support to data stream. Extended mode supports pixel rates between 25 MHz and 200 MP/s. The mode uses four data channels and is only supported on SDVOB. It leverages channel C (SDVOC) Red pair as the Alpha pair for channel B (SDVOB).
- Dual Standard – This mode uses standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 and 200 MP/s.
  - — Dual Independent Standard (82915G only) - In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVOB will not be the same as the data stream across SDVOC. This mode is only supported on the 82915G/82915GV/82915GL/82910GL GMCH.
  - — Dual Simultaneous Standard - In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVOB will be the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this uses just a single data stream, it uses a single pixel pipeline within the GMCH.

12.7.3 Multiple Display Configurations

Microsoft Windows* 2000 and Windows* XP operating systems have enabled support for multi-monitor display. Since the GMCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The GMCH supports Intel Dual Display Clone, Intel Dual Display Twin, and Extended Desktop.

Intel Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

Intel Dual Display Twin uses one of the display pipes to drive the same content, at the same resolution, color depth, and refresh rates to two different displays.

Extended Desktop (82915G only) uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows Desktop by using both displays as a work surface.

Note: The GMCH graphics engine is also incapable of operating in parallel with an external PCI Express graphics device. The GMCH graphics engine can, however, work in conjunction with a PCI graphics adapter.

12.8 Power Management

Power Management capabilities of the (G)MCH include the following:

- ACPI 1.0b support
- ACPI S0, S3, S4, S5, C0, C1, C2, C3, C4
- Enhanced power management state transitions for increasing time the processor spends in low power states
- Internal Graphics Display Device Control D0, D1, D2, D3 (82915G/82915GV/82915GL/82910GL GMCH only)
- Graphics Adapter States: D0, D3.
- PCI Express Link States: L0, L0s, L1, L2/L3 Ready, L3
- Conditional memory Self-Refresh during C2, C3, and C4 states

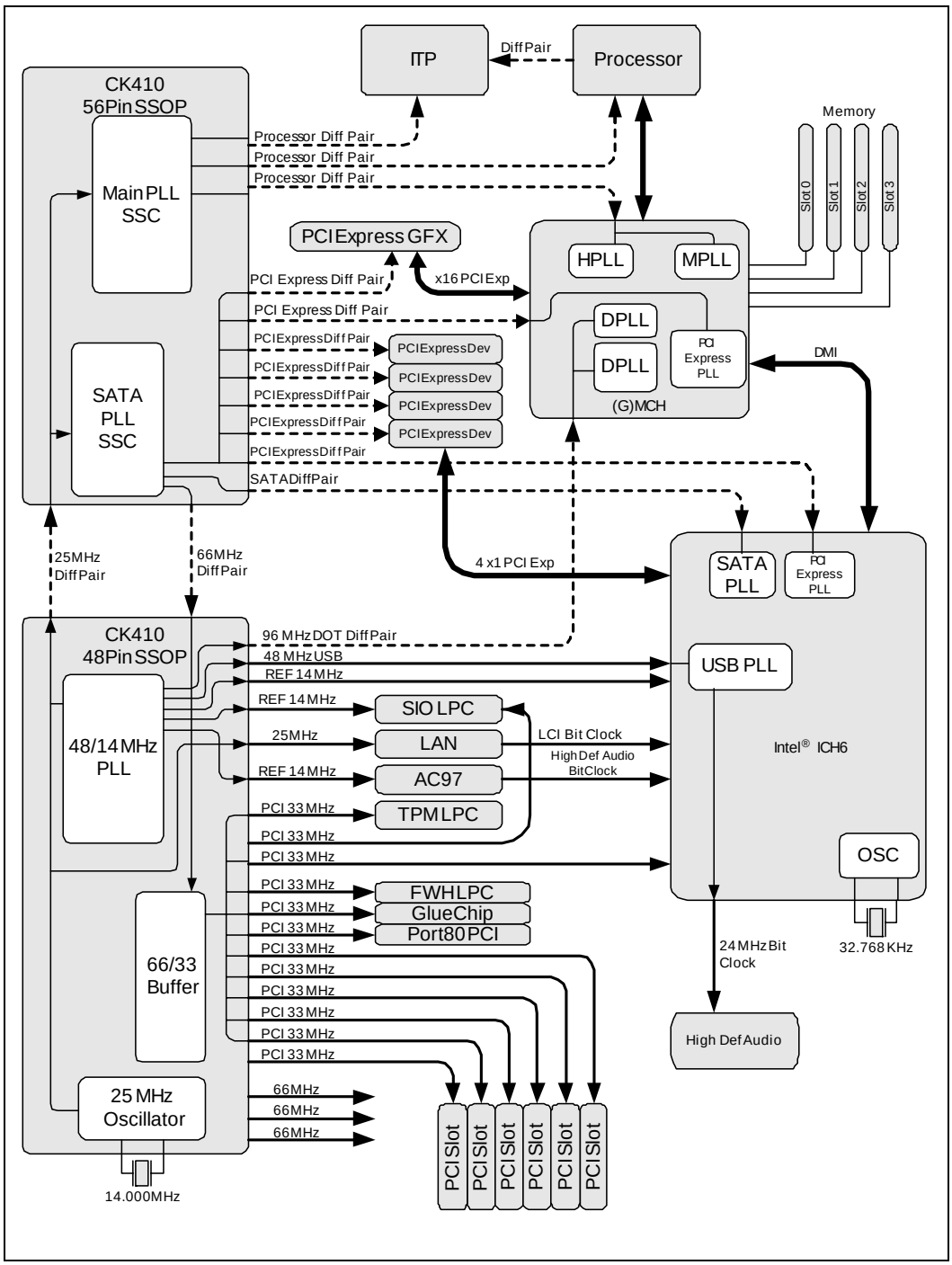
12.9 Clocking

The (G)MCH has a total of 5 PLLs providing the internal clocks. The PLLs are:

- Host PLL – This PLL generates the main core clocks in the host clock domain. The host PLL is used to generate memory and internal graphics core clocks. It uses the Host clock (H_CLKIN) as a reference.
- PCI Express PLL (82915G/92915P/82915PL (G)MCH Only) – This PLL generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH6. This PLL uses the 100 MHz (G_CLKIN) as a reference.
- Display PLL A PLL (82915G/92915GV/82915GL/82910GL GMCH Only) – This PLL generates the internal clocks for Display A. It uses D_REFCLKIN as a reference.
- Display PLL B (82915G/92915GV/82915GL/82910GL GMCH Only) – This PLL generates the internal clocks for Display B. It uses D_REFCLKIN as a reference.

Figure 12-3 illustrates the various clocks in the platform.

Figure 12-3. System Clocking Example



§

13 Electrical Characteristics

This chapter contains the (G)MCH absolute maximum electrical ratings, power dissipation values, and DC characteristics.

13.1 Absolute Maximum Ratings

Table 13-1 lists the (G)MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the DC characteristics tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 13-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	-55	150	°C	1
(G)MCH Core					
VCC	1.5 V Core Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
Host Interface (533 MHz/800 MHz)					
VTT	1.2 V System Bus Input Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_HPLL	1.5 V Host PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
DDR Interface (333 MHz/400 MHz)					
VCCSM (DDR)	2.6 V DDR System Memory Supply Voltage with respect to V_{SS}	-0.3	4.0	V	
VCCA_SMPLL (DDR)	1.5 V System Memory PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
DDR2 Interface (400 MHz/533 MHz)					
VCCSM (DDR2)	1.8 V DDR2 System Memory Supply Voltage with Respect to V_{SS}	-0.3	4.0	V	
VCCA_SMPLL (DDR2)	1.5 V System Memory PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	

Symbol	Parameter	Min	Max	Unit	Notes
PCI Express*/Intel® SDVO/DMI Interface					
VCC_EXP	1.5 V PCI Express and DMI Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_EXPPLL	1.5 V PCI Express PLL Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
RGB/CRT DAC Display Interface (8 bit) (Intel® 82915G/82915GV/82910GL GMCH only)					
VCCA_DAC	2.5 V Display DAC Analog Supply Voltage with respect to V_{SS}	-0.3	2.65	V	
VCCA_DPLLA	1.5 V Display PLL A Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
VCCA_DPLLB	1.5 V Display PLL B Analog Supply Voltage with respect to V_{SS}	-0.3	1.65	V	
CMOS Interface					
VCC2	2.5 V CMOS Supply Voltage with respect to V_{SS}	-0.3	2.65	V	

NOTES:
1. Possible damage to the (G)MCH may occur if the (G)MCH temperature exceeds 150 °C. Intel does not guarantee functionality for parts that have exceeded temperatures above 150 °C due to specification violation.

13.2 Power Characteristics

Table 13-2. Non-Memory Power Characteristics

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
I_{VTT}	1.2 V System Bus Supply Bus Current	VTT	—	—	1.0	A	1, 4
I_{VCC}	1.5 V Core Supply Current (Integrated)	VCC	—	—	9.7	A	2,3,4
I_{VCC}	1.5 V Core Supply Current (Discrete)	VCC	—	—	7.7	A	2,3,4
I_{VCC_EXP}	1.5 V PCI Express and DMI Supply Current	VCC_EXP	—	—	1.4	A	
I_{VCCA_DAC}	2.5 V Display DAC Analog Supply Current	VCCA_DAC	—	—	70	mA	
I_{VCC2}	2.5 V CMOS Supply Current	VCC2	—	—	2	mA	
I_{VCCA_EXPPLL}	1.5 V PCI Express and DMI PLL Analog Supply Current	VCCA_EXPPLL	—	—	45	mA	
I_{VCCA_HPLL}	1.5 V Host PLL Supply Current	VCCA_HPLL	—	—	45	mA	
I_{VCCA_DPLLA} I_{VCCA_DPLLB}	1.5 V Display PLL A and PLL B Supply Current	VCCA_DPLLA VCCA_DPLLB	—	—	55	mA	

NOTES:
1. Estimate is only for max current coming through Chipset's supply balls
2. Rail includes PLL current
3. Includes Worst case Leakage
4. Calculated for highest frequencies

Table 13-3. DDR Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{VCCSM} (DDR)	DDR System Memory Interface (2.6 V) Supply Current	—	4.1	A	
I_{SUS_VCCSM} (DDR)	DDR System Memory Interface (2.6 V) Standby Supply Current	—	25	mA	
I_{SMVREF} (DDR)	DDR System Memory Interface Reference Voltage (1.3 V) Supply Current	—	10	µA	
I_{SUS_SMVREF}	DDR System Memory Interface Reference Voltage (1.3 V) Standby Supply Current	—	10	µA	
I_{TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.6 V) Supply Current	—	42	mA	
I_{SUS_TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.6 V) Standby Supply Current	—	0	µA	
I_{VCCA_SMPLL} (DDR)	System Memory PLL Analog (1.5 V) Supply Current	—	60	mA	

Table 13-4. DDR2 Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) Supply Current	—	4.7	A	
I_{SUS_VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) Standby Supply Current	—	25	mA	
I_{SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current	—	10	µA	
I_{SUS_SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current	—	10	µA	
I_{TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	—	32	mA	
I_{SUS_TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current	—	0	µA	
I_{VCCA_SMPLL} (DDR2)	System Memory PLL Analog (1.5 V) Supply Current	—	60	mA	

13.3 Signal Groups

The signal description includes the type of buffer used for the particular signal:

GTL+ Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The (G)MCH integrates most GTL+ termination resistors.

DDR DDR System memory (2.6 V CMOS buffers)

DDR2 DDR2 System memory (1.8 V CMOS buffers)

PCI Express/SDVO PCI Express interface signals. These signals are compatible with PCI Express 1.0a signaling environment AC Specifications. The buffers are **not** 3.3 V tolerant.

Analog Analog signal interface

Ref Voltage reference signal

HVCMOS 2.5 V Tolerant High Voltage CMOS buffers

SSTL-2 2.6 V Tolerant Stub Series Termination Logic

SSTL-1.8 1.8 V Tolerant Stub Series Termination Logic

Table 13-5. Signal Groups

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	GTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0], HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK#	
(b)	GTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#, HEDRDY#	
(c)	GTL+ Asynchronous Input	BSEL[2:0], HPCREQ#	
(d)	Analog Host I/F Ref & Comp. Signals	HVREF, HSWING HRCOMP, HSCOMP	
PCI-Express Graphics and SDVO Interface Signal Groups			
(e)	PCI Express/SDVO Input	**PCI Express Interface (82915G/82915P/82915PL (G)MCH only):** EXP_RXN[15:0], EXP_RXP[15:0], **SDVO Interface (82915G/82915GV/82915GL/82910GL GMCH only):** SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVOB_INT#, SDVOB_INT, SDVO_STALL#, SDVO_STALL, SDVOC_INT#, SDVOC_INT	

Signal Group	Signal Type	Signals	Notes
(f)	PCI Express/SDVO Output	**PCI Express Interface (82915G/82915P/82915PL (G)MCH only):** EXP_TXN(15:0), EXP_TXP(15:0) **SDVO Interface (82915G/82915GV/82915GL/82910GL GMCH only):** SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLK, SDVOB_CLK#, SDVOC_RED#/SDVOB_ALPHA#, SDVOC_RED/SDVOB_ALPHA, SDVOC_GREEN#, SDVOC_GREEN SDVOC_BLUE#, SDVOC_BLUE, SDVOC_CLK, SDVOC_CLK#	
(g)	Analog PCI Express / SDVO Interface Compensation Signals	EXP_COMP0 EXP_COMPI	
DDR Interface Signal Groups			
(h)	SSTL- 2 DDR CMOS I/O	SDQ_A[63:0], SDQ_B[63:0], SDQS_A[7:0], SDQS_B[7:0]	
(i)	SSTL – 2 DDR CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA_A[13:0], SMA_B[13:0], SBS_A[1:0], SBS_B[1:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B# SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(j)	DDR Reference Voltage	SMVREF[1:0] (DDR)	
DDR2 Interface Signal Groups (Intel® 82915G/82915GV GMCH and 82915P MCH only)			
(k)	SSTL – 1.8 DDR2 CMOS I/O	SDQ_A[63:0]#, SDQ_B[63:0]#, SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0]#, SDQS_B[7:0]#	
(l)	SSTL – 1.8 DDR2 CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA[13:0], SMA_B[13:0], SBS_A[2:0], SBS_B[2:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(m)	DDR2 Reference Voltage	SMVREF[1:0] (DDR2)	

Signal Group	Signal Type	Signals	Notes
RGB/CRT DAC Display Signal Groups (Intel® 82915G/82915GV/82915GL/82910GL GMCH only)			
	Analog Current Outputs	RED, RED#, GREEN, GREEN#, BLUE, BLUE#	
	Analog/Ref DAC Miscellaneous	REFSET	Current Mode Reference pin. DC Spec. not required
	CMOS Type	HSYNC, VSYNC	
Clocks, Reset, and Miscellaneous Signal Groups			
(n)	HVCMOS Input	EXTTS#	
(n1)	Miscellaneous Inputs	RSTIN#, PWROK	
(0)	Low Voltage Diff. Clock Input	HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN	
(p)	HVCMOS I/O	SDVO_CRTLCLK, SDVO_CTRLDATA, DDC_CLK, DDC_DATA	
I/O Buffer Supply Voltages			
(q)	1.2 V System Bus Input Supply Voltage	VTT	
(r)	1.5 V SDVO, PCI Express Supply Voltages	VCC_EXP	
(s)	2.6 V DDR Supply Voltage	VCCSM (DDR)	
(t)	1.8 V DDR2 Supply Voltage	VCCSM (DDR2)	
(u)	1.5 V DDR PLL Analog Supply Voltage	VCCA_SMPLL (DDR)	
(v)	1.5 V DDR2 PLL Analog Supply Voltage	VCCA_SMPLL (DDR2)	
(w)	1.5 V (G)MCH Core Supply Voltage	VCC	
(x)	2.5 V CMOS Supply Voltage	VCC2	
(y)	2.5 V RGB/CRT DAC Display Analog Supply Voltage	VCCA_DAC	
(z)	PLL Analog Supply Voltages	VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	

13.4 DC Characteristics

13.4.1 General DC Characteristics

Table 13-6. DC Characteristics[3]

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage (AC Noise not included)							
VCCSM (DDR)	(s)	DDR I/O Supply Voltage	2.5	2.6	2.7	V	
VCCSM (DDR2)	(t)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCCA_SMPLL (DDR)	(u)	DDR I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCCA_SMPLL (DDR2)	(v)	DDR2 I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCC_EXP	(r)	SDVO, PCI-Express Supply Voltage	1.425	1.5	1.575	V	
VTT	(q)	System Bus Input Supply Voltage	1.09	1.2	1.26	V	
VCC	(w)	(G)MCH Core Supply Voltage	1.425	1.5	1.575	V	
VCC2	(x)	CMOS Supply Voltage	2.375	2.5	2.625	V	
VCCA_DAC	(y)	CRT Display DAC Supply Voltage	2.375	2.5	2.625	V	
VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB	(z)	Various PLL'S Analog Supply Voltages	1.425	1.5	1.575	V	
Reference Voltages							
HVREF	(d)	Host Address, Data, and Common Clock Signal Reference Voltage	2/3 x V_{TT1}– 2%	2/3 x V_{TT}	2/3 x V_{TT} + 2%	V	
HSWING	(d)	Host Compensation Reference Voltage	1/4 x V_{TT} – 2%	1/4 x VTT	1/4 x V_{TT} + 2%	V	
SMVREF (DDR)	(j)	DDR Reference Voltage	0.50 x VCCSM(DDR) – 0.05	0.50 x VCCSM (DDR)	0.50 x VCCSM(DDR) + 0.05	V	
SMVREF (DDR2)	(m)	DDR2 Reference Voltage	0.49 x VCCSM (DDR2)	0.50 x VCCSM (DDR2)	0.51 x VCCSM (DDR2)	V	
Host Interface							
V_{IL_H}	(a, c)	Host GTL+ Input Low Voltage	-0.10	0	(2/3 x V_{TT}) – 0.1	V	
V_{IH_H}	(a, c)	Host GTL+ Input High Voltage	(2/3 x V_{TT}) + 0.1	V_{TT}	V_{TT} + 0.1	V	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
V_{OL_H}	(a, b)	Host GTL+ Output Low Voltage	—	—	(0.25 x V_{TT})+0.1	V	
V_{OH_H}	(a, b)	Host GTL+ Output High Voltage	V_{TT} – 0.1	—	V_{TT}	V	
I_{OL_H}	(a, b)	Host GTL+ Output Low Current	—	—	V_{TTmax} / (1-0.25)Rttmin	mA	Rtt_{min} = 54Ω
I_{LEAK_H}	(a, c)	Host GTL+ Input Leakage Current	—	—	20	µA	V_{OL}<Vpad<Vtt
C_{PAD}	(a, c)	Host GTL+ Input Capacitance	2	—	3.5	pF	
C_{PCKG}	(a, c)	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	
DDR Interface							
$V_{IL(DC)}$ (DDR)	(h)	DDR Input Low Voltage	—	—	SMVREF (DDR) – 0.15	V	
$V_{IH(DC)}$ (DDR)	(h)	DDR Input High Voltage	SMVREF (DDR) + 0.15	—	—	V	
$V_{IL(AC)}$ (DDR)	(h)	DDR Input Low Voltage	—	—	SMVREF (DDR) – 0.31	V	
$V_{IH(AC)}$ (DDR)	(h)	DDR Input High Voltage	SMVREF (DDR) + 0.31	—	—	V	
V_{OL} (DDR)	(h, i)	DDR Output Low Voltage	—	—	0.4	V	1
V_{OH} (DDR)	(h, i)	DDR Output High Voltage	2.1	—		V	1
I_{Leak} (DDR)	(h)	Input Leakage Current	—	—	±10	µA	
$C_{I/O}$ (DDR)	(h, i)	DDR Input/Output Pin Capacitance	3.0	—	6.0	pF	
DDR2 Interface (Intel® 82915G/82915GV GMCH and 82915P MCH only)							
$V_{IL(DC)}$ (DDR2)	(k)	DDR2 Input Low Voltage	—	—	SMVREF (DDR2) – 0.125	V	
$V_{IH(DC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.125	—	—	V	
$V_{IL(AC)}$ (DDR2)	(k)	DDR2 Input Low Voltage	—	—	SMVREF (DDR2) – 0.250	V	
$V_{IH(AC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.250	—	—	V	
V_{OL} (DDR2)	(k, l)	DDR2 Output Low Voltage	—	—	0.3	V	1
V_{OH} (DDR2)	(k, l)	DDR2 Output High Voltage	1.5	—		V	1
I_{Leak} (DDR2)	(k)	Input Leakage Current	—	—	±10	uA	
$C_{I/O}$ (DDR2)	(k, l)	DDR2 Input/Output Pin Capacitance	3.0	—	6.0	pF	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
1.5 V PCI Express Interface 1.0a (includes PCI Express and SDVO)							
$V_{TX-DIFF\ P-P}$	(f)	Differential Peak to Peak Output Voltage	0.400	—	0.600	V	2
V_{TX_CM-ACp}	(f)	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX-DIFF-DC}$	(f)	DC Differential TX Impedance	80	100	120	Ohms	
$V_{RX-DIFF\ p-p}$	(e)	Differential Peak to Peak Input Voltage	0.175	—	0.600	V	3
V_{RX_CM-ACp}	(e)	AC peak Common Mode Input Voltage	—	—	150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(n)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(n)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(n)	Input Leakage Current	—	—	±10	µA	
C_{IN}	(n)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(o)	Input Low Voltage	—	0	—	V	
V_{IH}	(o)	Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS}	(o)	Crossing Voltage	0.45 x (V_{IH} – V_{IL})	0.5 x (V_{IH} – V_{IL})	0.55 x (V_{IH} – V_{IL})	V	
V_{OL}	(p)	Output Low Voltage (CMOS Outputs)	—	—	0.4	V	
V_{OH}	(p)	Output High Voltage (CMOS Outputs)	2.1	—	—	V	
I_{OL}	(p)	Output Low Current (CMOS Outputs)	—	—	1	mA	@V_{OL_HI} max
I_{OH}	(p)	Output High Current (CMOS Outputs)	-1	—	—	mA	@V_{OH_HI} min
V_{IL}	(p)	Input Low Voltage	—	—	1.1	V	
V_{IH}	(p)	Input High Voltage	1.4	—	—	V	
I_{LEAK}	(p)	Crossing Voltage	—	—	±10	µA	
C_{IN}	(p)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(n1)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(n1)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(n1)	Crossing Voltage	—	—	±100	µA	0<Vin<VCC3_3
C_{IN}	(n1)	Input Capacitance	4.690	—	5.370	pF	

NOTES:

1. Determined with 2x (G)MCH DDR/DDR2 Buffer Strength Settings into a 50 Ω to 0.5xVCCSM (DDR/DDR2) test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI-E specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI-E specification should be used as the RX device when taking measurements.

13.4.2 RGB/CRT DAC Display DC Characteristics (Intel® 82915G/82915GV/82915GL/82910GL GMCH Only)

Table 13-7. RGB/CRT DAC Display DC Characteristics (Functional Operating Range: VCCA_DAC = 2.5 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	—	8	—	Bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1, 2, 4; white video level voltage
Min Luminance	—	0.000	—	V	1, 3, 4; black video level voltage
LSB Current	—	73.2	—	µA	4, 5
Integral Linearity (INL)	-1.0	—	+1.0	LSB	1, 6
Differential Linearity (DNL)	-1.0	—	+1.0	LSB	1, 6
Video channel-channel voltage amplitude mismatch	—	—	6	%	7
Monotonicity	Guaranteed			—	

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75-Ohm termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA Video Signal Standards.
7. Max full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).

§

14 Ballout and Package Information

The (G)MCH ballout supports platforms using DDR2 and DDR system memory. The (G)MCH's system memory interface ballout differs between DDR2 and DDR modes.

Note: The DDR and DDR2 signals are multiplexed so that they are supported on the same package.

14.1 DDR2 Ballout

Figure 14-1, Figure 14-2, and Figure 14-3 show the 82915G GMCH ballout for platforms using DDR2 system memory, as viewed from the top side of the package. Figure 14-1 shows columns 1–12; Figure 14-2 shows columns 13–24; Figure 14-3 shows columns 25–35.

The complete DDR2 ballout for the 82915G/82915GV/82910GL GMCH and 82915P MCH are listed in Table 14-1 and Table 14-2. Table 14-1 is sorted by ball number. Table 14-2 is sorted alphabetically by signal name based on the signal names of the 82915G GMCH. Note that the first table has more entries than the second table. The second table does not include unpopulated balls whereas the first table does.

Note: Balls that are listed as RSV are Reserved. Board traces should **Not** be routed to these balls.

Note: Balls that are listed as NC are No Connects. Board traces to these balls are permitted as specified.

Figure 14-1. Intel® 82915G GMCH Ballout for DDR2 (Top View: Columns 1–12)

	1	2	3	4	5	6	7	8	9	10	11	12
A		NC	VSS		VSS	EXP_TXN3	EXP_TXP3	EXP_TXN1	EXP_TXP1	VSS	GCLKP	VCCA_ DPLLA
B	NC	VSS	EXP_RXP4	EXP_RXN4	VSS	VSS	VSS	VSS	VSS	VSS	GCLKN	VSS
C	VSS	EXP_TXP5	VSS	VSS	EXP_TXN4	EXP_TXP4	EXP_TXN2	EXP_TXP2	EXP_TXN0	EXP_TXP0	VSS	
D		EXP_TXN5	VSS	VSS	EXP_RXP5	VSS	VSS	VSS	VSS	VSS	VSS	VSYNC
E	VSS	VSS	EXP_TXP6	VSS	EXP_RXN5	VSS	EXP_RXN3	VSS	EXP_RXN2	VSS	EXP_RXP0	HSYNC
F	EXP_TXP7	VSS	EXP_TXN6	VSS	VSS	VSS	EXP_RXP3	VSS	EXP_RXP2	VSS	EXP_RXN0	NC
G	EXP_TXN7	VSS	EXP_TXP8	VSS	EXP_RXN6	EXP_RXP6	VSS	VSS	VSS	VSS	VSS	NC
H	EXP_TXP9	VSS	EXP_TXN8	VSS	VSS	VSS	EXP_RXN7	EXP_RXP7	VSS	VSS	EXP_RXN1	NC
J	EXP_TXN9	VSS	EXP_ TXP10	VSS	EXP_RXN8	EXP_RXP8	VSS	VSS	VSS	VSS	EXP_RXP1	NC
K	EXP_ TXP11	VSS	EXP_ TXN10	VSS	VSS	VSS	EXP_RXN9	EXP_RXP9	VSS	VSS	VSS	NC
L	EXP_ TXN11	VSS	EXP_ TXP12	VSS	EXP_ RXN10	EXP_ RXP10	VSS	VSS	VSS	VCC	VSS	NC
M	EXP_ TXP13	VSS	EXP_TXN1 2	VSS	VSS	VSS	EXP_ RXN12	EXP_ RXP12	VSS	VSS	VSS	DREFCLKN
N	EXP_ TXN13	VSS	EXP_ TXP14	VSS	EXP_ RXN13	EXP_ RXP13	VSS	VSS	VSS	VSS	VSS	NC
P	EXP_ TXP15	VSS	EXP_ TXN14	VSS	VSS	VSS	EXP_ RXP14	EXP_ RXN14	VSS	EXP_ RXP11	VSS	NC
R	EXP_ TXN15	VSS	DMI_TXP0	VSS	EXP_ RXN15	EXP_ RXP15	VSS	VSS	VSS	EXP_ RXN11	VSS	NC
T	DMI_TXP1	VSS	DMI_TXN0	VSS	VSS	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	VSS	NC
U	DMI_TXN1	VSS	DMI_TXP2	VSS	DMI_RXP0	DMI_RXN0	VSS	VSS	VSS	DMI_RXN3	VSS	NC
V	VSS	VSS	DMI_TXN2	VSS	DMI_TXP3	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXP3	VSS	NC
W	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	DMI_TXN3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_ COMPI	VSS	NC
Y	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_ COMPO	VSS	NC
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	NC
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSV
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B20
AE	SDQ_A5	SDQ_A4	SDQ_A0	VSS	SOCOMP1	VSS	SMVREF0	SMVREF1	VSS	SM_SLEW OUT1	SDQ_B11	VSS
AF	VSS	SDM_A0	SDQ_A1	VSS	SOCOMP0	VSS	RSTIN#	VSS	SM_ SLEWIN1	VSS	SDQ_B10	VSS
AG	SDQS_A0	SDQS_A0#	SDQ_A6	SRCOMP0	VSS	NC	PWROK	SRCOMP1	SDQ_B4	SDQ_B14	SDQ_B15	VSS
AH	VSS	SDQ_A7	SDQ_A2	SDQ_B0	VSS	VSS	SDQ_B5	VSS	SDM_B1	SDQS_B1#	VSS	SDQ_B17
AJ	SDQ_A12	SDQ_A3	SDQ_A13	VSS	SDM_B0	SDQ_B1	SDQ_B12	SDQ_B8	VSS	VSS	SCLK_B4	SM_ SLEWIN0
AK	VSS	SDQ_A8	SDQ_A9	VSS	SDQS_B0	VSS	VSS	VSS	SCLK_B1	SDQS_B1	VSS	SM_SLEW OUT0
AL	SDM_A1	SDQS_A1#	SDQS_A1	SDQS_B0#	SDQ_B6	SDQ_B2	SDQ_B13	SDQ_B9	SCLK_B1#	VSS	SCLK_B4#	SMA_B7
AM		SCLK_A1	SCLK_A1#	VSS	SDQ_B7	VSS	VSS	VSS	SCKE_B3	VCCSM	VCCSM	SMA_B5
AN	VSS	SCLK_A4#	SCLK_A4	SDQ_A10	SDQ_A20	SDQ_B3	SDM_A2	SDQ_A22	SDQ_A19	SCKE_B1	SBS_B2	
AP	NC	SDQ_A14	SDQ_A15	SDQ_A11	SDQ_A21	SDQ_A17	SDQS_A2	VSS	SDQ_A18	SCKE_B0	SMA_B11	VCCSM
AR	NC	NC	VSS		SDQ_A16	VSS	SDQS_A2#	SDQ_A23	SCKE_B2	VCCSM	SMA_B12	SMA_B9
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 14-2. Intel® 82915G GMCH Ballout for DDR2 (Top View: Columns 13–24)

	13	14	15	16	17	18	19	20	21	22	23	24
A	VCC2	VCCA_EXPPLL	REFSET	EXP_SLR	VCCA_HPLL	VSS	VTT	VTT	VTT	VTT	HSWING	HVREF
B	VCCA_DPLLB	VSS	RSV	VSS	VCCA_SMPLL	VSS	VTT	VTT	VTT	VTT	HRCOMP	VSS
C	VSS	RSV	MTYPE	NC	VSS	VSS	VTT	VTT	VTT	VTT	VSS	
D	VCCA_DAC	GREEN	VSS	VSS	BSEL2	VSS	VTT	VTT	VTT	VTT	VSS	HSCOMP
E	VCCA_DAC	GREEN#	BSEL1	NC	VSS	VSS	VTT	VTT	VTT	VTT	VSS	HD62
F	VSSA_DAC	RED	RSV	VSS	HD47	VSS	HDSTBN2#	VTT	VTT	VTT	VSS	NC
G	VSS	RED#	VSS	RSV	VSS	HD45	VSS	VSS	VTT	VTT	VSS	HCPURST#
H	VSS	BLUE	NC	BSEL0	NC	HD46	HD41	HD40	VSS	VTT	HD37	VSS
J	SDVO_CTRLCLK	BLUE#	VSS	VSS	VSS	VSS	HDSTBP2#	VSS	HD35	HD32	VSS	HD33
K	SDVO_CTRLDATA	VSS	RSV	EXTTS#	HD44	HD43	HDINV2#	VSS	HD39	HD34	HD31	VSS
L	VSS	DDC_DATA	VSS	VSS	VSS	VSS	NC	VSS	VSS	VSS	HD30	VSS
M	DREFCLKP	ICH_SYNC#	DDC_CLK	RSV	VSS	HD42	HD38	VSS	HD36	HCLKN	HCLKP	VSS
N	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VCC	NC	NC	NC
P	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	NC	NC
R	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	NC
T	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VSS	VCC	VCC
U	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC
V	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC
W	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC
Y	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VSS	VCC	VCC
AA	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC	VCC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC
AC	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	NC	NC
AD	VSS	SDQ_B18	SDQ_B19	VSS	SDQ_A30	SDQ_B28	VSS	SDQS_B3	SDQ_B27	VSS	SDQ_B37	SDM_B6
AE	SDQ_B21	VSS	VSS	RSV_TP0	VSS	VSS	SDQ_A31	VSS	VSS	SDQ_B30	VSS	VSS
AF	SDQ_B16	SDQ_B23	VSS	SDQ_A29	SDQS_A3	VSS	SDQ_A26	SDQS_B3#	VSS	SDQ_B31	SDQ_B36	SDQ_B32
AG	VSS	SDQ_B22	VSS	VSS	SDQS_A3#	VSS	VSS	SDM_B3	VSS	VSS	SCLK_B0#	SDM_B4
AH	SDM_B2	VSS	RSV_TP1	SDM_A3	VSS	SDQ_A27	SDQ_B25	VSS	SDQ_B26	SCLK_B0	VSS	NC
AJ	VSS	NC	VSS	VSS	SDQ_A25	RSV	VSS	RSV	RSV	VSS	RSV	RSV
AK	SDQS_B2	VSS	RSV_TP3	SDQ_A28	VSS	RSV	SDQ_B24	VSS	RSV	SCLK_B3#	VSS	RSV
AL	VSS	SDQS_B2#	SMA_B3	VSS	SDQ_A24	SDQ_B29	VSS	RSV	RSV	VSS	SCLK_B3	SMA_A2
AM	VCCSM	VCCSM	SMA_B0	VCCSM	VCCSM	SCKE_A1	VCCSM	VCCSM	SMA_A11	VCCSM	VCCSM	SCLK_A3#
AN	SMA_B8	RSV_TP2	SMA_B2	SBS_B1	SRAS_B#	SCKE_A2	NC	SBS_A2	SMA_A9	SMA_A8	SMA_A6	
AP	SMA_B6	SMA_B4	SMA_B10	VCCSM	SWE_B#	SCAS_B#	SCKE_A0	VCCSM	SMA_A7	SMA_A5	SMA_A3	VCCSM
AR	VSS	VCCSM	SMA_B1	SBS_B0	VSS	VCCSM	SCKE_A3	SMA_A12	VSS	VCCSM	SMA_A4	SMA_A1
	13	14	15	16	17	18	19	20	21	22	23	24

Figure 14-3. Intel® 82915G GMCH Ballout for DDR2 (Top View: Columns 25–35)

25	26	27	28	29	30	31	32	33	34	35	
HD48	VSS	HD61	HD57	HD55	VSS	HD53		VSS	NC	NC	A
HD63	HDINV3#	HD54	VSS	HDSTBP3#	HD51	HD52	HD15	HD13	HD11	NC	B
HD58	HD59	HD49	HD56	HDSTBN3#	HD17	HD50	HD14	HD9	HD12	VSS	C
VSS	VSS	HD60	VSS	HD18	VSS	VSS	VSS	HD10	HD8		D
HD25	VSS	HD24	HD16	VSS	HBPRI#	HPCREQ#	HREQ1#	HDSTBP0#	HDINV0#	HDSTBN0#	E
VSS	HDSTBN1#	HD23	HD22	VSS	VSS	HREQ4#	VSS	HREQ0#	HD6	VSS	F
HD26	VSS	VSS	VSS	HD20	HA6#	HREQ3#	HA7#	HD7	HD5	HD3	G
VSS	HDSTBP1#	VSS	HD19	HA3#	VSS	HREQ2#	VSS	HD1	VSS	HD4	H
HD27	HDINV1#	HD21	HA13#	HA5#	VSS	HADSTB0#	HRS2#	HD0	HD2	HDEFER#	J
HD28	VSS	HA14#	VSS	HA4#	HA8#	VSS	VSS	HA15#	HRS0#	VSS	K
HD29	HA18#	VSS	HA12#	HA9#	VSS	HA11#	VSS	HLOCK#	HHIT#	HDBSY#	L
VSS	HA20#	VSS	HA16#	VSS	HA10#	HADS#	HDRDY#		VSS	HBNR#	M
VSS	HA19#	HADSTB1#	VSS	HA23#	VSS	HA21#	VSS	HA26#	HTRDY#	HHITM#	N
VSS	HA22#	VSS	HA24#	VSS	NC	VSS	VSS	HEDRDY#	HRS1#	VSS	P
VSS	VSS	VSS	HA25#	HA17#	RSV	RSV	SDQ_A58	HBREQ0#	SDQ_A59	RSV	R
VSS	HA30#	HA27#	VSS	HA31#	VSS	HA28#	VSS	SDQ_A62	VSS	SDQ_A63	T
VSS	SDQ_B63	VSS	HA29#	VSS	RSV	VSS	VSS	SDM_A7	SDQS_A7	SDQS_A7#	U
VSS	VSS	VSS	SDQ_B58	SDQ_B59	RSV	RSV	RSV	SDQ_A57	SDQ_A56	VSS	V
VSS	SDQ_B62	SDQS_B7	VSS	SDQ_B57	VSS	SDM_B7	VSS	SDQ_A61	SDQ_A51	SDQ_A60	W
VSS	SDQ_B60	VSS	SDQS_B7#	VSS	RSV	VSS	VSS	SDQ_A50	VSS	SDQ_A55	Y
VSS	VSS	VSS	SDQ_B56	SDQ_B61	RSV	RSV	SDQ_A54	SDM_A6	SDQS_A6	SDQS_A6#	AA
VSS	SDQ_B51	SDQ_B55	VSS	RSV	VSS	SDQS_B6	VSS	RSV	SCLK_A5#	VSS	AB
VSS	SDQ_B50	VSS	SDQ_B54	VSS	SDQS_B6#	VSS	VSS	SCLK_A5	SCLK_A2	SCLK_A2#	AC
VSS	VSS	VSS	SCLK_B5	SCLK_B5#	NC	SDQ_A48	RSV		VSS	SDQ_A49	AD
SCLK_B2#	SCLK_B2	SDQ_B49	VSS	SDQ_B53	VSS	SDQ_B52	VSS	SDQ_A43	SDQ_A53	SDQ_A52	AE
SDQ_B33	VSS	SDQ_B48	SDQ_B43	VSS	VSS	VSS	VSS	SDQ_A42	SDQ_A47	VSS	AF
VSS	SDQS_B4#	SDQ_B47	VSS	VSS	SDQ_B46	SDQ_B42	SDQ_A46	SDQS_A5#	SDM_A5	SDQS_A5	AG
SDQS_B4	VSS	SDQ_A36	SDQS_B5	VSS	SDQS_B5#	SDM_B5	VSS	SDQ_A40	VSS	SDQ_A41	AH
SDQ_B39	SDQ_B35	VSS	SDQ_A33	SDQ_B44	VSS	SDQ_B41	VSS	SDQ_A44	SDQ_A45	VSS	AJ
VSS	VSS	SDQ_A32	VSS	SDM_A4	VSS	SDQ_A35	SDQ_B40	SDQ_B45	SODT_B3	VCCSM	AK
SDQ_B38	SDQ_B34	SDQ_A37	NC	SDQS_A4#	SDQ_A39	SDQ_A34	VSS	SMA_B13	SODT_B1	SODT_B2	AL
VCCSM	VCCSM	SMA_A10	VCCSM	VSS	SDQS_A4	VSS	VCCSM	SODT_B0	SCS_B1#		AM
SCLK_A3	SCLK_A0	SBS_A1	SWE_A#	SCAS_A#	SDQ_A38	SCS_A3#	SODT_A1	SCS_B0#	SCS_B3#	VCCSM	AN
SCLK_A0#	SMA_A0	SRAS_A#	VCCSM	SODT_A2	SODT_A0	SMA_A13	SCS_A1#	SODT_A3	SCS_B2#	NC	AP
VSS	VCCSM	SBS_A0	SCS_A2#	SCS_A0#	VSS	VCCSM		VCCSM	NC	NC	AR
25	26	27	28	29	30	31	32	33	34	35	

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
A1	—	—	—
A2	NC	NC	NC
A3	VSS	VSS	VSS
A4	—	—	—
A5	VSS	VSS	VSS
A6	EXP_TXN3	EXP_TXN3	SDVOB_CLK-
A7	EXP_TXP3	EXP_TXP3	SDVOB_CLK+
A8	EXP_TXN1	EXP_TXN1	SDVOB_GREEN-
A9	EXP_TXP1	EXP_TXP1	SDVOB_GREEN+
A10	VSS	VSS	VSS
A11	GCLKP	GCLKP	GCLKP
A12	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA
A13	VCC2	VCC2	VCC2
A14	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL
A15	RSV	REFSET	REFSET
A16	EXP_SLR	EXP_SLR	RSV
A17	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL
A18	VSS	VSS	VSS
A19	VTT	VTT	VTT
A20	VTT	VTT	VTT
A21	VTT	VTT	VTT
A22	VTT	VTT	VTT
A23	HSWING	HSWING	HSWING
A24	HVREF	HVREF	HVREF
A25	HD48	HD48	HD48
A26	VSS	VSS	VSS
A27	HD61	HD61	HD61
A28	HD57	HD57	HD57
A29	HD55	HD55	HD55
A30	VSS	VSS	VSS
A31	HD53	HD53	HD53
A32	—	—	—
A33	VSS	VSS	VSS
A34	NC	NC	NC
A35	NC	NC	NC
B1	NC	NC	NC
B2	VSS	VSS	VSS
B3	EXP_RXP4	EXP_RXP4	RSV
B4	EXP_RXN4	EXP_RXN4	RSV
B5	VSS	VSS	VSS
B6	VSS	VSS	VSS
B7	VSS	VSS	VSS
B8	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
B9	VSS	VSS	VSS
B10	VSS	VSS	VSS
B11	GCLKN	GCLKN	GCLKN
B12	VSS	VSS	VSS
B13	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB
B14	VSS	VSS	VSS
B15	RSV	RSV	RSV
B16	VSS	VSS	VSS
B17	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL
B18	VSS	VSS	VSS
B19	VTT	VTT	VTT
B20	VTT	VTT	VTT
B21	VTT	VTT	VTT
B22	VTT	VTT	VTT
B23	HRCOMP	HRCOMP	HRCOMP
B24	VSS	VSS	VSS
B25	HD63	HD63	HD63
B26	HDINV3#	HDINV3#	HDINV3#
B27	HD54	HD54	HD54
B28	VSS	VSS	VSS
B29	HDSTBP3#	HDSTBP3#	HDSTBP3#
B30	HD51	HD51	HD51
B31	HD52	HD52	HD52
B32	HD15	HD15	HD15
B33	HD13	HD13	HD13
B34	HD11	HD11	HD11
B35	NC	NC	NC
C1	VSS	VSS	VSS
C2	EXP_TXP5	EXP_TXP5	SDVOC_GREEN+
C3	VSS	VSS	VSS
C4	VSS	VSS	VSS
C5	EXP_TXN4	EXP_TXN4	SDVOC_RED-/ SDVOB_ALPHA-
C6	EXP_TXP4	EXP_TXP4	SDVOC_RED+/ SDVOB_ALPHA+
C7	EXP_TXN2	EXP_TXN2	SDVOB_BLUE-
C8	EXP_TXP2	EXP_TXP2	SDVOB_BLUE+
C9	EXP_TXN0	EXP_TXN0	SDVOB_RED-
C10	EXP_TXP0	EXP_TXP0	SDVOB_RED+
C11	VSS	VSS	VSS
C12	—	—	—
C13	VSS	VSS	VSS
C14	RSV	RSV	RSV

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
C15	MTYPE	MTYPE	MTYPE
C16	NC	NC	NC
C17	VSS	VSS	VSS
C18	VSS	VSS	VSS
C19	VTT	VTT	VTT
C20	VTT	VTT	VTT
C21	VTT	VTT	VTT
C22	VTT	VTT	VTT
C23	VSS	VSS	VSS
C24	—	—	—
C25	HD58	HD58	HD58
C26	HD59	HD59	HD59
C27	HD49	HD49	HD49
C28	HD56	HD56	HD56
C29	HDSTBN3#	HDSTBN3#	HDSTBN3#
C30	HD17	HD17	HD17
C31	HD50	HD50	HD50
C32	HD14	HD14	HD14
C33	HD9	HD9	HD9
C34	HD12	HD12	HD12
C35	VSS	VSS	VSS
D1	—	—	—
D2	EXP_TXN5	EXP_TXN5	SDVOC_GREEN-
D3	VSS	VSS	VSS
D4	VSS	VSS	VSS
D5	EXP_RXP5	EXP_RXP5	SDVOC_INT+
D6	VSS	VSS	VSS
D7	VSS	VSS	VSS
D8	VSS	VSS	VSS
D9	VSS	VSS	VSS
D10	VSS	VSS	VSS
D11	VSS	VSS	VSS
D12	RSV	VSYNC	VSYNC
D13	RSV	VCCA_DAC	VCCA_DAC
D14	RSV	GREEN	GREEN
D15	VSS	VSS	VSS
D16	VSS	VSS	VSS
D17	BSEL2	BSEL2	BSEL2
D18	VSS	VSS	VSS
D19	VTT	VTT	VTT
D20	VTT	VTT	VTT
D21	VTT	VTT	VTT
D22	VTT	VTT	VTT

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
D23	VSS	VSS	VSS
D24	HSCOMP	HSCOMP	HSCOMP
D25	VSS	VSS	VSS
D26	VSS	VSS	VSS
D27	HD60	HD60	HD60
D28	VSS	VSS	VSS
D29	HD18	HD18	HD18
D30	VSS	VSS	VSS
D31	VSS	VSS	VSS
D32	VSS	VSS	VSS
D33	HD10	HD10	HD10
D34	HD8	HD8	HD8
D35	—	—	—
E1	VSS	VSS	VSS
E2	VSS	VSS	VSS
E3	EXP_TXP6	EXP_TXP6	SDVOC_BLUE+
E4	VSS	VSS	VSS
E5	EXP_RXN5	EXP_RXN5	SDVOC_INT-
E6	VSS	VSS	VSS
E7	EXP_RXN3	EXP_RXN3	RSV
E8	VSS	VSS	VSS
E9	EXP_RXN2	EXP_RXN2	SDVOC_STALL-
E10	VSS	VSS	VSS
E11	EXP_RXP0	EXP_RXP0	SDVOC_TVCLKIN+
E12	RSV	HSYNC	HSYNC
E13	RSV	VCCA_DAC	VCCA_DAC
E14	RSV	GREEN#	GREEN#
E15	BSEL1	BSEL1	BSEL1
E16	NC	NC	NC
E17	VSS	VSS	VSS
E18	VSS	VSS	VSS
E19	VTT	VTT	VTT
E20	VTT	VTT	VTT
E21	VTT	VTT	VTT
E22	VTT	VTT	VTT
E23	VSS	VSS	VSS
E24	HD62	HD62	HD62
E25	HD25	HD25	HD25
E26	VSS	VSS	VSS
E27	HD24	HD24	HD24
E28	HD16	HD16	HD16
E29	VSS	VSS	VSS
E30	HBPRI#	HBPRI#	HBPRI#

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
E31	HPCREQ#	HPCREQ#	HPCREQ#
E32	HREQ1#	HREQ1#	HREQ1#
E33	HDSTBP0#	HDSTBP0#	HDSTBP0#
E34	HDINV0#	HDINV0#	HDINV0#
E35	HDSTBN0#	HDSTBN0#	HDSTBN0#
F1	EXP_TXP7	EXP_TXP7	SDVOC_CLK+
F2	VSS	VSS	VSS
F3	EXP_TXN6	EXP_TXN6	SDVOC_BLUE-
F4	VSS	VSS	VSS
F5	VSS	VSS	VSS
F6	VSS	VSS	VSS
F7	EXP_RXP3	EXP_RXP3	RSV
F8	VSS	VSS	VSS
F9	EXP_RXP2	EXP_RXP2	SDVOC_STALL+
F10	VSS	VSS	VSS
F11	EXP_RXN0	EXP_RXN0	SDVOC_TVCLKIN-
F12	NC	NC	NC
F13	RSV	VSSA_DAC	VSSA_DAC
F14	RSV	RED	RED
F15	RSV	RSV	RSV
F16	VSS	VSS	VSS
F17	HD47	HD47	HD47
F18	VSS	VSS	VSS
F19	HDSTBN2#	HDSTBN2#	HDSTBN2#
F20	VTT	VTT	VTT
F21	VTT	VTT	VTT
F22	VTT	VTT	VTT
F23	VSS	VSS	VSS
F24	NC	NC	NC
F25	VSS	VSS	VSS
F26	HDSTBN1#	HDSTBN1#	HDSTBN1#
F27	HD23	HD23	HD23
F28	HD22	HD22	HD22
F29	VSS	VSS	VSS
F30	VSS	VSS	VSS
F31	HREQ4#	HREQ4#	HREQ4#
F32	VSS	VSS	VSS
F33	HREQ0#	HREQ0#	HREQ0#
F34	HD6	HD6	HD6
F35	VSS	VSS	VSS
G1	EXP_TXN7	EXP_TXN7	SDVOC_CLK-
G2	VSS	VSS	VSS
G3	EXP_TXP8	EXP_TXP8	RSV

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
G4	VSS	VSS	VSS
G5	EXP_RXN6	EXP_RXN6	RSV
G6	EXP_RXP6	EXP_RXP6	RSV
G7	VSS	VSS	VSS
G8	VSS	VSS	VSS
G9	VSS	VSS	VSS
G10	VSS	VSS	VSS
G11	VSS	VSS	VSS
G12	NC	NC	NC
G13	VSS	VSS	VSS
G14	RSV	RED#	RED#
G15	VSS	VSS	VSS
G16	RSV	RSV	RSV
G17	VSS	VSS	VSS
G18	HD45	HD45	HD45
G19	VSS	VSS	VSS
G20	VSS	VSS	VSS
G21	VTT	VTT	VTT
G22	VTT	VTT	VTT
G23	VSS	VSS	VSS
G24	HCPURST#	HCPURST#	HCPURST#
G25	HD26	HD26	HD26
G26	VSS	VSS	VSS
G27	VSS	VSS	VSS
G28	VSS	VSS	VSS
G29	HD20	HD20	HD20
G30	HA6#	HA6#	HA6#
G31	HREQ3#	HREQ3#	HREQ3#
G32	HA7#	HA7#	HA7#
G33	HD7	HD7	HD7
G34	HD5	HD5	HD5
G35	HD3	HD3	HD3
H1	EXP_TXP9	EXP_TXP9	RSV
H2	VSS	VSS	VSS
H3	EXP_TXN8	EXP_TXN8	RSV
H4	VSS	VSS	VSS
H5	VSS	VSS	VSS
H6	VSS	VSS	VSS
H7	EXP_RXN7	EXP_RXN7	RSV
H8	EXP_RXP7	EXP_RXP7	RSV
H9	VSS	VSS	VSS
H10	VSS	VSS	VSS
H11	EXP_RXN1	EXP_RXN1	SDVOB_INT-

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
H12	NC	NC	NC
H13	VSS	VSS	VSS
H14	RSV	BLUE	BLUE
H15	NC	NC	NC
H16	BSEL0	BSEL0	BSEL0
H17	NC	NC	NC
H18	HD46	HD46	HD46
H19	HD41	HD41	HD41
H20	HD40	HD40	HD40
H21	VSS	VSS	VSS
H22	VTT	VTT	VTT
H23	HD37	HD37	HD37
H24	VSS	VSS	VSS
H25	VSS	VSS	VSS
H26	HDSTBP1#	HDSTBP1#	HDSTBP1#
H27	VSS	VSS	VSS
H28	HD19	HD19	HD19
H29	HA3#	HA3#	HA3#
H30	VSS	VSS	VSS
H31	HREQ2#	HREQ2#	HREQ2#
H32	VSS	VSS	VSS
H33	HD1	HD1	HD1
H34	VSS	VSS	VSS
H35	HD4	HD4	HD4
J1	EXP_TXN9	EXP_TXN9	RSV
J2	VSS	VSS	VSS
J3	EXP_TXP10	EXP_TXP10	RSV
J4	VSS	VSS	VSS
J5	EXP_RXN8	EXP_RXN8	RSV
J6	EXP_RXP8	EXP_RXP8	RSV
J7	VSS	VSS	VSS
J8	VSS	VSS	VSS
J9	VSS	VSS	VSS
J10	VSS	VSS	VSS
J11	EXP_RXP1	EXP_RXP1	SDVOB_INT+
J12	NC	NC	NC
J13	RSV	SDVO_CTRLCLK	SDVO_CTRLCLK
J14	RSV	BLUE#	BLUE#
J15	VSS	VSS	VSS
J16	VSS	VSS	VSS
J17	VSS	VSS	VSS
J18	VSS	VSS	VSS
J19	HDSTBP2#	HDSTBP2#	HDSTBP2#

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
J20	VSS	VSS	VSS
J21	HD35	HD35	HD35
J22	HD32	HD32	HD32
J23	VSS	VSS	VSS
J24	HD33	HD33	HD33
J25	HD27	HD27	HD27
J26	HDINV1#	HDINV1#	HDINV1#
J27	HD21	HD21	HD21
J28	HA13#	HA13#	HA13#
J29	HA5#	HA5#	HA5#
J30	VSS	VSS	VSS
J31	HADSTB0#	HADSTB0#	HADSTB0#
J32	HRS2#	HRS2#	HRS2#
J33	HD0	HD0	HD0
J34	HD2	HD2	HD2
J35	HDEFER#	HDEFER#	HDEFER#
K1	EXP_TXP11	EXP_TXP11	RSV
K2	VSS	VSS	VSS
K3	EXP_TXN10	EXP_TXN10	RSV
K4	VSS	VSS	VSS
K5	VSS	VSS	VSS
K6	VSS	VSS	VSS
K7	EXP_RXN9	EXP_RXN9	RSV
K8	EXP_RXP9	EXP_RXP9	RSV
K9	VSS	VSS	VSS
K10	VSS	VSS	VSS
K11	VSS	VSS	VSS
K12	NC	NC	NC
K13	RSV	SDVO_CTRLDATA	SDVO_CTRLDATA
K14	VSS	VSS	VSS
K15	RSV	RSV	RSV
K16	EXTTS#	EXTTS#	EXTTS#
K17	HD44	HD44	HD44
K18	HD43	HD43	HD43
K19	HDINV2#	HDINV2#	HDINV2#
K20	VSS	VSS	VSS
K21	HD39	HD39	HD39
K22	HD34	HD34	HD34
K23	HD31	HD31	HD31
K24	VSS	VSS	VSS
K25	HD28	HD28	HD28
K26	VSS	VSS	VSS
K27	HA14#	HA14#	HA14#

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
K28	VSS	VSS	VSS
K29	HA4#	HA4#	HA4#
K30	HA8#	HA8#	HA8#
K31	VSS	VSS	VSS
K32	VSS	VSS	VSS
K33	HA15#	HA15#	HA15#
K34	HRS0#	HRS0#	HRS0#
K35	VSS	VSS	VSS
L1	EXP_TXN11	EXP_TXN11	RSV
L2	VSS	VSS	VSS
L3	EXP_TXP12	EXP_TXP12	RSV
L4	VSS	VSS	VSS
L5	EXP_RXN10	EXP_RXN10	RSV
L6	EXP_RXP10	EXP_RXP10	RSV
L7	VSS	VSS	VSS
L8	VSS	VSS	VSS
L9	VSS	VSS	VSS
L10	VCC	VCC	VCC
L11	VSS	VSS	VSS
L12	NC	NC	NC
L13	VSS	VSS	VSS
L14	RSV	DDC_DATA	DDC_DATA
L15	VSS	VSS	VSS
L16	VSS	VSS	VSS
L17	VSS	VSS	VSS
L18	VSS	VSS	VSS
L19	NC	NC	NC
L20	VSS	VSS	VSS
L21	VSS	VSS	VSS
L22	VSS	VSS	VSS
L23	HD30	HD30	HD30
L24	VSS	VSS	VSS
L25	HD29	HD29	HD29
L26	HA18#	HA18#	HA18#
L27	VSS	VSS	VSS
L28	HA12#	HA12#	HA12#
L29	HA9#	HA9#	HA9#
L30	VSS	VSS	VSS
L31	HA11#	HA11#	HA11#
L32	VSS	VSS	VSS
L33	HLOCK#	HLOCK#	HLOCK#
L34	HHIT#	HHIT#	HHIT#
L35	HDBSY#	HDBSY#	HDBSY#

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
M1	EXP_TXP13	EXP_TXP13	RSV
M2	VSS	VSS	VSS
M3	EXP_TXN12	EXP_TXN12	RSV
M4	VSS	VSS	VSS
M5	VSS	VSS	VSS
M6	VSS	VSS	VSS
M7	EXP_RXN12	EXP_RXN12	RSV
M8	EXP_RXP12	EXP_RXP12	RSV
M9	VSS	VSS	VSS
M10	VSS	VSS	VSS
M11	VSS	VSS	VSS
M12	DREFCLKN	DREFCLKN	DREFCLKN
M13	DREFCLKP	DREFCLKP	DREFCLKP
M14	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#
M15	RSV	DDC_CLK	DDC_CLK
M16	RSV	RSV	RSV
M17	VSS	VSS	VSS
M18	HD42	HD42	HD42
M19	HD38	HD38	HD38
M20	VSS	VSS	VSS
M21	HD36	HD36	HD36
M22	HCLKN	HCLKN	HCLKN
M23	HCLKP	HCLKP	HCLKP
M24	VSS	VSS	VSS
M25	VSS	VSS	VSS
M26	HA20#	HA20#	HA20#
M27	VSS	VSS	VSS
M28	HA16#	HA16#	HA16#
M29	VSS	VSS	VSS
M30	HA10#	HA10#	HA10#
M31	HADS#	HADS#	HADS#
M32	HDRDY#	HDRDY#	HDRDY#
M33	—	—	—
M34	VSS	VSS	VSS
M35	HBNR#	HBNR#	HBNR#
N1	EXP_TXN13	EXP_TXN13	RSV
N2	VSS	VSS	VSS
N3	EXP_TXP14	EXP_TXP14	RSV
N4	VSS	VSS	VSS
N5	EXP_RXN13	EXP_RXN13	RSV
N6	EXP_RXP13	EXP_RXP13	RSV
N7	VSS	VSS	VSS
N8	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
N9	VSS	VSS	VSS
N10	VSS	VSS	VSS
N11	VSS	VSS	VSS
N12	NC	NC	NC
N13	VCC	VCC	VCC
N14	VCC	VCC	VCC
N15	VCC	VCC	VCC
N16	VCC	VCC	VCC
N17	VSS	VSS	VSS
N18	VCC	VCC	VCC
N19	VSS	VSS	VSS
N20	VCC	VCC	VCC
N21	VCC	VCC	VCC
N22	NC	NC	NC
N23	NC	NC	NC
N24	NC	NC	NC
N25	VSS	VSS	VSS
N26	HA19#	HA19#	HA19#
N27	HADSTB1#	HADSTB1#	HADSTB1#
N28	VSS	VSS	VSS
N29	HA23#	HA23#	HA23#
N30	VSS	VSS	VSS
N31	HA21#	HA21#	HA21#
N32	VSS	VSS	VSS
N33	HA26#	HA26#	HA26#
N34	HTRDY#	HTRDY#	HTRDY#
N35	HHITM#	HHITM#	HHITM#
P1	EXP_TXP15	EXP_TXP15	RSV
P2	VSS	VSS	VSS
P3	EXP_TXN14	EXP_TXN14	RSV
P4	VSS	VSS	VSS
P5	VSS	VSS	VSS
P6	VSS	VSS	VSS
P7	EXP_RXP14	EXP_RXP14	RSV
P8	EXP_RXN14	EXP_RXN14	RSV
P9	VSS	VSS	VSS
P10	EXP_RXP11	EXP_RXP11	RSV
P11	VSS	VSS	VSS
P12	NC	NC	NC
P13	VCC	VCC	VCC
P14	VCC	VCC	VCC
P15	VCC	VCC	VCC
P16	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
P17	VCC	VCC	VCC
P18	VSS	VSS	VSS
P19	VCC	VCC	VCC
P20	VSS	VSS	VSS
P21	VCC	VCC	VCC
P22	VCC	VCC	VCC
P23	NC	NC	NC
P24	NC	NC	NC
P25	VSS	VSS	VSS
P26	HA22#	HA22#	HA22#
P27	VSS	VSS	VSS
P28	HA24#	HA24#	HA24#
P29	VSS	VSS	VSS
P30	NC	NC	NC
P31	VSS	VSS	VSS
P32	VSS	VSS	VSS
P33	HEDRDY#	HEDRDY#	HEDRDY#
P34	HRS1#	HRS1#	HRS1#
P35	VSS	VSS	VSS
R1	EXP_TXN15	EXP_TXN15	RSV
R2	VSS	VSS	VSS
R3	DMI_TXP0	DMI_TXP0	DMI_TXP0
R4	VSS	VSS	VSS
R5	EXP_RXN15	EXP_RXN15	RSV
R6	EXP_RXP15	EXP_RXP15	RSV
R7	VSS	VSS	VSS
R8	VSS	VSS	VSS
R9	VSS	VSS	VSS
R10	EXP_RXN11	EXP_RXN11	RSV
R11	VSS	VSS	VSS
R12	NC	NC	NC
R13	VCC	VCC	VCC
R14	VCC	VCC	VCC
R15	VCC	VCC	VCC
R16	VCC	VCC	VCC
R17	VSS	VSS	VSS
R18	VCC	VCC	VCC
R19	VSS	VSS	VSS
R20	VCC	VCC	VCC
R21	VSS	VSS	VSS
R22	VCC	VCC	VCC
R23	VCC	VCC	VCC
R24	NC	NC	NC

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
R25	VSS	VSS	VSS
R26	VSS	VSS	VSS
R27	VSS	VSS	VSS
R28	HA25#	HA25#	HA25#
R29	HA17#	HA17#	HA17#
R30	RSV	RSV	RSV
R31	RSV	RSV	RSV
R32	SDQ_A58	SDQ_A58	SDQ_A58
R33	HBREQ0#	HBREQ0#	HBREQ0#
R34	SDQ_A59	SDQ_A59	SDQ_A59
R35	RSV	RSV	RSV
T1	DMI_TXP1	DMI_TXP1	DMI_TXP1
T2	VSS	VSS	VSS
T3	DMI_TXN0	DMI_TXN0	DMI_TXN0
T4	VSS	VSS	VSS
T5	VSS	VSS	VSS
T6	VSS	VSS	VSS
T7	VSS	VSS	VSS
T8	DMI_RXN1	DMI_RXN1	DMI_RXN1
T9	DMI_RXP1	DMI_RXP1	DMI_RXP1
T10	VSS	VSS	VSS
T11	VSS	VSS	VSS
T12	NC	NC	NC
T13	VCC	VCC	VCC
T14	VCC	VCC	VCC
T15	VCC	VCC	VCC
T16	VCC	VCC	VCC
T17	VCC	VCC	VCC
T18	VSS	VSS	VSS
T19	VCC	VCC	VCC
T20	VCC	VCC	VCC
T21	VCC	VCC	VCC
T22	VSS	VSS	VSS
T23	VCC	VCC	VCC
T24	VCC	VCC	VCC
T25	VSS	VSS	VSS
T26	HA30#	HA30#	HA30#
T27	HA27#	HA27#	HA27#
T28	VSS	VSS	VSS
T29	HA31#	HA31#	HA31#
T30	VSS	VSS	VSS
T31	HA28#	HA28#	HA28#
T32	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
T33	SDQ_A62	SDQ_A62	SDQ_A62
T34	VSS	VSS	VSS
T35	SDQ_A63	SDQ_A63	SDQ_A63
U1	DMI_TXN1	DMI_TXN1	DMI_TXN1
U2	VSS	VSS	VSS
U3	DMI_TXP2	DMI_TXP2	DMI_TXP2
U4	VSS	VSS	VSS
U5	DMI_RXP0	DMI_RXP0	DMI_RXP0
U6	DMI_RXN0	DMI_RXN0	DMI_RXN0
U7	VSS	VSS	VSS
U8	VSS	VSS	VSS
U9	VSS	VSS	VSS
U10	DMI_RXN3	DMI_RXN3	DMI_RXN3
U11	VSS	VSS	VSS
U12	NC	NC	NC
U13	VCC	VCC	VCC
U14	VCC	VCC	VCC
U15	VSS	VSS	VSS
U16	VCC	VCC	VCC
U17	VSS	VSS	VSS
U18	VCC	VCC	VCC
U19	VSS	VSS	VSS
U20	VCC	VCC	VCC
U21	VSS	VSS	VSS
U22	VCC	VCC	VCC
U23	VSS	VSS	VSS
U24	VCC	VCC	VCC
U25	VSS	VSS	VSS
U26	SDQ_B63	SDQ_B63	SDQ_B63
U27	VSS	VSS	VSS
U28	HA29#	HA29#	HA29#
U29	VSS	VSS	VSS
U30	RSV	RSV	RSV
U31	VSS	VSS	VSS
U32	VSS	VSS	VSS
U33	SDM_A7	SDM_A7	SDM_A7
U34	SDQS_A7	SDQS_A7	SDQS_A7
U35	SDQS_A7#	SDQS_A7#	SDQS_A7#
V1	VSS	VSS	VSS
V2	VSS	VSS	VSS
V3	DMI_TXN2	DMI_TXN2	DMI_TXN2
V4	VSS	VSS	VSS
V5	DMI_TXP3	DMI_TXP3	DMI_TXP3

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
V6	VSS	VSS	VSS
V7	DMI_RXP2	DMI_RXP2	DMI_RXP2
V8	DMI_RXN2	DMI_RXN2	DMI_RXN2
V9	VSS	VSS	VSS
V10	DMI_RXP3	DMI_RXP3	DMI_RXP3
V11	VSS	VSS	VSS
V12	NC	NC	NC
V13	VCC	VCC	VCC
V14	VCC	VCC	VCC
V15	VCC	VCC	VCC
V16	VSS	VSS	VSS
V17	VCC	VCC	VCC
V18	VSS	VSS	VSS
V19	VCC	VCC	VCC
V20	VSS	VSS	VSS
V21	VCC	VCC	VCC
V22	VSS	VSS	VSS
V23	VCC	VCC	VCC
V24	VCC	VCC	VCC
V25	VSS	VSS	VSS
V26	VSS	VSS	VSS
V27	VSS	VSS	VSS
V28	SDQ_B58	SDQ_B58	SDQ_B58
V29	SDQ_B59	SDQ_B59	SDQ_B59
V30	RSV	RSV	RSV
V31	RSV	RSV	RSV
V32	RSV	RSV	RSV
V33	SDQ_A57	SDQ_A57	SDQ_A57
V34	SDQ_A56	SDQ_A56	SDQ_A56
V35	VSS	VSS	VSS
W1	VCC_EXP	VCC_EXP	VCC_EXP
W2	VCC_EXP	VCC_EXP	VCC_EXP
W3	VCC_EXP	VCC_EXP	VCC_EXP
W4	VCC_EXP	VCC_EXP	VCC_EXP
W5	DMI_TXN3	DMI_TXN3	DMI_TXN3
W6	VCC_EXP	VCC_EXP	VCC_EXP
W7	VCC_EXP	VCC_EXP	VCC_EXP
W8	VCC_EXP	VCC_EXP	VCC_EXP
W9	VCC_EXP	VCC_EXP	VCC_EXP
W10	EXP_COMPI	EXP_COMPI	RSV
W11	VSS	VSS	VSS
W12	NC	NC	NC
W13	VCC	VCC	VCC

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
W14	VCC	VCC	VCC
W15	VSS	VSS	VSS
W16	VCC	VCC	VCC
W17	VSS	VSS	VSS
W18	VCC	VCC	VCC
W19	VSS	VSS	VSS
W20	VCC	VCC	VCC
W21	VSS	VSS	VSS
W22	VCC	VCC	VCC
W23	VSS	VSS	VSS
W24	VCC	VCC	VCC
W25	VSS	VSS	VSS
W26	SDQ_B62	SDQ_B62	SDQ_B62
W27	SDQS_B7	SDQS_B7	SDQS_B7
W28	VSS	VSS	VSS
W29	SDQ_B57	SDQ_B57	SDQ_B57
W30	VSS	VSS	VSS
W31	SDM_B7	SDM_B7	SDM_B7
W32	VSS	VSS	VSS
W33	SDQ_A61	SDQ_A61	SDQ_A61
W34	SDQ_A51	SDQ_A51	SDQ_A51
W35	SDQ_A60	SDQ_A60	SDQ_A60
Y1	VCC_EXP	VCC_EXP	VCC_EXP
Y2	VCC_EXP	VCC_EXP	VCC_EXP
Y3	VCC_EXP	VCC_EXP	VCC_EXP
Y4	VCC_EXP	VCC_EXP	VCC_EXP
Y5	VCC_EXP	VCC_EXP	VCC_EXP
Y6	VCC_EXP	VCC_EXP	VCC_EXP
Y7	VCC_EXP	VCC_EXP	VCC_EXP
Y8	VCC_EXP	VCC_EXP	VCC_EXP
Y9	VCC_EXP	VCC_EXP	VCC_EXP
Y10	EXP_COMPO	EXP_COMPO	RSV
Y11	VSS	VSS	VSS
Y12	NC	NC	NC
Y13	VCC	VCC	VCC
Y14	VCC	VCC	VCC
Y15	VCC	VCC	VCC
Y16	VCC	VCC	VCC
Y17	VCC	VCC	VCC
Y18	VSS	VSS	VSS
Y19	VCC	VCC	VCC
Y20	VCC	VCC	VCC
Y21	VCC	VCC	VCC

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
Y22	VSS	VSS	VSS
Y23	VCC	VCC	VCC
Y24	VCC	VCC	VCC
Y25	VSS	VSS	VSS
Y26	SDQ_B60	SDQ_B60	SDQ_B60
Y27	VSS	VSS	VSS
Y28	SDQS_B7#	SDQS_B7#	SDQS_B7#
Y29	VSS	VSS	VSS
Y30	RSV	RSV	RSV
Y31	VSS	VSS	VSS
Y32	VSS	VSS	VSS
Y33	SDQ_A50	SDQ_A50	SDQ_A50
Y34	VSS	VSS	VSS
Y35	SDQ_A55	SDQ_A55	SDQ_A55
AA1	VSS	VSS	VSS
AA2	VSS	VSS	VSS
AA3	VSS	VSS	VSS
AA4	VSS	VSS	VSS
AA5	VSS	VSS	VSS
AA6	VSS	VSS	VSS
AA7	VSS	VSS	VSS
AA8	VSS	VSS	VSS
AA9	VSS	VSS	VSS
AA10	VSS	VSS	VSS
AA11	VSS	VSS	VSS
AA12	NC	NC	NC
AA13	VCC	VCC	VCC
AA14	VCC	VCC	VCC
AA15	VSS	VSS	VSS
AA16	VCC	VCC	VCC
AA17	VSS	VSS	VSS
AA18	VCC	VCC	VCC
AA19	VSS	VSS	VSS
AA20	VCC	VCC	VCC
AA21	VCC	VCC	VCC
AA22	VCC	VCC	VCC
AA23	VCC	VCC	VCC
AA24	VCC	VCC	VCC
AA25	VSS	VSS	VSS
AA26	VSS	VSS	VSS
AA27	VSS	VSS	VSS
AA28	SDQ_B56	SDQ_B56	SDQ_B56
AA29	SDQ_B61	SDQ_B61	SDQ_B61

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AA30	RSV	RSV	RSV
AA31	RSV	RSV	RSV
AA32	SDQ_A54	SDQ_A54	SDQ_A54
AA33	SDM_A6	SDM_A6	SDM_A6
AA34	SDQS_A6	SDQS_A6	SDQS_A6
AA35	SDQS_A6#	SDQS_A6#	SDQS_A6#
AB1	VCC	VCC	VCC
AB2	VCC	VCC	VCC
AB3	VCC	VCC	VCC
AB4	VCC	VCC	VCC
AB5	VCC	VCC	VCC
AB6	VCC	VCC	VCC
AB7	VCC	VCC	VCC
AB8	VCC	VCC	VCC
AB9	VCC	VCC	VCC
AB10	VCC	VCC	VCC
AB11	VCC	VCC	VCC
AB12	NC	NC	NC
AB13	VCC	VCC	VCC
AB14	VCC	VCC	VCC
AB15	VCC	VCC	VCC
AB16	VCC	VCC	VCC
AB17	VCC	VCC	VCC
AB18	VCC	VCC	VCC
AB19	VCC	VCC	VCC
AB20	VCC	VCC	VCC
AB21	VCC	VCC	VCC
AB22	VCC	VCC	VCC
AB23	VCC	VCC	VCC
AB24	VCC	VCC	VCC
AB25	VSS	VSS	VSS
AB26	SDQ_B51	SDQ_B51	SDQ_B51
AB27	SDQ_B55	SDQ_B55	SDQ_B55
AB28	VSS	VSS	VSS
AB29	RSV	RSV	RSV
AB30	VSS	VSS	VSS
AB31	SDQS_B6	SDQS_B6	SDQS_B6
AB32	VSS	VSS	VSS
AB33	RSV	RSV	RSV
AB34	SCLK_A5#	SCLK_A5#	SCLK_A5#
AB35	VSS	VSS	VSS
AC1	VCC	VCC	VCC
AC2	VCC	VCC	VCC

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AC3	VCC	VCC	VCC
AC4	VCC	VCC	VCC
AC5	VCC	VCC	VCC
AC6	VCC	VCC	VCC
AC7	VCC	VCC	VCC
AC8	VCC	VCC	VCC
AC9	VCC	VCC	VCC
AC10	VCC	VCC	VCC
AC11	VCC	VCC	VCC
AC12	RSV	RSV	RSV
AC13	RSV	RSV	RSV
AC14	RSV	RSV	RSV
AC15	RSV	RSV	RSV
AC16	RSV	RSV	RSV
AC17	RSV	RSV	RSV
AC18	RSV	RSV	RSV
AC19	RSV	RSV	RSV
AC20	RSV	RSV	RSV
AC21	RSV	RSV	RSV
AC22	RSV	RSV	RSV
AC23	NC	NC	NC
AC24	NC	NC	NC
AC25	VSS	VSS	VSS
AC26	SDQ_B50	SDQ_B50	SDQ_B50
AC27	VSS	VSS	VSS
AC28	SDQ_B54	SDQ_B54	SDQ_B54
AC29	VSS	VSS	VSS
AC30	SDQS_B6#	SDQS_B6#	SDQS_B6#
AC31	VSS	VSS	VSS
AC32	VSS	VSS	VSS
AC33	SCLK_A5	SCLK_A5	SCLK_A5
AC34	SCLK_A2	SCLK_A2	SCLK_A2
AC35	SCLK_A2#	SCLK_A2#	SCLK_A2#
AD1	VCC	VCC	VCC
AD2	VCC	VCC	VCC
AD3	VCC	VCC	VCC
AD4	VCC	VCC	VCC
AD5	VCC	VCC	VCC
AD6	VCC	VCC	VCC
AD7	VCC	VCC	VCC
AD8	VCC	VCC	VCC
AD9	VCC	VCC	VCC
AD10	VCC	VCC	VCC

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AD11	VSS	VSS	VSS
AD12	SDQ_B20	SDQ_B20	SDQ_B20
AD13	VSS	VSS	VSS
AD14	SDQ_B18	SDQ_B18	SDQ_B18
AD15	SDQ_B19	SDQ_B19	SDQ_B19
AD16	VSS	VSS	VSS
AD17	SDQ_A30	SDQ_A30	SDQ_A30
AD18	SDQ_B28	SDQ_B28	SDQ_B28
AD19	VSS	VSS	VSS
AD20	SDQS_B3	SDQS_B3	SDQS_B3
AD21	SDQ_B27	SDQ_B27	SDQ_B27
AD22	VSS	VSS	VSS
AD23	SDQ_B37	SDQ_B37	SDQ_B37
AD24	SDM_B6	SDM_B6	SDM_B6
AD25	VSS	VSS	VSS
AD26	VSS	VSS	VSS
AD27	VSS	VSS	VSS
AD28	SCLK_B5	SCLK_B5	SCLK_B5
AD29	SCLK_B5#	SCLK_B5#	SCLK_B5#
AD30	NC	NC	NC
AD31	SDQ_A48	SDQ_A48	SDQ_A48
AD32	RSV	RSV	RSV
AD33	—	—	—
AD34	VSS	VSS	VSS
AD35	SDQ_A49	SDQ_A49	SDQ_A49
AE1	SDQ_A5	SDQ_A5	SDQ_A5
AE2	SDQ_A4	SDQ_A4	SDQ_A4
AE3	SDQ_A0	SDQ_A0	SDQ_A0
AE4	VSS	VSS	VSS
AE5	SOCOMP1	SOCOMP1	SOCOMP1
AE6	VSS	VSS	VSS
AE7	SVREF0	SVREF0	SVREF0
AE8	SVREF1	SVREF1	SVREF1
AE9	VSS	VSS	VSS
AE10	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1
AE11	SDQ_B11	SDQ_B11	SDQ_B11
AE12	VSS	VSS	VSS
AE13	SDQ_B21	SDQ_B21	SDQ_B21
AE14	VSS	VSS	VSS
AE15	VSS	VSS	VSS
AE16	RSV_TP0	RSV_TP0	RSV_TP0
AE17	VSS	VSS	VSS
AE18	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AE19	SDQ_A31	SDQ_A31	SDQ_A31
AE20	VSS	VSS	VSS
AE21	VSS	VSS	VSS
AE22	SDQ_B30	SDQ_B30	SDQ_B30
AE23	VSS	VSS	VSS
AE24	VSS	VSS	VSS
AE25	SCLK_B2#	SCLK_B2#	SCLK_B2#
AE26	SCLK_B2	SCLK_B2	SCLK_B2
AE27	SDQ_B49	SDQ_B49	SDQ_B49
AE28	VSS	VSS	VSS
AE29	SDQ_B53	SDQ_B53	SDQ_B53
AE30	VSS	VSS	VSS
AE31	SDQ_B52	SDQ_B52	SDQ_B52
AE32	VSS	VSS	VSS
AE33	SDQ_A43	SDQ_A43	SDQ_A43
AE34	SDQ_A53	SDQ_A53	SDQ_A53
AE35	SDQ_A52	SDQ_A52	SDQ_A52
AF1	VSS	VSS	VSS
AF2	SDM_A0	SDM_A0	SDM_A0
AF3	SDQ_A1	SDQ_A1	SDQ_A1
AF4	VSS	VSS	VSS
AF5	SOCOMP0	SOCOMP0	SOCOMP0
AF6	VSS	VSS	VSS
AF7	RSTIN#	RSTIN#	RSTIN#
AF8	VSS	VSS	VSS
AF9	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1
AF10	VSS	VSS	VSS
AF11	SDQ_B10	SDQ_B10	SDQ_B10
AF12	VSS	VSS	VSS
AF13	SDQ_B16	SDQ_B16	SDQ_B16
AF14	SDQ_B23	SDQ_B23	SDQ_B23
AF15	VSS	VSS	VSS
AF16	SDQ_A29	SDQ_A29	SDQ_A29
AF17	SDQS_A3	SDQS_A3	SDQS_A3
AF18	VSS	VSS	VSS
AF19	SDQ_A26	SDQ_A26	SDQ_A26
AF20	SDQS_B3#	SDQS_B3#	SDQS_B3#
AF21	VSS	VSS	VSS
AF22	SDQ_B31	SDQ_B31	SDQ_B31
AF23	SDQ_B36	SDQ_B36	SDQ_B36
AF24	SDQ_B32	SDQ_B32	SDQ_B32
AF25	SDQ_B33	SDQ_B33	SDQ_B33
AF26	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AF27	SDQ_B48	SDQ_B48	SDQ_B48
AF28	SDQ_B43	SDQ_B43	SDQ_B43
AF29	VSS	VSS	VSS
AF30	VSS	VSS	VSS
AF31	VSS	VSS	VSS
AF32	VSS	VSS	VSS
AF33	SDQ_A42	SDQ_A42	SDQ_A42
AF34	SDQ_A47	SDQ_A47	SDQ_A47
AF35	VSS	VSS	VSS
AG1	SDQS_A0	SDQS_A0	SDQS_A0
AG2	SDQS_A0#	SDQS_A0#	SDQS_A0#
AG3	SDQ_A6	SDQ_A6	SDQ_A6
AG4	SRCOMP0	SRCOMP0	SRCOMP0
AG5	VSS	VSS	VSS
AG6	NC	NC	NC
AG7	PWROK	PWROK	PWROK
AG8	SRCOMP1	SRCOMP1	SRCOMP1
AG9	SDQ_B4	SDQ_B4	SDQ_B4
AG10	SDQ_B14	SDQ_B14	SDQ_B14
AG11	SDQ_B15	SDQ_B15	SDQ_B15
AG12	VSS	VSS	VSS
AG13	VSS	VSS	VSS
AG14	SDQ_B22	SDQ_B22	SDQ_B22
AG15	VSS	VSS	VSS
AG16	VSS	VSS	VSS
AG17	SDQS_A3#	SDQS_A3#	SDQS_A3#
AG18	VSS	VSS	VSS
AG19	VSS	VSS	VSS
AG20	SDM_B3	SDM_B3	SDM_B3
AG21	VSS	VSS	VSS
AG22	VSS	VSS	VSS
AG23	SCLK_B0#	SCLK_B0#	SCLK_B0#
AG24	SDM_B4	SDM_B4	SDM_B4
AG25	VSS	VSS	VSS
AG26	SDQS_B4#	SDQS_B4#	SDQS_B4#
AG27	SDQ_B47	SDQ_B47	SDQ_B47
AG28	VSS	VSS	VSS
AG29	VSS	VSS	VSS
AG30	SDQ_B46	SDQ_B46	SDQ_B46
AG31	SDQ_B42	SDQ_B42	SDQ_B42
AG32	SDQ_A46	SDQ_A46	SDQ_A46
AG33	SDQS_A5#	SDQS_A5#	SDQS_A5#
AG34	SDM_A5	SDM_A5	SDM_A5

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AG35	SDQS_A5	SDQS_A5	SDQS_A5
AH1	VSS	VSS	VSS
AH2	SDQ_A7	SDQ_A7	SDQ_A7
AH3	SDQ_A2	SDQ_A2	SDQ_A2
AH4	SDQ_B0	SDQ_B0	SDQ_B0
AH5	VSS	VSS	VSS
AH6	VSS	VSS	VSS
AH7	SDQ_B5	SDQ_B5	SDQ_B5
AH8	VSS	VSS	VSS
AH9	SDM_B1	SDM_B1	SDM_B1
AH10	SDQS_B1#	SDQS_B1#	SDQS_B1#
AH11	VSS	VSS	VSS
AH12	SDQ_B17	SDQ_B17	SDQ_B17
AH13	SDM_B2	SDM_B2	SDM_B2
AH14	VSS	VSS	VSS
AH15	RSV_TP1	RSV_TP1	RSV_TP1
AH16	SDM_A3	SDM_A3	SDM_A3
AH17	VSS	VSS	VSS
AH18	SDQ_A27	SDQ_A27	SDQ_A27
AH19	SDQ_B25	SDQ_B25	SDQ_B25
AH20	VSS	VSS	VSS
AH21	SDQ_B26	SDQ_B26	SDQ_B26
AH22	SCLK_B0	SCLK_B0	SCLK_B0
AH23	VSS	VSS	VSS
AH24	NC	NC	NC
AH25	SDQS_B4	SDQS_B4	SDQS_B4
AH26	VSS	VSS	VSS
AH27	SDQ_A36	SDQ_A36	SDQ_A36
AH28	SDQS_B5	SDQS_B5	SDQS_B5
AH29	VSS	VSS	VSS
AH30	SDQS_B5#	SDQS_B5#	SDQS_B5#
AH31	SDM_B5	SDM_B5	SDM_B5
AH32	VSS	VSS	VSS
AH33	SDQ_A40	SDQ_A40	SDQ_A40
AH34	VSS	VSS	VSS
AH35	SDQ_A41	SDQ_A41	SDQ_A41
AJ1	SDQ_A12	SDQ_A12	SDQ_A12
AJ2	SDQ_A3	SDQ_A3	SDQ_A3
AJ3	SDQ_A13	SDQ_A13	SDQ_A13
AJ4	VSS	VSS	VSS
AJ5	SDM_B0	SDM_B0	SDM_B0
AJ6	SDQ_B1	SDQ_B1	SDQ_B1
AJ7	SDQ_B12	SDQ_B12	SDQ_B12

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AJ8	SDQ_B8	SDQ_B8	SDQ_B8
AJ9	VSS	VSS	VSS
AJ10	VSS	VSS	VSS
AJ11	SCLK_B4	SCLK_B4	SCLK_B4
AJ12	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0
AJ13	VSS	VSS	VSS
AJ14	NC	NC	NC
AJ15	VSS	VSS	VSS
AJ16	VSS	VSS	VSS
AJ17	SDQ_A25	SDQ_A25	SDQ_A25
AJ18	RSV	RSV	RSV
AJ19	VSS	VSS	VSS
AJ20	RSV	RSV	RSV
AJ21	RSV	RSV	RSV
AJ22	VSS	VSS	VSS
AJ23	RSV	RSV	RSV
AJ24	RSV	RSV	RSV
AJ25	SDQ_B39	SDQ_B39	SDQ_B39
AJ26	SDQ_B35	SDQ_B35	SDQ_B35
AJ27	VSS	VSS	VSS
AJ28	SDQ_A33	SDQ_A33	SDQ_A33
AJ29	SDQ_B44	SDQ_B44	SDQ_B44
AJ30	VSS	VSS	VSS
AJ31	SDQ_B41	SDQ_B41	SDQ_B41
AJ32	VSS	VSS	VSS
AJ33	SDQ_A44	SDQ_A44	SDQ_A44
AJ34	SDQ_A45	SDQ_A45	SDQ_A45
AJ35	VSS	VSS	VSS
AK1	VSS	VSS	VSS
AK2	SDQ_A8	SDQ_A8	SDQ_A8
AK3	SDQ_A9	SDQ_A9	SDQ_A9
AK4	VSS	VSS	VSS
AK5	SDQS_B0	SDQS_B0	SDQS_B0
AK6	VSS	VSS	VSS
AK7	VSS	VSS	VSS
AK8	VSS	VSS	VSS
AK9	SCLK_B1	SCLK_B1	SCLK_B1
AK10	SDQS_B1	SDQS_B1	SDQS_B1
AK11	VSS	VSS	VSS
AK12	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0
AK13	SDQS_B2	SDQS_B2	SDQS_B2
AK14	VSS	VSS	VSS
AK15	RSV_TP3	RSV_TP3	RSV_TP3

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AK16	SDQ_A28	SDQ_A28	SDQ_A28
AK17	VSS	VSS	VSS
AK18	RSV	RSV	RSV
AK19	SDQ_B24	SDQ_B24	SDQ_B24
AK20	VSS	VSS	VSS
AK21	RSV	RSV	RSV
AK22	SCLK_B3#	SCLK_B3#	SCLK_B3#
AK23	VSS	VSS	VSS
AK24	RSV	RSV	RSV
AK25	VSS	VSS	VSS
AK26	VSS	VSS	VSS
AK27	SDQ_A32	SDQ_A32	SDQ_A32
AK28	VSS	VSS	VSS
AK29	SDM_A4	SDM_A4	SDM_A4
AK30	VSS	VSS	VSS
AK31	SDQ_A35	SDQ_A35	SDQ_A35
AK32	SDQ_B40	SDQ_B40	SDQ_B40
AK33	SDQ_B45	SDQ_B45	SDQ_B45
AK34	SODT_B3	SODT_B3	SODT_B3
AK35	VCCSM	VCCSM	VCCSM
AL1	SDM_A1	SDM_A1	SDM_A1
AL2	SDQS_A1#	SDQS_A1#	SDQS_A1#
AL3	SDQS_A1	SDQS_A1	SDQS_A1
AL4	SDQS_B0#	SDQS_B0#	SDQS_B0#
AL5	SDQ_B6	SDQ_B6	SDQ_B6
AL6	SDQ_B2	SDQ_B2	SDQ_B2
AL7	SDQ_B13	SDQ_B13	SDQ_B13
AL8	SDQ_B9	SDQ_B9	SDQ_B9
AL9	SCLK_B1#	SCLK_B1#	SCLK_B1#
AL10	VSS	VSS	VSS
AL11	SCLK_B4#	SCLK_B4#	SCLK_B4#
AL12	SMA_B7	SMA_B7	SMA_B7
AL13	VSS	VSS	VSS
AL14	SDQS_B2#	SDQS_B2#	SDQS_B2#
AL15	SMA_B3	SMA_B3	SMA_B3
AL16	VSS	VSS	VSS
AL17	SDQ_A24	SDQ_A24	SDQ_A24
AL18	SDQ_B29	SDQ_B29	SDQ_B29
AL19	VSS	VSS	VSS
AL20	RSV	RSV	RSV
AL21	RSV	RSV	RSV
AL22	VSS	VSS	VSS
AL23	SCLK_B3	SCLK_B3	SCLK_B3

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AL24	SMA_A2	SMA_A2	SMA_A2
AL25	SDQ_B38	SDQ_B38	SDQ_B38
AL26	SDQ_B34	SDQ_B34	SDQ_B34
AL27	SDQ_A37	SDQ_A37	SDQ_A37
AL28	NC	NC	NC
AL29	SDQS_A4#	SDQS_A4#	SDQS_A4#
AL30	SDQ_A39	SDQ_A39	SDQ_A39
AL31	SDQ_A34	SDQ_A34	SDQ_A34
AL32	VSS	VSS	VSS
AL33	SMA_B13	SMA_B13	SMA_B13
AL34	SODT_B1	SODT_B1	SODT_B1
AL35	SODT_B2	SODT_B2	SODT_B2
AM1			
AM2	SCLK_A1	SCLK_A1	SCLK_A1
AM3	SCLK_A1#	SCLK_A1#	SCLK_A1#
AM4	VSS	VSS	VSS
AM5	SDQ_B7	SDQ_B7	SDQ_B7
AM6	VSS	VSS	VSS
AM7	VSS	VSS	VSS
AM8	VSS	VSS	VSS
AM9	SCKE_B3	SCKE_B3	SCKE_B3
AM10	VCCSM	VCCSM	VCCSM
AM11	VCCSM	VCCSM	VCCSM
AM12	SMA_B5	SMA_B5	SMA_B5
AM13	VCCSM	VCCSM	VCCSM
AM14	VCCSM	VCCSM	VCCSM
AM15	SMA_B0	SMA_B0	SMA_B0
AM16	VCCSM	VCCSM	VCCSM
AM17	VCCSM	VCCSM	VCCSM
AM18	SCKE_A1	SCKE_A1	SCKE_A1
AM19	VCCSM	VCCSM	VCCSM
AM20	VCCSM	VCCSM	VCCSM
AM21	SMA_A11	SMA_A11	SMA_A11
AM22	VCCSM	VCCSM	VCCSM
AM23	VCCSM	VCCSM	VCCSM
AM24	SCLK_A3#	SCLK_A3#	SCLK_A3#
AM25	VCCSM	VCCSM	VCCSM
AM26	VCCSM	VCCSM	VCCSM
AM27	SMA_A10	SMA_A10	SMA_A10
AM28	VCCSM	VCCSM	VCCSM
AM29	VSS	VSS	VSS
AM30	SDQS_A4	SDQS_A4	SDQS_A4
AM31	VSS	VSS	VSS

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AM32	VCCSM	VCCSM	VCCSM
AM33	SODT_B0	SODT_B0	SODT_B0
AM34	SCS_B1#	SCS_B1#	SCS_B1#
AM35	—	—	—
AN1	VSS	VSS	VSS
AN2	SCLK_A4#	SCLK_A4#	SCLK_A4#
AN3	SCLK_A4	SCLK_A4	SCLK_A4
AN4	SDQ_A10	SDQ_A10	SDQ_A10
AN5	SDQ_A20	SDQ_A20	SDQ_A20
AN6	SDQ_B3	SDQ_B3	SDQ_B3
AN7	SDM_A2	SDM_A2	SDM_A2
AN8	SDQ_A22	SDQ_A22	SDQ_A22
AN9	SDQ_A19	SDQ_A19	SDQ_A19
AN10	SCKE_B1	SCKE_B1	SCKE_B1
AN11	SBS_B2	SBS_B2	SBS_B2
AN12			
AN13	SMA_B8	SMA_B8	SMA_B8
AN14	RSV_TP2	RSV_TP2	RSV_TP2
AN15	SMA_B2	SMA_B2	SMA_B2
AN16	SBS_B1	SBS_B1	SBS_B1
AN17	SRAS_B#	SRAS_B#	SRAS_B#
AN18	SCKE_A2	SCKE_A2	SCKE_A2
AN19	NC	NC	NC
AN20	SBS_A2	SBS_A2	SBS_A2
AN21	SMA_A9	SMA_A9	SMA_A9
AN22	SMA_A8	SMA_A8	SMA_A8
AN23	SMA_A6	SMA_A6	SMA_A6
AN24	—	—	—
AN25	SCLK_A3	SCLK_A3	SCLK_A3
AN26	SCLK_A0	SCLK_A0	SCLK_A0
AN27	SBS_A1	SBS_A1	SBS_A1
AN28	SWE_A#	SWE_A#	SWE_A#
AN29	SCAS_A#	SCAS_A#	SCAS_A#
AN30	SDQ_A38	SDQ_A38	SDQ_A38
AN31	SCS_A3#	SCS_A3#	SCS_A3#
AN32	SODT_A1	SODT_A1	SODT_A1
AN33	SCS_B0#	SCS_B0#	SCS_B0#
AN34	SCS_B3#	SCS_B3#	SCS_B3#
AN35	VCCSM	VCCSM	VCCSM
AP1	NC	NC	NC
AP2	SDQ_A14	SDQ_A14	SDQ_A14
AP3	SDQ_A15	SDQ_A15	SDQ_A15
AP4	SDQ_A11	SDQ_A11	SDQ_A11

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AP5	SDQ_A21	SDQ_A21	SDQ_A21
AP6	SDQ_A17	SDQ_A17	SDQ_A17
AP7	SDQS_A2	SDQS_A2	SDQS_A2
AP8	VSS	VSS	VSS
AP9	SDQ_A18	SDQ_A18	SDQ_A18
AP10	SCKE_B0	SCKE_B0	SCKE_B0
AP11	SMA_B11	SMA_B11	SMA_B11
AP12	VCCSM	VCCSM	VCCSM
AP13	SMA_B6	SMA_B6	SMA_B6
AP14	SMA_B4	SMA_B4	SMA_B4
AP15	SMA_B10	SMA_B10	SMA_B10
AP16	VCCSM	VCCSM	VCCSM
AP17	SWE_B#	SWE_B#	SWE_B#
AP18	SCAS_B#	SCAS_B#	SCAS_B#
AP19	SCKE_A0	SCKE_A0	SCKE_A0
AP20	VCCSM	VCCSM	VCCSM
AP21	SMA_A7	SMA_A7	SMA_A7
AP22	SMA_A5	SMA_A5	SMA_A5
AP23	SMA_A3	SMA_A3	SMA_A3
AP24	VCCSM	VCCSM	VCCSM
AP25	SCLK_A0#	SCLK_A0#	SCLK_A0#
AP26	SMA_A0	SMA_A0	SMA_A0
AP27	SRAS_A#	SRAS_A#	SRAS_A#
AP28	VCCSM	VCCSM	VCCSM
AP29	SODT_A2	SODT_A2	SODT_A2
AP30	SODT_A0	SODT_A0	SODT_A0
AP31	SMA_A13	SMA_A13	SMA_A13
AP32	SCS_A1#	SCS_A1#	SCS_A1#
AP33	SODT_A3	SODT_A3	SODT_A3
AP34	SCS_B2#	SCS_B2#	SCS_B2#
AP35	NC	NC	NC
AR1	NC	NC	NC
AR2	NC	NC	NC
AR3	VSS	VSS	VSS
AR4			
AR5	SDQ_A16	SDQ_A16	SDQ_A16
AR6	VSS	VSS	VSS
AR7	SDQS_A2#	SDQS_A2#	SDQS_A2#
AR8	SDQ_A23	SDQ_A23	SDQ_A23
AR9	SCKE_B2	SCKE_B2	SCKE_B2
AR10	VCCSM	VCCSM	VCCSM
AR11	SMA_B12	SMA_B12	SMA_B12
AR12	SMA_B9	SMA_B9	SMA_B9

Table 14-1. GMCH/MCH Ballout for DDR2 Systems (Sorted by Ball Number)

Ball #	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]
AR13	VSS	VSS	VSS
AR14	VCCSM	VCCSM	VCCSM
AR15	SMA_B1	SMA_B1	SMA_B1
AR16	SBS_B0	SBS_B0	SBS_B0
AR17	VSS	VSS	VSS
AR18	VCCSM	VCCSM	VCCSM
AR19	SCKE_A3	SCKE_A3	SCKE_A3
AR20	SMA_A12	SMA_A12	SMA_A12
AR21	VSS	VSS	VSS
AR22	VCCSM	VCCSM	VCCSM
AR23	SMA_A4	SMA_A4	SMA_A4
AR24	SMA_A1	SMA_A1	SMA_A1
AR25	VSS	VSS	VSS
AR26	VCCSM	VCCSM	VCCSM
AR27	SBS_A0	SBS_A0	SBS_A0
AR28	SCS_A2#	SCS_A2#	SCS_A2#
AR29	SCS_A0#	SCS_A0#	SCS_A0#
AR30	VSS	VSS	VSS
AR31	VCCSM	VCCSM	VCCSM
AR32	—	—	—
AR33	VCCSM	VCCSM	VCCSM
AR34	NC	NC	NC
AR35	NC	NC	NC

NOTES:
1. DDR2, PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
2. DDR2, PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
3. DDR2, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
RSV	BLUE	BLUE	H14
RSV	BLUE#	BLUE#	J14
BSEL0	BSEL0	BSEL0	H16
BSEL1	BSEL1	BSEL1	E15
BSEL2	BSEL2	BSEL2	D17
RSV	DDC_CLK	DDC_CLK	M15
RSV	DDC_DATA	DDC_DATA	L14
DMI_RXN0	DMI_RXN0	DMI_RXN0	U6
DMI_RXN1	DMI_RXN1	DMI_RXN1	T8
DMI_RXN2	DMI_RXN2	DMI_RXN2	V8
DMI_RXN3	DMI_RXN3	DMI_RXN3	U10
DMI_RXP0	DMI_RXP0	DMI_RXP0	U5
DMI_RXP1	DMI_RXP1	DMI_RXP1	T9
DMI_RXP2	DMI_RXP2	DMI_RXP2	V7
DMI_RXP3	DMI_RXP3	DMI_RXP3	V10
DMI_TXN0	DMI_TXN0	DMI_TXN0	T3
DMI_TXN1	DMI_TXN1	DMI_TXN1	U1
DMI_TXN2	DMI_TXN2	DMI_TXN2	V3
DMI_TXN3	DMI_TXN3	DMI_TXN3	W5
DMI_TXP0	DMI_TXP0	DMI_TXP0	R3
DMI_TXP1	DMI_TXP1	DMI_TXP1	T1
DMI_TXP2	DMI_TXP2	DMI_TXP2	U3
DMI_TXP3	DMI_TXP3	DMI_TXP3	V5
DREFCLKN	DREFCLKN	DREFCLKN	M12
DREFCLKP	DREFCLKP	DREFCLKP	M13
EXP_COMPI	EXP_COMPI	EXP_COMPI	W10
EXP_COMPO	EXP_COMPO	EXP_COMPO	Y10
EXP_RXN0	EXP_RXN0	SDVOC_TVCLKIN-	F11
EXP_RXN1	EXP_RXN1	SDVOB_INT-	H11
EXP_RXN10	EXP_RXN10	RSV	L5
EXP_RXN11	EXP_RXN11	RSV	R10
EXP_RXN12	EXP_RXN12	RSV	M7
EXP_RXN13	EXP_RXN13	RSV	N5
EXP_RXN14	EXP_RXN14	RSV	P8
EXP_RXN15	EXP_RXN15	RSV	R5
EXP_RXN2	EXP_RXN2	SDVOC_STALL-	E9
EXP_RXN3	EXP_RXN3	RSV	E7
EXP_RXN4	EXP_RXN4	RSV	B4
EXP_RXN5	EXP_RXN5	SDVOC_INT-	E5
EXP_RXN6	EXP_RXN6	RSV	G5
EXP_RXN7	EXP_RXN7	RSV	H7
EXP_RXN8	EXP_RXN8	RSV	J5
EXP_RXN9	EXP_RXN9	RSV	K7

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
EXP_RXP0	EXP_RXP0	SDVOC_TVCLKIN+	E11
EXP_RXP1	EXP_RXP1	SDVOB_INT+	J11
EXP_RXP10	EXP_RXP10	RSV	L6
EXP_RXP11	EXP_RXP11	RSV	P10
EXP_RXP12	EXP_RXP12	RSV	M8
EXP_RXP13	EXP_RXP13	RSV	N6
EXP_RXP14	EXP_RXP14	RSV	P7
EXP_RXP15	EXP_RXP15	RSV	R6
EXP_RXP2	EXP_RXP2	SDVOC_STALL+	F9
EXP_RXP3	EXP_RXP3	RSV	F7
EXP_RXP4	EXP_RXP4	RSV	B3
EXP_RXP5	EXP_RXP5	SDVOC_INT+	D5
EXP_RXP6	EXP_RXP6	RSV	G6
EXP_RXP7	EXP_RXP7	RSV	H8
EXP_RXP8	EXP_RXP8	RSV	J6
EXP_RXP9	EXP_RXP9	RSV	K8
EXP_SLR	EXP_SLR	RSV	A16
EXP_TXN0	EXP_TXN0	SDVOB_RED-	C9
EXP_TXN1	EXP_TXN1	SDVOB_GREEN-	A8
EXP_TXN10	EXP_TXN10	RSV	K3
EXP_TXN11	EXP_TXN11	RSV	L1
EXP_TXN12	EXP_TXN12	RSV	M3
EXP_TXN13	EXP_TXN13	RSV	N1
EXP_TXN14	EXP_TXN14	RSV	P3
EXP_TXN15	EXP_TXN15	RSV	R1
EXP_TXN2	EXP_TXN2	SDVOB_BLUE-	C7
EXP_TXN3	EXP_TXN3	SDVOB_CLK-	A6
EXP_TXN4	EXP_TXN4	SDVOC_RED-/ SDVOB_ALPHA-	C5
EXP_TXN5	EXP_TXN5	SDVOC_GREEN-	D2
EXP_TXN6	EXP_TXN6	SDVOC_BLUE-	F3
EXP_TXN7	EXP_TXN7	SDVOC_CLK-	G1
EXP_TXN8	EXP_TXN8	RSV	H3
EXP_TXN9	EXP_TXN9	RSV	J1
EXP_TXP0	EXP_TXP0	SDVOB_RED+	C10
EXP_TXP1	EXP_TXP1	SDVOB_GREEN+	A9
EXP_TXP10	EXP_TXP10	RSV	J3
EXP_TXP11	EXP_TXP11	RSV	K1
EXP_TXP12	EXP_TXP12	RSV	L3
EXP_TXP13	EXP_TXP13	RSV	M1
EXP_TXP14	EXP_TXP14	RSV	N3
EXP_TXP15	EXP_TXP15	RSV	P1
EXP_TXP2	EXP_TXP2	SDVOB_BLUE+	C8

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
EXP_TXP3	EXP_TXP3	SDVOB_CLK+	A7
EXP_TXP4	EXP_TXP4	SDVOC_RED+/ SDVOB_ALPHA+	C6
EXP_TXP5	EXP_TXP5	SDVOC_GREEN+	C2
EXP_TXP6	EXP_TXP6	SDVOC_BLUE+	E3
EXP_TXP7	EXP_TXP7	SDVOC_CLK+	F1
EXP_TXP8	EXP_TXP8	RSV	G3
EXP_TXP9	EXP_TXP9	RSV	H1
EXTTS#	EXTTS#	EXTTS#	K16
GCLKN	GCLKN	GCLKN	B11
GCLKP	GCLKP	GCLKP	A11
RSV	GREEN	GREEN	D14
RSV	GREEN#	GREEN#	E14
HA3#	HA3#	HA3#	H29
HA4#	HA4#	HA4#	K29
HA5#	HA5#	HA5#	J29
HA6#	HA6#	HA6#	G30
HA7#	HA7#	HA7#	G32
HA8#	HA8#	HA8#	K30
HA9#	HA9#	HA9#	L29
HA10#	HA10#	HA10#	M30
HA11#	HA11#	HA11#	L31
HA12#	HA12#	HA12#	L28
HA13#	HA13#	HA13#	J28
HA14#	HA14#	HA14#	K27
HA15#	HA15#	HA15#	K33
HA16#	HA16#	HA16#	M28
HA17#	HA17#	HA17#	R29
HA18#	HA18#	HA18#	L26
HA19#	HA19#	HA19#	N26
HA20#	HA20#	HA20#	M26
HA21#	HA21#	HA21#	N31
HA22#	HA22#	HA22#	P26
HA23#	HA23#	HA23#	N29
HA24#	HA24#	HA24#	P28
HA25#	HA25#	HA25#	R28
HA26#	HA26#	HA26#	N33
HA27#	HA27#	HA27#	T27
HA28#	HA28#	HA28#	T31
HA29#	HA29#	HA29#	U28
HA30#	HA30#	HA30#	T26
HA31#	HA31#	HA31#	T29
HADS#	HADS#	HADS#	M31

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
HADSTB0#	HADSTB0#	HADSTB0#	J31
HADSTB1#	HADSTB1#	HADSTB1#	N27
HBNR#	HBNR#	HBNR#	M35
HBPRI#	HBPRI#	HBPRI#	E30
HBREQ0#	HBREQ0#	HBREQ0#	R33
HCLKN	HCLKN	HCLKN	M22
HCLKP	HCLKP	HCLKP	M23
HCPURST#	HCPURST#	HCPURST#	G24
HD0	HD0	HD0	J33
HD1	HD1	HD1	H33
HD2	HD2	HD2	J34
HD3	HD3	HD3	G35
HD4	HD4	HD4	H35
HD5	HD5	HD5	G34
HD6	HD6	HD6	F34
HD7	HD7	HD7	G33
HD8	HD8	HD8	D34
HD9	HD9	HD9	C33
HD10	HD10	HD10	D33
HD11	HD11	HD11	B34
HD12	HD12	HD12	C34
HD13	HD13	HD13	B33
HD14	HD14	HD14	C32
HD15	HD15	HD15	B32
HD16	HD16	HD16	E28
HD17	HD17	HD17	C30
HD18	HD18	HD18	D29
HD19	HD19	HD19	H28
HD20	HD20	HD20	G29
HD21	HD21	HD21	J27
HD22	HD22	HD22	F28
HD23	HD23	HD23	F27
HD24	HD24	HD24	E27
HD25	HD25	HD25	E25
HD26	HD26	HD26	G25
HD27	HD27	HD27	J25
HD28	HD28	HD28	K25
HD29	HD29	HD29	L25
HD30	HD30	HD30	L23
HD31	HD31	HD31	K23
HD32	HD32	HD32	J22
HD33	HD33	HD33	J24
HD34	HD34	HD34	K22

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
HD35	HD35	HD35	J21
HD36	HD36	HD36	M21
HD37	HD37	HD37	H23
HD38	HD38	HD38	M19
HD39	HD39	HD39	K21
HD40	HD40	HD40	H20
HD41	HD41	HD41	H19
HD42	HD42	HD42	M18
HD43	HD43	HD43	K18
HD44	HD44	HD44	K17
HD45	HD45	HD45	G18
HD46	HD46	HD46	H18
HD47	HD47	HD47	F17
HD48	HD48	HD48	A25
HD49	HD49	HD49	C27
HD50	HD50	HD50	C31
HD51	HD51	HD51	B30
HD52	HD52	HD52	B31
HD53	HD53	HD53	A31
HD54	HD54	HD54	B27
HD55	HD55	HD55	A29
HD56	HD56	HD56	C28
HD57	HD57	HD57	A28
HD58	HD58	HD58	C25
HD59	HD59	HD59	C26
HD60	HD60	HD60	D27
HD61	HD61	HD61	A27
HD62	HD62	HD62	E24
HD63	HD63	HD63	B25
HDBSY#	HDBSY#	HDBSY#	L35
HDEFER#	HDEFER#	HDEFER#	J35
HDINV0#	HDINV0#	HDINV0#	E34
HDINV1#	HDINV1#	HDINV1#	J26
HDINV2#	HDINV2#	HDINV2#	K19
HDINV3#	HDINV3#	HDINV3#	B26
HDRDY#	HDRDY#	HDRDY#	M32
HDSTBN0#	HDSTBN0#	HDSTBN0#	E35
HDSTBN1#	HDSTBN1#	HDSTBN1#	F26
HDSTBN2#	HDSTBN2#	HDSTBN2#	F19
HDSTBN3#	HDSTBN3#	HDSTBN3#	C29
HDSTBP0#	HDSTBP0#	HDSTBP0#	E33
HDSTBP1#	HDSTBP1#	HDSTBP1#	H26
HDSTBP2#	HDSTBP2#	HDSTBP2#	J19

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
HDSTBP3#	HDSTBP3#	HDSTBP3#	B29
HEDRDY#	HEDRDY#	HEDRDY#	P33
HHIT#	HHIT#	HHIT#	L34
HHITM#	HHITM#	HHITM#	N35
HLOCK#	HLOCK#	HLOCK#	L33
HPCREQ#	HPCREQ#	HPCREQ#	E31
HRCOMP	HRCOMP	HRCOMP	B23
HREQ0#	HREQ0#	HREQ0#	F33
HREQ1#	HREQ1#	HREQ1#	E32
HREQ2#	HREQ2#	HREQ2#	H31
HREQ3#	HREQ3#	HREQ3#	G31
HREQ4#	HREQ4#	HREQ4#	F31
HRS0#	HRS0#	HRS0#	K34
HRS1#	HRS1#	HRS1#	P34
HRS2#	HRS2#	HRS2#	J32
HSCOMP	HSCOMP	HSCOMP	D24
HSWING	HSWING	HSWING	A23
RSV	HSYNC	HSYNC	E12
HTRDY#	HTRDY#	HTRDY#	N34
HVREF	HVREF	HVREF	A24
ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	M14
MTYPE	MTYPE	MTYPE	C15
NC	NC	NC	A2
NC	NC	NC	A34
NC	NC	NC	A35
NC	NC	NC	AA12
NC	NC	NC	AB12
NC	NC	NC	AC23
NC	NC	NC	AC24
NC	NC	NC	AD30
NC	NC	NC	AG6
NC	NC	NC	AH24
NC	NC	NC	AJ14
NC	NC	NC	AL28
NC	NC	NC	AN19
NC	NC	NC	AP1
NC	NC	NC	AP35
NC	NC	NC	AR1
NC	NC	NC	AR2
NC	NC	NC	AR34
NC	NC	NC	AR35
NC	NC	NC	B1
NC	NC	NC	B35

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
NC	NC	NC	C16
NC	NC	NC	E16
NC	NC	NC	F12
NC	NC	NC	F24
NC	NC	NC	G12
NC	NC	NC	H12
NC	NC	NC	H15
NC	NC	NC	H17
NC	NC	NC	J12
NC	NC	NC	K12
NC	NC	NC	L12
NC	NC	NC	L19
NC	NC	NC	N12
NC	NC	NC	N22
NC	NC	NC	N23
NC	NC	NC	N24
NC	NC	NC	P12
NC	NC	NC	P23
NC	NC	NC	P24
NC	NC	NC	P30
NC	NC	NC	R12
NC	NC	NC	R24
NC	NC	NC	T12
NC	NC	NC	U12
NC	NC	NC	V12
NC	NC	NC	W12
NC	NC	NC	Y12
PWROK	PWROK	PWROK	AG7
RSV	RED	RED	F14
RSV	RED#	RED#	G14
RSV	REFSET	REFSET	A15
RSTIN#	RSTIN#	RSTIN#	AF7
RSV	RSV	RSV	AA30
RSV	RSV	RSV	AA31
RSV	RSV	RSV	AB29
RSV	RSV	RSV	AB33
RSV	RSV	RSV	AC12
RSV	RSV	RSV	AC13
RSV	RSV	RSV	AC14
RSV	RSV	RSV	AC15
RSV	RSV	RSV	AC16
RSV	RSV	RSV	AC17
RSV	RSV	RSV	AC18

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
RSV	RSV	RSV	AC19
RSV	RSV	RSV	AC20
RSV	RSV	RSV	AC21
RSV	RSV	RSV	AC22
RSV	RSV	RSV	AD32
RSV	RSV	RSV	AJ18
RSV	RSV	RSV	AJ20
RSV	RSV	RSV	AJ21
RSV	RSV	RSV	AJ23
RSV	RSV	RSV	AJ24
RSV	RSV	RSV	AK18
RSV	RSV	RSV	AK21
RSV	RSV	RSV	AK24
RSV	RSV	RSV	AL20
RSV	RSV	RSV	AL21
RSV	RSV	RSV	B15
RSV	RSV	RSV	C14
RSV	RSV	RSV	F15
RSV	RSV	RSV	G16
RSV	RSV	RSV	K15
RSV	RSV	RSV	M16
RSV	RSV	RSV	R30
RSV	RSV	RSV	R31
RSV	RSV	RSV	R35
RSV	RSV	RSV	U30
RSV	RSV	RSV	V30
RSV	RSV	RSV	V31
RSV	RSV	RSV	V32
RSV	RSV	RSV	Y30
RSV_TP0	RSV_TP0	RSV_TP0	AE16
RSV_TP1	RSV_TP1	RSV_TP1	AH15
RSV_TP2	RSV_TP2	RSV_TP2	AN14
RSV_TP3	RSV_TP3	RSV_TP3	AK15
SBS_A0	SBS_A0	SBS_A0	AR27
SBS_A1	SBS_A1	SBS_A1	AN27
SBS_A2	SBS_A2	SBS_A2	AN20
SBS_B0	SBS_B0	SBS_B0	AR16
SBS_B1	SBS_B1	SBS_B1	AN16
SBS_B2	SBS_B2	SBS_B2	AN11
SCAS_A#	SCAS_A#	SCAS_A#	AN29
SCAS_B#	SCAS_B#	SCAS_B#	AP18
SCKE_A0	SCKE_A0	SCKE_A0	AP19
SCKE_A1	SCKE_A1	SCKE_A1	AM18

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SCKE_A2	SCKE_A2	SCKE_A2	AN18
SCKE_A3	SCKE_A3	SCKE_A3	AR19
SCKE_B0	SCKE_B0	SCKE_B0	AP10
SCKE_B1	SCKE_B1	SCKE_B1	AN10
SCKE_B2	SCKE_B2	SCKE_B2	AR9
SCKE_B3	SCKE_B3	SCKE_B3	AM9
SCLK_A0	SCLK_A0	SCLK_A0	AN26
SCLK_A0#	SCLK_A0#	SCLK_A0#	AP25
SCLK_A1	SCLK_A1	SCLK_A1	AM2
SCLK_A1#	SCLK_A1#	SCLK_A1#	AM3
SCLK_A2	SCLK_A2	SCLK_A2	AC34
SCLK_A2#	SCLK_A2#	SCLK_A2#	AC35
SCLK_A3	SCLK_A3	SCLK_A3	AN25
SCLK_A3#	SCLK_A3#	SCLK_A3#	AM24
SCLK_A4	SCLK_A4	SCLK_A4	AN3
SCLK_A4#	SCLK_A4#	SCLK_A4#	AN2
SCLK_A5	SCLK_A5	SCLK_A5	AC33
SCLK_A5#	SCLK_A5#	SCLK_A5#	AB34
SCLK_B0	SCLK_B0	SCLK_B0	AH22
SCLK_B0#	SCLK_B0#	SCLK_B0#	AG23
SCLK_B1	SCLK_B1	SCLK_B1	AK9
SCLK_B1#	SCLK_B1#	SCLK_B1#	AL9
SCLK_B2	SCLK_B2	SCLK_B2	AE26
SCLK_B2#	SCLK_B2#	SCLK_B2#	AE25
SCLK_B3	SCLK_B3	SCLK_B3	AL23
SCLK_B3#	SCLK_B3#	SCLK_B3#	AK22
SCLK_B4	SCLK_B4	SCLK_B4	AJ11
SCLK_B4#	SCLK_B4#	SCLK_B4#	AL11
SCLK_B5	SCLK_B5	SCLK_B5	AD28
SCLK_B5#	SCLK_B5#	SCLK_B5#	AD29
SCS_A0#	SCS_A0#	SCS_A0#	AR29
SCS_A1#	SCS_A1#	SCS_A1#	AP32
SCS_A2#	SCS_A2#	SCS_A2#	AR28
SCS_A3#	SCS_A3#	SCS_A3#	AN31
SCS_B0#	SCS_B0#	SCS_B0#	AN33
SCS_B1#	SCS_B1#	SCS_B1#	AM34
SCS_B2#	SCS_B2#	SCS_B2#	AP34
SCS_B3#	SCS_B3#	SCS_B3#	AN34
SDM_A0	SDM_A0	SDM_A0	AF2
SDM_A1	SDM_A1	SDM_A1	AL1
SDM_A2	SDM_A2	SDM_A2	AN7
SDM_A3	SDM_A3	SDM_A3	AH16
SDM_A4	SDM_A4	SDM_A4	AK29

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SDM_A5	SDM_A5	SDM_A5	AG34
SDM_A6	SDM_A6	SDM_A6	AA33
SDM_A7	SDM_A7	SDM_A7	U33
SDM_B0	SDM_B0	SDM_B0	AJ5
SDM_B1	SDM_B1	SDM_B1	AH9
SDM_B2	SDM_B2	SDM_B2	AH13
SDM_B3	SDM_B3	SDM_B3	AG20
SDM_B4	SDM_B4	SDM_B4	AG24
SDM_B5	SDM_B5	SDM_B5	AH31
SDM_B6	SDM_B6	SDM_B6	AD24
SDM_B7	SDM_B7	SDM_B7	W31
SDQ_A0	SDQ_A0	SDQ_A0	AE3
SDQ_A1	SDQ_A1	SDQ_A1	AF3
SDQ_A2	SDQ_A2	SDQ_A2	AH3
SDQ_A3	SDQ_A3	SDQ_A3	AJ2
SDQ_A4	SDQ_A4	SDQ_A4	AE2
SDQ_A5	SDQ_A5	SDQ_A5	AE1
SDQ_A6	SDQ_A6	SDQ_A6	AG3
SDQ_A7	SDQ_A7	SDQ_A7	AH2
SDQ_A8	SDQ_A8	SDQ_A8	AK2
SDQ_A9	SDQ_A9	SDQ_A9	AK3
SDQ_A10	SDQ_A10	SDQ_A10	AN4
SDQ_A11	SDQ_A11	SDQ_A11	AP4
SDQ_A12	SDQ_A12	SDQ_A12	AJ1
SDQ_A13	SDQ_A13	SDQ_A13	AJ3
SDQ_A14	SDQ_A14	SDQ_A14	AP2
SDQ_A15	SDQ_A15	SDQ_A15	AP3
SDQ_A16	SDQ_A16	SDQ_A16	AR5
SDQ_A17	SDQ_A17	SDQ_A17	AP6
SDQ_A18	SDQ_A18	SDQ_A18	AP9
SDQ_A19	SDQ_A19	SDQ_A19	AN9
SDQ_A20	SDQ_A20	SDQ_A20	AN5
SDQ_A21	SDQ_A21	SDQ_A21	AP5
SDQ_A22	SDQ_A22	SDQ_A22	AN8
SDQ_A23	SDQ_A23	SDQ_A23	AR8
SDQ_A24	SDQ_A24	SDQ_A24	AL17
SDQ_A25	SDQ_A25	SDQ_A25	AJ17
SDQ_A26	SDQ_A26	SDQ_A26	AF19
SDQ_A27	SDQ_A27	SDQ_A27	AH18
SDQ_A28	SDQ_A28	SDQ_A28	AK16
SDQ_A29	SDQ_A29	SDQ_A29	AF16
SDQ_A30	SDQ_A30	SDQ_A30	AD17
SDQ_A31	SDQ_A31	SDQ_A31	AE19

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SDQ_A32	SDQ_A32	SDQ_A32	AK27
SDQ_A33	SDQ_A33	SDQ_A33	AJ28
SDQ_A34	SDQ_A34	SDQ_A34	AL31
SDQ_A35	SDQ_A35	SDQ_A35	AK31
SDQ_A36	SDQ_A36	SDQ_A36	AH27
SDQ_A37	SDQ_A37	SDQ_A37	AL27
SDQ_A38	SDQ_A38	SDQ_A38	AN30
SDQ_A39	SDQ_A39	SDQ_A39	AL30
SDQ_A40	SDQ_A40	SDQ_A40	AH33
SDQ_A41	SDQ_A41	SDQ_A41	AH35
SDQ_A42	SDQ_A42	SDQ_A42	AF33
SDQ_A43	SDQ_A43	SDQ_A43	AE33
SDQ_A44	SDQ_A44	SDQ_A44	AJ33
SDQ_A45	SDQ_A45	SDQ_A45	AJ34
SDQ_A46	SDQ_A46	SDQ_A46	AG32
SDQ_A47	SDQ_A47	SDQ_A47	AF34
SDQ_A48	SDQ_A48	SDQ_A48	AD31
SDQ_A49	SDQ_A49	SDQ_A49	AD35
SDQ_A50	SDQ_A50	SDQ_A50	Y33
SDQ_A51	SDQ_A51	SDQ_A51	W34
SDQ_A52	SDQ_A52	SDQ_A52	AE35
SDQ_A53	SDQ_A53	SDQ_A53	AE34
SDQ_A54	SDQ_A54	SDQ_A54	AA32
SDQ_A55	SDQ_A55	SDQ_A55	Y35
SDQ_A56	SDQ_A56	SDQ_A56	V34
SDQ_A57	SDQ_A57	SDQ_A57	V33
SDQ_A58	SDQ_A58	SDQ_A58	R32
SDQ_A59	SDQ_A59	SDQ_A59	R34
SDQ_A60	SDQ_A60	SDQ_A60	W35
SDQ_A61	SDQ_A61	SDQ_A61	W33
SDQ_A62	SDQ_A62	SDQ_A62	T33
SDQ_A63	SDQ_A63	SDQ_A63	T35
SDQ_B0	SDQ_B0	SDQ_B0	AH4
SDQ_B1	SDQ_B1	SDQ_B1	AJ6
SDQ_B2	SDQ_B2	SDQ_B2	AL6
SDQ_B3	SDQ_B3	SDQ_B3	AN6
SDQ_B4	SDQ_B4	SDQ_B4	AG9
SDQ_B5	SDQ_B5	SDQ_B5	AH7
SDQ_B6	SDQ_B6	SDQ_B6	AL5
SDQ_B7	SDQ_B7	SDQ_B7	AM5
SDQ_B8	SDQ_B8	SDQ_B8	AJ8
SDQ_B9	SDQ_B9	SDQ_B9	AL8
SDQ_B10	SDQ_B10	SDQ_B10	AF11

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SDQ_B11	SDQ_B11	SDQ_B11	AE11
SDQ_B12	SDQ_B12	SDQ_B12	AJ7
SDQ_B13	SDQ_B13	SDQ_B13	AL7
SDQ_B14	SDQ_B14	SDQ_B14	AG10
SDQ_B15	SDQ_B15	SDQ_B15	AG11
SDQ_B16	SDQ_B16	SDQ_B16	AF13
SDQ_B17	SDQ_B17	SDQ_B17	AH12
SDQ_B18	SDQ_B18	SDQ_B18	AD14
SDQ_B19	SDQ_B19	SDQ_B19	AD15
SDQ_B20	SDQ_B20	SDQ_B20	AD12
SDQ_B21	SDQ_B21	SDQ_B21	AE13
SDQ_B22	SDQ_B22	SDQ_B22	AG14
SDQ_B23	SDQ_B23	SDQ_B23	AF14
SDQ_B24	SDQ_B24	SDQ_B24	AK19
SDQ_B25	SDQ_B25	SDQ_B25	AH19
SDQ_B26	SDQ_B26	SDQ_B26	AH21
SDQ_B27	SDQ_B27	SDQ_B27	AD21
SDQ_B28	SDQ_B28	SDQ_B28	AD18
SDQ_B29	SDQ_B29	SDQ_B29	AL18
SDQ_B30	SDQ_B30	SDQ_B30	AE22
SDQ_B31	SDQ_B31	SDQ_B31	AF22
SDQ_B32	SDQ_B32	SDQ_B32	AF24
SDQ_B33	SDQ_B33	SDQ_B33	AF25
SDQ_B34	SDQ_B34	SDQ_B34	AL26
SDQ_B35	SDQ_B35	SDQ_B35	AJ26
SDQ_B36	SDQ_B36	SDQ_B36	AF23
SDQ_B37	SDQ_B37	SDQ_B37	AD23
SDQ_B38	SDQ_B38	SDQ_B38	AL25
SDQ_B39	SDQ_B39	SDQ_B39	AJ25
SDQ_B40	SDQ_B40	SDQ_B40	AK32
SDQ_B41	SDQ_B41	SDQ_B41	AJ31
SDQ_B42	SDQ_B42	SDQ_B42	AG31
SDQ_B43	SDQ_B43	SDQ_B43	AF28
SDQ_B44	SDQ_B44	SDQ_B44	AJ29
SDQ_B45	SDQ_B45	SDQ_B45	AK33
SDQ_B46	SDQ_B46	SDQ_B46	AG30
SDQ_B47	SDQ_B47	SDQ_B47	AG27
SDQ_B48	SDQ_B48	SDQ_B48	AF27
SDQ_B49	SDQ_B49	SDQ_B49	AE27
SDQ_B50	SDQ_B50	SDQ_B50	AC26
SDQ_B51	SDQ_B51	SDQ_B51	AB26
SDQ_B52	SDQ_B52	SDQ_B52	AE31
SDQ_B53	SDQ_B53	SDQ_B53	AE29

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SDQ_B54	SDQ_B54	SDQ_B54	AC28
SDQ_B55	SDQ_B55	SDQ_B55	AB27
SDQ_B56	SDQ_B56	SDQ_B56	AA28
SDQ_B57	SDQ_B57	SDQ_B57	W29
SDQ_B58	SDQ_B58	SDQ_B58	V28
SDQ_B59	SDQ_B59	SDQ_B59	V29
SDQ_B60	SDQ_B60	SDQ_B60	Y26
SDQ_B61	SDQ_B61	SDQ_B61	AA29
SDQ_B62	SDQ_B62	SDQ_B62	W26
SDQ_B63	SDQ_B63	SDQ_B63	U26
SDQS_A0	SDQS_A0	SDQS_A0	AG1
SDQS_A0#	SDQS_A0#	SDQS_A0#	AG2
SDQS_A1	SDQS_A1	SDQS_A1	AL3
SDQS_A1#	SDQS_A1#	SDQS_A1#	AL2
SDQS_A2	SDQS_A2	SDQS_A2	AP7
SDQS_A2#	SDQS_A2#	SDQS_A2#	AR7
SDQS_A3	SDQS_A3	SDQS_A3	AF17
SDQS_A3#	SDQS_A3#	SDQS_A3#	AG17
SDQS_A4	SDQS_A4	SDQS_A4	AM30
SDQS_A4#	SDQS_A4#	SDQS_A4#	AL29
SDQS_A5	SDQS_A5	SDQS_A5	AG35
SDQS_A5#	SDQS_A5#	SDQS_A5#	AG33
SDQS_A6	SDQS_A6	SDQS_A6	AA34
SDQS_A6#	SDQS_A6#	SDQS_A6#	AA35
SDQS_A7	SDQS_A7	SDQS_A7	U34
SDQS_A7#	SDQS_A7#	SDQS_A7#	U35
SDQS_B0	SDQS_B0	SDQS_B0	AK5
SDQS_B0#	SDQS_B0#	SDQS_B0#	AL4
SDQS_B1	SDQS_B1	SDQS_B1	AK10
SDQS_B1#	SDQS_B1#	SDQS_B1#	AH10
SDQS_B2	SDQS_B2	SDQS_B2	AK13
SDQS_B2#	SDQS_B2#	SDQS_B2#	AL14
SDQS_B3	SDQS_B3	SDQS_B3	AD20
SDQS_B3#	SDQS_B3#	SDQS_B3#	AF20
SDQS_B4	SDQS_B4	SDQS_B4	AH25
SDQS_B4#	SDQS_B4#	SDQS_B4#	AG26
SDQS_B5	SDQS_B5	SDQS_B5	AH28
SDQS_B5#	SDQS_B5#	SDQS_B5#	AH30
SDQS_B6	SDQS_B6	SDQS_B6	AB31
SDQS_B6#	SDQS_B6#	SDQS_B6#	AC30
SDQS_B7	SDQS_B7	SDQS_B7	W27
SDQS_B7#	SDQS_B7#	SDQS_B7#	Y28
RSV	SDVO_CTRLCLK	SDVO_CTRLCLK	J13

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
RSV	SDVO_CTRLDATA	SDVO_CTRLDATA	K13
SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	AJ12
SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	AF9
SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	AK12
SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	AE10
SMA_A0	SMA_A0	SMA_A0	AP26
SMA_A1	SMA_A1	SMA_A1	AR24
SMA_A2	SMA_A2	SMA_A2	AL24
SMA_A3	SMA_A3	SMA_A3	AP23
SMA_A4	SMA_A4	SMA_A4	AR23
SMA_A5	SMA_A5	SMA_A5	AP22
SMA_A6	SMA_A6	SMA_A6	AN23
SMA_A7	SMA_A7	SMA_A7	AP21
SMA_A8	SMA_A8	SMA_A8	AN22
SMA_A9	SMA_A9	SMA_A9	AN21
SMA_A10	SMA_A10	SMA_A10	AM27
SMA_A11	SMA_A11	SMA_A11	AM21
SMA_A12	SMA_A12	SMA_A12	AR20
SMA_A13	SMA_A13	SMA_A13	AP31
SMA_B0	SMA_B0	SMA_B0	AM15
SMA_B1	SMA_B1	SMA_B1	AR15
SMA_B2	SMA_B2	SMA_B2	AN15
SMA_B3	SMA_B3	SMA_B3	AL15
SMA_B4	SMA_B4	SMA_B4	AP14
SMA_B5	SMA_B5	SMA_B5	AM12
SMA_B6	SMA_B6	SMA_B6	AP13
SMA_B7	SMA_B7	SMA_B7	AL12
SMA_B8	SMA_B8	SMA_B8	AN13
SMA_B9	SMA_B9	SMA_B9	AR12
SMA_B10	SMA_B10	SMA_B10	AP15
SMA_B11	SMA_B11	SMA_B11	AP11
SMA_B12	SMA_B12	SMA_B12	AR11
SMA_B13	SMA_B13	SMA_B13	AL33
SOCOMP0	SOCOMP0	SOCOMP0	AF5
SOCOMP1	SOCOMP1	SOCOMP1	AE5
SODT_A0	SODT_A0	SODT_A0	AP30
SODT_A1	SODT_A1	SODT_A1	AN32
SODT_A2	SODT_A2	SODT_A2	AP29
SODT_A3	SODT_A3	SODT_A3	AP33
SODT_B0	SODT_B0	SODT_B0	AM33
SODT_B1	SODT_B1	SODT_B1	AL34
SODT_B2	SODT_B2	SODT_B2	AL35
SODT_B3	SODT_B3	SODT_B3	AK34

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
SRAS_A#	SRAS_A#	SRAS_A#	AP27
SRAS_B#	SRAS_B#	SRAS_B#	AN17
SRCOMP0	SRCOMP0	SRCOMP0	AG4
SRCOMP1	SRCOMP1	SRCOMP1	AG8
SVREF0	SVREF0	SVREF0	AE7
SVREF1	SVREF1	SVREF1	AE8
SWE_A#	SWE_A#	SWE_A#	AN28
SWE_B#	SWE_B#	SWE_B#	AP17
VCC	VCC	VCC	AA13
VCC	VCC	VCC	AA14
VCC	VCC	VCC	AA16
VCC	VCC	VCC	AA18
VCC	VCC	VCC	AA20
VCC	VCC	VCC	AA21
VCC	VCC	VCC	AA22
VCC	VCC	VCC	AA23
VCC	VCC	VCC	AA24
VCC	VCC	VCC	AB1
VCC	VCC	VCC	AB10
VCC	VCC	VCC	AB11
VCC	VCC	VCC	AB13
VCC	VCC	VCC	AB14
VCC	VCC	VCC	AB15
VCC	VCC	VCC	AB16
VCC	VCC	VCC	AB17
VCC	VCC	VCC	AB18
VCC	VCC	VCC	AB19
VCC	VCC	VCC	AB2
VCC	VCC	VCC	AB20
VCC	VCC	VCC	AB21
VCC	VCC	VCC	AB22
VCC	VCC	VCC	AB23
VCC	VCC	VCC	AB24
VCC	VCC	VCC	AB3
VCC	VCC	VCC	AB4
VCC	VCC	VCC	AB5
VCC	VCC	VCC	AB6
VCC	VCC	VCC	AB7
VCC	VCC	VCC	AB8
VCC	VCC	VCC	AB9
VCC	VCC	VCC	AC1
VCC	VCC	VCC	AC10
VCC	VCC	VCC	AC11

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VCC	VCC	VCC	AC2
VCC	VCC	VCC	AC3
VCC	VCC	VCC	AC4
VCC	VCC	VCC	AC5
VCC	VCC	VCC	AC6
VCC	VCC	VCC	AC7
VCC	VCC	VCC	AC8
VCC	VCC	VCC	AC9
VCC	VCC	VCC	AD1
VCC	VCC	VCC	AD10
VCC	VCC	VCC	AD2
VCC	VCC	VCC	AD3
VCC	VCC	VCC	AD4
VCC	VCC	VCC	AD5
VCC	VCC	VCC	AD6
VCC	VCC	VCC	AD7
VCC	VCC	VCC	AD8
VCC	VCC	VCC	AD9
VCC	VCC	VCC	L10
VCC	VCC	VCC	N13
VCC	VCC	VCC	N14
VCC	VCC	VCC	N15
VCC	VCC	VCC	N16
VCC	VCC	VCC	N18
VCC	VCC	VCC	N20
VCC	VCC	VCC	N21
VCC	VCC	VCC	P13
VCC	VCC	VCC	P14
VCC	VCC	VCC	P15
VCC	VCC	VCC	P17
VCC	VCC	VCC	P19
VCC	VCC	VCC	P21
VCC	VCC	VCC	P22
VCC	VCC	VCC	R13
VCC	VCC	VCC	R14
VCC	VCC	VCC	R15
VCC	VCC	VCC	R16
VCC	VCC	VCC	R18
VCC	VCC	VCC	R20
VCC	VCC	VCC	R22
VCC	VCC	VCC	R23
VCC	VCC	VCC	T13
VCC	VCC	VCC	T14

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VCC	VCC	VCC	T15
VCC	VCC	VCC	T16
VCC	VCC	VCC	T17
VCC	VCC	VCC	T19
VCC	VCC	VCC	T20
VCC	VCC	VCC	T21
VCC	VCC	VCC	T23
VCC	VCC	VCC	T24
VCC	VCC	VCC	U13
VCC	VCC	VCC	U14
VCC	VCC	VCC	U16
VCC	VCC	VCC	U18
VCC	VCC	VCC	U20
VCC	VCC	VCC	U22
VCC	VCC	VCC	U24
VCC	VCC	VCC	V13
VCC	VCC	VCC	V14
VCC	VCC	VCC	V15
VCC	VCC	VCC	V17
VCC	VCC	VCC	V19
VCC	VCC	VCC	V21
VCC	VCC	VCC	V23
VCC	VCC	VCC	V24
VCC	VCC	VCC	W13
VCC	VCC	VCC	W14
VCC	VCC	VCC	W16
VCC	VCC	VCC	W18
VCC	VCC	VCC	W20
VCC	VCC	VCC	W22
VCC	VCC	VCC	W24
VCC	VCC	VCC	Y13
VCC	VCC	VCC	Y14
VCC	VCC	VCC	Y15
VCC	VCC	VCC	Y16
VCC	VCC	VCC	Y17
VCC	VCC	VCC	Y19
VCC	VCC	VCC	Y20
VCC	VCC	VCC	Y21
VCC	VCC	VCC	Y23
VCC	VCC	VCC	Y24
VCC_EXP	VCC_EXP	VCC_EXP	W1
VCC_EXP	VCC_EXP	VCC_EXP	W2
VCC_EXP	VCC_EXP	VCC_EXP	W3

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VCC_EXP	VCC_EXP	VCC_EXP	W4
VCC_EXP	VCC_EXP	VCC_EXP	W6
VCC_EXP	VCC_EXP	VCC_EXP	W7
VCC_EXP	VCC_EXP	VCC_EXP	W8
VCC_EXP	VCC_EXP	VCC_EXP	W9
VCC_EXP	VCC_EXP	VCC_EXP	Y1
VCC_EXP	VCC_EXP	VCC_EXP	Y2
VCC_EXP	VCC_EXP	VCC_EXP	Y3
VCC_EXP	VCC_EXP	VCC_EXP	Y4
VCC_EXP	VCC_EXP	VCC_EXP	Y5
VCC_EXP	VCC_EXP	VCC_EXP	Y6
VCC_EXP	VCC_EXP	VCC_EXP	Y7
VCC_EXP	VCC_EXP	VCC_EXP	Y8
VCC_EXP	VCC_EXP	VCC_EXP	Y9
VCC2	VCC2	VCC2	A13
RSV	VCCA_DAC	VCCA_DAC	D13
RSV	VCCA_DAC	VCCA_DAC	E13
VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	A12
VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	B13
VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	A14
VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	A17
VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	B17
VCCSM	VCCSM	VCCSM	AK35
VCCSM	VCCSM	VCCSM	AM10
VCCSM	VCCSM	VCCSM	AM11
VCCSM	VCCSM	VCCSM	AM13
VCCSM	VCCSM	VCCSM	AM14
VCCSM	VCCSM	VCCSM	AM16
VCCSM	VCCSM	VCCSM	AM17
VCCSM	VCCSM	VCCSM	AM19
VCCSM	VCCSM	VCCSM	AM20
VCCSM	VCCSM	VCCSM	AM22
VCCSM	VCCSM	VCCSM	AM23
VCCSM	VCCSM	VCCSM	AM25
VCCSM	VCCSM	VCCSM	AM26
VCCSM	VCCSM	VCCSM	AM28
VCCSM	VCCSM	VCCSM	AM32
VCCSM	VCCSM	VCCSM	AN35
VCCSM	VCCSM	VCCSM	AP12
VCCSM	VCCSM	VCCSM	AP16
VCCSM	VCCSM	VCCSM	AP20
VCCSM	VCCSM	VCCSM	AP24
VCCSM	VCCSM	VCCSM	AP28

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VCCSM	VCCSM	VCCSM	AR10
VCCSM	VCCSM	VCCSM	AR14
VCCSM	VCCSM	VCCSM	AR18
VCCSM	VCCSM	VCCSM	AR22
VCCSM	VCCSM	VCCSM	AR26
VCCSM	VCCSM	VCCSM	AR31
VCCSM	VCCSM	VCCSM	AR33
VSS	VSS	VSS	A10
VSS	VSS	VSS	A18
VSS	VSS	VSS	A26
VSS	VSS	VSS	A3
VSS	VSS	VSS	A30
VSS	VSS	VSS	A33
VSS	VSS	VSS	A5
VSS	VSS	VSS	AA1
VSS	VSS	VSS	AA10
VSS	VSS	VSS	AA11
VSS	VSS	VSS	AA15
VSS	VSS	VSS	AA17
VSS	VSS	VSS	AA19
VSS	VSS	VSS	AA2
VSS	VSS	VSS	AA25
VSS	VSS	VSS	AA26
VSS	VSS	VSS	AA27
VSS	VSS	VSS	AA3
VSS	VSS	VSS	AA4
VSS	VSS	VSS	AA5
VSS	VSS	VSS	AA6
VSS	VSS	VSS	AA7
VSS	VSS	VSS	AA8
VSS	VSS	VSS	AA9
VSS	VSS	VSS	AB25
VSS	VSS	VSS	AB28
VSS	VSS	VSS	AB30
VSS	VSS	VSS	AB32
VSS	VSS	VSS	AB35
VSS	VSS	VSS	AC25
VSS	VSS	VSS	AC27
VSS	VSS	VSS	AC29
VSS	VSS	VSS	AC31
VSS	VSS	VSS	AC32
VSS	VSS	VSS	AD11
VSS	VSS	VSS	AD13

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	AD16
VSS	VSS	VSS	AD19
VSS	VSS	VSS	AD22
VSS	VSS	VSS	AD25
VSS	VSS	VSS	AD26
VSS	VSS	VSS	AD27
VSS	VSS	VSS	AD34
VSS	VSS	VSS	AE12
VSS	VSS	VSS	AE14
VSS	VSS	VSS	AE15
VSS	VSS	VSS	AE17
VSS	VSS	VSS	AE18
VSS	VSS	VSS	AE20
VSS	VSS	VSS	AE21
VSS	VSS	VSS	AE23
VSS	VSS	VSS	AE24
VSS	VSS	VSS	AE28
VSS	VSS	VSS	AE30
VSS	VSS	VSS	AE32
VSS	VSS	VSS	AE4
VSS	VSS	VSS	AE6
VSS	VSS	VSS	AE9
VSS	VSS	VSS	AF1
VSS	VSS	VSS	AF10
VSS	VSS	VSS	AF12
VSS	VSS	VSS	AF15
VSS	VSS	VSS	AF18
VSS	VSS	VSS	AF21
VSS	VSS	VSS	AF26
VSS	VSS	VSS	AF29
VSS	VSS	VSS	AF30
VSS	VSS	VSS	AF31
VSS	VSS	VSS	AF32
VSS	VSS	VSS	AF35
VSS	VSS	VSS	AF4
VSS	VSS	VSS	AF6
VSS	VSS	VSS	AF8
VSS	VSS	VSS	AG12
VSS	VSS	VSS	AG13
VSS	VSS	VSS	AG15
VSS	VSS	VSS	AG16
VSS	VSS	VSS	AG18
VSS	VSS	VSS	AG19

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	AG21
VSS	VSS	VSS	AG22
VSS	VSS	VSS	AG25
VSS	VSS	VSS	AG28
VSS	VSS	VSS	AG29
VSS	VSS	VSS	AG5
VSS	VSS	VSS	AH1
VSS	VSS	VSS	AH11
VSS	VSS	VSS	AH14
VSS	VSS	VSS	AH17
VSS	VSS	VSS	AH20
VSS	VSS	VSS	AH23
VSS	VSS	VSS	AH26
VSS	VSS	VSS	AH29
VSS	VSS	VSS	AH32
VSS	VSS	VSS	AH34
VSS	VSS	VSS	AH5
VSS	VSS	VSS	AH6
VSS	VSS	VSS	AH8
VSS	VSS	VSS	AJ10
VSS	VSS	VSS	AJ13
VSS	VSS	VSS	AJ15
VSS	VSS	VSS	AJ16
VSS	VSS	VSS	AJ19
VSS	VSS	VSS	AJ22
VSS	VSS	VSS	AJ27
VSS	VSS	VSS	AJ30
VSS	VSS	VSS	AJ32
VSS	VSS	VSS	AJ35
VSS	VSS	VSS	AJ4
VSS	VSS	VSS	AJ9
VSS	VSS	VSS	AK1
VSS	VSS	VSS	AK11
VSS	VSS	VSS	AK14
VSS	VSS	VSS	AK17
VSS	VSS	VSS	AK20
VSS	VSS	VSS	AK23
VSS	VSS	VSS	AK25
VSS	VSS	VSS	AK26
VSS	VSS	VSS	AK28
VSS	VSS	VSS	AK30
VSS	VSS	VSS	AK4
VSS	VSS	VSS	AK6

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	AK7
VSS	VSS	VSS	AK8
VSS	VSS	VSS	AL10
VSS	VSS	VSS	AL13
VSS	VSS	VSS	AL16
VSS	VSS	VSS	AL19
VSS	VSS	VSS	AL22
VSS	VSS	VSS	AL32
VSS	VSS	VSS	AM29
VSS	VSS	VSS	AM31
VSS	VSS	VSS	AM4
VSS	VSS	VSS	AM6
VSS	VSS	VSS	AM7
VSS	VSS	VSS	AM8
VSS	VSS	VSS	AN1
VSS	VSS	VSS	AP8
VSS	VSS	VSS	AR13
VSS	VSS	VSS	AR17
VSS	VSS	VSS	AR21
VSS	VSS	VSS	AR25
VSS	VSS	VSS	AR3
VSS	VSS	VSS	AR30
VSS	VSS	VSS	AR6
VSS	VSS	VSS	B10
VSS	VSS	VSS	B12
VSS	VSS	VSS	B14
VSS	VSS	VSS	B16
VSS	VSS	VSS	B18
VSS	VSS	VSS	B2
VSS	VSS	VSS	B24
VSS	VSS	VSS	B28
VSS	VSS	VSS	B5
VSS	VSS	VSS	B6
VSS	VSS	VSS	B7
VSS	VSS	VSS	B8
VSS	VSS	VSS	B9
VSS	VSS	VSS	C1
VSS	VSS	VSS	C11
VSS	VSS	VSS	C13
VSS	VSS	VSS	C17
VSS	VSS	VSS	C18
VSS	VSS	VSS	C23
VSS	VSS	VSS	C3

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	C35
VSS	VSS	VSS	C4
VSS	VSS	VSS	D10
VSS	VSS	VSS	D11
VSS	VSS	VSS	D15
VSS	VSS	VSS	D16
VSS	VSS	VSS	D18
VSS	VSS	VSS	D23
VSS	VSS	VSS	D25
VSS	VSS	VSS	D26
VSS	VSS	VSS	D28
VSS	VSS	VSS	D3
VSS	VSS	VSS	D30
VSS	VSS	VSS	D31
VSS	VSS	VSS	D32
VSS	VSS	VSS	D4
VSS	VSS	VSS	D6
VSS	VSS	VSS	D7
VSS	VSS	VSS	D8
VSS	VSS	VSS	D9
VSS	VSS	VSS	E1
VSS	VSS	VSS	E10
VSS	VSS	VSS	E17
VSS	VSS	VSS	E18
VSS	VSS	VSS	E2
VSS	VSS	VSS	E23
VSS	VSS	VSS	E26
VSS	VSS	VSS	E29
VSS	VSS	VSS	E4
VSS	VSS	VSS	E6
VSS	VSS	VSS	E8
VSS	VSS	VSS	F10
VSS	VSS	VSS	F16
VSS	VSS	VSS	F18
VSS	VSS	VSS	F2
VSS	VSS	VSS	F23
VSS	VSS	VSS	F25
VSS	VSS	VSS	F29
VSS	VSS	VSS	F30
VSS	VSS	VSS	F32
VSS	VSS	VSS	F35
VSS	VSS	VSS	F4
VSS	VSS	VSS	F5

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	F6
VSS	VSS	VSS	F8
VSS	VSS	VSS	G10
VSS	VSS	VSS	G11
VSS	VSS	VSS	G13
VSS	VSS	VSS	G15
VSS	VSS	VSS	G17
VSS	VSS	VSS	G19
VSS	VSS	VSS	G2
VSS	VSS	VSS	G20
VSS	VSS	VSS	G23
VSS	VSS	VSS	G26
VSS	VSS	VSS	G27
VSS	VSS	VSS	G28
VSS	VSS	VSS	G4
VSS	VSS	VSS	G7
VSS	VSS	VSS	G8
VSS	VSS	VSS	G9
VSS	VSS	VSS	H10
VSS	VSS	VSS	H13
VSS	VSS	VSS	H2
VSS	VSS	VSS	H21
VSS	VSS	VSS	H24
VSS	VSS	VSS	H25
VSS	VSS	VSS	H27
VSS	VSS	VSS	H30
VSS	VSS	VSS	H32
VSS	VSS	VSS	H34
VSS	VSS	VSS	H4
VSS	VSS	VSS	H5
VSS	VSS	VSS	H6
VSS	VSS	VSS	H9
VSS	VSS	VSS	J10
VSS	VSS	VSS	J15
VSS	VSS	VSS	J16
VSS	VSS	VSS	J17
VSS	VSS	VSS	J18
VSS	VSS	VSS	J2
VSS	VSS	VSS	J20
VSS	VSS	VSS	J23
VSS	VSS	VSS	J30
VSS	VSS	VSS	J4
VSS	VSS	VSS	J7

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	J8
VSS	VSS	VSS	J9
VSS	VSS	VSS	K10
VSS	VSS	VSS	K11
VSS	VSS	VSS	K14
VSS	VSS	VSS	K2
VSS	VSS	VSS	K20
VSS	VSS	VSS	K24
VSS	VSS	VSS	K26
VSS	VSS	VSS	K28
VSS	VSS	VSS	K31
VSS	VSS	VSS	K32
VSS	VSS	VSS	K35
VSS	VSS	VSS	K4
VSS	VSS	VSS	K5
VSS	VSS	VSS	K6
VSS	VSS	VSS	K9
VSS	VSS	VSS	L11
VSS	VSS	VSS	L13
VSS	VSS	VSS	L15
VSS	VSS	VSS	L16
VSS	VSS	VSS	L17
VSS	VSS	VSS	L18
VSS	VSS	VSS	L2
VSS	VSS	VSS	L20
VSS	VSS	VSS	L21
VSS	VSS	VSS	L22
VSS	VSS	VSS	L24
VSS	VSS	VSS	L27
VSS	VSS	VSS	L30
VSS	VSS	VSS	L32
VSS	VSS	VSS	L4
VSS	VSS	VSS	L7
VSS	VSS	VSS	L8
VSS	VSS	VSS	L9
VSS	VSS	VSS	M10
VSS	VSS	VSS	M11
VSS	VSS	VSS	M17
VSS	VSS	VSS	M2
VSS	VSS	VSS	M20
VSS	VSS	VSS	M24
VSS	VSS	VSS	M25
VSS	VSS	VSS	M27

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	M29
VSS	VSS	VSS	M34
VSS	VSS	VSS	M4
VSS	VSS	VSS	M5
VSS	VSS	VSS	M6
VSS	VSS	VSS	M9
VSS	VSS	VSS	N10
VSS	VSS	VSS	N11
VSS	VSS	VSS	N17
VSS	VSS	VSS	N19
VSS	VSS	VSS	N2
VSS	VSS	VSS	N25
VSS	VSS	VSS	N28
VSS	VSS	VSS	N30
VSS	VSS	VSS	N32
VSS	VSS	VSS	N4
VSS	VSS	VSS	N7
VSS	VSS	VSS	N8
VSS	VSS	VSS	N9
VSS	VSS	VSS	P11
VSS	VSS	VSS	P16
VSS	VSS	VSS	P18
VSS	VSS	VSS	P2
VSS	VSS	VSS	P20
VSS	VSS	VSS	P25
VSS	VSS	VSS	P27
VSS	VSS	VSS	P29
VSS	VSS	VSS	P31
VSS	VSS	VSS	P32
VSS	VSS	VSS	P35
VSS	VSS	VSS	P4
VSS	VSS	VSS	P5
VSS	VSS	VSS	P6
VSS	VSS	VSS	P9
VSS	VSS	VSS	R11
VSS	VSS	VSS	R17
VSS	VSS	VSS	R19
VSS	VSS	VSS	R2
VSS	VSS	VSS	R21
VSS	VSS	VSS	R25
VSS	VSS	VSS	R26
VSS	VSS	VSS	R27
VSS	VSS	VSS	R4

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	R7
VSS	VSS	VSS	R8
VSS	VSS	VSS	R9
VSS	VSS	VSS	T10
VSS	VSS	VSS	T11
VSS	VSS	VSS	T18
VSS	VSS	VSS	T2
VSS	VSS	VSS	T22
VSS	VSS	VSS	T25
VSS	VSS	VSS	T28
VSS	VSS	VSS	T30
VSS	VSS	VSS	T32
VSS	VSS	VSS	T34
VSS	VSS	VSS	T4
VSS	VSS	VSS	T5
VSS	VSS	VSS	T6
VSS	VSS	VSS	T7
VSS	VSS	VSS	U11
VSS	VSS	VSS	U15
VSS	VSS	VSS	U17
VSS	VSS	VSS	U19
VSS	VSS	VSS	U2
VSS	VSS	VSS	U21
VSS	VSS	VSS	U23
VSS	VSS	VSS	U25
VSS	VSS	VSS	U27
VSS	VSS	VSS	U29
VSS	VSS	VSS	U31
VSS	VSS	VSS	U32
VSS	VSS	VSS	U4
VSS	VSS	VSS	U7
VSS	VSS	VSS	U8
VSS	VSS	VSS	U9
VSS	VSS	VSS	V1
VSS	VSS	VSS	V11
VSS	VSS	VSS	V16
VSS	VSS	VSS	V18
VSS	VSS	VSS	V2
VSS	VSS	VSS	V20
VSS	VSS	VSS	V22
VSS	VSS	VSS	V25
VSS	VSS	VSS	V26
VSS	VSS	VSS	V27

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VSS	VSS	VSS	V35
VSS	VSS	VSS	V4
VSS	VSS	VSS	V6
VSS	VSS	VSS	V9
VSS	VSS	VSS	W11
VSS	VSS	VSS	W15
VSS	VSS	VSS	W17
VSS	VSS	VSS	W19
VSS	VSS	VSS	W21
VSS	VSS	VSS	W23
VSS	VSS	VSS	W25
VSS	VSS	VSS	W28
VSS	VSS	VSS	W30
VSS	VSS	VSS	W32
VSS	VSS	VSS	Y11
VSS	VSS	VSS	Y18
VSS	VSS	VSS	Y22
VSS	VSS	VSS	Y25
VSS	VSS	VSS	Y27
VSS	VSS	VSS	Y29
VSS	VSS	VSS	Y31
VSS	VSS	VSS	Y32
VSS	VSS	VSS	Y34
RSV	VSSA_DAC	VSSA_DAC	F13
RSV	VSYNC	VSYNC	D12
VTT	VTT	VTT	A19
VTT	VTT	VTT	A20
VTT	VTT	VTT	A21
VTT	VTT	VTT	A22
VTT	VTT	VTT	B19
VTT	VTT	VTT	B20
VTT	VTT	VTT	B21
VTT	VTT	VTT	B22
VTT	VTT	VTT	C19
VTT	VTT	VTT	C20
VTT	VTT	VTT	C21
VTT	VTT	VTT	C22
VTT	VTT	VTT	D19
VTT	VTT	VTT	D20
VTT	VTT	VTT	D21
VTT	VTT	VTT	D22
VTT	VTT	VTT	E19
VTT	VTT	VTT	E20

Table 14-2. GMCH/MCH Ballout for DDR2 Systems (Sorted by Signal Name)

Intel® 82915P MCH [1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Ball #
VTT	VTT	VTT	E21
VTT	VTT	VTT	E22
VTT	VTT	VTT	F20
VTT	VTT	VTT	F21
VTT	VTT	VTT	F22
VTT	VTT	VTT	G21
VTT	VTT	VTT	G22
VTT	VTT	VTT	H22

NOTES:
1. DDR2, PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
2. DDR2, PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
3. DDR2, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO

14.2 DDR Ballout

Figure 14-4, Figure 14-5, and Figure 14-6 show the 82915G GMCH ballout for platforms using DDR system memory, as viewed from the top side of the package. Figure 14-4 shows columns 1–12; Figure 14-5 shows columns 13–24; Figure 14-6 shows columns 25–35.

The complete DDR ballout for both the 82915G/82915GV/82915GL GMCH and 82915P/82915PL MCH are listed in Table 2-1and Table 14-4
is sorted by ball number. Table 14-4 is sorted alphabetically by signal name based on the signal names of the 82915G GMCH. Note that the first table has more entries than the second table. The second table does not include unpopulated balls whereas the first table does.

Note: Balls that are listed as RSV are Reserved. Board traces should **Not** be routed to these balls.

Note: Balls that are listed as NC are No Connects. Board traces to these balls are permitted as specified.

Figure 14-4. Intel® 82915G GMCH Ballout for DDR (Top View: Columns 1–12)

	1	2	3	4	5	6	7	8	9	10	11	12
A		NC	VSS		VSS	EXP_TXN3	EXP_TXP3	EXP_TXN1	EXP_TXP1	VSS	GCLKP	VCCA_DPLLA
B	NC	VSS	EXP_RXP4	EXP_RXN4	VSS	VSS	VSS	VSS	VSS	VSS	GCLKN	VSS
C	VSS	EXP_TXP5	VSS	VSS	EXP_TXN4	EXP_TXP4	EXP_TXN2	EXP_TXP2	EXP_TXN0	EXP_TXP0	VSS	
D		EXP_TXN5	VSS	VSS	EXP_RXP5	VSS	VSS	VSS	VSS	VSS	VSS	VSYNC
E	VSS	VSS	EXP_TXP6	VSS	EXP_RXN5	VSS	EXP_RXN3	VSS	EXP_RXN2	VSS	EXP_RXP0	HSYNC
F	EXP_TXP7	VSS	EXP_TXN6	VSS	VSS	VSS	EXP_RXP3	VSS	EXP_RXP2	VSS	EXP_RXN0	NC
G	EXP_TXN7	VSS	EXP_TXP8	VSS	EXP_RXN6	EXP_RXP6	VSS	VSS	VSS	VSS	VSS	NC
H	EXP_TXP9	VSS	EXP_TXN8	VSS	VSS	VSS	EXP_RXN7	EXP_RXP7	VSS	VSS	EXP_RXN1	NC
J	EXP_TXN9	VSS	EXP_TXP10	VSS	EXP_RXN8	EXP_RXP8	VSS	VSS	VSS	VSS	EXP_RXP1	NC
K	EXP_TXP11	VSS	EXP_TXN10	VSS	VSS	VSS	EXP_RXN9	EXP_RXP9	VSS	VSS	VSS	NC
L	EXP_TXN11	VSS	EXP_TXP12	VSS	EXP_RXN10	EXP_RXP10	VSS	VSS	VSS	VCC	VSS	NC
M	EXP_TXP13	VSS	EXP_TXN12	VSS	VSS	VSS	EXP_RXN12	EXP_RXP12	VSS	VSS	VSS	DREF_CLKN
N	EXP_TXN13	VSS	EXP_TXP14	VSS	EXP_RXN13	EXP_RXP13	VSS	VSS	VSS	VSS	VSS	NC
P	EXP_TXP15	VSS	EXP_TXN14	VSS	VSS	VSS	EXP_RXP14	EXP_RXN14	VSS	EXP_RXP11	VSS	NC
R	EXP_TXN15	VSS	DMI_TXP0	VSS	EXP_RXN15	EXP_RXP15	VSS	VSS	VSS	EXP_RXN11	VSS	NC
T	DMI_TXP1	VSS	DMI_TXN0	VSS	VSS	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	VSS	NC
U	DMI_TXN1	VSS	DMI_TXP2	VSS	DMI_RXP0	DMI_RXN0	VSS	VSS	VSS	DMI_RXN3	VSS	NC
V	VSS	VSS	DMI_TXN2	VSS	DMI_TXP3	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXP3	VSS	NC
W	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	DMI_TXN3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPI	VSS	NC
Y	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPO	VSS	NC
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	NC
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSV
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B20
AE	SDQ_A5	SDQ_A4	SDQ_A0	VSS	RSV	VSS	SMVREF0	SMVREF1	VSS	SM_SLEWOUT1	SDQ_B11	VSS
AF	VSS	SDM_A0	SDQ_A1	VSS	RSV	VSS	RSTIN#	VSS	SM_SLEWIN1	VSS	SDQ_B10	VSS
AG	SDQS_A0	RSV	SDQ_A6	SRCOMP0	VSS	NC	PWROK	SRCOMP1	SDQ_B4	SDQ_B14	SDQ_B15	VSS
AH	VSS	SDQ_A2	SDQ_A7	SDQ_B5	VSS	VSS	SDQ_B0	VSS	SDM_B1	RSV	VSS	SDQ_B21
AJ	SDQ_A8	SDQ_A3	SDQ_A12	VSS	SDM_B0	SDQ_B1	SDQ_B8	SDQ_B12	VSS	VSS	SCLK_B1#	SM_SLEWIN0
AK	VSS	SDQ_A9	SDQ_A13	VSS	SDQS_B0	VSS	VSS	VSS	SCLK_B4	SDQS_B1	VSS	SM_SLEWOUT0
AL	SDM_A1	RSV	SDQS_A1	RSV	SDQ_B2	SDQ_B7	SDQ_B9	SDQ_B13	SCLK_B4#	VSS	SCLK_B1	SCKE_A0
AM		SCLK_A4	SCLK_A4#	VSS	SDQ_B6	VSS	VSS	VSS	SCKE_B1	VCCSM	VCCSM	SMA_B12
AN	VSS	SCLK_A1	SCLK_A1#	SDQ_A10	SDQ_A20	SDQ_B3	SDM_A2	SDQ_A18	SDQ_A23	SCKE_B0	SCKE_A1	
AP	NC	SDQ_A14	SDQ_A15	SDQ_A11	SDQ_A16	SDQ_A21	SDQS_A2	VSS	SDQ_A19	SCKE_B2	SCKE_A2	VCCSM
AR	NC	NC	VSS		SDQ_A17	VSS	RSV	SDQ_A22	SCKE_B3	VCCSM	SCKE_A3	SMA_B11
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 14-5. Intel® 82915G GMCH Ballout for DDR (Top View: Columns 13–24)

	13	14	15	16	17	18	19	20	21	22	23	24
A	VCC2	VCCA_EXPPLL	REFSET	EXP_SLR	VCCA_HPLL	VSS	VTT	VTT	VTT	VTT	HSWING	HVREF
B	VCCA_DPLLB	VSS	RSV	VSS	VCCA_SMPLL	VSS	VTT	VTT	VTT	VTT	HRCOMP	VSS
C	VSS	RSV	MTYPE	NC	VSS	VSS	VTT	VTT	VTT	VTT	VSS	
D	VCCA_DAC	GREEN	VSS	VSS	BSEL2	VSS	VTT	VTT	VTT	VTT	VSS	HSCOMP
E	VCCA_DAC	GREEN#	BSEL1	NC	VSS	VSS	VTT	VTT	VTT	VTT	VSS	HD62
F	VSSA_DAC	RED	RSV	VSS	HD47	VSS	HDSTBN2#	VTT	VTT	VTT	VSS	NC
G	VSS	RED#	VSS	RSV	VSS	HD45	VSS	VSS	VTT	VTT	VSS	HCPURST#
H	VSS	BLUE	NC	BSEL0	NC	HD46	HD41	HD40	VSS	VTT	HD37	VSS
J	SDVO_CTRLCLK	BLUE#	VSS	VSS	VSS	VSS	HDSTBP2#	VSS	HD35	HD32	VSS	HD33
K	SDVO_CTRLDATA	VSS	RSV	EXTTS#	HD44	HD43	HDINV2#	VSS	HD39	HD34	HD31	VSS
L	VSS	DDC_DATA	VSS	VSS	VSS	VSS	NC	VSS	VSS	VSS	HD30	VSS
M	DREFCLKP	ICH_SYNC#	DDC_CLK	RSV	VSS	HD42	HD38	VSS	HD36	HCLKN	HCLKP	VSS
N	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VCC	NC	NC	NC
P	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	NC	NC
R	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	NC
T	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VSS	VCC	VCC
U	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC
V	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC
W	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC
Y	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VCC	VCC	VSS	VCC	VCC
AA	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC	VCC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC
AC	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	NC	NC
AD	VSS	SDQ_B19	SDQ_B23	VSS	SDQ_A26	SDQ_B24	VSS	SDQS_B3	SDQ_B31	VSS	SDQ_B36	SDM_B6
AE	SDQ_B16	VSS	VSS	RSV_TP0	VSS	VSS	SDQ_A30	VSS	VSS	SDQ_B26	VSS	VSS
AF	SDQ_B17	SDQ_B22	VSS	SDQ_A28	SDQS_A3	VSS	SDQ_A27	RSV	VSS	SDQ_B30	SDQ_B32	SDQ_B37
AG	VSS	SDQ_B18	VSS	VSS	RSV	VSS	VSS	SDM_B3	VSS	VSS	SCLK_B0#	SDM_B4
AH	SDM_B2	VSS	RSV_TP1	SDM_A3	VSS	SDQ_A31	SDQ_B29	VSS	SDQ_B27	SCLK_B0	VSS	NC
AJ	VSS	NC	VSS	VSS	SDQ_A29	RSV	VSS	RSV	RSV	VSS	RSV	RSV
AK	SDQS_B2	VSS	RSV_TP3	SDQ_A24	VSS	RSV	SDQ_B25	VSS	RSV	SCLK_B3#	VSS	RSV
AL	VSS	RSV	SMA_B7	VSS	SDQ_A25	SDQ_B28	VSS	RSV	RSV	VSS	SCLK_B3	RSV
AM	VCCSM	VCCSM	SMA_A9	VCCSM	VCCSM	SMA_B0	VCCSM	VCCSM	SMA_A4	VCCSM	VCCSM	SCLK_A0
AN	SMA_B9	RSV_TP2	SMA_B5	SMA_A7	SMA_B2	SMA_A8	NC	SMA_B10	SMA_A2	SMA_A0	SMA_A10	
AP	SMA_A12	SMA_B8	SMA_A11	VCCSM	SMA_B6	SMA_B1	SMA_A5	VCCSM	SMA_A3	SMA_A1	RSV	VCCSM
AR	VSS	VCCSM	SMA_B4	SMA_B3	VSS	VCCSM	SBS_B1	SMA_A6	VSS	VCCSM	RSV	RSV
	13	14	15	16	17	18	19	20	21	22	23	24

Figure 14-6. Intel® 82915G GMCH Ballout for DDR (Top View: Columns 25–35)

25	26	27	28	29	30	31	32	33	34	35	
HD48	VSS	HD61	HD57	HD55	VSS	HD53		VSS	NC	NC	A
HD63	HDINV3#	HD54	VSS	HDSTBP3#	HD51	HD52	HD15	HD13	HD11	NC	B
HD58	HD59	HD49	HD56	HDSTBN3#	HD17	HD50	HD14	HD9	HD12	VSS	C
VSS	VSS	HD60	VSS	HD18	VSS	VSS	VSS	HD10	HD8		D
HD25	VSS	HD24	HD16	VSS	HBPRI#	HPCREQ#	HREQ1#	HDSTBP0#	HDINV0#	HDSTBN0#	E
VSS	HDSTBN1#	HD23	HD22	VSS	VSS	HREQ4#	VSS	HREQ0#	HD6	VSS	F
HD26	VSS	VSS	VSS	HD20	HA6#	HREQ3#	HA7#	HD7	HD5	HD3	G
VSS	HDSTBP1#	VSS	HD19	HA3#	VSS	HREQ2#	VSS	HD1	VSS	HD4	H
HD27	HDINV1#	HD21	HA13#	HA5#	VSS	HADSTB0#	HRS2#	HD0	HD2	HDEFER#	J
HD28	VSS	HA14#	VSS	HA4#	HA8#	VSS	VSS	HA15#	HRS0#	VSS	K
HD29	HA18#	VSS	HA12#	HA9#	VSS	HA11#	VSS	HLOCK#	HHIT#	HDBSY#	L
VSS	HA20#	VSS	HA16#	VSS	HA10#	HADS#	HDRDY#		VSS	HBNR#	M
VSS	HA19#	HADSTB1#	VSS	HA23#	VSS	HA21#	VSS	HA26#	HTRDY#	HHITM#	N
VSS	HA22#	VSS	HA24#	VSS	NC	VSS	VSS	HEDRDY#	HRS1#	VSS	P
VSS	VSS	VSS	HA25#	HA17#	RSV	RSV	SDQ_A58	HBREQ0#	SDQ_A59	RSV	R
VSS	HA30#	HA27#	VSS	HA31#	VSS	HA28#	VSS	SDQ_A62	VSS	SDQ_A63	T
VSS	SDQ_B58	VSS	HA29#	VSS	RSV	VSS	VSS	SDM_A7	SDQS_A7	RSV	U
VSS	VSS	VSS	SDQ_B63	SDQ_B59	RSV	RSV	RSV	SDQ_A57	SDQ_A56	VSS	V
VSS	SDQ_B62	SDQS_B7	VSS	SDQ_B57	VSS	SDM_B7	VSS	SDQ_A61	SDQ_A51	SDQ_A60	W
VSS	SDQ_B60	VSS	RSV	VSS	RSV	VSS	VSS	SDQ_A50	VSS	SDQ_A55	Y
VSS	VSS	VSS	SDQ_B61	SDQ_B56	RSV	RSV	SDQ_A54	SDM_A6	SDQS_A6	RSV	AA
VSS	SDQ_B51	SDQ_B50	VSS	RSV	VSS	SDQS_B6	VSS	SMA_A13	SCLK_A2	VSS	AB
VSS	SDQ_B55	VSS	SDQ_B54	VSS	RSV	VSS	VSS	SCLK_A2#	SCLK_A5#	SCLK_A5	AC
VSS	VSS	VSS	SCLK_B5#	SCLK_B5	NC	SDQ_A52	SMA_B13		VSS	SDQ_A53	AD
SCLK_B2#	SCLK_B2	SDQ_B53	VSS	SDQ_B52	VSS	SDQ_B48	VSS	SDQ_A47	SDQ_A49	SDQ_A48	AE
SDQ_B33	VSS	SDQ_B49	SDQ_B47	VSS	VSS	VSS	VSS	SDQ_A46	SDQ_A43	VSS	AF
VSS	RSV	SDQ_B46	VSS	VSS	SDQ_B42	SDQ_B43	SDQ_A42	RSV	SDM_A5	SDQS_A5	AG
SDQS_B4	VSS	SDQ_A32	SDQS_B5	VSS	RSV	SDM_B5	VSS	SDQ_A45	VSS	SDQ_A41	AH
SDQ_B38	SDQ_B35	VSS	SDQ_A37	SDQ_B40	VSS	SDQ_B41	VSS	SDQ_A44	SDQ_A40	VSS	AJ
VSS	VSS	SDQ_A33	VSS	SDM_A4	VSS	SDQ_A35	SDQ_B45	SDQ_B44	SCS_A2#	VCCSM	AK
SDQ_B34	SDQ_B39	SDQ_A36	NC	RSV	SDQ_A38	SDQ_A39	VSS	SCS_A3#	SCAS_A#	SCS_A1#	AL
VCCSM	VCCSM	SBS_B0	VCCSM	VSS	SDQS_A4	VSS	VCCSM	SCS_B3#	SCS_A0#		AM
SCLK_A0#	SCLK_A3#	SCAS_B#	SBS_A0	SRAS_A#	SDQ_A34	RSV	RSV	SCS_B2#	SCS_B1#	VCCSM	AN
SCLK_A3	SBS_A1	SRAS_B#	VCCSM	RSV	RSV	SWE_A#	RSV	RSV	SCS_B0#	NC	AP
VSS	VCCSM	SWE_B#	RSV	RSV	VSS	VCCSM		VCCSM	NC	NC	AR
25	26	27	28	29	30	31	32	33	34	35	

Table 14-3. GMCH/MCH Ballout for DDR Systems (Sorted by Ball Number)

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Intel® 82910GL GMCH [4]
A1	—	—	—	—	—	—
A2	NC	NC	NC	NC	NC	NC
A3	VSS	VSS	VSS	VSS	VSS	VSS
A4	—	—	—	—	—	—
A5	VSS	VSS	VSS	VSS	VSS	VSS
A6	SDVOB_CLK-	EXP_TXN3	EXP_TXN3	EXP_TXN3	SDVOB_CLK-	SDVOB_CLK-
A7	SDVOB_CLK+	EXP_TXP3	EXP_TXP3	EXP_TXP3	SDVOB_CLK+	SDVOB_CLK+
A8	SDVOB_GREEN-	EXP_TXN1	EXP_TXN1	EXP_TXN1	SDVOB_GREEN-	SDVOB_GREEN-
A9	SDVOB_GREEN+	EXP_TXP1	EXP_TXP1	EXP_TXP1	SDVOB_GREEN+	SDVOB_GREEN+
A10	VSS	VSS	VSS	VSS	VSS	VSS
A11	GCLKP	GCLKP	GCLKP	GCLKP	GCLKP	GCLKP
A12	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA
A13	VCC2	VCC2	VCC2	VCC2	VCC2	VCC2
A14	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL
A15	REFSET	RSV	RSV	REFSET	REFSET	REFSET
A16	RSV	EXP_SLR	EXP_SLR	EXP_SLR	RSV	RSV
A17	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL
A18	VSS	VSS	VSS	VSS	VSS	VSS
A19	VTT	VTT	VTT	VTT	VTT	VTT
A20	VTT	VTT	VTT	VTT	VTT	VTT
A21	VTT	VTT	VTT	VTT	VTT	VTT
A22	VTT	VTT	VTT	VTT	VTT	VTT
A23	HSWING	HSWING	HSWING	HSWING	HSWING	HSWING
A24	HVREF	HVREF	HVREF	HVREF	HVREF	HVREF
A25	HD48	HD48	HD48	HD48	HD48	HD48
A26	VSS	VSS	VSS	VSS	VSS	VSS
A27	HD61	HD61	HD61	HD61	HD61	HD61
A28	HD57	HD57	HD57	HD57	HD57	HD57
A29	HD55	HD55	HD55	HD55	HD55	HD55
A30	VSS	VSS	VSS	VSS	VSS	VSS
A31	HD53	HD53	HD53	HD53	HD53	HD53
A32	—	—	—	—	—	—
A33	VSS	VSS	VSS	VSS	VSS	VSS
A34	NC	NC	NC	NC	NC	NC

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
A35	NC	NC	NC	NC	NC	NC
B1	NC	NC	NC	NC	NC	NC
B2	VSS	VSS	VSS	VSS	VSS	VSS
B3	RSV	EXP_RXP4	EXP_RXP4	EXP_RXP4	RSV	RSV
B4	RSV	EXP_RXN4	EXP_RXN4	EXP_RXN4	RSV	RSV
B5	VSS	VSS	VSS	VSS	VSS	VSS
B6	VSS	VSS	VSS	VSS	VSS	VSS
B7	VSS	VSS	VSS	VSS	VSS	VSS
B8	VSS	VSS	VSS	VSS	VSS	VSS
B9	VSS	VSS	VSS	VSS	VSS	VSS
B10	VSS	VSS	VSS	VSS	VSS	VSS
B11	GCLKN	GCLKN	GCLKN	GCLKN	GCLKN	GCLKN
B12	VSS	VSS	VSS	VSS	VSS	VSS
B13	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB
B14	VSS	VSS	VSS	VSS	VSS	VSS
B15	RSV	RSV	RSV	RSV	RSV	RSV
B16	VSS	VSS	VSS	VSS	VSS	VSS
B17	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL
B18	VSS	VSS	VSS	VSS	VSS	VSS
B19	VTT	VTT	VTT	VTT	VTT	VTT
B20	VTT	VTT	VTT	VTT	VTT	VTT
B21	VTT	VTT	VTT	VTT	VTT	VTT
B22	VTT	VTT	VTT	VTT	VTT	VTT
B23	HRCOMP	HRCOMP	HRCOMP	HRCOMP	HRCOMP	HRCOMP
B24	VSS	VSS	VSS	VSS	VSS	VSS
B25	HD63	HD63	HD63	HD63	HD63	HD63
B26	HDINV3#	HDINV3#	HDINV3#	HDINV3#	HDINV3#	HDINV3#
B27	HD54	HD54	HD54	HD54	HD54	HD54
B28	VSS	VSS	VSS	VSS	VSS	VSS
B29	HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#
B30	HD51	HD51	HD51	HD51	HD51	HD51
B31	HD52	HD52	HD52	HD52	HD52	HD52
B32	HD15	HD15	HD15	HD15	HD15	HD15
B33	HD13	HD13	HD13	HD13	HD13	HD13
B34	HD11	HD11	HD11	HD11	HD11	HD11
B35	NC	NC	NC	NC	NC	NC
C1	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Intel® 82910GL GMCH [4]
C2	SDVOC_GREEN+	EXP_TXP5	EXP_TXP5	EXP_TXP5	SDVOC_GREEN+	SDVOC_GREEN+
C3	VSS	VSS	VSS	VSS	VSS	VSS
C4	VSS	VSS	VSS	VSS	VSS	VSS
C5	SDVOC_RED-/ SDVOB_ALPHA-	EXP_TXN4	EXP_TXN4	EXP_TXN4	SDVOC_RED-/ SDVOB_ALPHA-	SDVOC_RED-/ SDVOB_ALPHA-
C6	SDVOC_RED+/ SDVOB_ALPHA+	EXP_TXP4	EXP_TXP4	EXP_TXP4	SDVOC_RED+/ SDVOB_ALPHA+	SDVOC_RED+/ SDVOB_ALPHA+
C7	SDVOB_BLUE-	EXP_TXN2	EXP_TXN2	EXP_TXN2	SDVOB_BLUE-	SDVOB_BLUE-
C8	SDVOB_BLUE+	EXP_TXP2	EXP_TXP2	EXP_TXP2	SDVOB_BLUE+	SDVOB_BLUE+
C9	SDVOB_RED-	EXP_TXN0	EXP_TXN0	EXP_TXN0	SDVOB_RED-	SDVOB_RED-
C10	SDVOB_RED+	EXP_TXP0	EXP_TXP0	EXP_TXP0	SDVOB_RED+	SDVOB_RED+
C11	VSS	VSS	VSS	VSS	VSS	VSS
C12	—	—	—	—	—	—
C13	VSS	VSS	VSS	VSS	VSS	VSS
C14	RSV	RSV	RSV	RSV	RSV	RSV
C15	MTYPE	MTYPE	MTYPE	MTYPE	MTYPE	MTYPE
C16	NC	NC	NC	NC	NC	NC
C17	VSS	VSS	VSS	VSS	VSS	VSS
C18	VSS	VSS	VSS	VSS	VSS	VSS
C19	VTT	VTT	VTT	VTT	VTT	VTT
C20	VTT	VTT	VTT	VTT	VTT	VTT
C21	VTT	VTT	VTT	VTT	VTT	VTT
C22	VTT	VTT	VTT	VTT	VTT	VTT
C23	VSS	VSS	VSS	VSS	VSS	VSS
C24	—	—	—	—	—	—
C25	HD58	HD58	HD58	HD58	HD58	HD58
C26	HD59	HD59	HD59	HD59	HD59	HD59
C27	HD49	HD49	HD49	HD49	HD49	HD49
C28	HD56	HD56	HD56	HD56	HD56	HD56
C29	HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#
C30	HD17	HD17	HD17	HD17	HD17	HD17
C31	HD50	HD50	HD50	HD50	HD50	HD50
C32	HD14	HD14	HD14	HD14	HD14	HD14
C33	HD9	HD9	HD9	HD9	HD9	HD9

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
C34	HD12	HD12	HD12	HD12	HD12	HD12
C35	VSS	VSS	VSS	VSS	VSS	VSS
D1	—	—	—	—	—	—
D2	SDVOC_GREEN-	EXP_TXN5	EXP_TXN5	EXP_TXN5	SDVOC_GREEN-	SDVOC_GREEN-
D3	VSS	VSS	VSS	VSS	VSS	VSS
D4	VSS	VSS	VSS	VSS	VSS	VSS
D5	SDVOC_INT+	EXP_RXP5	EXP_RXP5	EXP_RXP5	SDVOC_INT+	SDVOC_INT+
D6	VSS	VSS	VSS	VSS	VSS	VSS
D7	VSS	VSS	VSS	VSS	VSS	VSS
D8	VSS	VSS	VSS	VSS	VSS	VSS
D9	VSS	VSS	VSS	VSS	VSS	VSS
D10	VSS	VSS	VSS	VSS	VSS	VSS
D11	VSS	VSS	VSS	VSS	VSS	VSS
D12	VSYNC	RSV	RSV	VSYNC	VSYNC	VSYNC
D13	VCCA_DAC	RSV	RSV	VCCA_DAC	VCCA_DAC	VCCA_DAC
D14	GREEN	RSV	RSV	GREEN	GREEN	GREEN
D15	VSS	VSS	VSS	VSS	VSS	VSS
D16	VSS	VSS	VSS	VSS	VSS	VSS
D17	BSEL2	BSEL2	BSEL2	BSEL2	BSEL2	BSEL2
D18	VSS	VSS	VSS	VSS	VSS	VSS
D19	VTT	VTT	VTT	VTT	VTT	VTT
D20	VTT	VTT	VTT	VTT	VTT	VTT
D21	VTT	VTT	VTT	VTT	VTT	VTT
D22	VTT	VTT	VTT	VTT	VTT	VTT
D23	VSS	VSS	VSS	VSS	VSS	VSS
D24	HSCOMP	HSCOMP	HSCOMP	HSCOMP	HSCOMP	HSCOMP
D25	VSS	VSS	VSS	VSS	VSS	VSS
D26	VSS	VSS	VSS	VSS	VSS	VSS
D27	HD60	HD60	HD60	HD60	HD60	HD60
D28	VSS	VSS	VSS	VSS	VSS	VSS
D29	HD18	HD18	HD18	HD18	HD18	HD18
D30	VSS	VSS	VSS	VSS	VSS	VSS
D31	VSS	VSS	VSS	VSS	VSS	VSS
D32	VSS	VSS	VSS	VSS	VSS	VSS
D33	HD10	HD10	HD10	HD10	HD10	HD10
D34	HD8	HD8	HD8	HD8	HD8	HD8
D35	—	—	—	—	—	—
E1	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Intel® 82910GL GMCH [4]
E2	VSS	VSS	VSS	VSS	VSS	VSS
E3	SDVOC_BLUE+	EXP_TXP6	EXP_TXP6	EXP_TXP6	SDVOC_BLUE+	SDVOC_BLUE+
E4	VSS	VSS	VSS	VSS	VSS	VSS
E5	SDVOC_INT-	EXP_RXN5	EXP_RXN5	EXP_RXN5	SDVOC_INT-	SDVOC_INT-
E6	VSS	VSS	VSS	VSS	VSS	VSS
E7	RSV	EXP_RXN3	EXP_RXN3	EXP_RXN3	RSV	RSV
E8	VSS	VSS	VSS	VSS	VSS	VSS
E9	SDVOC_STALL-	EXP_RXN2	EXP_RXN2	EXP_RXN2	SDVOC_STALL-	SDVOC_STALL-
E10	VSS	VSS	VSS	VSS	VSS	VSS
E11	SDVOC_TVCLKIN+	EXP_RXP0	EXP_RXP0	EXP_RXP0	SDVOC_TVCLKIN+	SDVOC_TVCLKIN+
E12	HSYNC	RSV	RSV	HSYNC	HSYNC	HSYNC
E13	VCCA_DAC	RSV	RSV	VCCA_DAC	VCCA_DAC	VCCA_DAC
E14	GREEN#	RSV	RSV	GREEN#	GREEN#	GREEN#
E15	BSEL1	BSEL1	BSEL1	BSEL1	BSEL1	BSEL1
E16	NC	NC	NC	NC	NC	NC
E17	VSS	VSS	VSS	VSS	VSS	VSS
E18	VSS	VSS	VSS	VSS	VSS	VSS
E19	VTT	VTT	VTT	VTT	VTT	VTT
E20	VTT	VTT	VTT	VTT	VTT	VTT
E21	VTT	VTT	VTT	VTT	VTT	VTT
E22	VTT	VTT	VTT	VTT	VTT	VTT
E23	VSS	VSS	VSS	VSS	VSS	VSS
E24	HD62	HD62	HD62	HD62	HD62	HD62
E25	HD25	HD25	HD25	HD25	HD25	HD25
E26	VSS	VSS	VSS	VSS	VSS	VSS
E27	HD24	HD24	HD24	HD24	HD24	HD24
E28	HD16	HD16	HD16	HD16	HD16	HD16
E29	VSS	VSS	VSS	VSS	VSS	VSS
E30	HBPRI#	HBPRI#	HBPRI#	HBPRI#	HBPRI#	HBPRI#
E31	HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#
E32	HREQ1#	HREQ1#	HREQ1#	HREQ1#	HREQ1#	HREQ1#
E33	HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#
E34	HDINV0#	HDINV0#	HDINV0#	HDINV0#	HDINV0#	HDINV0#
E35	HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#
F1	EXP_TXP7	EXP_TXP7	EXP_TXP7	EXP_TXP7	EXP_TXP7	EXP_TXP7
F2	VSS	VSS	VSS	VSS	VSS	VSS
F3	SDVOC_BLUE-	EXP_TXN6	EXP_TXN6	EXP_TXN6	SDVOC_BLUE-	SDVOC_BLUE-

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Intel® 82910GL GMCH [4]
F4	VSS	VSS	VSS	VSS	VSS	VSS
F5	VSS	VSS	VSS	VSS	VSS	VSS
F6	VSS	VSS	VSS	VSS	VSS	VSS
F7	RSV	EXP_RXP3	EXP_RXP3	EXP_RXP3	RSV	RSV
F8	VSS	VSS	VSS	VSS	VSS	VSS
F9	SDVOC_STALL+	EXP_RXP2	EXP_RXP2	EXP_RXP2	SDVOC_STALL+	SDVOC_STALL+
F10	VSS	VSS	VSS	VSS	VSS	VSS
F11	SDVOC_TVCLKIN-	EXP_RXN0	EXP_RXN0	EXP_RXN0	SDVOC_TVCLKIN-	SDVOC_TVCLKIN-
F12	NC	NC	NC	NC	NC	NC
F13	VSSA_DAC	RSV	RSV	VSSA_DAC	VSSA_DAC	VSSA_DAC
F14	RED	RSV	RSV	RED	RED	RED
F15	RSV	RSV	RSV	RSV	RSV	RSV
F16	VSS	VSS	VSS	VSS	VSS	VSS
F17	HD47	HD47	HD47	HD47	HD47	HD47
F18	VSS	VSS	VSS	VSS	VSS	VSS
F19	HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#
F20	VTT	VTT	VTT	VTT	VTT	VTT
F21	VTT	VTT	VTT	VTT	VTT	VTT
F22	VTT	VTT	VTT	VTT	VTT	VTT
F23	VSS	VSS	VSS	VSS	VSS	VSS
F24	NC	NC	NC	NC	NC	NC
F25	VSS	VSS	VSS	VSS	VSS	VSS
F26	HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#
F27	HD23	HD23	HD23	HD23	HD23	HD23
F28	HD22	HD22	HD22	HD22	HD22	HD22
F29	VSS	VSS	VSS	VSS	VSS	VSS
F30	VSS	VSS	VSS	VSS	VSS	VSS
F31	HREQ4#	HREQ4#	HREQ4#	HREQ4#	HREQ4#	HREQ4#
F32	VSS	VSS	VSS	VSS	VSS	VSS
F33	HREQ0#	HREQ0#	HREQ0#	HREQ0#	HREQ0#	HREQ0#
F34	HD6	HD6	HD6	HD6	HD6	HD6
F35	VSS	VSS	VSS	VSS	VSS	VSS
G1	SDVOC_CLK-	EXP_TXN7	EXP_TXN7	EXP_TXN7	SDVOC_CLK-	SDVOC_CLK-
G2	VSS	VSS	VSS	VSS	VSS	VSS
G3	RSV	EXP_TXP8	EXP_TXP8	EXP_TXP8	RSV	RSV
G4	VSS	VSS	VSS	VSS	VSS	VSS
G5	RSV	EXP_RXN6	EXP_RXN6	EXP_RXN6	RSV	RSV

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
G6	RSV	EXP_RXP6	EXP_RXP6	EXP_RXP6	RSV	RSV
G7	VSS	VSS	VSS	VSS	VSS	VSS
G8	VSS	VSS	VSS	VSS	VSS	VSS
G9	VSS	VSS	VSS	VSS	VSS	VSS
G10	VSS	VSS	VSS	VSS	VSS	VSS
G11	VSS	VSS	VSS	VSS	VSS	VSS
G12	NC	NC	NC	NC	NC	NC
G13	VSS	VSS	VSS	VSS	VSS	VSS
G14	RED#	RSV	RSV	RED#	RED#	RED#
G15	VSS	VSS	VSS	VSS	VSS	VSS
G16	RSV	RSV	RSV	RSV	RSV	RSV
G17	VSS	VSS	VSS	VSS	VSS	VSS
G18	HD45	HD45	HD45	HD45	HD45	HD45
G19	VSS	VSS	VSS	VSS	VSS	VSS
G20	VSS	VSS	VSS	VSS	VSS	VSS
G21	VTT	VTT	VTT	VTT	VTT	VTT
G22	VTT	VTT	VTT	VTT	VTT	VTT
G23	VSS	VSS	VSS	VSS	VSS	VSS
G24	HCPURST#	HCPURST#	HCPURST#	HCPURST#	HCPURST#	HCPURST#
G25	HD26	HD26	HD26	HD26	HD26	HD26
G26	VSS	VSS	VSS	VSS	VSS	VSS
G27	VSS	VSS	VSS	VSS	VSS	VSS
G28	VSS	VSS	VSS	VSS	VSS	VSS
G29	HD20	HD20	HD20	HD20	HD20	HD20
G30	HA6#	HA6#	HA6#	HA6#	HA6#	HA6#
G31	HREQ3#	HREQ3#	HREQ3#	HREQ3#	HREQ3#	HREQ3#
G32	HA7#	HA7#	HA7#	HA7#	HA7#	HA7#
G33	HD7	HD7	HD7	HD7	HD7	HD7
G34	HD5	HD5	HD5	HD5	HD5	HD5
G35	HD3	HD3	HD3	HD3	HD3	HD3
H1	RSV	EXP_TXP9	EXP_TXP9	EXP_TXP9	RSV	RSV
H2	VSS	VSS	VSS	VSS	VSS	VSS
H3	RSV	EXP_TXN8	EXP_TXN8	EXP_TXN8	RSV	RSV
H4	VSS	VSS	VSS	VSS	VSS	VSS
H5	VSS	VSS	VSS	VSS	VSS	VSS
H6	VSS	VSS	VSS	VSS	VSS	VSS
H7	RSV	EXP_RXN7	EXP_RXN7	EXP_RXN7	RSV	RSV
H8	RSV	EXP_RXP7	EXP_RXP7	EXP_RXP7	RSV	RSV
H9	VSS	VSS	VSS	VSS	VSS	VSS
H10	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH [2]	Intel® 82915GV GMCH [3]	Intel® 82910GL GMCH [4]
H11	SDVOB_INT-	EXP_RXN1	EXP_RXN1	EXP_RXN1	SDVOB_INT-	SDVOB_INT-
H12	NC	NC	NC	NC	NC	NC
H13	VSS	VSS	VSS	VSS	VSS	VSS
H14	BLUE	RSV	RSV	BLUE	BLUE	BLUE
H15	NC	NC	NC	NC	NC	NC
H16	BSEL0	BSEL0	BSEL0	BSEL0	BSEL0	BSEL0
H17	NC	NC	NC	NC	NC	NC
H18	HD46	HD46	HD46	HD46	HD46	HD46
H19	HD41	HD41	HD41	HD41	HD41	HD41
H20	HD40	HD40	HD40	HD40	HD40	HD40
H21	VSS	VSS	VSS	VSS	VSS	VSS
H22	VTT	VTT	VTT	VTT	VTT	VTT
H23	HD37	HD37	HD37	HD37	HD37	HD37
H24	VSS	VSS	VSS	VSS	VSS	VSS
H25	VSS	VSS	VSS	VSS	VSS	VSS
H26	HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#
H27	VSS	VSS	VSS	VSS	VSS	VSS
H28	HD19	HD19	HD19	HD19	HD19	HD19
H29	HA3#	HA3#	HA3#	HA3#	HA3#	HA3#
H30	VSS	VSS	VSS	VSS	VSS	VSS
H31	HREQ2#	HREQ2#	HREQ2#	HREQ2#	HREQ2#	HREQ2#
H32	VSS	VSS	VSS	VSS	VSS	VSS
H33	HD1	HD1	HD1	HD1	HD1	HD1
H34	VSS	VSS	VSS	VSS	VSS	VSS
H35	HD4	HD4	HD4	HD4	HD4	HD4
J1	RSV	EXP_TXN9	EXP_TXN9	EXP_TXN9	RSV	RSV
J2	VSS	VSS	VSS	VSS	VSS	VSS
J3	RSV	EXP_TXP10	EXP_TXP10	EXP_TXP10	RSV	RSV
J4	VSS	VSS	VSS	VSS	VSS	VSS
J5	RSV	EXP_RXN8	EXP_RXN8	EXP_RXN8	RSV	RSV
J6	RSV	EXP_RXP8	EXP_RXP8	EXP_RXP8	RSV	RSV
J7	VSS	VSS	VSS	VSS	VSS	VSS
J8	VSS	VSS	VSS	VSS	VSS	VSS
J9	VSS	VSS	VSS	VSS	VSS	VSS
J10	VSS	VSS	VSS	VSS	VSS	VSS
J11	SDVOB_INT+	EXP_RXP1	EXP_RXP1	EXP_RXP1	SDVOB_INT+	SDVOB_INT+
J12	NC	NC	NC	NC	NC	NC
J13	SDVO_CTRLCLK	RSV	RSV	SDVO_CTRLCLK	SDVO_CTRLCLK	SDVO_CTRLCLK
J14	BLUE#	RSV	RSV	BLUE#	BLUE#	BLUE#

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
J15	VSS	VSS	VSS	VSS	VSS	VSS
J16	VSS	VSS	VSS	VSS	VSS	VSS
J17	VSS	VSS	VSS	VSS	VSS	VSS
J18	VSS	VSS	VSS	VSS	VSS	VSS
J19	HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#
J20	VSS	VSS	VSS	VSS	VSS	VSS
J21	HD35	HD35	HD35	HD35	HD35	HD35
J22	HD32	HD32	HD32	HD32	HD32	HD32
J23	VSS	VSS	VSS	VSS	VSS	VSS
J24	HD33	HD33	HD33	HD33	HD33	HD33
J25	HD27	HD27	HD27	HD27	HD27	HD27
J26	HDINV1#	HDINV1#	HDINV1#	HDINV1#	HDINV1#	HDINV1#
J27	HD21	HD21	HD21	HD21	HD21	HD21
J28	HA13#	HA13#	HA13#	HA13#	HA13#	HA13#
J29	HA5#	HA5#	HA5#	HA5#	HA5#	HA5#
J30	VSS	VSS	VSS	VSS	VSS	VSS
J31	HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#
J32	HRS2#	HRS2#	HRS2#	HRS2#	HRS2#	HRS2#
J33	HD0	HD0	HD0	HD0	HD0	HD0
J34	HD2	HD2	HD2	HD2	HD2	HD2
J35	HDEFER#	HDEFER#	HDEFER#	HDEFER#	HDEFER#	HDEFER#
K1	RSV	EXP_TXP11	EXP_TXP11	EXP_TXP11	RSV	RSV
K2	VSS	VSS	VSS	VSS	VSS	VSS
K3	RSV	EXP_TXN10	EXP_TXN10	EXP_TXN10	RSV	RSV
K4	VSS	VSS	VSS	VSS	VSS	VSS
K5	VSS	VSS	VSS	VSS	VSS	VSS
K6	VSS	VSS	VSS	VSS	VSS	VSS
K7	RSV	EXP_RXN9	EXP_RXN9	EXP_RXN9	RSV	RSV
K8	RSV	EXP_RXP9	EXP_RXP9	EXP_RXP9	RSV	RSV
K9	VSS	VSS	VSS	VSS	VSS	VSS
K10	VSS	VSS	VSS	VSS	VSS	VSS
K11	VSS	VSS	VSS	VSS	VSS	VSS
K12	NC	NC	NC	NC	NC	NC
K13	SDVO_CTRL DATA	RSV	RSV	SDVO_CTRLDATA	SDVO_CTRLDA TA	SDVO_CTRLDATA
K14	VSS	VSS	VSS	VSS	VSS	VSS
K15	RSV	RSV	RSV	RSV	RSV	RSV
K16	EXTTS#	EXTTS#	EXTTS#	EXTTS#	EXTTS#	EXTTS#
K17	HD44	HD44	HD44	HD44	HD44	HD44
K18	HD43	HD43	HD43	HD43	HD43	HD43

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
K19	HDINV2#	HDINV2#	HDINV2#	HDINV2#	HDINV2#	HDINV2#
K20	VSS	VSS	VSS	VSS	VSS	VSS
K21	HD39	HD39	HD39	HD39	HD39	HD39
K22	HD34	HD34	HD34	HD34	HD34	HD34
K23	HD31	HD31	HD31	HD31	HD31	HD31
K24	VSS	VSS	VSS	VSS	VSS	VSS
K25	HD28	HD28	HD28	HD28	HD28	HD28
K26	VSS	VSS	VSS	VSS	VSS	VSS
K27	HA14#	HA14#	HA14#	HA14#	HA14#	HA14#
K28	VSS	VSS	VSS	VSS	VSS	VSS
K29	HA4#	HA4#	HA4#	HA4#	HA4#	HA4#
K30	HA8#	HA8#	HA8#	HA8#	HA8#	HA8#
K31	VSS	VSS	VSS	VSS	VSS	VSS
K32	VSS	VSS	VSS	VSS	VSS	VSS
K33	HA15#	HA15#	HA15#	HA15#	HA15#	HA15#
K34	HRS0#	HRS0#	HRS0#	HRS0#	HRS0#	HRS0#
K35	VSS	VSS	VSS	VSS	VSS	VSS
L1	RSV	EXP_TXN11	EXP_TXN11	EXP_TXN11	RSV	RSV
L2	VSS	VSS	VSS	VSS	VSS	VSS
L3	RSV	EXP_TXP12	EXP_TXP12	EXP_TXP12	RSV	RSV
L4	VSS	VSS	VSS	VSS	VSS	VSS
L5	RSV	EXP_RXN10	EXP_RXN10	EXP_RXN10	RSV	RSV
L6	RSV	EXP_RXP10	EXP_RXP10	EXP_RXP10	RSV	RSV
L7	VSS	VSS	VSS	VSS	VSS	VSS
L8	VSS	VSS	VSS	VSS	VSS	VSS
L9	VSS	VSS	VSS	VSS	VSS	VSS
L10	VCC	VCC	VCC	VCC	VCC	VCC
L11	VSS	VSS	VSS	VSS	VSS	VSS
L12	NC	NC	NC	NC	NC	NC
L13	VSS	VSS	VSS	VSS	VSS	VSS
L14	DDC_DATA	RSV	RSV	DDC_DATA	DDC_DATA	DDC_DATA
L15	VSS	VSS	VSS	VSS	VSS	VSS
L16	VSS	VSS	VSS	VSS	VSS	VSS
L17	VSS	VSS	VSS	VSS	VSS	VSS
L18	VSS	VSS	VSS	VSS	VSS	VSS
L19	NC	NC	NC	NC	NC	NC
L20	VSS	VSS	VSS	VSS	VSS	VSS
L21	VSS	VSS	VSS	VSS	VSS	VSS
L22	VSS	VSS	VSS	VSS	VSS	VSS
L23	HD30	HD30	HD30	HD30	HD30	HD30

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
L24	VSS	VSS	VSS	VSS	VSS	VSS
L25	HD29	HD29	HD29	HD29	HD29	HD29
L26	HA18#	HA18#	HA18#	HA18#	HA18#	HA18#
L27	VSS	VSS	VSS	VSS	VSS	VSS
L28	HA12#	HA12#	HA12#	HA12#	HA12#	HA12#
L29	HA9#	HA9#	HA9#	HA9#	HA9#	HA9#
L30	VSS	VSS	VSS	VSS	VSS	VSS
L31	HA11#	HA11#	HA11#	HA11#	HA11#	HA11#
L32	VSS	VSS	VSS	VSS	VSS	VSS
L33	HLOCK#	HLOCK#	HLOCK#	HLOCK#	HLOCK#	HLOCK#
L34	HHIT#	HHIT#	HHIT#	HHIT#	HHIT#	HHIT#
L35	HDBSY#	HDBSY#	HDBSY#	HDBSY#	HDBSY#	HDBSY#
M1	RSV	EXP_TXP13	EXP_TXP13	EXP_TXP13	RSV	RSV
M2	VSS	VSS	VSS	VSS	VSS	VSS
M3	RSV	EXP_TXN12	EXP_TXN12	EXP_TXN12	RSV	RSV
M4	VSS	VSS	VSS	VSS	VSS	VSS
M5	VSS	VSS	VSS	VSS	VSS	VSS
M6	VSS	VSS	VSS	VSS	VSS	VSS
M7	RSV	EXP_RXN12	EXP_RXN12	EXP_RXN12	RSV	RSV
M8	RSV	EXP_RXP12	EXP_RXP12	EXP_RXP12	RSV	RSV
M9	VSS	VSS	VSS	VSS	VSS	VSS
M10	VSS	VSS	VSS	VSS	VSS	VSS
M11	VSS	VSS	VSS	VSS	VSS	VSS
M12	DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN
M13	DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP
M14	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#
M15	DDC_CLK	RSV	RSV	DDC_CLK	DDC_CLK	DDC_CLK
M16	RSV	RSV	RSV	RSV	RSV	RSV
M17	VSS	VSS	VSS	VSS	VSS	VSS
M18	HD42	HD42	HD42	HD42	HD42	HD42
M19	HD38	HD38	HD38	HD38	HD38	HD38
M20	VSS	VSS	VSS	VSS	VSS	VSS
M21	HD36	HD36	HD36	HD36	HD36	HD36
M22	HCLKN	HCLKN	HCLKN	HCLKN	HCLKN	HCLKN
M23	HCLKP	HCLKP	HCLKP	HCLKP	HCLKP	HCLKP
M24	VSS	VSS	VSS	VSS	VSS	VSS
M25	VSS	VSS	VSS	VSS	VSS	VSS
M26	HA20#	HA20#	HA20#	HA20#	HA20#	HA20#
M27	VSS	VSS	VSS	VSS	VSS	VSS
M28	HA16#	HA16#	HA16#	HA16#	HA16#	HA16#

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
M29	VSS	VSS	VSS	VSS	VSS	VSS
M30	HA10#	HA10#	HA10#	HA10#	HA10#	HA10#
M31	HADS#	HADS#	HADS#	HADS#	HADS#	HADS#
M32	HDRDY#	HDRDY#	HDRDY#	HDRDY#	HDRDY#	HDRDY#
M33	—	—	—	—	—	—
M34	VSS	VSS	VSS	VSS	VSS	VSS
M35	HBNR#	HBNR#	HBNR#	HBNR#	HBNR#	HBNR#
N1	RSV	EXP_TXN13	EXP_TXN13	EXP_TXN13	RSV	RSV
N2	VSS	VSS	VSS	VSS	VSS	VSS
N3	RSV	EXP_TXP14	EXP_TXP14	EXP_TXP14	RSV	RSV
N4	VSS	VSS	VSS	VSS	VSS	VSS
N5	RSV	EXP_RXN13	EXP_RXN13	EXP_RXN13	RSV	RSV
N6	RSV	EXP_RXP13	EXP_RXP13	EXP_RXP13	RSV	RSV
N7	VSS	VSS	VSS	VSS	VSS	VSS
N8	VSS	VSS	VSS	VSS	VSS	VSS
N9	VSS	VSS	VSS	VSS	VSS	VSS
N10	VSS	VSS	VSS	VSS	VSS	VSS
N11	VSS	VSS	VSS	VSS	VSS	VSS
N12	NC	NC	NC	NC	NC	NC
N13	VCC	VCC	VCC	VCC	VCC	VCC
N14	VCC	VCC	VCC	VCC	VCC	VCC
N15	VCC	VCC	VCC	VCC	VCC	VCC
N16	VCC	VCC	VCC	VCC	VCC	VCC
N17	VSS	VSS	VSS	VSS	VSS	VSS
N18	VCC	VCC	VCC	VCC	VCC	VCC
N19	VSS	VSS	VSS	VSS	VSS	VSS
N20	VCC	VCC	VCC	VCC	VCC	VCC
N21	VCC	VCC	VCC	VCC	VCC	VCC
N22	NC	NC	NC	NC	NC	NC
N23	NC	NC	NC	NC	NC	NC
N24	NC	NC	NC	NC	NC	NC
N25	VSS	VSS	VSS	VSS	VSS	VSS
N26	HA19#	HA19#	HA19#	HA19#	HA19#	HA19#
N27	HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#
N28	VSS	VSS	VSS	VSS	VSS	VSS
N29	HA23#	HA23#	HA23#	HA23#	HA23#	HA23#
N30	VSS	VSS	VSS	VSS	VSS	VSS
N31	HA21#	HA21#	HA21#	HA21#	HA21#	HA21#
N32	VSS	VSS	VSS	VSS	VSS	VSS
N33	HA26#	HA26#	HA26#	HA26#	HA26#	HA26#

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
N34	HTRDY#	HTRDY#	HTRDY#	HTRDY#	HTRDY#	HTRDY#
N35	HHITM#	HHITM#	HHITM#	HHITM#	HHITM#	HHITM#
P1	RSV	EXP_TXP15	EXP_TXP15	EXP_TXP15	RSV	RSV
P2	VSS	VSS	VSS	VSS	VSS	VSS
P3	RSV	EXP_TXN14	EXP_TXN14	EXP_TXN14	RSV	RSV
P4	VSS	VSS	VSS	VSS	VSS	VSS
P5	VSS	VSS	VSS	VSS	VSS	VSS
P6	VSS	VSS	VSS	VSS	VSS	VSS
P7	RSV	EXP_RXP14	EXP_RXP14	EXP_RXP14	RSV	RSV
P8	RSV	EXP_RXN14	EXP_RXN14	EXP_RXN14	RSV	RSV
P9	VSS	VSS	VSS	VSS	VSS	VSS
P10	RSV	EXP_RXP11	EXP_RXP11	EXP_RXP11	RSV	RSV
P11	VSS	VSS	VSS	VSS	VSS	VSS
P12	NC	NC	NC	NC	NC	NC
P13	VCC	VCC	VCC	VCC	VCC	VCC
P14	VCC	VCC	VCC	VCC	VCC	VCC
P15	VCC	VCC	VCC	VCC	VCC	VCC
P16	VSS	VSS	VSS	VSS	VSS	VSS
P17	VCC	VCC	VCC	VCC	VCC	VCC
P18	VSS	VSS	VSS	VSS	VSS	VSS
P19	VCC	VCC	VCC	VCC	VCC	VCC
P20	VSS	VSS	VSS	VSS	VSS	VSS
P21	VCC	VCC	VCC	VCC	VCC	VCC
P22	VCC	VCC	VCC	VCC	VCC	VCC
P23	NC	NC	NC	NC	NC	NC
P24	NC	NC	NC	NC	NC	NC
P25	VSS	VSS	VSS	VSS	VSS	VSS
P26	HA22#	HA22#	HA22#	HA22#	HA22#	HA22#
P27	VSS	VSS	VSS	VSS	VSS	VSS
P28	HA24#	HA24#	HA24#	HA24#	HA24#	HA24#
P29	VSS	VSS	VSS	VSS	VSS	VSS
P30	NC	NC	NC	NC	NC	NC
P31	VSS	VSS	VSS	VSS	VSS	VSS
P32	VSS	VSS	VSS	VSS	VSS	VSS
P33	HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#
P34	HRS1#	HRS1#	HRS1#	HRS1#	HRS1#	HRS1#
P35	VSS	VSS	VSS	VSS	VSS	VSS
R1	RSV	EXP_TXN15	EXP_TXN15	EXP_TXN15	RSV	RSV
R2	VSS	VSS	VSS	VSS	VSS	VSS
R3	DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
R4	VSS	VSS	VSS	VSS	VSS	VSS
R5	RSV	EXP_RXN15	EXP_RXN15	EXP_RXN15	RSV	RSV
R6	RSV	EXP_RXP15	EXP_RXP15	EXP_RXP15	RSV	RSV
R7	VSS	VSS	VSS	VSS	VSS	VSS
R8	VSS	VSS	VSS	VSS	VSS	VSS
R9	VSS	VSS	VSS	VSS	VSS	VSS
R10	RSV	EXP_RXN11	EXP_RXN11	EXP_RXN11	RSV	RSV
R11	VSS	VSS	VSS	VSS	VSS	VSS
R12	NC	NC	NC	NC	NC	NC
R13	VCC	VCC	VCC	VCC	VCC	VCC
R14	VCC	VCC	VCC	VCC	VCC	VCC
R15	VCC	VCC	VCC	VCC	VCC	VCC
R16	VCC	VCC	VCC	VCC	VCC	VCC
R17	VSS	VSS	VSS	VSS	VSS	VSS
R18	VCC	VCC	VCC	VCC	VCC	VCC
R19	VSS	VSS	VSS	VSS	VSS	VSS
R20	VCC	VCC	VCC	VCC	VCC	VCC
R21	VSS	VSS	VSS	VSS	VSS	VSS
R22	VCC	VCC	VCC	VCC	VCC	VCC
R23	VCC	VCC	VCC	VCC	VCC	VCC
R24	NC	NC	NC	NC	NC	NC
R25	VSS	VSS	VSS	VSS	VSS	VSS
R26	VSS	VSS	VSS	VSS	VSS	VSS
R27	VSS	VSS	VSS	VSS	VSS	VSS
R28	HA25#	HA25#	HA25#	HA25#	HA25#	HA25#
R29	HA17#	HA17#	HA17#	HA17#	HA17#	HA17#
R30	RSV	RSV	RSV	RSV	RSV	RSV
R31	RSV	RSV	RSV	RSV	RSV	RSV
R32	SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58
R33	HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#
R34	SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59
R35	RSV	RSV	RSV	RSV	RSV	RSV
T1	DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1
T2	VSS	VSS	VSS	VSS	VSS	VSS
T3	DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0
T4	VSS	VSS	VSS	VSS	VSS	VSS
T5	VSS	VSS	VSS	VSS	VSS	VSS
T6	VSS	VSS	VSS	VSS	VSS	VSS
T7	VSS	VSS	VSS	VSS	VSS	VSS
T8	DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
T9	DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1
T10	VSS	VSS	VSS	VSS	VSS	VSS
T11	VSS	VSS	VSS	VSS	VSS	VSS
T12	NC	NC	NC	NC	NC	NC
T13	VCC	VCC	VCC	VCC	VCC	VCC
T14	VCC	VCC	VCC	VCC	VCC	VCC
T15	VCC	VCC	VCC	VCC	VCC	VCC
T16	VCC	VCC	VCC	VCC	VCC	VCC
T17	VCC	VCC	VCC	VCC	VCC	VCC
T18	VSS	VSS	VSS	VSS	VSS	VSS
T19	VCC	VCC	VCC	VCC	VCC	VCC
T20	VCC	VCC	VCC	VCC	VCC	VCC
T21	VCC	VCC	VCC	VCC	VCC	VCC
T22	VSS	VSS	VSS	VSS	VSS	VSS
T23	VCC	VCC	VCC	VCC	VCC	VCC
T24	VCC	VCC	VCC	VCC	VCC	VCC
T25	VSS	VSS	VSS	VSS	VSS	VSS
T26	HA30#	HA30#	HA30#	HA30#	HA30#	HA30#
T27	HA27#	HA27#	HA27#	HA27#	HA27#	HA27#
T28	VSS	VSS	VSS	VSS	VSS	VSS
T29	HA31#	HA31#	HA31#	HA31#	HA31#	HA31#
T30	VSS	VSS	VSS	VSS	VSS	VSS
T31	HA28#	HA28#	HA28#	HA28#	HA28#	HA28#
T32	VSS	VSS	VSS	VSS	VSS	VSS
T33	SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62
T34	VSS	VSS	VSS	VSS	VSS	VSS
T35	SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63
U1	DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1
U2	VSS	VSS	VSS	VSS	VSS	VSS
U3	DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2
U4	VSS	VSS	VSS	VSS	VSS	VSS
U5	DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0
U6	DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0
U7	VSS	VSS	VSS	VSS	VSS	VSS
U8	VSS	VSS	VSS	VSS	VSS	VSS
U9	VSS	VSS	VSS	VSS	VSS	VSS
U10	DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3
U11	VSS	VSS	VSS	VSS	VSS	VSS
U12	NC	NC	NC	NC	NC	NC
U13	VCC	VCC	VCC	VCC	VCC	VCC

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
U14	VCC	VCC	VCC	VCC	VCC	VCC
U15	VSS	VSS	VSS	VSS	VSS	VSS
U16	VCC	VCC	VCC	VCC	VCC	VCC
U17	VSS	VSS	VSS	VSS	VSS	VSS
U18	VCC	VCC	VCC	VCC	VCC	VCC
U19	VSS	VSS	VSS	VSS	VSS	VSS
U20	VCC	VCC	VCC	VCC	VCC	VCC
U21	VSS	VSS	VSS	VSS	VSS	VSS
U22	VCC	VCC	VCC	VCC	VCC	VCC
U23	VSS	VSS	VSS	VSS	VSS	VSS
U24	VCC	VCC	VCC	VCC	VCC	VCC
U25	VSS	VSS	VSS	VSS	VSS	VSS
U26	SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58
U27	VSS	VSS	VSS	VSS	VSS	VSS
U28	HA29#	HA29#	HA29#	HA29#	HA29#	HA29#
U29	VSS	VSS	VSS	VSS	VSS	VSS
U30	RSV	RSV	RSV	RSV	RSV	RSV
U31	VSS	VSS	VSS	VSS	VSS	VSS
U32	VSS	VSS	VSS	VSS	VSS	VSS
U33	SDM_A7	SDM_A7	SDM_A7	SDM_A7	SDM_A7	SDM_A7
U34	SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7
U35	RSV	RSV	RSV	RSV	RSV	RSV
V1	VSS	VSS	VSS	VSS	VSS	VSS
V2	VSS	VSS	VSS	VSS	VSS	VSS
V3	DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2
V4	VSS	VSS	VSS	VSS	VSS	VSS
V5	DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3
V6	VSS	VSS	VSS	VSS	VSS	VSS
V7	DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2
V8	DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2
V9	VSS	VSS	VSS	VSS	VSS	VSS
V10	DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3
V11	VSS	VSS	VSS	VSS	VSS	VSS
V12	NC	NC	NC	NC	NC	NC
V13	VCC	VCC	VCC	VCC	VCC	VCC
V14	VCC	VCC	VCC	VCC	VCC	VCC
V15	VCC	VCC	VCC	VCC	VCC	VCC
V16	VSS	VSS	VSS	VSS	VSS	VSS
V17	VCC	VCC	VCC	VCC	VCC	VCC
V18	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
V19	VCC	VCC	VCC	VCC	VCC	VCC
V20	VSS	VSS	VSS	VSS	VSS	VSS
V21	VCC	VCC	VCC	VCC	VCC	VCC
V22	VSS	VSS	VSS	VSS	VSS	VSS
V23	VCC	VCC	VCC	VCC	VCC	VCC
V24	VCC	VCC	VCC	VCC	VCC	VCC
V25	VSS	VSS	VSS	VSS	VSS	VSS
V26	VSS	VSS	VSS	VSS	VSS	VSS
V27	VSS	VSS	VSS	VSS	VSS	VSS
V28	SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63
V29	SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59
V30	RSV	RSV	RSV	RSV	RSV	RSV
V31	RSV	RSV	RSV	RSV	RSV	RSV
V32	RSV	RSV	RSV	RSV	RSV	RSV
V33	SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57
V34	SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56
V35	VSS	VSS	VSS	VSS	VSS	VSS
W1	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W2	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W4	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W5	DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3
W6	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W7	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W8	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W9	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
W10	EXP_COMPI	EXP_COMPI	EXP_COMPI	EXP_COMPI	EXP_COMPI	EXP_COMPI
W11	VSS	VSS	VSS	VSS	VSS	VSS
W12	NC	NC	NC	NC	NC	NC
W13	VCC	VCC	VCC	VCC	VCC	VCC
W14	VCC	VCC	VCC	VCC	VCC	VCC
W15	VSS	VSS	VSS	VSS	VSS	VSS
W16	VCC	VCC	VCC	VCC	VCC	VCC
W17	VSS	VSS	VSS	VSS	VSS	VSS
W18	VCC	VCC	VCC	VCC	VCC	VCC
W19	VSS	VSS	VSS	VSS	VSS	VSS
W20	VCC	VCC	VCC	VCC	VCC	VCC
W21	VSS	VSS	VSS	VSS	VSS	VSS
W22	VCC	VCC	VCC	VCC	VCC	VCC
W23	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
W24	VCC	VCC	VCC	VCC	VCC	VCC
W25	VSS	VSS	VSS	VSS	VSS	VSS
W26	SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62
W27	SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7
W28	VSS	VSS	VSS	VSS	VSS	VSS
W29	SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57
W30	VSS	VSS	VSS	VSS	VSS	VSS
W31	SDM_B7	SDM_B7	SDM_B7	SDM_B7	SDM_B7	SDM_B7
W32	VSS	VSS	VSS	VSS	VSS	VSS
W33	SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61
W34	SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51
W35	SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60
Y1	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y2	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y4	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y5	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y6	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y7	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y8	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y9	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP
Y10	EXP_COMPO	EXP_COMPO	EXP_COMPO	EXP_COMPO	EXP_COMPO	EXP_COMPO
Y11	VSS	VSS	VSS	VSS	VSS	VSS
Y12	NC	NC	NC	NC	NC	NC
Y13	VCC	VCC	VCC	VCC	VCC	VCC
Y14	VCC	VCC	VCC	VCC	VCC	VCC
Y15	VCC	VCC	VCC	VCC	VCC	VCC
Y16	VCC	VCC	VCC	VCC	VCC	VCC
Y17	VCC	VCC	VCC	VCC	VCC	VCC
Y18	VSS	VSS	VSS	VSS	VSS	VSS
Y19	VCC	VCC	VCC	VCC	VCC	VCC
Y20	VCC	VCC	VCC	VCC	VCC	VCC
Y21	VCC	VCC	VCC	VCC	VCC	VCC
Y22	VSS	VSS	VSS	VSS	VSS	VSS
Y23	VCC	VCC	VCC	VCC	VCC	VCC
Y24	VCC	VCC	VCC	VCC	VCC	VCC
Y25	VSS	VSS	VSS	VSS	VSS	VSS
Y26	SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60
Y27	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
Y28	RSV	RSV	RSV	RSV	RSV	RSV
Y29	VSS	VSS	VSS	VSS	VSS	VSS
Y30	RSV	RSV	RSV	RSV	RSV	RSV
Y31	VSS	VSS	VSS	VSS	VSS	VSS
Y32	VSS	VSS	VSS	VSS	VSS	VSS
Y33	SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50
Y34	VSS	VSS	VSS	VSS	VSS	VSS
Y35	SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55
AA1	VSS	VSS	VSS	VSS	VSS	VSS
AA2	VSS	VSS	VSS	VSS	VSS	VSS
AA3	VSS	VSS	VSS	VSS	VSS	VSS
AA4	VSS	VSS	VSS	VSS	VSS	VSS
AA5	VSS	VSS	VSS	VSS	VSS	VSS
AA6	VSS	VSS	VSS	VSS	VSS	VSS
AA7	VSS	VSS	VSS	VSS	VSS	VSS
AA8	VSS	VSS	VSS	VSS	VSS	VSS
AA9	VSS	VSS	VSS	VSS	VSS	VSS
AA10	VSS	VSS	VSS	VSS	VSS	VSS
AA11	VSS	VSS	VSS	VSS	VSS	VSS
AA12	NC	NC	NC	NC	NC	NC
AA13	VCC	VCC	VCC	VCC	VCC	VCC
AA14	VCC	VCC	VCC	VCC	VCC	VCC
AA15	VSS	VSS	VSS	VSS	VSS	VSS
AA16	VCC	VCC	VCC	VCC	VCC	VCC
AA17	VSS	VSS	VSS	VSS	VSS	VSS
AA18	VCC	VCC	VCC	VCC	VCC	VCC
AA19	VSS	VSS	VSS	VSS	VSS	VSS
AA20	VCC	VCC	VCC	VCC	VCC	VCC
AA21	VCC	VCC	VCC	VCC	VCC	VCC
AA22	VCC	VCC	VCC	VCC	VCC	VCC
AA23	VCC	VCC	VCC	VCC	VCC	VCC
AA24	VCC	VCC	VCC	VCC	VCC	VCC
AA25	VSS	VSS	VSS	VSS	VSS	VSS
AA26	VSS	VSS	VSS	VSS	VSS	VSS
AA27	VSS	VSS	VSS	VSS	VSS	VSS
AA28	SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61
AA29	SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56
AA30	RSV	RSV	RSV	RSV	RSV	RSV
AA31	RSV	RSV	RSV	RSV	RSV	RSV
AA32	SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AA33	SDM_A6	SDM_A6	SDM_A6	SDM_A6	SDM_A6	SDM_A6
AA34	SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6
AA35	RSV	RSV	RSV	RSV	RSV	RSV
AB1	VCC	VCC	VCC	VCC	VCC	VCC
AB2	VCC	VCC	VCC	VCC	VCC	VCC
AB3	VCC	VCC	VCC	VCC	VCC	VCC
AB4	VCC	VCC	VCC	VCC	VCC	VCC
AB5	VCC	VCC	VCC	VCC	VCC	VCC
AB6	VCC	VCC	VCC	VCC	VCC	VCC
AB7	VCC	VCC	VCC	VCC	VCC	VCC
AB8	VCC	VCC	VCC	VCC	VCC	VCC
AB9	VCC	VCC	VCC	VCC	VCC	VCC
AB10	VCC	VCC	VCC	VCC	VCC	VCC
AB11	VCC	VCC	VCC	VCC	VCC	VCC
AB12	NC	NC	NC	NC	NC	NC
AB13	VCC	VCC	VCC	VCC	VCC	VCC
AB14	VCC	VCC	VCC	VCC	VCC	VCC
AB15	VCC	VCC	VCC	VCC	VCC	VCC
AB16	VCC	VCC	VCC	VCC	VCC	VCC
AB17	VCC	VCC	VCC	VCC	VCC	VCC
AB18	VCC	VCC	VCC	VCC	VCC	VCC
AB19	VCC	VCC	VCC	VCC	VCC	VCC
AB20	VCC	VCC	VCC	VCC	VCC	VCC
AB21	VCC	VCC	VCC	VCC	VCC	VCC
AB22	VCC	VCC	VCC	VCC	VCC	VCC
AB23	VCC	VCC	VCC	VCC	VCC	VCC
AB24	VCC	VCC	VCC	VCC	VCC	VCC
AB25	VSS	VSS	VSS	VSS	VSS	VSS
AB26	SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51
AB27	SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50
AB28	VSS	VSS	VSS	VSS	VSS	VSS
AB29	RSV	RSV	RSV	RSV	RSV	RSV
AB30	VSS	VSS	VSS	VSS	VSS	VSS
AB31	SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6
AB32	VSS	VSS	VSS	VSS	VSS	VSS
AB33	SMA_A13	SMA_A13	SMA_A13	SMA_A13	SMA_A13	SMA_A13
AB34	SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2
AB35	VSS	VSS	VSS	VSS	VSS	VSS
AC1	VCC	VCC	VCC	VCC	VCC	VCC
AC2	VCC	VCC	VCC	VCC	VCC	VCC

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AC3	VCC	VCC	VCC	VCC	VCC	VCC
AC4	VCC	VCC	VCC	VCC	VCC	VCC
AC5	VCC	VCC	VCC	VCC	VCC	VCC
AC6	VCC	VCC	VCC	VCC	VCC	VCC
AC7	VCC	VCC	VCC	VCC	VCC	VCC
AC8	VCC	VCC	VCC	VCC	VCC	VCC
AC9	VCC	VCC	VCC	VCC	VCC	VCC
AC10	VCC	VCC	VCC	VCC	VCC	VCC
AC11	VCC	VCC	VCC	VCC	VCC	VCC
AC12	RSV	RSV	RSV	RSV	RSV	RSV
AC13	RSV	RSV	RSV	RSV	RSV	RSV
AC14	RSV	RSV	RSV	RSV	RSV	RSV
AC15	RSV	RSV	RSV	RSV	RSV	RSV
AC16	RSV	RSV	RSV	RSV	RSV	RSV
AC17	RSV	RSV	RSV	RSV	RSV	RSV
AC18	RSV	RSV	RSV	RSV	RSV	RSV
AC19	RSV	RSV	RSV	RSV	RSV	RSV
AC20	RSV	RSV	RSV	RSV	RSV	RSV
AC21	RSV	RSV	RSV	RSV	RSV	RSV
AC22	RSV	RSV	RSV	RSV	RSV	RSV
AC23	NC	NC	NC	NC	NC	NC
AC24	NC	NC	NC	NC	NC	NC
AC25	VSS	VSS	VSS	VSS	VSS	VSS
AC26	SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55
AC27	VSS	VSS	VSS	VSS	VSS	VSS
AC28	SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54
AC29	VSS	VSS	VSS	VSS	VSS	VSS
AC30	RSV	RSV	RSV	RSV	RSV	RSV
AC31	VSS	VSS	VSS	VSS	VSS	VSS
AC32	VSS	VSS	VSS	VSS	VSS	VSS
AC33	SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#
AC34	SCLK_A5#	RSV	SCLK_A5#	SCLK_A5#	SCLK_A5#	RSV
AC35	SCLK_A5	RSV	SCLK_A5	SCLK_A5	SCLK_A5	RSV
AD1	VCC	VCC	VCC	VCC	VCC	VCC
AD2	VCC	VCC	VCC	VCC	VCC	VCC
AD3	VCC	VCC	VCC	VCC	VCC	VCC
AD4	VCC	VCC	VCC	VCC	VCC	VCC
AD5	VCC	VCC	VCC	VCC	VCC	VCC
AD6	VCC	VCC	VCC	VCC	VCC	VCC
AD7	VCC	VCC	VCC	VCC	VCC	VCC

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AD8	VCC	VCC	VCC	VCC	VCC	VCC
AD9	VCC	VCC	VCC	VCC	VCC	VCC
AD10	VCC	VCC	VCC	VCC	VCC	VCC
AD11	VSS	VSS	VSS	VSS	VSS	VSS
AD12	SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20
AD13	VSS	VSS	VSS	VSS	VSS	VSS
AD14	SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19
AD15	SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23
AD16	VSS	VSS	VSS	VSS	VSS	VSS
AD17	SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26
AD18	SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24
AD19	VSS	VSS	VSS	VSS	VSS	VSS
AD20	SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3
AD21	SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31
AD22	VSS	VSS	VSS	VSS	VSS	VSS
AD23	SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36
AD24	SDM_B6	SDM_B6	SDM_B6	SDM_B6	SDM_B6	SDM_B6
AD25	VSS	VSS	VSS	VSS	VSS	VSS
AD26	VSS	VSS	VSS	VSS	VSS	VSS
AD27	VSS	VSS	VSS	VSS	VSS	VSS
AD28	SCLK_B5#	RSV	SCLK_B5#	SCLK_B5#	SCLK_B5#	RSV
AD29	SCLK_B5	RSV	SCLK_B5	SCLK_B5	SCLK_B5	RSV
AD30	NC	NC	NC	NC	NC	NC
AD31	SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52
AD32	SMA_B13	SMA_B13	SMA_B13	SMA_B13	SMA_B13	SMA_B13
AD33	—	—	—	—	—	—
AD34	VSS	VSS	VSS	VSS	VSS	VSS
AD35	SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53
AE1	SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5
AE2	SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4
AE3	SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0
AE4	VSS	VSS	VSS	VSS	VSS	VSS
AE5	RSV	RSV	RSV	RSV	RSV	RSV
AE6	VSS	VSS	VSS	VSS	VSS	VSS
AE7	SVREF0	SVREF0	SVREF0	SVREF0	SVREF0	SVREF0
AE8	SVREF1	SVREF1	SVREF1	SVREF1	SVREF1	SVREF1
AE9	VSS	VSS	VSS	VSS	VSS	VSS
AE10	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1
AE11	SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AE12	VSS	VSS	VSS	VSS	VSS	VSS
AE13	SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16
AE14	VSS	VSS	VSS	VSS	VSS	VSS
AE15	VSS	VSS	VSS	VSS	VSS	VSS
AE16	RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0
AE17	VSS	VSS	VSS	VSS	VSS	VSS
AE18	VSS	VSS	VSS	VSS	VSS	VSS
AE19	SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30
AE20	VSS	VSS	VSS	VSS	VSS	VSS
AE21	VSS	VSS	VSS	VSS	VSS	VSS
AE22	SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26
AE23	VSS	VSS	VSS	VSS	VSS	VSS
AE24	VSS	VSS	VSS	VSS	VSS	VSS
AE25	SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#
AE26	SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2
AE27	SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53
AE28	VSS	VSS	VSS	VSS	VSS	VSS
AE29	SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52
AE30	VSS	VSS	VSS	VSS	VSS	VSS
AE31	SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48
AE32	VSS	VSS	VSS	VSS	VSS	VSS
AE33	SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47
AE34	SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49
AE35	SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48
AF1	VSS	VSS	VSS	VSS	VSS	VSS
AF2	SDM_A0	SDM_A0	SDM_A0	SDM_A0	SDM_A0	SDM_A0
AF3	SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1
AF4	VSS	VSS	VSS	VSS	VSS	VSS
AF5	RSV	RSV	RSV	RSV	RSV	RSV
AF6	VSS	VSS	VSS	VSS	VSS	VSS
AF7	RSTIN#	RSTIN#	RSTIN#	RSTIN#	RSTIN#	RSTIN#
AF8	VSS	VSS	VSS	VSS	VSS	VSS
AF9	SM_SLEWIN 1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1
AF10	VSS	VSS	VSS	VSS	VSS	VSS
AF11	SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10
AF12	VSS	VSS	VSS	VSS	VSS	VSS
AF13	SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17
AF14	SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22
AF15	VSS	VSS	VSS	VSS	VSS	VSS

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AF16	SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28
AF17	SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3
AF18	VSS	VSS	VSS	VSS	VSS	VSS
AF19	SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27
AF20	RSV	RSV	RSV	RSV	RSV	RSV
AF21	VSS	VSS	VSS	VSS	VSS	VSS
AF22	SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30
AF23	SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32
AF24	SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37
AF25	SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33
AF26	VSS	VSS	VSS	VSS	VSS	VSS
AF27	SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49
AF28	SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47
AF29	VSS	VSS	VSS	VSS	VSS	VSS
AF30	VSS	VSS	VSS	VSS	VSS	VSS
AF31	VSS	VSS	VSS	VSS	VSS	VSS
AF32	VSS	VSS	VSS	VSS	VSS	VSS
AF33	SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46
AF34	SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43
AF35	VSS	VSS	VSS	VSS	VSS	VSS
AG1	SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0
AG2	RSV	RSV	RSV	RSV	RSV	RSV
AG3	SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6
AG4	SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0
AG5	VSS	VSS	VSS	VSS	VSS	VSS
AG6	NC	NC	NC	NC	NC	NC
AG7	PWROK	PWROK	PWROK	PWROK	PWROK	PWROK
AG8	SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1
AG9	SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4
AG10	SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14
AG11	SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15
AG12	VSS	VSS	VSS	VSS	VSS	VSS
AG13	VSS	VSS	VSS	VSS	VSS	VSS
AG14	SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18
AG15	VSS	VSS	VSS	VSS	VSS	VSS
AG16	VSS	VSS	VSS	VSS	VSS	VSS
AG17	RSV	RSV	RSV	RSV	RSV	RSV
AG18	VSS	VSS	VSS	VSS	VSS	VSS
AG19	VSS	VSS	VSS	VSS	VSS	VSS
AG20	SDM_B3	SDM_B3	SDM_B3	SDM_B3	SDM_B3	SDM_B3

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AG21	VSS	VSS	VSS	VSS	VSS	VSS
AG22	VSS	VSS	VSS	VSS	VSS	VSS
AG23	SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#
AG24	SDM_B4	SDM_B4	SDM_B4	SDM_B4	SDM_B4	SDM_B4
AG25	VSS	VSS	VSS	VSS	VSS	VSS
AG26	RSV	RSV	RSV	RSV	RSV	RSV
AG27	SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46
AG28	VSS	VSS	VSS	VSS	VSS	VSS
AG29	VSS	VSS	VSS	VSS	VSS	VSS
AG30	SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42
AG31	SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43
AG32	SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42
AG33	RSV	RSV	RSV	RSV	RSV	RSV
AG34	SDM_A5	SDM_A5	SDM_A5	SDM_A5	SDM_A5	SDM_A5
AG35	SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5
AH1	VSS	VSS	VSS	VSS	VSS	VSS
AH2	SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2
AH3	SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7
AH4	SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5
AH5	VSS	VSS	VSS	VSS	VSS	VSS
AH6	VSS	VSS	VSS	VSS	VSS	VSS
AH7	SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0
AH8	VSS	VSS	VSS	VSS	VSS	VSS
AH9	SDM_B1	SDM_B1	SDM_B1	SDM_B1	SDM_B1	SDM_B1
AH10	RSV	RSV	RSV	RSV	RSV	RSV
AH11	VSS	VSS	VSS	VSS	VSS	VSS
AH12	SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21
AH13	SDM_B2	SDM_B2	SDM_B2	SDM_B2	SDM_B2	SDM_B2
AH14	VSS	VSS	VSS	VSS	VSS	VSS
AH15	RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1
AH16	SDM_A3	SDM_A3	SDM_A3	SDM_A3	SDM_A3	SDM_A3
AH17	VSS	VSS	VSS	VSS	VSS	VSS
AH18	SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31
AH19	SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29
AH20	VSS	VSS	VSS	VSS	VSS	VSS
AH21	SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27
AH22	SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0
AH23	VSS	VSS	VSS	VSS	VSS	VSS
AH24	NC	NC	NC	NC	NC	NC
AH25	SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AH26	VSS	VSS	VSS	VSS	VSS	VSS
AH27	SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32
AH28	SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5
AH29	VSS	VSS	VSS	VSS	VSS	VSS
AH30	RSV	RSV	RSV	RSV	RSV	RSV
AH31	SDM_B5	SDM_B5	SDM_B5	SDM_B5	SDM_B5	SDM_B5
AH32	VSS	VSS	VSS	VSS	VSS	VSS
AH33	SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45
AH34	VSS	VSS	VSS	VSS	VSS	VSS
AH35	SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41
AJ1	SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8
AJ2	SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3
AJ3	SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12
AJ4	VSS	VSS	VSS	VSS	VSS	VSS
AJ5	SDM_B0	SDM_B0	SDM_B0	SDM_B0	SDM_B0	SDM_B0
AJ6	SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1
AJ7	SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8
AJ8	SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12
AJ9	VSS	VSS	VSS	VSS	VSS	VSS
AJ10	VSS	VSS	VSS	VSS	VSS	VSS
AJ11	SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#
AJ12	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0
AJ13	VSS	VSS	VSS	VSS	VSS	VSS
AJ14	NC	NC	NC	NC	NC	NC
AJ15	VSS	VSS	VSS	VSS	VSS	VSS
AJ16	VSS	VSS	VSS	VSS	VSS	VSS
AJ17	SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29
AJ18	RSV	RSV	RSV	RSV	RSV	RSV
AJ19	VSS	VSS	VSS	VSS	VSS	VSS
AJ20	RSV	RSV	RSV	RSV	RSV	RSV
AJ21	RSV	RSV	RSV	RSV	RSV	RSV
AJ22	VSS	VSS	VSS	VSS	VSS	VSS
AJ23	RSV	RSV	RSV	RSV	RSV	RSV
AJ24	RSV	RSV	RSV	RSV	RSV	RSV
AJ25	SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38
AJ26	SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35
AJ27	VSS	VSS	VSS	VSS	VSS	VSS
AJ28	SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37
AJ29	SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AJ30	VSS	VSS	VSS	VSS	VSS	VSS
AJ31	SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41
AJ32	VSS	VSS	VSS	VSS	VSS	VSS
AJ33	SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44
AJ34	SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40
AJ35	VSS	VSS	VSS	VSS	VSS	VSS
AK1	VSS	VSS	VSS	VSS	VSS	VSS
AK2	SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9
AK3	SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13
AK4	VSS	VSS	VSS	VSS	VSS	VSS
AK5	SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0
AK6	VSS	VSS	VSS	VSS	VSS	VSS
AK7	VSS	VSS	VSS	VSS	VSS	VSS
AK8	VSS	VSS	VSS	VSS	VSS	VSS
AK9	SCLK_B4	SCLK_B4	SCLK_B4	SCLK_B4	SCLK_B4	RSV
AK10	SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1
AK11	VSS	VSS	VSS	VSS	VSS	VSS
AK12	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0
AK13	SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2
AK14	VSS	VSS	VSS	VSS	VSS	VSS
AK15	RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3
AK16	SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24
AK17	VSS	VSS	VSS	VSS	VSS	VSS
AK18	RSV	RSV	RSV	RSV	RSV	RSV
AK19	SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25
AK20	VSS	VSS	VSS	VSS	VSS	VSS
AK21	RSV	RSV	RSV	RSV	RSV	RSV
AK22	SCLK_B3#	RSV	SCLK_B3#	SCLK_B3#	SCLK_B3#	RSV
AK23	VSS	RSV	VSS	VSS	VSS	VSS
AK24	RSV	RSV	RSV	RSV	RSV	RSV
AK25	VSS	VSS	VSS	VSS	VSS	VSS
AK26	VSS	VSS	VSS	VSS	VSS	VSS
AK27	SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33
AK28	VSS	VSS	VSS	VSS	VSS	VSS
AK29	SDM_A4	SDM_A4	SDM_A4	SDM_A4	SDM_A4	SDM_A4
AK30	VSS	VSS	VSS	VSS	VSS	VSS
AK31	SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35
AK32	SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45
AK33	SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AK34	SCS_A2#	SCS_A2#	SCS_A2#	SCS_A2#	SCS_A2#	RSV
AK35	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AL1	SDM_A1	SDM_A1	SDM_A1	SDM_A1	SDM_A1	SDM_A1
AL2	RSV	RSV	RSV	RSV	RSV	RSV
AL3	SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1
AL4	RSV	RSV	RSV	RSV	RSV	RSV
AL5	SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2
AL6	SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7
AL7	SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9
AL8	SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13
AL9	SCLK_B4#	RSV	SCLK_B4#	SCLK_B4#	SCLK_B4#	RSV
AL10	VSS	VSS	VSS	VSS	VSS	VSS
AL11	SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1
AL12	SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0
AL13	VSS	VSS	VSS	VSS	VSS	VSS
AL14	RSV	RSV	RSV	RSV	RSV	RSV
AL15	SMA_B7	SMA_B7	SMA_B7	SMA_B7	SMA_B7	SMA_B7
AL16	VSS	VSS	VSS	VSS	VSS	VSS
AL17	SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25
AL18	SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28
AL19	VSS	VSS	VSS	VSS	VSS	VSS
AL20	RSV	RSV	RSV	RSV	RSV	RSV
AL21	RSV	RSV	RSV	RSV	RSV	RSV
AL22	VSS	VSS	VSS	VSS	VSS	VSS
AL23	SCLK_B3	RSV	SCLK_B3	SCLK_B3	SCLK_B3	RSV
AL24	RSV	RSV	RSV	RSV	RSV	RSV
AL25	SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34
AL26	SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39
AL27	SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36
AL28	NC	NC	NC	NC	NC	NC
AL29	RSV	RSV	RSV	RSV	RSV	RSV
AL30	SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38
AL31	SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39
AL32	VSS	VSS	VSS	VSS	VSS	VSS
AL33	SCS_A3#	RSV	SCS_A3#	SCS_A3#	SCS_A3#	RSV
AL34	SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#
AL35	SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#
AM1	—	—	—	—	—	—
AM2	SCLK_A4	RSV	SCLK_A4	SCLK_A4	SCLK_A4	RSV
AM3	SCLK_A4#	RSV	SCLK_A4#	SCLK_A4#	SCLK_A4#	RSV

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AM4	VSS	VSS	VSS	VSS	VSS	VSS
AM5	SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6
AM6	VSS	VSS	VSS	VSS	VSS	VSS
AM7	VSS	VSS	VSS	VSS	VSS	VSS
AM8	VSS	VSS	VSS	VSS	VSS	VSS
AM9	SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1
AM10	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM11	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM12	SMA_B12	SMA_B12	SMA_B12	SMA_B12	SMA_B12	SMA_B12
AM13	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM14	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM15	SMA_A9	SMA_A9	SMA_A9	SMA_A9	SMA_A9	SMA_A9
AM16	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM17	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM18	SMA_B0	SMA_B0	SMA_B0	SMA_B0	SMA_B0	SMA_B0
AM19	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM20	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM21	SMA_A4	SMA_A4	SMA_A4	SMA_A4	SMA_A4	SMA_A4
AM22	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM23	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM24	SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0
AM25	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM26	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM27	SBS_B0	SBS_B0	SBS_B0	SBS_B0	SBS_B0	SBS_B0
AM28	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM29	VSS	VSS	VSS	VSS	VSS	VSS
AM30	SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4
AM31	VSS	VSS	VSS	VSS	VSS	VSS
AM32	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AM33	SCS_B3#	RSV	SCS_B3#	SCS_B3#	SCS_B3#	RSV
AM34	SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#
AM35	—	—	—	—	—	—
AN1	VSS	VSS	VSS	VSS	VSS	VSS
AN2	SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1
AN3	SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#
AN4	SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10
AN5	SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20
AN6	SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3
AN7	SDM_A2	SDM_A2	SDM_A2	SDM_A2	SDM_A2	SDM_A2
AN8	SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AN9	SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23
AN10	SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0
AN11	SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1
AN12	—	—	—	—	—	—
AN13	SMA_B9	SMA_B9	SMA_B9	SMA_B9	SMA_B9	SMA_B9
AN14	RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2
AN15	SMA_B5	SMA_B5	SMA_B5	SMA_B5	SMA_B5	SMA_B5
AN16	SMA_A7	SMA_A7	SMA_A7	SMA_A7	SMA_A7	SMA_A7
AN17	SMA_B2	SMA_B2	SMA_B2	SMA_B2	SMA_B2	SMA_B2
AN18	SMA_A8	SMA_A8	SMA_A8	SMA_A8	SMA_A8	SMA_A8
AN19	NC	NC	NC	NC	NC	NC
AN20	SMA_B10	SMA_B10	SMA_B10	SMA_B10	SMA_B10	SMA_B10
AN21	SMA_A2	SMA_A2	SMA_A2	SMA_A2	SMA_A2	SMA_A2
AN22	SMA_A0	SMA_A0	SMA_A0	SMA_A0	SMA_A0	SMA_A0
AN23	SMA_A10	SMA_A10	SMA_A10	SMA_A10	SMA_A10	SMA_A10
AN24	—	—	—	—	—	—
AN25	SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#
AN26	SCLK_A3#	SCLK_A3#	SCLK_A3#	SCLK_A3#	SCLK_A3#	RSV
AN27	SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#
AN28	SBS_A0	SBS_A0	SBS_A0	SBS_A0	SBS_A0	SBS_A0
AN29	SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#
AN30	SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34
AN31	RSV	RSV	RSV	RSV	RSV	RSV
AN32	RSV	RSV	RSV	RSV	RSV	RSV
AN33	SCS_B2#	RSV	SCS_B2#	SCS_B2#	SCS_B2#	RSV
AN34	SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#
AN35	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP1	NC	NC	NC	NC	NC	NC
AP2	SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14
AP3	SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15
AP4	SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11
AP5	SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16
AP6	SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21
AP7	SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2
AP8	VSS	VSS	VSS	VSS	VSS	VSS
AP9	SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19
AP10	SCKE_B2	RSV	SCKE_B2	SCKE_B2	SCKE_B2	RSV
AP11	SCKE_A2	RSV	SCKE_A2	SCKE_A2	SCKE_A2	RSV
AP12	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP13	SMA_A12	SMA_A12	SMA_A12	SMA_A12	SMA_A12	SMA_A12

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AP14	SMA_B8	SMA_B8	SMA_B8	SMA_B8	SMA_B8	SMA_B8
AP15	SMA_A11	SMA_A11	SMA_A11	SMA_A11	SMA_A11	SMA_A11
AP16	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP17	SMA_B6	SMA_B6	SMA_B6	SMA_B6	SMA_B6	SMA_B6
AP18	SMA_B1	SMA_B1	SMA_B1	SMA_B1	SMA_B1	SMA_B1
AP19	SMA_A5	SMA_A5	SMA_A5	SMA_A5	SMA_A5	SMA_A5
AP20	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP21	SMA_A3	SMA_A3	SMA_A3	SMA_A3	SMA_A3	SMA_A3
AP22	SMA_A1	SMA_A1	SMA_A1	SMA_A1	SMA_A1	SMA_A1
AP23	RSV	RSV	RSV	RSV	RSV	RSV
AP24	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP25	SCLK_A3	RSV	SCLK_A3	SCLK_A3	SCLK_A3	RSV
AP26	SBS_A1	SBS_A1	SBS_A1	SBS_A1	SBS_A1	SBS_A1
AP27	SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#
AP28	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AP29	RSV	RSV	RSV	RSV	RSV	RSV
AP30	RSV	RSV	RSV	RSV	RSV	RSV
AP31	SWE_A#	SWE_A#	SWE_A#	SWE_A#	SWE_A#	SWE_A#
AP32	RSV	RSV	RSV	RSV	RSV	RSV
AP33	RSV	RSV	RSV	RSV	RSV	RSV
AP34	SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#
AP35	NC	NC	NC	NC	NC	NC
AR1	NC	NC	NC	NC	NC	NC
AR2	NC	NC	NC	NC	NC	NC
AR3	VSS	VSS	VSS	VSS	VSS	VSS
AR4	—	—	—	—	—	—
AR5	SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17
AR6	VSS	VSS	VSS	VSS	VSS	VSS
AR7	RSV	RSV	RSV	RSV	RSV	RSV
AR8	SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22
AR9	SCKE_B3	RSV	SCKE_B3	SCKE_B3	SCKE_B3	RSV
AR10	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR11	SCKE_A3	RSV	SCKE_A3	SCKE_A3	SCKE_A3	RSV
AR12	SMA_B11	SMA_B11	SMA_B11	SMA_B11	SMA_B11	SMA_B11
AR13	VSS	VSS	VSS	VSS	VSS	VSS
AR14	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR15	SMA_B4	SMA_B4	SMA_B4	SMA_B4	SMA_B4	SMA_B4
AR16	SMA_B3	SMA_B3	SMA_B3	SMA_B3	SMA_B3	SMA_B3
AR17	VSS	VSS	VSS	VSS	VSS	VSS
AR18	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM

Ball #	Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]
AR19	SBS_B1	SBS_B1	SBS_B1	SBS_B1	SBS_B1	SBS_B1
AR20	SMA_A6	SMA_A6	SMA_A6	SMA_A6	SMA_A6	SMA_A6
AR21	VSS	VSS	VSS	VSS	VSS	VSS
AR22	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR23	RSV	RSV	RSV	RSV	RSV	RSV
AR24	RSV	RSV	RSV	RSV	RSV	RSV
AR25	VSS	VSS	VSS	VSS	VSS	VSS
AR26	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR27	SWE_B#	SWE_B#	SWE_B#	SWE_B#	SWE_B#	SWE_B#
AR28	RSV	RSV	RSV	RSV	RSV	RSV
AR29	RSV	RSV	RSV	RSV	RSV	RSV
AR30	VSS	VSS	VSS	VSS	VSS	VSS
AR31	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR32	—	—	—	—	—	—
AR33	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AR34	NC	NC	NC	NC	NC	NC
AR35	NC	NC	NC	NC	NC	NC

NOTES:
1. DDR, PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
2. DDR, PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
3. DDR, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
4. DDR (One DIMM per Channel), No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
5. DDR (One DIMM per Channel), PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
6. DDR, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO

Table 14-4. GMCH/MCH Ballout for DDR Systems (Sorted by Signal Name)

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
BLUE	RSV	RSV	BLUE	BLUE	BLUE	H14
BLUE#	RSV	RSV	BLUE#	BLUE#	BLUE#	J14
BSEL0	BSEL0	BSEL0	BSEL0	BSEL0	BSEL0	H16
BSEL1	BSEL1	BSEL1	BSEL1	BSEL1	BSEL1	E15
BSEL2	BSEL2	BSEL2	BSEL2	BSEL2	BSEL2	D17
DDC_CLK	RSV	RSV	DDC_CLK	DDC_CLK	DDC_CLK	M15
DDC_DATA	RSV	RSV	DDC_DATA	DDC_DATA	DDC_DATA	L14
DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0	DMI_RXN0	U6
DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1	DMI_RXN1	T8
DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2	DMI_RXN2	V8
DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3	DMI_RXN3	U10
DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0	DMI_RXP0	U5
DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1	DMI_RXP1	T9
DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2	DMI_RXP2	V7
DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3	DMI_RXP3	V10
DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0	DMI_TXN0	T3
DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1	DMI_TXN1	U1
DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2	DMI_TXN2	V3
DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3	DMI_TXN3	W5
DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0	DMI_TXP0	R3
DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1	DMI_TXP1	T1
DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2	DMI_TXP2	U3
DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3	DMI_TXP3	V5
DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN	DREFCLKN	M12
DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP	DREFCLKP	M13
RSV	EXP_COMPI	EXP_COMPI	EXP_COMPI	RSV	RSV	W10
RSV	EXP_COMPO	EXP_COMPO	EXP_COMPO	RSV	RSV	Y10
SDVOC_TVCLKIN-	EXP_RXN0	EXP_RXN0	EXP_RXN0	SDVOC_ TVCLKIN-	SDVOC_ TVCLKIN-	F11
SDVOB_INT-	EXP_RXN1	EXP_RXN1	EXP_RXN1	SDVOB_INT-	SDVOB_INT-	H11
SDVOC_STALL-	EXP_RXN2	EXP_RXN2	EXP_RXN2	SDVOC_STALL-	SDVOC_STALL-	E9
RSV	EXP_RXN3	EXP_RXN3	EXP_RXN3	RSV	RSV	E7
RSV	EXP_RXN4	EXP_RXN4	EXP_RXN4	RSV	RSV	B4
SDVOC_INT-	EXP_RXN5	EXP_RXN5	EXP_RXN5	SDVOC_INT-	SDVOC_INT-	E5
RSV	EXP_RXN6	EXP_RXN6	EXP_RXN6	RSV	RSV	G5
RSV	EXP_RXN7	EXP_RXN7	EXP_RXN7	RSV	RSV	H7
RSV	EXP_RXN8	EXP_RXN8	EXP_RXN8	RSV	RSV	J5
RSV	EXP_RXN9	EXP_RXN9	EXP_RXN9	RSV	RSV	K7

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
RSV	EXP_RXN10	EXP_RXN10	EXP_RXN10	RSV	RSV	L5
RSV	EXP_RXN11	EXP_RXN11	EXP_RXN11	RSV	RSV	R10
RSV	EXP_RXN12	EXP_RXN12	EXP_RXN12	RSV	RSV	M7
RSV	EXP_RXN13	EXP_RXN13	EXP_RXN13	RSV	RSV	N5
RSV	EXP_RXN14	EXP_RXN14	EXP_RXN14	RSV	RSV	P8
RSV	EXP_RXN15	EXP_RXN15	EXP_RXN15	RSV	RSV	R5
SDVOC_TVCLKIN+	EXP_RXP0	EXP_RXP0	EXP_RXP0	SDVOC_ TVCLKIN+	SDVOC_ TVCLKIN+	E11
SDVOB_INT+	EXP_RXP1	EXP_RXP1	EXP_RXP1	SDVOB_INT+	SDVOB_INT+	J11
SDVOC_STALL+	EXP_RXP2	EXP_RXP2	EXP_RXP2	SDVOC_STALL+	SDVOC_STALL+	F9
RSV	EXP_RXP3	EXP_RXP3	EXP_RXP3	RSV	RSV	F7
RSV	EXP_RXP4	EXP_RXP4	EXP_RXP4	RSV	RSV	B3
SDVOC_INT+	EXP_RXP5	EXP_RXP5	EXP_RXP5	SDVOC_INT+	SDVOC_INT+	D5
RSV	EXP_RXP6	EXP_RXP6	EXP_RXP6	RSV	RSV	G6
RSV	EXP_RXP7	EXP_RXP7	EXP_RXP7	RSV	RSV	H8
RSV	EXP_RXP8	EXP_RXP8	EXP_RXP8	RSV	RSV	J6
RSV	EXP_RXP9	EXP_RXP9	EXP_RXP9	RSV	RSV	K8
RSV	EXP_RXP10	EXP_RXP10	EXP_RXP10	RSV	RSV	L6
RSV	EXP_RXP11	EXP_RXP11	EXP_RXP11	RSV	RSV	P10
RSV	EXP_RXP12	EXP_RXP12	EXP_RXP12	RSV	RSV	M8
RSV	EXP_RXP13	EXP_RXP13	EXP_RXP13	RSV	RSV	N6
RSV	EXP_RXP14	EXP_RXP14	EXP_RXP14	RSV	RSV	P7
RSV	EXP_RXP15	EXP_RXP15	EXP_RXP15	RSV	RSV	R6
RSV	EXP_SLR	EXP_SLR	EXP_SLR	RSV	RSV	A16
SDVOB_RED-	EXP_TXN0	EXP_TXN0	EXP_TXN0	SDVOB_RED-	SDVOB_RED-	C9
SDVOB_GREEN-	EXP_TXN1	EXP_TXN1	EXP_TXN1	SDVOB_GREEN-	SDVOB_GREEN-	A8
SDVOB_BLUE-	EXP_TXN2	EXP_TXN2	EXP_TXN2	SDVOB_BLUE-	SDVOB_BLUE-	C7
SDVOB_CLK-	EXP_TXN3	EXP_TXN3	EXP_TXN3	SDVOB_CLK-	SDVOB_CLK-	A6
SDVOC_RED-/ SDVOB_ALPHA-	EXP_TXN4	EXP_TXN4	EXP_TXN4	SDVOC_RED-/ SDVOB_ALPHA-	SDVOC_RED-/ SDVOB_ALPHA-	C5
SDVOC_GREEN-	EXP_TXN5	EXP_TXN5	EXP_TXN5	SDVOC_GREEN-	SDVOC_GREEN-	D2
SDVOC_BLUE-	EXP_TXN6	EXP_TXN6	EXP_TXN6	SDVOC_BLUE-	SDVOC_BLUE-	F3
SDVOC_CLK-	EXP_TXN7	EXP_TXN7	EXP_TXN7	SDVOC_CLK-	SDVOC_CLK-	G1
RSV	EXP_TXN8	EXP_TXN8	EXP_TXN8	RSV	RSV	H3
RSV	EXP_TXN9	EXP_TXN9	EXP_TXN9	RSV	RSV	J1
RSV	EXP_TXN10	EXP_TXN10	EXP_TXN10	RSV	RSV	K3
RSV	EXP_TXN11	EXP_TXN11	EXP_TXN11	RSV	RSV	L1
RSV	EXP_TXN12	EXP_TXN12	EXP_TXN12	RSV	RSV	M3
RSV	EXP_TXN13	EXP_TXN13	EXP_TXN13	RSV	RSV	N1
RSV	EXP_TXN14	EXP_TXN14	EXP_TXN14	RSV	RSV	P3
RSV	EXP_TXN15	EXP_TXN15	EXP_TXN15	RSV	RSV	R1

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SDVOB_RED+	EXP_TXP0	EXP_TXP0	EXP_TXP0	SDVOB_RED+	SDVOB_RED+	C10
SDVOB_GREEN+	EXP_TXP1	EXP_TXP1	EXP_TXP1	SDVOB_ GREEN+	SDVOB_ GREEN+	A9
SDVOB_BLUE+	EXP_TXP2	EXP_TXP2	EXP_TXP2	SDVOB_BLUE+	SDVOB_BLUE+	C8
SDVOB_CLK+	EXP_TXP3	EXP_TXP3	EXP_TXP3	SDVOB_CLK+	SDVOB_CLK+	A7
SDVOC_RED+/ SDVOB_ALPHA+	EXP_TXP4	EXP_TXP4	EXP_TXP4	SDVOC_RED+/ SDVOB_ ALPHA+	SDVOC_RED+/ SDVOB_ ALPHA+	C6
SDVOC_GREEN+	EXP_TXP5	EXP_TXP5	EXP_TXP5	SDVOC_GREEN +	SDVOC_GREEN +	C2
SDVOC_BLUE+	EXP_TXP6	EXP_TXP6	EXP_TXP6	SDVOC_BLUE+	SDVOC_BLUE+	E3
SDVOC_CLK+	EXP_TXP7	EXP_TXP7	EXP_TXP7	SDVOC_CLK+	SDVOC_CLK+	F1
RSV	EXP_TXP8	EXP_TXP8	EXP_TXP8	RSV	RSV	G3
RSV	EXP_TXP9	EXP_TXP9	EXP_TXP9	RSV	RSV	H1
RSV	EXP_TXP10	EXP_TXP10	EXP_TXP10	RSV	RSV	J3
RSV	EXP_TXP11	EXP_TXP11	EXP_TXP11	RSV	RSV	K1
RSV	EXP_TXP12	EXP_TXP12	EXP_TXP12	RSV	RSV	L3
RSV	EXP_TXP13	EXP_TXP13	EXP_TXP13	RSV	RSV	M1
RSV	EXP_TXP14	EXP_TXP14	EXP_TXP14	RSV	RSV	N3
RSV	EXP_TXP15	EXP_TXP15	EXP_TXP15	RSV	RSV	P1
EXTTS#	EXTTS#	EXTTS#	EXTTS#	EXTTS#	EXTTS#	K16
GCLKN	GCLKN	GCLKN	GCLKN	GCLKN	GCLKN	B11
GCLKP	GCLKP	GCLKP	GCLKP	GCLKP	GCLKP	A11
GREEN	RSV	RSV	GREEN	GREEN	GREEN	D14
GREEN#	RSV	RSV	GREEN#	GREEN#	GREEN#	E14
HA3#	HA3#	HA3#	HA3#	HA3#	HA3#	H29
HA4#	HA4#	HA4#	HA4#	HA4#	HA4#	K29
HA5#	HA5#	HA5#	HA5#	HA5#	HA5#	J29
HA6#	HA6#	HA6#	HA6#	HA6#	HA6#	G30
HA7#	HA7#	HA7#	HA7#	HA7#	HA7#	G32
HA8#	HA8#	HA8#	HA8#	HA8#	HA8#	K30
HA9#	HA9#	HA9#	HA9#	HA9#	HA9#	L29
HA10#	HA10#	HA10#	HA10#	HA10#	HA10#	M30
HA11#	HA11#	HA11#	HA11#	HA11#	HA11#	L31
HA12#	HA12#	HA12#	HA12#	HA12#	HA12#	L28
HA13#	HA13#	HA13#	HA13#	HA13#	HA13#	J28
HA14#	HA14#	HA14#	HA14#	HA14#	HA14#	K27
HA15#	HA15#	HA15#	HA15#	HA15#	HA15#	K33
HA16#	HA16#	HA16#	HA16#	HA16#	HA16#	M28
HA17#	HA17#	HA17#	HA17#	HA17#	HA17#	R29
HA18#	HA18#	HA18#	HA18#	HA18#	HA18#	L26

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
HA19#	HA19#	HA19#	HA19#	HA19#	HA19#	N26
HA20#	HA20#	HA20#	HA20#	HA20#	HA20#	M26
HA21#	HA21#	HA21#	HA21#	HA21#	HA21#	N31
HA22#	HA22#	HA22#	HA22#	HA22#	HA22#	P26
HA23#	HA23#	HA23#	HA23#	HA23#	HA23#	N29
HA24#	HA24#	HA24#	HA24#	HA24#	HA24#	P28
HA25#	HA25#	HA25#	HA25#	HA25#	HA25#	R28
HA26#	HA26#	HA26#	HA26#	HA26#	HA26#	N33
HA27#	HA27#	HA27#	HA27#	HA27#	HA27#	T27
HA28#	HA28#	HA28#	HA28#	HA28#	HA28#	T31
HA29#	HA29#	HA29#	HA29#	HA29#	HA29#	U28
HA30#	HA30#	HA30#	HA30#	HA30#	HA30#	T26
HA31#	HA31#	HA31#	HA31#	HA31#	HA31#	T29
HADS#	HADS#	HADS#	HADS#	HADS#	HADS#	M31
HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#	HADSTB0#	J31
HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#	HADSTB1#	N27
HBNR#	HBNR#	HBNR#	HBNR#	HBNR#	HBNR#	M35
HBPRI#	HBPRI#	HBPRI#	HBPRI#	HBPRI#	HBPRI#	E30
HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#	HBREQ0#	R33
HCLKN	HCLKN	HCLKN	HCLKN	HCLKN	HCLKN	M22
HCLKP	HCLKP	HCLKP	HCLKP	HCLKP	HCLKP	M23
HCPURST#	HCPURST#	HCPURST#	HCPURST#	HCPURST#	HCPURST#	G24
HD0	HD0	HD0	HD0	HD0	HD0	J33
HD1	HD1	HD1	HD1	HD1	HD1	H33
HD2	HD2	HD2	HD2	HD2	HD2	J34
HD3	HD3	HD3	HD3	HD3	HD3	G35
HD4	HD4	HD4	HD4	HD4	HD4	H35
HD5	HD5	HD5	HD5	HD5	HD5	G34
HD6	HD6	HD6	HD6	HD6	HD6	F34
HD7	HD7	HD7	HD7	HD7	HD7	G33
HD8	HD8	HD8	HD8	HD8	HD8	D34
HD9	HD9	HD9	HD9	HD9	HD9	C33
HD10	HD10	HD10	HD10	HD10	HD10	D33
HD11	HD11	HD11	HD11	HD11	HD11	B34
HD12	HD12	HD12	HD12	HD12	HD12	C34
HD13	HD13	HD13	HD13	HD13	HD13	B33
HD14	HD14	HD14	HD14	HD14	HD14	C32
HD15	HD15	HD15	HD15	HD15	HD15	B32
HD16	HD16	HD16	HD16	HD16	HD16	E28
HD17	HD17	HD17	HD17	HD17	HD17	C30

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
HD18	HD18	HD18	HD18	HD18	HD18	D29
HD19	HD19	HD19	HD19	HD19	HD19	H28
HD20	HD20	HD20	HD20	HD20	HD20	G29
HD21	HD21	HD21	HD21	HD21	HD21	J27
HD22	HD22	HD22	HD22	HD22	HD22	F28
HD23	HD23	HD23	HD23	HD23	HD23	F27
HD24	HD24	HD24	HD24	HD24	HD24	E27
HD25	HD25	HD25	HD25	HD25	HD25	E25
HD26	HD26	HD26	HD26	HD26	HD26	G25
HD27	HD27	HD27	HD27	HD27	HD27	J25
HD28	HD28	HD28	HD28	HD28	HD28	K25
HD29	HD29	HD29	HD29	HD29	HD29	L25
HD30	HD30	HD30	HD30	HD30	HD30	L23
HD31	HD31	HD31	HD31	HD31	HD31	K23
HD32	HD32	HD32	HD32	HD32	HD32	J22
HD33	HD33	HD33	HD33	HD33	HD33	J24
HD34	HD34	HD34	HD34	HD34	HD34	K22
HD35	HD35	HD35	HD35	HD35	HD35	J21
HD36	HD36	HD36	HD36	HD36	HD36	M21
HD37	HD37	HD37	HD37	HD37	HD37	H23
HD38	HD38	HD38	HD38	HD38	HD38	M19
HD39	HD39	HD39	HD39	HD39	HD39	K21
HD40	HD40	HD40	HD40	HD40	HD40	H20
HD41	HD41	HD41	HD41	HD41	HD41	H19
HD42	HD42	HD42	HD42	HD42	HD42	M18
HD43	HD43	HD43	HD43	HD43	HD43	K18
HD44	HD44	HD44	HD44	HD44	HD44	K17
HD45	HD45	HD45	HD45	HD45	HD45	G18
HD46	HD46	HD46	HD46	HD46	HD46	H18
HD47	HD47	HD47	HD47	HD47	HD47	F17
HD48	HD48	HD48	HD48	HD48	HD48	A25
HD49	HD49	HD49	HD49	HD49	HD49	C27
HD50	HD50	HD50	HD50	HD50	HD50	C31
HD51	HD51	HD51	HD51	HD51	HD51	B30
HD52	HD52	HD52	HD52	HD52	HD52	B31
HD53	HD53	HD53	HD53	HD53	HD53	A31
HD54	HD54	HD54	HD54	HD54	HD54	B27
HD55	HD55	HD55	HD55	HD55	HD55	A29
HD56	HD56	HD56	HD56	HD56	HD56	C28
HD57	HD57	HD57	HD57	HD57	HD57	A28

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
HD58	HD58	HD58	HD58	HD58	HD58	C25
HD59	HD59	HD59	HD59	HD59	HD59	C26
HD60	HD60	HD60	HD60	HD60	HD60	D27
HD61	HD61	HD61	HD61	HD61	HD61	A27
HD62	HD62	HD62	HD62	HD62	HD62	E24
HD63	HD63	HD63	HD63	HD63	HD63	B25
HDBSY#	HDBSY#	HDBSY#	HDBSY#	HDBSY#	HDBSY#	L35
HDEFER#	HDEFER#	HDEFER#	HDEFER#	HDEFER#	HDEFER#	J35
HDINV0#	HDINV0#	HDINV0#	HDINV0#	HDINV0#	HDINV0#	E34
HDINV1#	HDINV1#	HDINV1#	HDINV1#	HDINV1#	HDINV1#	J26
HDINV2#	HDINV2#	HDINV2#	HDINV2#	HDINV2#	HDINV2#	K19
HDINV3#	HDINV3#	HDINV3#	HDINV3#	HDINV3#	HDINV3#	B26
HDRDY#	HDRDY#	HDRDY#	HDRDY#	HDRDY#	HDRDY#	M32
HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#	HDSTBN0#	E35
HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#	HDSTBN1#	F26
HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#	HDSTBN2#	F19
HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#	HDSTBN3#	C29
HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#	HDSTBP0#	E33
HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#	HDSTBP1#	H26
HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#	HDSTBP2#	J19
HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#	HDSTBP3#	B29
HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#	HEDRDY#	P33
HHIT#	HHIT#	HHIT#	HHIT#	HHIT#	HHIT#	L34
HHITM#	HHITM#	HHITM#	HHITM#	HHITM#	HHITM#	N35
HLOCK#	HLOCK#	HLOCK#	HLOCK#	HLOCK#	HLOCK#	L33
HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#	HPCREQ#	E31
HRCOMP	HRCOMP	HRCOMP	HRCOMP	HRCOMP	HRCOMP	B23
HREQ0#	HREQ0#	HREQ0#	HREQ0#	HREQ0#	HREQ0#	F33
HREQ1#	HREQ1#	HREQ1#	HREQ1#	HREQ1#	HREQ1#	E32
HREQ2#	HREQ2#	HREQ2#	HREQ2#	HREQ2#	HREQ2#	H31
HREQ3#	HREQ3#	HREQ3#	HREQ3#	HREQ3#	HREQ3#	G31
HREQ4#	HREQ4#	HREQ4#	HREQ4#	HREQ4#	HREQ4#	F31
HRS0#	HRS0#	HRS0#	HRS0#	HRS0#	HRS0#	K34
HRS1#	HRS1#	HRS1#	HRS1#	HRS1#	HRS1#	P34
HRS2#	HRS2#	HRS2#	HRS2#	HRS2#	HRS2#	J32
HSCOMP	HSCOMP	HSCOMP	HSCOMP	HSCOMP	HSCOMP	D24
HSWING	HSWING	HSWING	HSWING	HSWING	HSWING	A23
HSYNC	RSV	RSV	HSYNC	HSYNC	HSYNC	E12
HTRDY#	HTRDY#	HTRDY#	HTRDY#	HTRDY#	HTRDY#	N34
HVREF	HVREF	HVREF	HVREF	HVREF	HVREF	A24

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	ICH_SYNC#	M14
MTYPE	MTYPE	MTYPE	MTYPE	MTYPE	MTYPE	C15
NC	NC	NC	NC	NC	NC	A2
NC	NC	NC	NC	NC	NC	A34
NC	NC	NC	NC	NC	NC	A35
NC	NC	NC	NC	NC	NC	AA12
NC	NC	NC	NC	NC	NC	AB12
NC	NC	NC	NC	NC	NC	AC23
NC	NC	NC	NC	NC	NC	AC24
NC	NC	NC	NC	NC	NC	AD30
NC	NC	NC	NC	NC	NC	AG6
NC	NC	NC	NC	NC	NC	AH24
NC	NC	NC	NC	NC	NC	AJ14
NC	NC	NC	NC	NC	NC	AL28
NC	NC	NC	NC	NC	NC	AN19
NC	NC	NC	NC	NC	NC	AP1
NC	NC	NC	NC	NC	NC	AP35
NC	NC	NC	NC	NC	NC	AR1
NC	NC	NC	NC	NC	NC	AR2
NC	NC	NC	NC	NC	NC	AR34
NC	NC	NC	NC	NC	NC	AR35
NC	NC	NC	NC	NC	NC	B1
NC	NC	NC	NC	NC	NC	B35
NC	NC	NC	NC	NC	NC	C16
NC	NC	NC	NC	NC	NC	E16
NC	NC	NC	NC	NC	NC	F12
NC	NC	NC	NC	NC	NC	F24
NC	NC	NC	NC	NC	NC	G12
NC	NC	NC	NC	NC	NC	H12
NC	NC	NC	NC	NC	NC	H15
NC	NC	NC	NC	NC	NC	H17
NC	NC	NC	NC	NC	NC	J12
NC	NC	NC	NC	NC	NC	K12
NC	NC	NC	NC	NC	NC	L12
NC	NC	NC	NC	NC	NC	L19
NC	NC	NC	NC	NC	NC	N12
NC	NC	NC	NC	NC	NC	N22
NC	NC	NC	NC	NC	NC	N23
NC	NC	NC	NC	NC	NC	N24
NC	NC	NC	NC	NC	NC	P12

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
NC	NC	NC	NC	NC	NC	P23
NC	NC	NC	NC	NC	NC	P24
NC	NC	NC	NC	NC	NC	P30
NC	NC	NC	NC	NC	NC	R12
NC	NC	NC	NC	NC	NC	R24
NC	NC	NC	NC	NC	NC	T12
NC	NC	NC	NC	NC	NC	U12
NC	NC	NC	NC	NC	NC	V12
NC	NC	NC	NC	NC	NC	W12
NC	NC	NC	NC	NC	NC	Y12
PWROK	PWROK	PWROK	PWROK	PWROK	PWROK	AG7
RED	RSV	RSV	RED	RED	RED	F14
RED#	RSV	RSV	RED#	RED#	RED#	G14
REFSET	RSV	RSV	REFSET	REFSET	REFSET	A15
RSTIN#	RSTIN#	RSTIN#	RSTIN#	RSTIN#	RSTIN#	AF7
RSV	RSV	RSV	RSV	RSV	RSV	AA30
RSV	RSV	RSV	RSV	RSV	RSV	AA31
RSV	RSV	RSV	RSV	RSV	RSV	AA35
RSV	RSV	RSV	RSV	RSV	RSV	AB29
RSV	RSV	RSV	RSV	RSV	RSV	AC12
RSV	RSV	RSV	RSV	RSV	RSV	AC13
RSV	RSV	RSV	RSV	RSV	RSV	AC14
RSV	RSV	RSV	RSV	RSV	RSV	AC15
RSV	RSV	RSV	RSV	RSV	RSV	AC16
RSV	RSV	RSV	RSV	RSV	RSV	AC17
RSV	RSV	RSV	RSV	RSV	RSV	AC18
RSV	RSV	RSV	RSV	RSV	RSV	AC19
RSV	RSV	RSV	RSV	RSV	RSV	AC20
RSV	RSV	RSV	RSV	RSV	RSV	AC21
RSV	RSV	RSV	RSV	RSV	RSV	AC22
RSV	RSV	RSV	RSV	RSV	RSV	AC30
RSV	RSV	RSV	RSV	RSV	RSV	AE5
RSV	RSV	RSV	RSV	RSV	RSV	AF20
RSV	RSV	RSV	RSV	RSV	RSV	AF5
RSV	RSV	RSV	RSV	RSV	RSV	AG17
RSV	RSV	RSV	RSV	RSV	RSV	AG2
RSV	RSV	RSV	RSV	RSV	RSV	AG26
RSV	RSV	RSV	RSV	RSV	RSV	AG33
RSV	RSV	RSV	RSV	RSV	RSV	AH10
RSV	RSV	RSV	RSV	RSV	RSV	AH30

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
RSV	RSV	RSV	RSV	RSV	RSV	AJ18
RSV	RSV	RSV	RSV	RSV	RSV	AJ20
RSV	RSV	RSV	RSV	RSV	RSV	AJ21
RSV	RSV	RSV	RSV	RSV	RSV	AJ23
RSV	RSV	RSV	RSV	RSV	RSV	AJ24
RSV	RSV	RSV	RSV	RSV	RSV	AK18
RSV	RSV	RSV	RSV	RSV	RSV	AK21
RSV	RSV	RSV	RSV	RSV	RSV	AK24
RSV	RSV	RSV	RSV	RSV	RSV	AL14
RSV	RSV	RSV	RSV	RSV	RSV	AL2
RSV	RSV	RSV	RSV	RSV	RSV	AL20
RSV	RSV	RSV	RSV	RSV	RSV	AL21
RSV	RSV	RSV	RSV	RSV	RSV	AL24
RSV	RSV	RSV	RSV	RSV	RSV	AL29
RSV	RSV	RSV	RSV	RSV	RSV	AL4
RSV	RSV	RSV	RSV	RSV	RSV	AN31
RSV	RSV	RSV	RSV	RSV	RSV	AN32
RSV	RSV	RSV	RSV	RSV	RSV	AP23
RSV	RSV	RSV	RSV	RSV	RSV	AP29
RSV	RSV	RSV	RSV	RSV	RSV	AP30
RSV	RSV	RSV	RSV	RSV	RSV	AP32
RSV	RSV	RSV	RSV	RSV	RSV	AP33
RSV	RSV	RSV	RSV	RSV	RSV	AR23
RSV	RSV	RSV	RSV	RSV	RSV	AR24
RSV	RSV	RSV	RSV	RSV	RSV	AR28
RSV	RSV	RSV	RSV	RSV	RSV	AR29
RSV	RSV	RSV	RSV	RSV	RSV	AR7
RSV	RSV	RSV	RSV	RSV	RSV	B15
RSV	RSV	RSV	RSV	RSV	RSV	C14
RSV	RSV	RSV	RSV	RSV	RSV	F15
RSV	RSV	RSV	RSV	RSV	RSV	G16
RSV	RSV	RSV	RSV	RSV	RSV	K15
RSV	RSV	RSV	RSV	RSV	RSV	M16
RSV	RSV	RSV	RSV	RSV	RSV	R30
RSV	RSV	RSV	RSV	RSV	RSV	R31
RSV	RSV	RSV	RSV	RSV	RSV	R35
RSV	RSV	RSV	RSV	RSV	RSV	U30
RSV	RSV	RSV	RSV	RSV	RSV	U35
RSV	RSV	RSV	RSV	RSV	RSV	V30
RSV	RSV	RSV	RSV	RSV	RSV	V31

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
RSV	RSV	RSV	RSV	RSV	RSV	V32
RSV	RSV	RSV	RSV	RSV	RSV	Y28
RSV	RSV	RSV	RSV	RSV	RSV	Y30
RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0	RSV_TP0	AE16
RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1	RSV_TP1	AH15
RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2	RSV_TP2	AN14
RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3	RSV_TP3	AK15
SBS_A0	SBS_A0	SBS_A0	SBS_A0	SBS_A0	SBS_A0	AN28
SBS_A1	SBS_A1	SBS_A1	SBS_A1	SBS_A1	SBS_A1	AP26
SBS_B0	SBS_B0	SBS_B0	SBS_B0	SBS_B0	SBS_B0	AM27
SBS_B1	SBS_B1	SBS_B1	SBS_B1	SBS_B1	SBS_B1	AR19
SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#	SCAS_A#	AL34
SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#	SCAS_B#	AN27
SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0	SCKE_A0	AL12
SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1	SCKE_A1	AN11
SCKE_A2	RSV	SCKE_A2	SCKE_A2	SCKE_A2	RSV	AP11
SCKE_A3	RSV	SCKE_A3	SCKE_A3	SCKE_A3	RSV	AR11
SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0	SCKE_B0	AN10
SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1	SCKE_B1	AM9
SCKE_B2	RSV	SCKE_B2	SCKE_B2	SCKE_B2	RSV	AP10
SCKE_B3	RSV	SCKE_B3	SCKE_B3	SCKE_B3	RSV	AR9
SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0	SCLK_A0	AM24
SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#	SCLK_A0#	AN25
SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1	SCLK_A1	AN2
SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#	SCLK_A1#	AN3
SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2	SCLK_A2	AB34
SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#	SCLK_A2#	AC33
SCLK_A3	RSV	SCLK_A3	SCLK_A3	SCLK_A3	RSV	AP25
SCLK_A3#	RSV	SCLK_A3#	SCLK_A3#	SCLK_A3#	RSV	AN26
SCLK_A4	RSV	SCLK_A4	SCLK_A4	SCLK_A4	RSV	AM2
SCLK_A4#	RSV	SCLK_A4#	SCLK_A4#	SCLK_A4#	RSV	AM3
SCLK_A5	RSV	SCLK_A5	SCLK_A5	SCLK_A5	RSV	AC35
SCLK_A5#	RSV	SCLK_A5#	SCLK_A5#	SCLK_A5#	RSV	AC34
SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0	SCLK_B0	AH22
SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#	SCLK_B0#	AG23
SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1	SCLK_B1	AL11
SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#	SCLK_B1#	AJ11
SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2	SCLK_B2	AE26
SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#	SCLK_B2#	AE25
SCLK_B3	RSV	SCLK_B3	SCLK_B3	SCLK_B3	RSV	AL23

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SCLK_B3#	RSV	SCLK_B3#	SCLK_B3#	SCLK_B3#	RSV	AK22
SCLK_B4	RSV	SCLK_B4	SCLK_B4	SCLK_B4	RSV	AK9
SCLK_B4#	RSV	SCLK_B4#	SCLK_B4#	SCLK_B4#	RSV	AL9
SCLK_B5	RSV	SCLK_B5	SCLK_B5	SCLK_B5	RSV	AD29
SCLK_B5#	RSV	SCLK_B5#	SCLK_B5#	SCLK_B5#	RSV	AD28
SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#	SCS_A0#	AM34
SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#	SCS_A1#	AL35
SCS_A2#	RSV	SCS_A2#	SCS_A2#	SCS_A2#	RSV	AK34
SCS_A3#	RSV	SCS_A3#	SCS_A3#	SCS_A3#	RSV	AL33
SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#	SCS_B0#	AP34
SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#	SCS_B1#	AN34
SCS_B2#	RSV	SCS_B2#	SCS_B2#	SCS_B2#	RSV	AN33
SCS_B3#	RSV	SCS_B3#	SCS_B3#	SCS_B3#	RSV	AM33
SDM_A0	SDM_A0	SDM_A0	SDM_A0	SDM_A0	SDM_A0	AF2
SDM_A1	SDM_A1	SDM_A1	SDM_A1	SDM_A1	SDM_A1	AL1
SDM_A2	SDM_A2	SDM_A2	SDM_A2	SDM_A2	SDM_A2	AN7
SDM_A3	SDM_A3	SDM_A3	SDM_A3	SDM_A3	SDM_A3	AH16
SDM_A4	SDM_A4	SDM_A4	SDM_A4	SDM_A4	SDM_A4	AK29
SDM_A5	SDM_A5	SDM_A5	SDM_A5	SDM_A5	SDM_A5	AG34
SDM_A6	SDM_A6	SDM_A6	SDM_A6	SDM_A6	SDM_A6	AA33
SDM_A7	SDM_A7	SDM_A7	SDM_A7	SDM_A7	SDM_A7	U33
SDM_B0	SDM_B0	SDM_B0	SDM_B0	SDM_B0	SDM_B0	AJ5
SDM_B1	SDM_B1	SDM_B1	SDM_B1	SDM_B1	SDM_B1	AH9
SDM_B2	SDM_B2	SDM_B2	SDM_B2	SDM_B2	SDM_B2	AH13
SDM_B3	SDM_B3	SDM_B3	SDM_B3	SDM_B3	SDM_B3	AG20
SDM_B4	SDM_B4	SDM_B4	SDM_B4	SDM_B4	SDM_B4	AG24
SDM_B5	SDM_B5	SDM_B5	SDM_B5	SDM_B5	SDM_B5	AH31
SDM_B6	SDM_B6	SDM_B6	SDM_B6	SDM_B6	SDM_B6	AD24
SDM_B7	SDM_B7	SDM_B7	SDM_B7	SDM_B7	SDM_B7	W31
SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0	SDQ_A0	AE3
SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1	SDQ_A1	AF3
SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2	SDQ_A2	AH2
SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3	SDQ_A3	AJ2
SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4	SDQ_A4	AE2
SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5	SDQ_A5	AE1
SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6	SDQ_A6	AG3
SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7	SDQ_A7	AH3
SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8	SDQ_A8	AJ1
SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9	SDQ_A9	AK2
SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10	SDQ_A10	AN4

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11	SDQ_A11	AP4
SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12	SDQ_A12	AJ3
SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13	SDQ_A13	AK3
SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14	SDQ_A14	AP2
SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15	SDQ_A15	AP3
SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16	SDQ_A16	AP5
SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17	SDQ_A17	AR5
SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18	SDQ_A18	AN8
SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19	SDQ_A19	AP9
SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20	SDQ_A20	AN5
SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21	SDQ_A21	AP6
SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22	SDQ_A22	AR8
SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23	SDQ_A23	AN9
SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24	SDQ_A24	AK16
SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25	SDQ_A25	AL17
SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26	SDQ_A26	AD17
SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27	SDQ_A27	AF19
SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28	SDQ_A28	AF16
SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29	SDQ_A29	AJ17
SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30	SDQ_A30	AE19
SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31	SDQ_A31	AH18
SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32	SDQ_A32	AH27
SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33	SDQ_A33	AK27
SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34	SDQ_A34	AN30
SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35	SDQ_A35	AK31
SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36	SDQ_A36	AL27
SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37	SDQ_A37	AJ28
SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38	SDQ_A38	AL30
SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39	SDQ_A39	AL31
SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40	SDQ_A40	AJ34
SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41	SDQ_A41	AH35
SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42	SDQ_A42	AG32
SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43	SDQ_A43	AF34
SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44	SDQ_A44	AJ33
SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45	SDQ_A45	AH33
SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46	SDQ_A46	AF33
SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47	SDQ_A47	AE33
SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48	SDQ_A48	AE35
SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49	SDQ_A49	AE34
SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50	SDQ_A50	Y33

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51	SDQ_A51	W34
SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52	SDQ_A52	AD31
SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53	SDQ_A53	AD35
SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54	SDQ_A54	AA32
SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55	SDQ_A55	Y35
SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56	SDQ_A56	V34
SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57	SDQ_A57	V33
SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58	SDQ_A58	R32
SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59	SDQ_A59	R34
SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60	SDQ_A60	W35
SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61	SDQ_A61	W33
SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62	SDQ_A62	T33
SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63	SDQ_A63	T35
SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0	SDQ_B0	AH7
SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1	SDQ_B1	AJ6
SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2	SDQ_B2	AL5
SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3	SDQ_B3	AN6
SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4	SDQ_B4	AG9
SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5	SDQ_B5	AH4
SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6	SDQ_B6	AM5
SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7	SDQ_B7	AL6
SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8	SDQ_B8	AJ7
SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9	SDQ_B9	AL7
SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10	SDQ_B10	AF11
SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11	SDQ_B11	AE11
SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12	SDQ_B12	AJ8
SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13	SDQ_B13	AL8
SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14	SDQ_B14	AG10
SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15	SDQ_B15	AG11
SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16	SDQ_B16	AE13
SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17	SDQ_B17	AF13
SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18	SDQ_B18	AG14
SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19	SDQ_B19	AD14
SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20	SDQ_B20	AD12
SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21	SDQ_B21	AH12
SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22	SDQ_B22	AF14
SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23	SDQ_B23	AD15
SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24	SDQ_B24	AD18
SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25	SDQ_B25	AK19
SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26	SDQ_B26	AE22

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27	SDQ_B27	AH21
SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28	SDQ_B28	AL18
SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29	SDQ_B29	AH19
SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30	SDQ_B30	AF22
SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31	SDQ_B31	AD21
SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32	SDQ_B32	AF23
SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33	SDQ_B33	AF25
SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34	SDQ_B34	AL25
SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35	SDQ_B35	AJ26
SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36	SDQ_B36	AD23
SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37	SDQ_B37	AF24
SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38	SDQ_B38	AJ25
SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39	SDQ_B39	AL26
SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40	SDQ_B40	AJ29
SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41	SDQ_B41	AJ31
SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42	SDQ_B42	AG30
SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43	SDQ_B43	AG31
SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44	SDQ_B44	AK33
SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45	SDQ_B45	AK32
SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46	SDQ_B46	AG27
SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47	SDQ_B47	AF28
SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48	SDQ_B48	AE31
SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49	SDQ_B49	AF27
SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50	SDQ_B50	AB27
SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51	SDQ_B51	AB26
SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52	SDQ_B52	AE29
SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53	SDQ_B53	AE27
SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54	SDQ_B54	AC28
SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55	SDQ_B55	AC26
SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56	SDQ_B56	AA29
SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57	SDQ_B57	W29
SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58	SDQ_B58	U26
SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59	SDQ_B59	V29
SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60	SDQ_B60	Y26
SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61	SDQ_B61	AA28
SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62	SDQ_B62	W26
SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63	SDQ_B63	V28
SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0	SDQS_A0	AG1
SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1	SDQS_A1	AL3
SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2	SDQS_A2	AP7

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3	SDQS_A3	AF17
SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4	SDQS_A4	AM30
SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5	SDQS_A5	AG35
SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6	SDQS_A6	AA34
SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7	SDQS_A7	U34
SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0	SDQS_B0	AK5
SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1	SDQS_B1	AK10
SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2	SDQS_B2	AK13
SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3	SDQS_B3	AD20
SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4	SDQS_B4	AH25
SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5	SDQS_B5	AH28
SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6	SDQS_B6	AB31
SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7	SDQS_B7	W27
SDVO_CTRLCLK	RSV	RSV	SDVO_CTRLCLK	SDVO_CTRLCLK	SDVO_CTRLCLK	J13
SDVO_CTRLDATA	RSV	RSV	SDVO_CTRLDATA	SDVO_CTRLDATA	SDVO_CTRLDATA	K13
SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	SM_SLEWIN0	AJ12
SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	SM_SLEWIN1	AF9
SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	SM_SLEWOUT0	AK12
SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	SM_SLEWOUT1	AE10
SMA_A0	SMA_A0	SMA_A0	SMA_A0	SMA_A0	SMA_A0	AN22
SMA_A1	SMA_A1	SMA_A1	SMA_A1	SMA_A1	SMA_A1	AP22
SMA_A2	SMA_A2	SMA_A2	SMA_A2	SMA_A2	SMA_A2	AN21
SMA_A3	SMA_A3	SMA_A3	SMA_A3	SMA_A3	SMA_A3	AP21
SMA_A4	SMA_A4	SMA_A4	SMA_A4	SMA_A4	SMA_A4	AM21
SMA_A5	SMA_A5	SMA_A5	SMA_A5	SMA_A5	SMA_A5	AP19
SMA_A6	SMA_A6	SMA_A6	SMA_A6	SMA_A6	SMA_A6	AR20
SMA_A7	SMA_A7	SMA_A7	SMA_A7	SMA_A7	SMA_A7	AN16
SMA_A8	SMA_A8	SMA_A8	SMA_A8	SMA_A8	SMA_A8	AN18
SMA_A9	SMA_A9	SMA_A9	SMA_A9	SMA_A9	SMA_A9	AM15
SMA_A10	SMA_A10	SMA_A10	SMA_A10	SMA_A10	SMA_A10	AN23
SMA_A11	SMA_A11	SMA_A11	SMA_A11	SMA_A11	SMA_A11	AP15
SMA_A12	SMA_A12	SMA_A12	SMA_A12	SMA_A12	SMA_A12	AP13
SMA_A13	SMA_A13	SMA_A13	SMA_A13	SMA_A13	SMA_A13	AB33
SMA_B0	SMA_B0	SMA_B0	SMA_B0	SMA_B0	SMA_B0	AM18
SMA_B1	SMA_B1	SMA_B1	SMA_B1	SMA_B1	SMA_B1	AP18
SMA_B2	SMA_B2	SMA_B2	SMA_B2	SMA_B2	SMA_B2	AN17
SMA_B3	SMA_B3	SMA_B3	SMA_B3	SMA_B3	SMA_B3	AR16

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
SMA_B4	SMA_B4	SMA_B4	SMA_B4	SMA_B4	SMA_B4	AR15
SMA_B5	SMA_B5	SMA_B5	SMA_B5	SMA_B5	SMA_B5	AN15
SMA_B6	SMA_B6	SMA_B6	SMA_B6	SMA_B6	SMA_B6	AP17
SMA_B7	SMA_B7	SMA_B7	SMA_B7	SMA_B7	SMA_B7	AL15
SMA_B8	SMA_B8	SMA_B8	SMA_B8	SMA_B8	SMA_B8	AP14
SMA_B9	SMA_B9	SMA_B9	SMA_B9	SMA_B9	SMA_B9	AN13
SMA_B10	SMA_B10	SMA_B10	SMA_B10	SMA_B10	SMA_B10	AN20
SMA_B11	SMA_B11	SMA_B11	SMA_B11	SMA_B11	SMA_B11	AR12
SMA_B12	SMA_B12	SMA_B12	SMA_B12	SMA_B12	SMA_B12	AM12
SMA_B13	SMA_B13	SMA_B13	SMA_B13	SMA_B13	SMA_B13	AD32
SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#	SRAS_A#	AN29
SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#	SRAS_B#	AP27
SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0	SRCOMP0	AG4
SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1	SRCOMP1	AG8
SVREF0	SVREF0	SVREF0	SVREF0	SVREF0	SVREF0	AE7
SVREF1	SVREF1	SVREF1	SVREF1	SVREF1	SVREF1	AE8
SWE_A#	SWE_A#	SWE_A#	SWE_A#	SWE_A#	SWE_A#	AP31
SWE_B#	SWE_B#	SWE_B#	SWE_B#	SWE_B#	SWE_B#	AR27
VCC	VCC	VCC	VCC	VCC	VCC	AA13
VCC	VCC	VCC	VCC	VCC	VCC	AA14
VCC	VCC	VCC	VCC	VCC	VCC	AA16
VCC	VCC	VCC	VCC	VCC	VCC	AA18
VCC	VCC	VCC	VCC	VCC	VCC	AA20
VCC	VCC	VCC	VCC	VCC	VCC	AA21
VCC	VCC	VCC	VCC	VCC	VCC	AA22
VCC	VCC	VCC	VCC	VCC	VCC	AA23
VCC	VCC	VCC	VCC	VCC	VCC	AA24
VCC	VCC	VCC	VCC	VCC	VCC	AB1
VCC	VCC	VCC	VCC	VCC	VCC	AB10
VCC	VCC	VCC	VCC	VCC	VCC	AB11
VCC	VCC	VCC	VCC	VCC	VCC	AB13
VCC	VCC	VCC	VCC	VCC	VCC	AB14
VCC	VCC	VCC	VCC	VCC	VCC	AB15
VCC	VCC	VCC	VCC	VCC	VCC	AB16
VCC	VCC	VCC	VCC	VCC	VCC	AB17
VCC	VCC	VCC	VCC	VCC	VCC	AB18
VCC	VCC	VCC	VCC	VCC	VCC	AB19
VCC	VCC	VCC	VCC	VCC	VCC	AB2
VCC	VCC	VCC	VCC	VCC	VCC	AB20
VCC	VCC	VCC	VCC	VCC	VCC	AB21

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VCC	VCC	VCC	VCC	VCC	VCC	AB22
VCC	VCC	VCC	VCC	VCC	VCC	AB23
VCC	VCC	VCC	VCC	VCC	VCC	AB24
VCC	VCC	VCC	VCC	VCC	VCC	AB3
VCC	VCC	VCC	VCC	VCC	VCC	AB4
VCC	VCC	VCC	VCC	VCC	VCC	AB5
VCC	VCC	VCC	VCC	VCC	VCC	AB6
VCC	VCC	VCC	VCC	VCC	VCC	AB7
VCC	VCC	VCC	VCC	VCC	VCC	AB8
VCC	VCC	VCC	VCC	VCC	VCC	AB9
VCC	VCC	VCC	VCC	VCC	VCC	AC1
VCC	VCC	VCC	VCC	VCC	VCC	AC10
VCC	VCC	VCC	VCC	VCC	VCC	AC11
VCC	VCC	VCC	VCC	VCC	VCC	AC2
VCC	VCC	VCC	VCC	VCC	VCC	AC3
VCC	VCC	VCC	VCC	VCC	VCC	AC4
VCC	VCC	VCC	VCC	VCC	VCC	AC5
VCC	VCC	VCC	VCC	VCC	VCC	AC6
VCC	VCC	VCC	VCC	VCC	VCC	AC7
VCC	VCC	VCC	VCC	VCC	VCC	AC8
VCC	VCC	VCC	VCC	VCC	VCC	AC9
VCC	VCC	VCC	VCC	VCC	VCC	AD1
VCC	VCC	VCC	VCC	VCC	VCC	AD10
VCC	VCC	VCC	VCC	VCC	VCC	AD2
VCC	VCC	VCC	VCC	VCC	VCC	AD3
VCC	VCC	VCC	VCC	VCC	VCC	AD4
VCC	VCC	VCC	VCC	VCC	VCC	AD5
VCC	VCC	VCC	VCC	VCC	VCC	AD6
VCC	VCC	VCC	VCC	VCC	VCC	AD7
VCC	VCC	VCC	VCC	VCC	VCC	AD8
VCC	VCC	VCC	VCC	VCC	VCC	AD9
VCC	VCC	VCC	VCC	VCC	VCC	L10
VCC	VCC	VCC	VCC	VCC	VCC	N13
VCC	VCC	VCC	VCC	VCC	VCC	N14
VCC	VCC	VCC	VCC	VCC	VCC	N15
VCC	VCC	VCC	VCC	VCC	VCC	N16
VCC	VCC	VCC	VCC	VCC	VCC	N18
VCC	VCC	VCC	VCC	VCC	VCC	N20
VCC	VCC	VCC	VCC	VCC	VCC	N21
VCC	VCC	VCC	VCC	VCC	VCC	P13

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VCC	VCC	VCC	VCC	VCC	VCC	P14
VCC	VCC	VCC	VCC	VCC	VCC	P15
VCC	VCC	VCC	VCC	VCC	VCC	P17
VCC	VCC	VCC	VCC	VCC	VCC	P19
VCC	VCC	VCC	VCC	VCC	VCC	P21
VCC	VCC	VCC	VCC	VCC	VCC	P22
VCC	VCC	VCC	VCC	VCC	VCC	R13
VCC	VCC	VCC	VCC	VCC	VCC	R14
VCC	VCC	VCC	VCC	VCC	VCC	R15
VCC	VCC	VCC	VCC	VCC	VCC	R16
VCC	VCC	VCC	VCC	VCC	VCC	R18
VCC	VCC	VCC	VCC	VCC	VCC	R20
VCC	VCC	VCC	VCC	VCC	VCC	R22
VCC	VCC	VCC	VCC	VCC	VCC	R23
VCC	VCC	VCC	VCC	VCC	VCC	T13
VCC	VCC	VCC	VCC	VCC	VCC	T14
VCC	VCC	VCC	VCC	VCC	VCC	T15
VCC	VCC	VCC	VCC	VCC	VCC	T16
VCC	VCC	VCC	VCC	VCC	VCC	T17
VCC	VCC	VCC	VCC	VCC	VCC	T19
VCC	VCC	VCC	VCC	VCC	VCC	T20
VCC	VCC	VCC	VCC	VCC	VCC	T21
VCC	VCC	VCC	VCC	VCC	VCC	T23
VCC	VCC	VCC	VCC	VCC	VCC	T24
VCC	VCC	VCC	VCC	VCC	VCC	U13
VCC	VCC	VCC	VCC	VCC	VCC	U14
VCC	VCC	VCC	VCC	VCC	VCC	U16
VCC	VCC	VCC	VCC	VCC	VCC	U18
VCC	VCC	VCC	VCC	VCC	VCC	U20
VCC	VCC	VCC	VCC	VCC	VCC	U22
VCC	VCC	VCC	VCC	VCC	VCC	U24
VCC	VCC	VCC	VCC	VCC	VCC	V13
VCC	VCC	VCC	VCC	VCC	VCC	V14
VCC	VCC	VCC	VCC	VCC	VCC	V15
VCC	VCC	VCC	VCC	VCC	VCC	V17
VCC	VCC	VCC	VCC	VCC	VCC	V19
VCC	VCC	VCC	VCC	VCC	VCC	V21
VCC	VCC	VCC	VCC	VCC	VCC	V23
VCC	VCC	VCC	VCC	VCC	VCC	V24
VCC	VCC	VCC	VCC	VCC	VCC	W13

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VCC	VCC	VCC	VCC	VCC	VCC	W14
VCC	VCC	VCC	VCC	VCC	VCC	W16
VCC	VCC	VCC	VCC	VCC	VCC	W18
VCC	VCC	VCC	VCC	VCC	VCC	W20
VCC	VCC	VCC	VCC	VCC	VCC	W22
VCC	VCC	VCC	VCC	VCC	VCC	W24
VCC	VCC	VCC	VCC	VCC	VCC	Y13
VCC	VCC	VCC	VCC	VCC	VCC	Y14
VCC	VCC	VCC	VCC	VCC	VCC	Y15
VCC	VCC	VCC	VCC	VCC	VCC	Y16
VCC	VCC	VCC	VCC	VCC	VCC	Y17
VCC	VCC	VCC	VCC	VCC	VCC	Y19
VCC	VCC	VCC	VCC	VCC	VCC	Y20
VCC	VCC	VCC	VCC	VCC	VCC	Y21
VCC	VCC	VCC	VCC	VCC	VCC	Y23
VCC	VCC	VCC	VCC	VCC	VCC	Y24
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W1
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W2
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W3
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W4
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W6
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W7
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W8
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	W9
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y1
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y2
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y3
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y4
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y5
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y6
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y7
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y8
VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	Y9
VCC2	VCC2	VCC2	VCC2	VCC2	VCC2	A13
VCCA_DAC	RSV	RSV	VCCA_DAC	VCCA_DAC	VCCA_DAC	D13
VCCA_DAC	RSV	RSV	VCCA_DAC	VCCA_DAC	VCCA_DAC	E13
VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	VCCA_DPLLA	A12
VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	VCCA_DPLLB	B13
VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	VCCA_EXPPLL	A14

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	VCCA_HPLL	A17
VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	VCCA_SMPLL	B17
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AK35
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM10
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM11
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM13
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM14
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM16
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM17
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM19
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM20
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM22
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM23
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM25
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM26
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM28
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AM32
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AN35
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AP12
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AP16
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AP20
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AP24
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AP28
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR10
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR14
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR18
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR22
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR26
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR31
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	AR33
VSS	VSS	VSS	VSS	VSS	VSS	A10
VSS	VSS	VSS	VSS	VSS	VSS	A18
VSS	VSS	VSS	VSS	VSS	VSS	A26
VSS	VSS	VSS	VSS	VSS	VSS	A3
VSS	VSS	VSS	VSS	VSS	VSS	A30
VSS	VSS	VSS	VSS	VSS	VSS	A33
VSS	VSS	VSS	VSS	VSS	VSS	A5
VSS	VSS	VSS	VSS	VSS	VSS	AA1
VSS	VSS	VSS	VSS	VSS	VSS	AA10
VSS	VSS	VSS	VSS	VSS	VSS	AA11

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	AA15
VSS	VSS	VSS	VSS	VSS	VSS	AA17
VSS	VSS	VSS	VSS	VSS	VSS	AA19
VSS	VSS	VSS	VSS	VSS	VSS	AA2
VSS	VSS	VSS	VSS	VSS	VSS	AA25
VSS	VSS	VSS	VSS	VSS	VSS	AA26
VSS	VSS	VSS	VSS	VSS	VSS	AA27
VSS	VSS	VSS	VSS	VSS	VSS	AA3
VSS	VSS	VSS	VSS	VSS	VSS	AA4
VSS	VSS	VSS	VSS	VSS	VSS	AA5
VSS	VSS	VSS	VSS	VSS	VSS	AA6
VSS	VSS	VSS	VSS	VSS	VSS	AA7
VSS	VSS	VSS	VSS	VSS	VSS	AA8
VSS	VSS	VSS	VSS	VSS	VSS	AA9
VSS	VSS	VSS	VSS	VSS	VSS	AB25
VSS	VSS	VSS	VSS	VSS	VSS	AB28
VSS	VSS	VSS	VSS	VSS	VSS	AB30
VSS	VSS	VSS	VSS	VSS	VSS	AB32
VSS	VSS	VSS	VSS	VSS	VSS	AB35
VSS	VSS	VSS	VSS	VSS	VSS	AC25
VSS	VSS	VSS	VSS	VSS	VSS	AC27
VSS	VSS	VSS	VSS	VSS	VSS	AC29
VSS	VSS	VSS	VSS	VSS	VSS	AC31
VSS	VSS	VSS	VSS	VSS	VSS	AC32
VSS	VSS	VSS	VSS	VSS	VSS	AD11
VSS	VSS	VSS	VSS	VSS	VSS	AD13
VSS	VSS	VSS	VSS	VSS	VSS	AD16
VSS	VSS	VSS	VSS	VSS	VSS	AD19
VSS	VSS	VSS	VSS	VSS	VSS	AD22
VSS	VSS	VSS	VSS	VSS	VSS	AD25
VSS	VSS	VSS	VSS	VSS	VSS	AD26
VSS	VSS	VSS	VSS	VSS	VSS	AD27
VSS	VSS	VSS	VSS	VSS	VSS	AD34
VSS	VSS	VSS	VSS	VSS	VSS	AE12
VSS	VSS	VSS	VSS	VSS	VSS	AE14
VSS	VSS	VSS	VSS	VSS	VSS	AE15
VSS	VSS	VSS	VSS	VSS	VSS	AE17
VSS	VSS	VSS	VSS	VSS	VSS	AE18
VSS	VSS	VSS	VSS	VSS	VSS	AE20
VSS	VSS	VSS	VSS	VSS	VSS	AE21

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	AE23
VSS	VSS	VSS	VSS	VSS	VSS	AE24
VSS	VSS	VSS	VSS	VSS	VSS	AE28
VSS	VSS	VSS	VSS	VSS	VSS	AE30
VSS	VSS	VSS	VSS	VSS	VSS	AE32
VSS	VSS	VSS	VSS	VSS	VSS	AE4
VSS	VSS	VSS	VSS	VSS	VSS	AE6
VSS	VSS	VSS	VSS	VSS	VSS	AE9
VSS	VSS	VSS	VSS	VSS	VSS	AF1
VSS	VSS	VSS	VSS	VSS	VSS	AF10
VSS	VSS	VSS	VSS	VSS	VSS	AF12
VSS	VSS	VSS	VSS	VSS	VSS	AF15
VSS	VSS	VSS	VSS	VSS	VSS	AF18
VSS	VSS	VSS	VSS	VSS	VSS	AF21
VSS	VSS	VSS	VSS	VSS	VSS	AF26
VSS	VSS	VSS	VSS	VSS	VSS	AF29
VSS	VSS	VSS	VSS	VSS	VSS	AF30
VSS	VSS	VSS	VSS	VSS	VSS	AF31
VSS	VSS	VSS	VSS	VSS	VSS	AF32
VSS	VSS	VSS	VSS	VSS	VSS	AF35
VSS	VSS	VSS	VSS	VSS	VSS	AF4
VSS	VSS	VSS	VSS	VSS	VSS	AF6
VSS	VSS	VSS	VSS	VSS	VSS	AF8
VSS	VSS	VSS	VSS	VSS	VSS	AG12
VSS	VSS	VSS	VSS	VSS	VSS	AG13
VSS	VSS	VSS	VSS	VSS	VSS	AG15
VSS	VSS	VSS	VSS	VSS	VSS	AG16
VSS	VSS	VSS	VSS	VSS	VSS	AG18
VSS	VSS	VSS	VSS	VSS	VSS	AG19
VSS	VSS	VSS	VSS	VSS	VSS	AG21
VSS	VSS	VSS	VSS	VSS	VSS	AG22
VSS	VSS	VSS	VSS	VSS	VSS	AG25
VSS	VSS	VSS	VSS	VSS	VSS	AG28
VSS	VSS	VSS	VSS	VSS	VSS	AG29
VSS	VSS	VSS	VSS	VSS	VSS	AG5
VSS	VSS	VSS	VSS	VSS	VSS	AH1
VSS	VSS	VSS	VSS	VSS	VSS	AH11
VSS	VSS	VSS	VSS	VSS	VSS	AH14
VSS	VSS	VSS	VSS	VSS	VSS	AH17
VSS	VSS	VSS	VSS	VSS	VSS	AH20

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	AH23
VSS	VSS	VSS	VSS	VSS	VSS	AH26
VSS	VSS	VSS	VSS	VSS	VSS	AH29
VSS	VSS	VSS	VSS	VSS	VSS	AH32
VSS	VSS	VSS	VSS	VSS	VSS	AH34
VSS	VSS	VSS	VSS	VSS	VSS	AH5
VSS	VSS	VSS	VSS	VSS	VSS	AH6
VSS	VSS	VSS	VSS	VSS	VSS	AH8
VSS	VSS	VSS	VSS	VSS	VSS	AJ10
VSS	VSS	VSS	VSS	VSS	VSS	AJ13
VSS	VSS	VSS	VSS	VSS	VSS	AJ15
VSS	VSS	VSS	VSS	VSS	VSS	AJ16
VSS	VSS	VSS	VSS	VSS	VSS	AJ19
VSS	VSS	VSS	VSS	VSS	VSS	AJ22
VSS	VSS	VSS	VSS	VSS	VSS	AJ27
VSS	VSS	VSS	VSS	VSS	VSS	AJ30
VSS	VSS	VSS	VSS	VSS	VSS	AJ32
VSS	VSS	VSS	VSS	VSS	VSS	AJ35
VSS	VSS	VSS	VSS	VSS	VSS	AJ4
VSS	VSS	VSS	VSS	VSS	VSS	AJ9
VSS	VSS	VSS	VSS	VSS	VSS	AK1
VSS	VSS	VSS	VSS	VSS	VSS	AK11
VSS	VSS	VSS	VSS	VSS	VSS	AK14
VSS	VSS	VSS	VSS	VSS	VSS	AK17
VSS	VSS	VSS	VSS	VSS	VSS	AK20
VSS	VSS	VSS	VSS	VSS	VSS	AK23
VSS	VSS	VSS	VSS	VSS	VSS	AK25
VSS	VSS	VSS	VSS	VSS	VSS	AK26
VSS	VSS	VSS	VSS	VSS	VSS	AK28
VSS	VSS	VSS	VSS	VSS	VSS	AK30
VSS	VSS	VSS	VSS	VSS	VSS	AK4
VSS	VSS	VSS	VSS	VSS	VSS	AK6
VSS	VSS	VSS	VSS	VSS	VSS	AK7
VSS	VSS	VSS	VSS	VSS	VSS	AK8
VSS	VSS	VSS	VSS	VSS	VSS	AL10
VSS	VSS	VSS	VSS	VSS	VSS	AL13
VSS	VSS	VSS	VSS	VSS	VSS	AL16
VSS	VSS	VSS	VSS	VSS	VSS	AL19
VSS	VSS	VSS	VSS	VSS	VSS	AL22
VSS	VSS	VSS	VSS	VSS	VSS	AL32

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	AM29
VSS	VSS	VSS	VSS	VSS	VSS	AM31
VSS	VSS	VSS	VSS	VSS	VSS	AM4
VSS	VSS	VSS	VSS	VSS	VSS	AM6
VSS	VSS	VSS	VSS	VSS	VSS	AM7
VSS	VSS	VSS	VSS	VSS	VSS	AM8
VSS	VSS	VSS	VSS	VSS	VSS	AN1
VSS	VSS	VSS	VSS	VSS	VSS	AP8
VSS	VSS	VSS	VSS	VSS	VSS	AR13
VSS	VSS	VSS	VSS	VSS	VSS	AR17
VSS	VSS	VSS	VSS	VSS	VSS	AR21
VSS	VSS	VSS	VSS	VSS	VSS	AR25
VSS	VSS	VSS	VSS	VSS	VSS	AR3
VSS	VSS	VSS	VSS	VSS	VSS	AR30
VSS	VSS	VSS	VSS	VSS	VSS	AR6
VSS	VSS	VSS	VSS	VSS	VSS	B10
VSS	VSS	VSS	VSS	VSS	VSS	B12
VSS	VSS	VSS	VSS	VSS	VSS	B14
VSS	VSS	VSS	VSS	VSS	VSS	B16
VSS	VSS	VSS	VSS	VSS	VSS	B18
VSS	VSS	VSS	VSS	VSS	VSS	B2
VSS	VSS	VSS	VSS	VSS	VSS	B24
VSS	VSS	VSS	VSS	VSS	VSS	B28
VSS	VSS	VSS	VSS	VSS	VSS	B5
VSS	VSS	VSS	VSS	VSS	VSS	B6
VSS	VSS	VSS	VSS	VSS	VSS	B7
VSS	VSS	VSS	VSS	VSS	VSS	B8
VSS	VSS	VSS	VSS	VSS	VSS	B9
VSS	VSS	VSS	VSS	VSS	VSS	C1
VSS	VSS	VSS	VSS	VSS	VSS	C11
VSS	VSS	VSS	VSS	VSS	VSS	C13
VSS	VSS	VSS	VSS	VSS	VSS	C17
VSS	VSS	VSS	VSS	VSS	VSS	C18
VSS	VSS	VSS	VSS	VSS	VSS	C23
VSS	VSS	VSS	VSS	VSS	VSS	C3
VSS	VSS	VSS	VSS	VSS	VSS	C35
VSS	VSS	VSS	VSS	VSS	VSS	C4
VSS	VSS	VSS	VSS	VSS	VSS	D10
VSS	VSS	VSS	VSS	VSS	VSS	D11
VSS	VSS	VSS	VSS	VSS	VSS	D15

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	D16
VSS	VSS	VSS	VSS	VSS	VSS	D18
VSS	VSS	VSS	VSS	VSS	VSS	D23
VSS	VSS	VSS	VSS	VSS	VSS	D25
VSS	VSS	VSS	VSS	VSS	VSS	D26
VSS	VSS	VSS	VSS	VSS	VSS	D28
VSS	VSS	VSS	VSS	VSS	VSS	D3
VSS	VSS	VSS	VSS	VSS	VSS	D30
VSS	VSS	VSS	VSS	VSS	VSS	D31
VSS	VSS	VSS	VSS	VSS	VSS	D32
VSS	VSS	VSS	VSS	VSS	VSS	D4
VSS	VSS	VSS	VSS	VSS	VSS	D6
VSS	VSS	VSS	VSS	VSS	VSS	D7
VSS	VSS	VSS	VSS	VSS	VSS	D8
VSS	VSS	VSS	VSS	VSS	VSS	D9
VSS	VSS	VSS	VSS	VSS	VSS	E1
VSS	VSS	VSS	VSS	VSS	VSS	E10
VSS	VSS	VSS	VSS	VSS	VSS	E17
VSS	VSS	VSS	VSS	VSS	VSS	E18
VSS	VSS	VSS	VSS	VSS	VSS	E2
VSS	VSS	VSS	VSS	VSS	VSS	E23
VSS	VSS	VSS	VSS	VSS	VSS	E26
VSS	VSS	VSS	VSS	VSS	VSS	E29
VSS	VSS	VSS	VSS	VSS	VSS	E4
VSS	VSS	VSS	VSS	VSS	VSS	E6
VSS	VSS	VSS	VSS	VSS	VSS	E8
VSS	VSS	VSS	VSS	VSS	VSS	F10
VSS	VSS	VSS	VSS	VSS	VSS	F16
VSS	VSS	VSS	VSS	VSS	VSS	F18
VSS	VSS	VSS	VSS	VSS	VSS	F2
VSS	VSS	VSS	VSS	VSS	VSS	F23
VSS	VSS	VSS	VSS	VSS	VSS	F25
VSS	VSS	VSS	VSS	VSS	VSS	F29
VSS	VSS	VSS	VSS	VSS	VSS	F30
VSS	VSS	VSS	VSS	VSS	VSS	F32
VSS	VSS	VSS	VSS	VSS	VSS	F35
VSS	VSS	VSS	VSS	VSS	VSS	F4
VSS	VSS	VSS	VSS	VSS	VSS	F5
VSS	VSS	VSS	VSS	VSS	VSS	F6
VSS	VSS	VSS	VSS	VSS	VSS	F8

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	G10
VSS	VSS	VSS	VSS	VSS	VSS	G11
VSS	VSS	VSS	VSS	VSS	VSS	G13
VSS	VSS	VSS	VSS	VSS	VSS	G15
VSS	VSS	VSS	VSS	VSS	VSS	G17
VSS	VSS	VSS	VSS	VSS	VSS	G19
VSS	VSS	VSS	VSS	VSS	VSS	G2
VSS	VSS	VSS	VSS	VSS	VSS	G20
VSS	VSS	VSS	VSS	VSS	VSS	G23
VSS	VSS	VSS	VSS	VSS	VSS	G26
VSS	VSS	VSS	VSS	VSS	VSS	G27
VSS	VSS	VSS	VSS	VSS	VSS	G28
VSS	VSS	VSS	VSS	VSS	VSS	G4
VSS	VSS	VSS	VSS	VSS	VSS	G7
VSS	VSS	VSS	VSS	VSS	VSS	G8
VSS	VSS	VSS	VSS	VSS	VSS	G9
VSS	VSS	VSS	VSS	VSS	VSS	H10
VSS	VSS	VSS	VSS	VSS	VSS	H13
VSS	VSS	VSS	VSS	VSS	VSS	H2
VSS	VSS	VSS	VSS	VSS	VSS	H21
VSS	VSS	VSS	VSS	VSS	VSS	H24
VSS	VSS	VSS	VSS	VSS	VSS	H25
VSS	VSS	VSS	VSS	VSS	VSS	H27
VSS	VSS	VSS	VSS	VSS	VSS	H30
VSS	VSS	VSS	VSS	VSS	VSS	H32
VSS	VSS	VSS	VSS	VSS	VSS	H34
VSS	VSS	VSS	VSS	VSS	VSS	H4
VSS	VSS	VSS	VSS	VSS	VSS	H5
VSS	VSS	VSS	VSS	VSS	VSS	H6
VSS	VSS	VSS	VSS	VSS	VSS	H9
VSS	VSS	VSS	VSS	VSS	VSS	J10
VSS	VSS	VSS	VSS	VSS	VSS	J15
VSS	VSS	VSS	VSS	VSS	VSS	J16
VSS	VSS	VSS	VSS	VSS	VSS	J17
VSS	VSS	VSS	VSS	VSS	VSS	J18
VSS	VSS	VSS	VSS	VSS	VSS	J2
VSS	VSS	VSS	VSS	VSS	VSS	J20
VSS	VSS	VSS	VSS	VSS	VSS	J23
VSS	VSS	VSS	VSS	VSS	VSS	J30
VSS	VSS	VSS	VSS	VSS	VSS	J4

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	J7
VSS	VSS	VSS	VSS	VSS	VSS	J8
VSS	VSS	VSS	VSS	VSS	VSS	J9
VSS	VSS	VSS	VSS	VSS	VSS	K10
VSS	VSS	VSS	VSS	VSS	VSS	K11
VSS	VSS	VSS	VSS	VSS	VSS	K14
VSS	VSS	VSS	VSS	VSS	VSS	K2
VSS	VSS	VSS	VSS	VSS	VSS	K20
VSS	VSS	VSS	VSS	VSS	VSS	K24
VSS	VSS	VSS	VSS	VSS	VSS	K26
VSS	VSS	VSS	VSS	VSS	VSS	K28
VSS	VSS	VSS	VSS	VSS	VSS	K31
VSS	VSS	VSS	VSS	VSS	VSS	K32
VSS	VSS	VSS	VSS	VSS	VSS	K35
VSS	VSS	VSS	VSS	VSS	VSS	K4
VSS	VSS	VSS	VSS	VSS	VSS	K5
VSS	VSS	VSS	VSS	VSS	VSS	K6
VSS	VSS	VSS	VSS	VSS	VSS	K9
VSS	VSS	VSS	VSS	VSS	VSS	L11
VSS	VSS	VSS	VSS	VSS	VSS	L13
VSS	VSS	VSS	VSS	VSS	VSS	L15
VSS	VSS	VSS	VSS	VSS	VSS	L16
VSS	VSS	VSS	VSS	VSS	VSS	L17
VSS	VSS	VSS	VSS	VSS	VSS	L18
VSS	VSS	VSS	VSS	VSS	VSS	L2
VSS	VSS	VSS	VSS	VSS	VSS	L20
VSS	VSS	VSS	VSS	VSS	VSS	L21
VSS	VSS	VSS	VSS	VSS	VSS	L22
VSS	VSS	VSS	VSS	VSS	VSS	L24
VSS	VSS	VSS	VSS	VSS	VSS	L27
VSS	VSS	VSS	VSS	VSS	VSS	L30
VSS	VSS	VSS	VSS	VSS	VSS	L32
VSS	VSS	VSS	VSS	VSS	VSS	L4
VSS	VSS	VSS	VSS	VSS	VSS	L7
VSS	VSS	VSS	VSS	VSS	VSS	L8
VSS	VSS	VSS	VSS	VSS	VSS	L9
VSS	VSS	VSS	VSS	VSS	VSS	M10
VSS	VSS	VSS	VSS	VSS	VSS	M11
VSS	VSS	VSS	VSS	VSS	VSS	M17
VSS	VSS	VSS	VSS	VSS	VSS	M2

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	M20
VSS	VSS	VSS	VSS	VSS	VSS	M24
VSS	VSS	VSS	VSS	VSS	VSS	M25
VSS	VSS	VSS	VSS	VSS	VSS	M27
VSS	VSS	VSS	VSS	VSS	VSS	M29
VSS	VSS	VSS	VSS	VSS	VSS	M34
VSS	VSS	VSS	VSS	VSS	VSS	M4
VSS	VSS	VSS	VSS	VSS	VSS	M5
VSS	VSS	VSS	VSS	VSS	VSS	M6
VSS	VSS	VSS	VSS	VSS	VSS	M9
VSS	VSS	VSS	VSS	VSS	VSS	N10
VSS	VSS	VSS	VSS	VSS	VSS	N11
VSS	VSS	VSS	VSS	VSS	VSS	N17
VSS	VSS	VSS	VSS	VSS	VSS	N19
VSS	VSS	VSS	VSS	VSS	VSS	N2
VSS	VSS	VSS	VSS	VSS	VSS	N25
VSS	VSS	VSS	VSS	VSS	VSS	N28
VSS	VSS	VSS	VSS	VSS	VSS	N30
VSS	VSS	VSS	VSS	VSS	VSS	N32
VSS	VSS	VSS	VSS	VSS	VSS	N4
VSS	VSS	VSS	VSS	VSS	VSS	N7
VSS	VSS	VSS	VSS	VSS	VSS	N8
VSS	VSS	VSS	VSS	VSS	VSS	N9
VSS	VSS	VSS	VSS	VSS	VSS	P11
VSS	VSS	VSS	VSS	VSS	VSS	P16
VSS	VSS	VSS	VSS	VSS	VSS	P18
VSS	VSS	VSS	VSS	VSS	VSS	P2
VSS	VSS	VSS	VSS	VSS	VSS	P20
VSS	VSS	VSS	VSS	VSS	VSS	P25
VSS	VSS	VSS	VSS	VSS	VSS	P27
VSS	VSS	VSS	VSS	VSS	VSS	P29
VSS	VSS	VSS	VSS	VSS	VSS	P31
VSS	VSS	VSS	VSS	VSS	VSS	P32
VSS	VSS	VSS	VSS	VSS	VSS	P35
VSS	VSS	VSS	VSS	VSS	VSS	P4
VSS	VSS	VSS	VSS	VSS	VSS	P5
VSS	VSS	VSS	VSS	VSS	VSS	P6
VSS	VSS	VSS	VSS	VSS	VSS	P9
VSS	VSS	VSS	VSS	VSS	VSS	R11
VSS	VSS	VSS	VSS	VSS	VSS	R17

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	R19
VSS	VSS	VSS	VSS	VSS	VSS	R2
VSS	VSS	VSS	VSS	VSS	VSS	R21
VSS	VSS	VSS	VSS	VSS	VSS	R25
VSS	VSS	VSS	VSS	VSS	VSS	R26
VSS	VSS	VSS	VSS	VSS	VSS	R27
VSS	VSS	VSS	VSS	VSS	VSS	R4
VSS	VSS	VSS	VSS	VSS	VSS	R7
VSS	VSS	VSS	VSS	VSS	VSS	R8
VSS	VSS	VSS	VSS	VSS	VSS	R9
VSS	VSS	VSS	VSS	VSS	VSS	T10
VSS	VSS	VSS	VSS	VSS	VSS	T11
VSS	VSS	VSS	VSS	VSS	VSS	T18
VSS	VSS	VSS	VSS	VSS	VSS	T2
VSS	VSS	VSS	VSS	VSS	VSS	T22
VSS	VSS	VSS	VSS	VSS	VSS	T25
VSS	VSS	VSS	VSS	VSS	VSS	T28
VSS	VSS	VSS	VSS	VSS	VSS	T30
VSS	VSS	VSS	VSS	VSS	VSS	T32
VSS	VSS	VSS	VSS	VSS	VSS	T34
VSS	VSS	VSS	VSS	VSS	VSS	T4
VSS	VSS	VSS	VSS	VSS	VSS	T5
VSS	VSS	VSS	VSS	VSS	VSS	T6
VSS	VSS	VSS	VSS	VSS	VSS	T7
VSS	VSS	VSS	VSS	VSS	VSS	U11
VSS	VSS	VSS	VSS	VSS	VSS	U15
VSS	VSS	VSS	VSS	VSS	VSS	U17
VSS	VSS	VSS	VSS	VSS	VSS	U19
VSS	VSS	VSS	VSS	VSS	VSS	U2
VSS	VSS	VSS	VSS	VSS	VSS	U21
VSS	VSS	VSS	VSS	VSS	VSS	U23
VSS	VSS	VSS	VSS	VSS	VSS	U25
VSS	VSS	VSS	VSS	VSS	VSS	U27
VSS	VSS	VSS	VSS	VSS	VSS	U29
VSS	VSS	VSS	VSS	VSS	VSS	U31
VSS	VSS	VSS	VSS	VSS	VSS	U32
VSS	VSS	VSS	VSS	VSS	VSS	U4
VSS	VSS	VSS	VSS	VSS	VSS	U7
VSS	VSS	VSS	VSS	VSS	VSS	U8
VSS	VSS	VSS	VSS	VSS	VSS	U9

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VSS	VSS	VSS	VSS	VSS	VSS	V1
VSS	VSS	VSS	VSS	VSS	VSS	V11
VSS	VSS	VSS	VSS	VSS	VSS	V16
VSS	VSS	VSS	VSS	VSS	VSS	V18
VSS	VSS	VSS	VSS	VSS	VSS	V2
VSS	VSS	VSS	VSS	VSS	VSS	V20
VSS	VSS	VSS	VSS	VSS	VSS	V22
VSS	VSS	VSS	VSS	VSS	VSS	V25
VSS	VSS	VSS	VSS	VSS	VSS	V26
VSS	VSS	VSS	VSS	VSS	VSS	V27
VSS	VSS	VSS	VSS	VSS	VSS	V35
VSS	VSS	VSS	VSS	VSS	VSS	V4
VSS	VSS	VSS	VSS	VSS	VSS	V6
VSS	VSS	VSS	VSS	VSS	VSS	V9
VSS	VSS	VSS	VSS	VSS	VSS	W11
VSS	VSS	VSS	VSS	VSS	VSS	W15
VSS	VSS	VSS	VSS	VSS	VSS	W17
VSS	VSS	VSS	VSS	VSS	VSS	W19
VSS	VSS	VSS	VSS	VSS	VSS	W21
VSS	VSS	VSS	VSS	VSS	VSS	W23
VSS	VSS	VSS	VSS	VSS	VSS	W25
VSS	VSS	VSS	VSS	VSS	VSS	W28
VSS	VSS	VSS	VSS	VSS	VSS	W30
VSS	VSS	VSS	VSS	VSS	VSS	W32
VSS	VSS	VSS	VSS	VSS	VSS	Y11
VSS	VSS	VSS	VSS	VSS	VSS	Y18
VSS	VSS	VSS	VSS	VSS	VSS	Y22
VSS	VSS	VSS	VSS	VSS	VSS	Y25
VSS	VSS	VSS	VSS	VSS	VSS	Y27
VSS	VSS	VSS	VSS	VSS	VSS	Y29
VSS	VSS	VSS	VSS	VSS	VSS	Y31
VSS	VSS	VSS	VSS	VSS	VSS	Y32
VSS	VSS	VSS	VSS	VSS	VSS	Y34
VSSA_DAC	RSV	RSV	VSSA_DAC	VSSA_DAC	VSSA_DAC	F13
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	D12
VTT	VTT	VTT	VTT	VTT	VTT	A19
VTT	VTT	VTT	VTT	VTT	VTT	A20
VTT	VTT	VTT	VTT	VTT	VTT	A21
VTT	VTT	VTT	VTT	VTT	VTT	A22
VTT	VTT	VTT	VTT	VTT	VTT	B19

Intel® 82915GL GMCH[6]	Intel® 82915PL MCH[5]	Intel® 82915P MCH[1]	Intel® 82915G GMCH[2]	Intel® 82915GV GMCH[3]	Intel® 82910GL GMCH[4]	Ball #
VTT	VTT	VTT	VTT	VTT	VTT	B20
VTT	VTT	VTT	VTT	VTT	VTT	B21
VTT	VTT	VTT	VTT	VTT	VTT	B22
VTT	VTT	VTT	VTT	VTT	VTT	C19
VTT	VTT	VTT	VTT	VTT	VTT	C20
VTT	VTT	VTT	VTT	VTT	VTT	C21
VTT	VTT	VTT	VTT	VTT	VTT	C22
VTT	VTT	VTT	VTT	VTT	VTT	D19
VTT	VTT	VTT	VTT	VTT	VTT	D20
VTT	VTT	VTT	VTT	VTT	VTT	D21
VTT	VTT	VTT	VTT	VTT	VTT	D22
VTT	VTT	VTT	VTT	VTT	VTT	E19
VTT	VTT	VTT	VTT	VTT	VTT	E20
VTT	VTT	VTT	VTT	VTT	VTT	E21
VTT	VTT	VTT	VTT	VTT	VTT	E22
VTT	VTT	VTT	VTT	VTT	VTT	F20
VTT	VTT	VTT	VTT	VTT	VTT	F21
VTT	VTT	VTT	VTT	VTT	VTT	F22
VTT	VTT	VTT	VTT	VTT	VTT	G21
VTT	VTT	VTT	VTT	VTT	VTT	G22
VTT	VTT	VTT	VTT	VTT	VTT	H22

NOTES:
1. DDR, PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
2. DDR, PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
3. DDR, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
4. DDR (One DIMM per Channel), No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO
5. DDR (One DIMM per Channel), PCI Express* x16 Graphics Interface, No DAC, No Intel® SDVO
6. DDR, No PCI Express* x16 Graphics Interface, DAC, Intel® SDVO

14.3 Package Information

The (G)MCH package measures 37.5 mm × 37.5 mm. The 1210 balls are located in a non-grid pattern. For example, the ball pitch varies from 31.8 mils to 43.0 mils, depending upon the X-axis or Y-axis direction. Figure 14-7 shows the physical dimensions of the package and Figure 14-8 shows the (G)MCH keep-out regions.

Figure 14-7. (G)MCH Package Dimensions

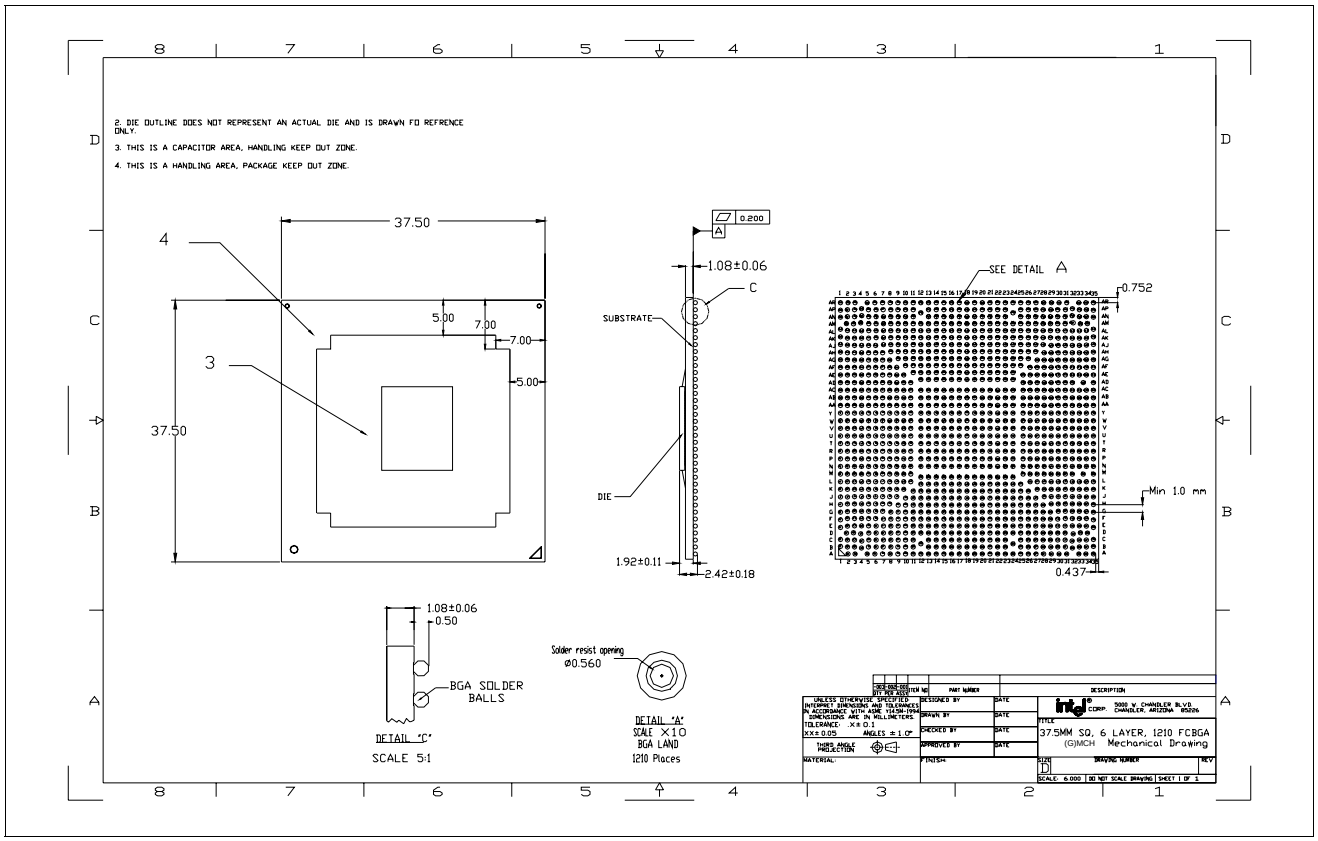
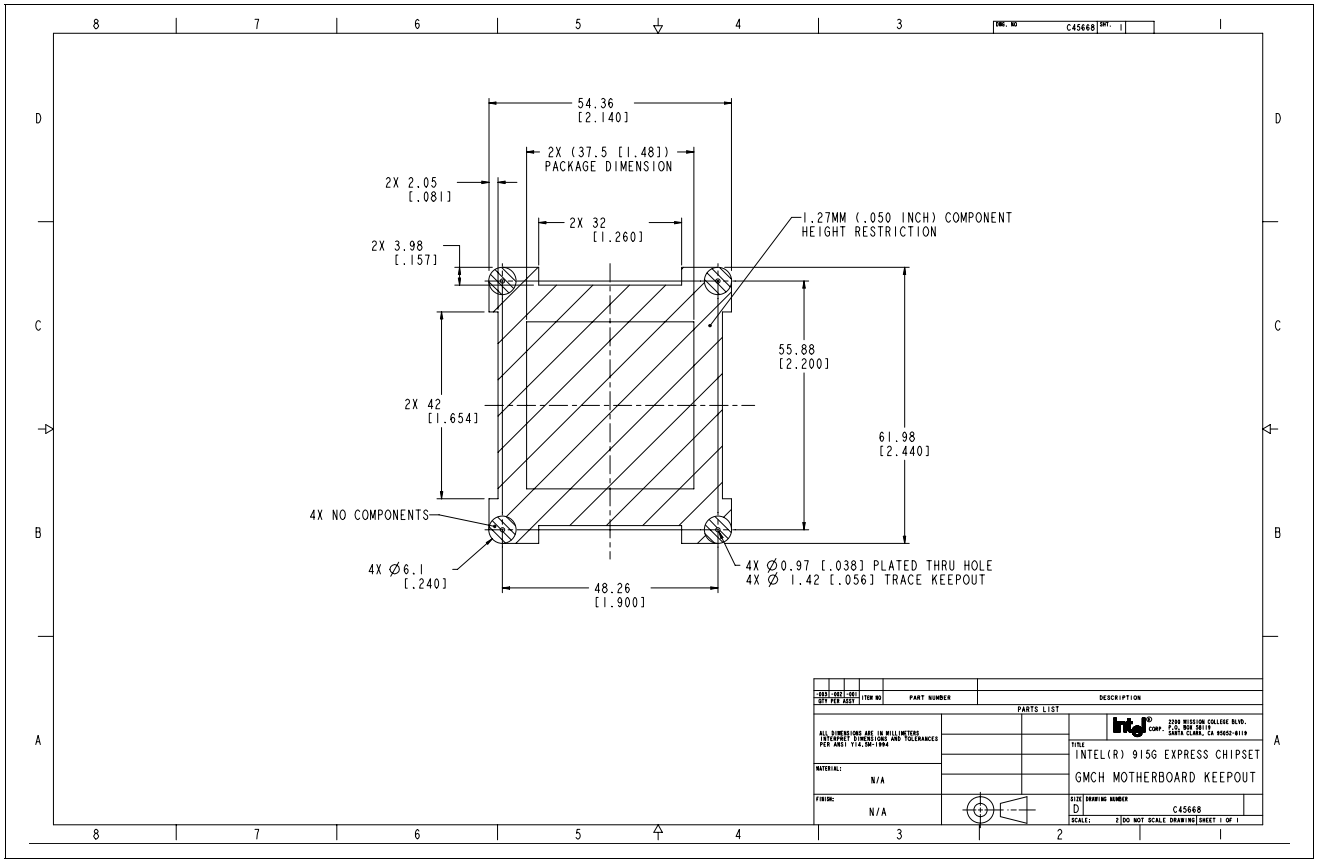


Figure 14-8. (G)MCH Component Keep-Out Restrictions



§

15 Testability

In the (G)MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it.

15.1 Complimentary Pins

Table 15-1 contains pins which must remain complimentary while performing XOR testing. The first and third columns contain the pin and its compliment. The second and fourth columns specify which chain the associated pins are on.

Note: The SDQSx# pins are only used in DDR2 mode. In DDR it is not necessary to drive SDQS_A[7:0]# or SDQS_B[7:0]#.

Table 15-1. Complimentary Pins to Drive

Complimentary Pin	XOR Chain	Complimentary Pin	XOR Chain
HDSTBP0#	FSB XOR 1	H_DSTBN0#	FSB XOR 1
HDSTBP1#	FSB XOR 0	HDSTBN1#	FSB XOR 0
HDSTBP2#	FSB XOR 0	HDSTBN2#	FSB XOR 0
HDSTBP3#	FSB XOR 0	HDSTBN3#	FSB XOR 0
SDQS_A0	SM XOR 6	SDQS_A0#	SM XOR 4
SDQS_A1	SM XOR 6	SDQS_A1#	SM XOR 4
SDQS_A2	SM XOR 6	SDQS_A2#	SM XOR 4
SDQS_A3	SM XOR 4	SDQS_A3#	SM XOR 6
SDQS_A4	SM XOR 4	SDQS_A4	SM XOR 2
SDQS_A5	SM XOR 2	SDQS_A5#	SM XOR 4
SDQS_A6	SM XOR 2	SDQS_A6#	SM XOR 4
SDQS_A7	SM XOR 2	SDQS_A7#	SM XOR 4
SDQS_A8	SM XOR 2	SDQS_A8#	SM XOR 4
SDQS_B0	SM XOR 7	SDQS_B0#	SM XOR 5
SDQS_B1	SM XOR 7	SDQS_B1#	SM XOR 5
SDQS_B2	SM XOR 7	SDQS_B2#	SM XOR 5
SDQS_B3	SM XOR 7	SDQS_B3#	SM XOR 5
SDQS_B4	SM XOR 7	SDQS_B4#	SM XOR 5
SDQS_B5	SM XOR 3	SDQS_B5#	SM XOR 5
SDQS_B6	SM XOR 3	SDQS_B6#	SM XOR 5
SDQS_B7	SM XOR 3	SDQS_B7#	SM XOR 5
SDQS_B8	SM XOR 7	SDQS_B8#	SM XOR 5

15.2 XOR Test Mode Initialization for DDR

XOR test mode (DDR) can be entered by pulling the reserved ballout RSV (located at F15) low through the de-assertion of external reset (RSTIN#). It was intended that no clocks should be required to enter this test mode; however, it is recommended that customers used the following sequence.

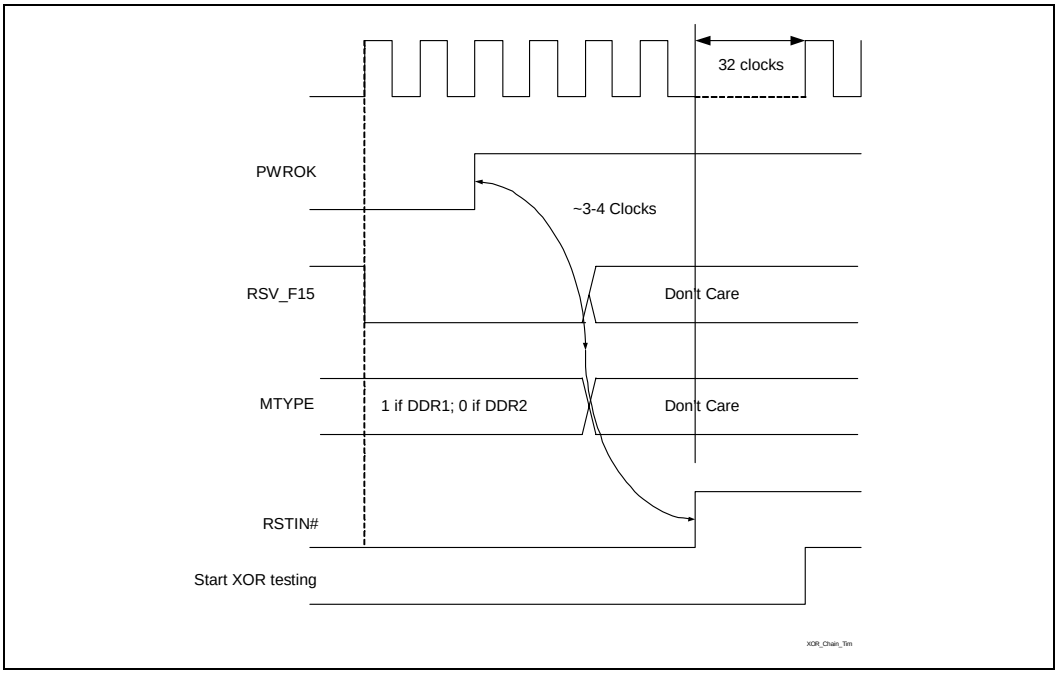
On power up, hold PWROK, PCIRST#, and reserved ballout RSV (located at F15) low and start external clocks, refer to the timing diagram below. After a few clock cycles, pull PWROK high. After ~3–4 clocks, de-assert PCIRST# (pull it high). Release reserved ballout RSV (located at F15). No external drive. Allow the clocks to run for an additional 32 clocks. Begin testing the XOR chains. Refer to timing diagram in below.

15.3 XOR Test Mode Initialization for DDR2

XOR test mode (DDR2) can be entered by pulling reserved ballout RSV(located at F15) and MTYPE low through the de-assertion of external reset (RSTIN#). It was intended that no clocks should be required to enter this test mode; however, it is recommended that customers use the following sequence.

On power up, hold PWROK, PCIRST#, and reserved ballout RSV (located at F15) low and start external clocks. After a few clock cycles, pull PWROK high. After ~3-4 clocks, de-assert PCIRST# (pull it high). Release reserved ballout RSV (located at F15) and MTYPE. No external drive. Allow the clocks to run for an additional 32 clocks. Begin testing the XOR chains. Refer to Figure 15-1.

Figure 15-1. XOR Test Mode Initialization Cycles



15.4 XOR Chain Definition

The 82915G/82915GV/82915GL/82910GL GMCH, and the 82915P/ 82915PL MCH each have 10 XOR chains. The XOR chain outputs are driven out on the following output pins. During full-width testing, XOR chain outputs are visible on both pins. For example, xor_out0 is visible on BSEL2.

Table 15-2. XOR Chain Outputs for both DDR and DDR2

XOR Chain	Output Pins	Coordinate Location
xor_out0	BSEL2	D17
xor_out1	RSV	M16
xor_out2	RSV	F15
xor_out3	MTYPE	C15
xor_out4	EXP_SLR	A16
xor_out5	RSV	B15
xor_out6	RSV	C14
xor_out7	RSV	K15
xor_out8	BSEL0	H16
xor_out9	BSEL1	E15

15.5 DDR XOR Chains

The tables in this section show the DDR XOR chains. The last section in this chapter has a pin exclusion list. The chain files are golden, if there is a pin missing from the chain files and exclusion list, it should be added to the exclusion list.

Note: The DDR XOR Chain information is based on the 82915G GMCH. Differences for the 82915GV/82915GL/82910GL GMCH and 82915P/82915PL MCH are indicated in the “Comments” column.

Table 15-3. DDR XOR Chain #0

Pin Count	Ball #	DDR Signal Name	Comments
1	M15	DDC_CLK	**RSV** on the 82915P/82915PL MCH
2	M14	ICH_SYNC#	
3	K16	EXTTS#	
4	L14	DDC_DATA	**RSV** on the 82915P/82915PL MCH
5	K13	SDVO_CTRLDATA	**RSV** on the 82915P/82915PL MCH
6	J13	SDVO_CTRLCLK	**RSV** on the 82915P/82915PL MCH
7	G16	RSV	
8	G24	HCPURST#	
9	K17	HD44	
10	M18	HD42	
11	K18	HD43	
12	F17	HD47	
13	M19	HD38	
14	K21	HD39	
15	K19	HDINV2#	
16	H18	HD46	
17	J19	HDSTBP2#	
18	F19	HDSTBN2#	
19	G18	HD45	
20	K22	HD34	
21	M21	HD36	
22	J21	HD35	
23	H20	HD40	
24	H19	HD41	
25	J24	HD33	
26	J22	HD32	
27	H23	HD37	
28	A25	HD48	
29	A29	HD55	
30	D27	HD60	
31	B26	HDINV3#	
32	B29	HDSTBP3#	
33	C29	HDSTBN3#	
34	C25	HD58	
35	B30	HD51	
36	E27	HD24	
37	C30	HD17	
38	E25	HD25	
39	H28	HD19	
40	F27	HD23	
41	F28	HD22	
42	H26	HDSTBP1#	

Pin Count	Ball #	DDR Signal Name	Comments
43	F26	HDSTBN1#	
44	J27	HD21	
45	J25	HD27	
46	K25	HD28	
47	K23	HD31	
48	L23	HD30	
49	J26	HDINV1#	
50	G25	HD26	
51	L25	HD29	
52	B32	HD15	
53	G33	HD7	
54	H33	HD1	
55	H35	HD4	
56	J34	HD2	
57	G30	HA6#	
58	H29	HA3#	
59	J28	HA13#	
60	J29	HA5#	
61	K33	HA15#	
62	F31	HREQ4#	
63	K29	HA4#	
64	L31	HA11#	
65	K27	HA14#	
66	M30	HA10#	
67	F33	HREQ0#	
68	E30	HBPRI#	
69	J35	HDEFER#	
70	P33	HEDRDY#	
	D17	**BSEL2**	**XOR Chain #0 Output**

Table 15-4. DDR XOR Chain #1

Pin Count	Ball #	DDR Signal Name	Comments
1	A28	HD57	
2	A27	HD61	
3	B27	HD54	
4	B25	HD63	
5	E24	HD62	
6	C26	HD59	
7	C27	HD49	
8	C28	HD56	
9	A31	HD53	
10	C31	HD50	
11	B31	HD52	
12	D29	HD18	
13	E28	HD16	
14	G29	HD20	
15	B34	HD11	
16	B33	HD13	
17	C32	HD14	
18	C33	HD9	
19	C34	HD12	
20	D34	HD8	
21	D33	HD10	
22	E34	HDINV0#	
23	E33	HDSTBP0#	
24	E35	HDSTBN0#	
25	F34	HD6	
26	G34	HD5	
27	G35	HD3	
28	J33	HD0	
29	G32	HA7#	
30	H31	HREQ2#	
31	K30	HA8#	
32	J31	HADSTB0#	
33	G31	HREQ3#	
34	E31	HPCREQ#	
35	L29	HA9#	
36	L28	HA12#	
37	J32	HRS2#	
38	K34	HRS0#	
39	L33	HLOCK#	
40	M32	HDRDY#	
41	M31	HADS#	
42	L34	HHIT#	
43	M35	HBNR#	
44	L35	HDBSY#	
45	N35	HHITM#	

Pin Count	Ball #	DDR Signal Name	Comments
46	P34	HRS1#	
47	N34	HTRDY#	
48	R33	HBREQ0#	
49	N31	HA21#	
50	N33	HA26#	
51	T31	HA28#	
52	E32	HREQ1#	
53	T27	HA27#	
54	M26	HA20#	
55	N26	HA19#	
56	P28	HA24#	
57	U28	HA29#	
58	N27	HADSTB1#	
59	L26	HA18#	
60	M28	HA16#	
61	T29	HA31#	
62	R28	HA25#	
63	N29	HA23#	
64	T26	HA30#	
65	P26	HA22#	
66	R29	HA17#	
	M16	**RSV**	**XOR Chain #1 Output**

Table 15-5. DDR XOR Chain #2

Pin Count	Ball #	DDR Signal Name	Comments
1	R32	SDQ_A58	
2	R34	SDQ_A59	
3	T35	SDQ_A63	
4	W35	SDQ_A60	
5	T33	SDQ_A62	
6	V34	SDQ_A56	
7	V33	SDQ_A57	
8	U33	SDM_A7	
9	W33	SDQ_A61	
10	U34	SDQS_A7	
11	AA34	SDQS_A6	
12	W34	SDQ_A51	
13	Y35	SDQ_A55	
14	Y33	SDQ_A50	
15	AD35	SDQ_A53	
16	AE35	SDQ_A48	
17	AE34	SDQ_A49	
18	AA33	SDM_A6	
19	AA32	SDQ_A54	
20	AD31	SDQ_A52	
21	AB33	SMA_A13	
22	AC35	SCLK_A5	
23	AB34	SCLK_A2	
24	AC33	SCLK_A2#	
25	AF34	SDQ_A43	
26	AH35	SDQ_A41	
27	AJ34	SDQ_A40	
28	AG34	SDM_A5	
29	AE33	SDQ_A47	
30	AF33	SDQ_A46	
31	AG32	SDQ_A42	
32	AH33	SDQ_A45	
33	AJ33	SDQ_A44	
34	AG35	SDQS_A5	
35	AR29	RSV	
36	AP33	RSV	
37	AP29	RSV	
38	AN32	RSV	
39	AP30	RSV	
40	AL29	RSV	
	F15	**RSV**	**XOR Chain #2 Output**

Table 15-6. DDR XOR Chain #3

Pin Count	Ball #	DDR Signal Name	Comments
1	W26	SDQ_B62	
2	U26	SDQ_B58	
3	V28	SDQ_B63	
4	V29	SDQ_B59	
5	W29	SDQ_B57	
6	W31	SDM_B7	
7	AA29	SDQ_B56	
8	AA28	SDQ_B61	
9	Y26	SDQ_B60	
10	W27	SDQS_B7	
11	AD32	SMA_B13	
12	AB31	SDQS_B6	
13	AB27	SDQ_B50	
14	AE31	SDQ_B48	
15	AC26	SDQ_B55	
16	AE27	SDQ_B53	
17	AE29	SDQ_B52	
18	AF27	SDQ_B49	
19	AB26	SDQ_B51	
20	AC28	SDQ_B54	
21	AD24	SDM_B6	
22	AP34	SCS_B0#	
23	AD29	SCLK_B5	
24	AE25	SCLK_B2#	
25	AE26	SCLK_B2	
26	AN34	SCS_B1#	
27	AN33	SCS_B2#	
28	AM34	SCS_A0#	
29	AK34	SCS_A2#	
30	AL34	SCAS_A#	
31	AL35	SCS_A1#	
32	AM33	SCS_B3#	
33	AF28	SDQ_B47	
34	AK32	SDQ_B45	
35	AH31	SDM_B5	
36	AK33	SDQ_B44	
37	AJ31	SDQ_B41	
38	AG27	SDQ_B46	
39	AJ29	SDQ_B40	
40	AG31	SDQ_B43	
41	AH28	SDQS_B5	
42	AL33	SCS_A3#	
43	AJ25	SDQ_B38	
44	AL25	SDQ_B34	
45	AJ26	SDQ_B35	
46	AL26	SDQ_B39	
47	AF23	SDQ_B32	
48	AF25	SDQ_B33	
	C15	**MTYPE**	**XOR Chain #3 Output**

Table 15-7. DDR XOR Chain #4

Pin Count	Ball #	DDR Signal Name	Comments
1	U35	RSV	
2	AA35	RSV	
3	AC34	SCLK_A5#	
4	AG33	RSV	
5	AP32	RSV	
6	AN31	RSV	
7	AM30	SDQS_A4	
8	AK31	SDQ_A35	
9	AH27	SDQ_A32	
10	AK29	SDM_A4	
11	AJ28	SDQ_A37	
12	AL30	SDQ_A38	
13	AL31	SDQ_A39	
14	AN30	SDQ_A34	
15	AL27	SDQ_A36	
16	AK27	SDQ_A33	
17	AN29	SRAS_A#	
18	AN28	SBS_A0	
19	AR28	RSV	
20	AN27	SCAS_B#	
21	AP27	SRAS_B#	
22	AR27	SWE_B#	
23	AP25	SCLK_A3	
24	AN26	SCLK_A3#	
25	AN25	SCLK_A0#	
26	AM24	SCLK_A0	
27	AL24	RSV	
28	AM27	SBS_B0	
29	AP26	SBS_A1	
30	AP31	SWE_A#	
31	AR24	RSV	
32	AR23	RSV	
33	AP23	RSV	
34	AN23	SMA_A10	
35	AN22	SMA_A0	
36	AF17	SDQS_A3	
37	AH18	SDQ_A31	
38	AF19	SDQ_A27	
39	AJ17	SDQ_A29	
40	AL17	SDQ_A25	
41	AF16	SDQ_A28	
42	AN18	SMA_A8	
43	AR7	RSV	
44	AM3	SCLK_A4#	
45	AL2	RSV	
46	AG2	RSV	
	A16	**EXP_SLR**	**XOR Chain #4 Output**

Table 15-8. DDR XOR Chain #5

Pin Count	Ball #	DDR Signal Name	Comments
1	Y28	RSV	
2	AC30	RSV	
3	AD28	SCLK_B5#	
4	AG30	SDQ_B42	
5	AH30	RSV	
6	AG24	SDM_B4	
7	AD23	SDQ_B36	
8	AF24	SDQ_B37	
9	AG26	RSV	
10	AF20	RSV	
11	AE22	SDQ_B26	
12	AL18	SDQ_B28	
13	AK19	SDQ_B25	
14	AG20	SDM_B3	
15	AD21	SDQ_B31	
16	AF22	SDQ_B30	
17	AH21	SDQ_B27	
18	AD18	SDQ_B24	
19	AH19	SDQ_B29	
20	AK22	SCLK_B3#	
21	AG23	SCLK_B0#	
22	AH22	SCLK_B0	
23	AN17	SMA_B2	
24	AP18	SMA_B1	
25	AP17	SMA_B6	
26	AR16	SMA_B3	
27	AN16	SMA_A7	
28	AN15	SMA_B5	
29	AM15	SMA_A9	
30	AP15	SMA_A11	
31	AR15	SMA_B4	
32	AL15	SMA_B7	
33	AP14	SMA_B8	
34	AP10	SCKE_B2	
35	AL14	RSV	
36	AL9	SCLK_B4#	
37	AH10	RSV	
38	AL4	RSV	
	B15	**RSV**	**XOR Chain #5 Output**

Table 15-9. DDR XOR Chain #6

Pin Count	Ball #	DDR Signal Name	Comments
1	AG17	RSV	
2	AH16	SDM_A3	
3	AE19	SDQ_A30	
4	AD17	SDQ_A26	
5	AK16	SDQ_A24	
6	AM18	SMA_B0	
7	AM21	SMA_A4	
8	AN21	SMA_A2	
9	AP22	SMA_A1	
10	AN20	SMA_B10	
11	AP21	SMA_A3	
12	AR20	SMA_A6	
13	AP19	SMA_A5	
14	AR19	SBS_B1	
15	AP7	SDQS_A2	
16	AP9	SDQ_A19	
17	AN9	SDQ_A23	
18	AR8	SDQ_A22	
19	AN8	SDQ_A18	
20	AN7	SDM_A2	
21	AP6	SDQ_A21	
22	AR5	SDQ_A17	
23	AP5	SDQ_A16	
24	AN5	SDQ_A20	
25	AN2	SCLK_A1	
26	AN3	SCLK_A1#	
27	AM2	SCLK_A4	
28	AP4	SDQ_A11	
29	AP3	SDQ_A15	
30	AP2	SDQ_A14	
31	AN4	SDQ_A10	
32	AK3	SDQ_A13	
33	AK2	SDQ_A9	
34	AJ3	SDQ_A12	
35	AJ1	SDQ_A8	
36	AL1	SDM_A1	
37	AL3	SDQS_A1	
38	AG1	SDQS_A0	
39	AG3	SDQ_A6	
40	AF2	SDM_A0	
41	AH2	SDQ_A2	
42	AH3	SDQ_A7	
43	AJ2	SDQ_A3	
44	AF3	SDQ_A1	
45	AE3	SDQ_A0	
46	AE2	SDQ_A4	
47	AE1	SDQ_A5	
	C14	**RSV**	**XOR Chain #6 Output**

Table 15-10. DDR XOR Chain #7

Pin Count	Ball #	DDR Signal Name	Comments
1	AH25	SDQS_B4	
2	AD20	SDQS_B3	
3	AL23	SCLK_B3	
4	AP13	SMA_A12	
5	AR12	SMA_B11	
6	AN13	SMA_B9	
7	AL12	SCKE_A0	
8	AR11	SCKE_A3	
9	AP11	SCKE_A2	
10	AN11	SCKE_A1	
11	AM12	SMA_B12	
12	AR9	SCKE_B3	
13	AN10	SCKE_B0	
14	AM9	SCKE_B1	
15	AD15	SDQ_B23	
16	AD14	SDQ_B19	
17	AG14	SDQ_B18	
18	AH13	SDM_B2	
19	AH12	SDQ_B21	
20	AF14	SDQ_B22	
21	AD12	SDQ_B20	
22	AF13	SDQ_B17	
23	AE13	SDQ_B16	
24	AK13	SDQS_B2	
25	AL11	SCLK_B1	
26	AJ11	SCLK_B1#	
27	AK9	SCLK_B4	
28	AL8	SDQ_B13	
29	AL7	SDQ_B9	
30	AJ7	SDQ_B8	
31	AJ8	SDQ_B12	
32	AF11	SDQ_B10	
33	AG11	SDQ_B15	
34	AG10	SDQ_B14	
35	AH9	SDM_B1	
36	AE11	SDQ_B11	
37	AK10	SDQS_B1	
38	AK5	SDQS_B0	
39	AG9	SDQ_B4	
40	AH7	SDQ_B0	
41	AJ6	SDQ_B1	
42	AL6	SDQ_B7	
43	AN6	SDQ_B3	
44	AL5	SDQ_B2	
45	AJ5	SDM_B0	
46	AH4	SDQ_B5	
47	AM5	SDQ_B6	
	K15	**RSV**	**XOR Chain #7 Output**

Table 15-11. DDR XOR Chain #8

Pin Count	Ball #	DDR Signal Name	Comments
1	F11	EXP_RXN0	For SDVO interface signal name, see ballout table.
2	C9	EXP_TXN0	For SDVO interface signal name, see ballout table.
3	H11	EXP_RXN1	For SDVO interface signal name, see ballout table.
4	A8	EXP_TXN1	For SDVO interface signal name, see ballout table.
5	E9	EXP_RXN2	For SDVO interface signal name, see ballout table.
6	C7	EXP_TXN2	For SDVO interface signal name, see ballout table.
7	E7	EXP_RXN3	For SDVO interface signal name, see ballout table.
8	A6	EXP_TXN3	For SDVO interface signal name, see ballout table.
9	B4	EXP_RXN4	For SDVO interface signal name, see ballout table.
10	C5	EXP_TXN4	For SDVO interface signal name, see ballout table.
11	E5	EXP_RXN5	For SDVO interface signal name, see ballout table.
12	D2	EXP_TXN5	For SDVO interface signal name, see ballout table.
13	G5	EXP_RXN6	For SDVO interface signal name, see ballout table.
14	F3	EXP_TXN6	For SDVO interface signal name, see ballout table.
15	H7	EXP_RXN7	For SDVO interface signal name, see ballout table.
16	G1	EXP_TXN7	For SDVO interface signal name, see ballout table.
17	J5	EXP_RXN8	For SDVO interface signal name, see ballout table.
18	H3	EXP_TXN8	For SDVO interface signal name, see ballout table.
19	K7	EXP_RXN9	For SDVO interface signal name, see ballout table.
20	J1	EXP_TXN9	For SDVO interface signal name, see ballout table.
21	L5	EXP_RXN10	For SDVO interface signal name, see ballout table.
22	K3	EXP_TXN10	For SDVO interface signal name, see ballout table.
23	R10	EXP_RXN11	For SDVO interface signal name, see ballout table.
24	L1	EXP_TXN11	For SDVO interface signal name, see ballout table.
25	M7	EXP_RXN12	For SDVO interface signal name, see ballout table.
26	M3	EXP_TXN12	For SDVO interface signal name, see ballout table.
27	N5	EXP_RXN13	For SDVO interface signal name, see ballout table.
28	N1	EXP_TXN13	For SDVO interface signal name, see ballout table.
29	P8	EXP_RXN14	For SDVO interface signal name, see ballout table.
30	P3	EXP_TXN14	For SDVO interface signal name, see ballout table.
31	R5	EXP_RXN15	For SDVO interface signal name, see ballout table.
32	R1	EXP_TXN15	For SDVO interface signal name, see ballout table.
33	E11	EXP_RXP0	For SDVO interface signal name, see ballout table.
34	C10	EXP_TXP0	For SDVO interface signal name, see ballout table.
35	J11	EXP_RXP1	For SDVO interface signal name, see ballout table.
36	A9	EXP_TXP1	For SDVO interface signal name, see ballout table.
37	F9	EXP_RXP2	For SDVO interface signal name, see ballout table.
38	C8	EXP_TXP2	For SDVO interface signal name, see ballout table.
39	F7	EXP_RXP3	For SDVO interface signal name, see ballout table.
40	A7	EXP_TXP3	For SDVO interface signal name, see ballout table.
41	B3	EXP_RXP4	For SDVO interface signal name, see ballout table.
42	C6	EXP_TXP4	For SDVO interface signal name, see ballout table.
43	D5	EXP_RXP5	For SDVO interface signal name, see ballout table.
44	C2	EXP_TXP5	For SDVO interface signal name, see ballout table.
45	G6	EXP_RXP6	For SDVO interface signal name, see ballout table.

Pin Count	Ball #	DDR Signal Name	Comments
46	E3	EXP_TXP6	For SDVO interface signal name, see ballout table.
47	H8	EXP_RXP7	For SDVO interface signal name, see ballout table.
48	F1	EXP_TXP7	For SDVO interface signal name, see ballout table.
49	J6	EXP_RXP8	For SDVO interface signal name, see ballout table.
50	G3	EXP_TXP8	For SDVO interface signal name, see ballout table.
51	K8	EXP_RXP9	For SDVO interface signal name, see ballout table.
52	H1	EXP_TXP9	For SDVO interface signal name, see ballout table.
53	L6	EXP_RXP10	For SDVO interface signal name, see ballout table.
54	J3	EXP_TXP10	For SDVO interface signal name, see ballout table.
55	P10	EXP_RXP11	For SDVO interface signal name, see ballout table.
56	K1	EXP_TXP11	For SDVO interface signal name, see ballout table.
57	M8	EXP_RXP12	For SDVO interface signal name, see ballout table.
58	L3	EXP_TXP12	For SDVO interface signal name, see ballout table.
59	N6	EXP_RXP13	For SDVO interface signal name, see ballout table.
60	M1	EXP_TXP13	For SDVO interface signal name, see ballout table.
61	P7	EXP_RXP14	For SDVO interface signal name, see ballout table.
62	N3	EXP_TXP14	For SDVO interface signal name, see ballout table.
63	R6	EXP_RXP15	For SDVO interface signal name, see ballout table.
64	P1	EXP_TXP15	For SDVO interface signal name, see ballout table.
	H16	**BSEL0**	**XOR Chain #8 Output**

Table 15-12. DDR XOR Chain #9

Pin Count	Ball #	DDR Signal Name	Comments
1	U6	DMI_RXN0	
2	U5	DMI_RXP0	
3	T3	DMI_TXN0	
4	R3	DMI_TXP0	
5	T8	DMI_RXN1	
6	T9	DMI_RXP1	
7	U1	DMI_TXN1	
8	T1	DMI_TXP1	
9	V8	DMI_RXN2	
10	V7	DMI_RXP2	
11	V3	DMI_TXN2	
12	U3	DMI_TXP2	
13	U10	DMI_RXN3	
14	V10	DMI_RXP3	
15	W5	DMI_TXN3	
16	V5	DMI_TXP3	
	E15	**BSEL1**	**XOR Chain #9 Output**

15.6 DDR2 XOR Chains

The tables in this section list all of the pads used in DDR2 XOR testing. Any pads not listed in the table can be considered part of the exclude list.

Note: The DDR2 XOR Chain information is based on the 82915G GMCH. Differences for the 82915GV GMCH and 82915P MCH are indicated in the "Comments" column.

Table 15-13. DDR2 XOR Chain #0

Pin Count	Ball #	DDR2 Signal Name	Comments
1	M15	DDC_CLK	**RSV** on the 82915P
2	M14	ICH_SYNC#	
3	K16	EXTTS#	
4	L14	DDC_DATA	**RSV** on the 82915P
5	K13	SDVO_CTRLDATA	**RSV** on the 82915P
6	J13	SDVO_CTRLCLK	**RSV** on the 82915P
7	G16	RSV	
8	G24	HCPURST#	
9	K17	HD44	
10	M18	HD42	
11	K18	HD43	
12	F17	HD47	
13	M19	HD38	
14	K21	HD39	
15	K19	HDINV2#	
16	H18	HD46	
17	J19	HDSTBP2#	
18	F19	HDSTBN2#	
19	G18	HD45	
20	K22	HD34	
21	M21	HD36	
22	J21	HD35	
23	H20	HD40	
24	H19	HD41	
25	J24	HD33	
26	J22	HD32	
27	H23	HD37	
28	A25	HD48	
29	A29	HD55	
30	D27	HD60	
31	B26	HDINV3#	
32	B29	HDSTBP3#	
33	C29	HDSTBN3#	
34	C25	HD58	
35	B30	HD51	
36	E27	HD24	

Pin Count	Ball #	DDR2 Signal Name	Comments
37	C30	HD17	
38	E25	HD25	
39	H28	HD19	
40	F27	HD23	
41	F28	HD22	
42	H26	HDSTBP1#	
43	F26	HDSTBN1#	
44	J27	HD21	
45	J25	HD27	
46	K25	HD28	
47	K23	HD31	
48	L23	HD30	
49	J26	HDINV1#	
50	G25	HD26	
51	L25	HD29	
52	B32	HD15	
53	G33	HD7	
54	H33	HD1	
55	H35	HD4	
56	J34	HD2	
57	G30	HA6#	
58	H29	HA3#	
59	J28	HA13#	
60	J29	HA5#	
61	K33	HA15#	
62	F31	HREQ4#	
63	K29	HA4#	
64	L31	HA11#	
65	K27	HA14#	
66	M30	HA10#	
67	F33	HREQ0#	
68	E30	HBPRI#	
69	J35	HDEFER#	
70	P33	HEDRDY#	
	D17	**BSEL2**	**XOR Chain #0 Output**

Table 15-14. DDR2 XOR Chain #1

Pin Count	Ball #	DDR2 Signal Name	Comments
1	A28	HD57	
2	A27	HD61	
3	B27	HD54	
4	B25	HD63	
5	E24	HD62	
6	C26	HD59	
7	C27	HD49	
8	C28	HD56	
9	A31	HD53	
10	C31	HD50	
11	B31	HD52	
12	D29	HD18	
13	E28	HD16	
14	G29	HD20	
15	B34	HD11	
16	B33	HD13	
17	C32	HD14	
18	C33	HD9	
19	C34	HD12	
20	D34	HD8	
21	D33	HD10	
22	E34	HDINV0#	
23	E33	HDSTBP0#	
24	E35	HDSTBN0#	
25	F34	HD6	
26	G34	HD5	
27	G35	HD3	
28	J33	HD0	
29	G32	HA7#	
30	H31	HREQ2#	
31	K30	HA8#	
32	J31	HADSTB0#	
33	G31	HREQ3#	
34	E31	HPCREQ#	
35	L29	HA9#	
36	L28	HA12#	
37	J32	HRS2#	
38	K34	HRS0#	
39	L33	HLOCK#	
40	M32	HDRDY#	
41	M31	HADS#	
42	L34	HHIT#	
43	M35	HBNR#	
44	L35	HDBSY#	
45	N35	HHITM#	

Pin Count	Ball #	DDR2 Signal Name	Comments
46	P34	HRS1#	
47	N34	HTRDY#	
48	R33	HBREQ0#	
49	N31	HA21#	
50	N33	HA26#	
51	T31	HA28#	
52	E32	HREQ1#	
53	T27	HA27#	
54	M26	HA20#	
55	N26	HA19#	
56	P28	HA24#	
57	U28	HA29#	
58	N27	HADSTB1#	
59	L26	HA18#	
60	M28	HA16#	
61	T29	HA31#	
62	R28	HA25#	
63	N29	HA23#	
64	T26	HA30#	
65	P26	HA22#	
66	R29	HA17#	
	M16	**RSV**	**XOR Chain #1 Output**

Table 15-15. DDR2 XOR Chain #2

Pin Count	Ball #	DDR2 Signal Name	Comments
1	R32	SDQ_A58	
2	R34	SDQ_A59	
3	T35	SDQ_A63	
4	W35	SDQ_A60	
5	T33	SDQ_A62	
6	V34	SDQ_A56	
7	V33	SDQ_A57	
8	U33	SDM_A7	
9	W33	SDQ_A61	
10	U34	SDQS_A7	
11	AA34	SDQS_A6	
12	W34	SDQ_A51	
13	Y35	SDQ_A55	
14	Y33	SDQ_A50	
15	AD35	SDQ_A49	
16	AE35	SDQ_A52	
17	AE34	SDQ_A53	
18	AA33	SDM_A6	
19	AA32	SDQ_A54	
20	AD31	SDQ_A48	
21	AB33	RSV	
22	AC35	SCLK_A2#	
23	AB34	SCLK_A5#	
24	AC33	SCLK_A5	
25	AF34	SDQ_A47	
26	AH35	SDQ_A41	
27	AJ34	SDQ_A45	
28	AG34	SDM_A5	
29	AE33	SDQ_A43	
30	AF33	SDQ_A42	
31	AG32	SDQ_A46	
32	AH33	SDQ_A40	
33	AJ33	SDQ_A44	
34	AG35	SDQS_A5	
35	AR29	SCS_A0#	
36	AP33	SODT_A3	
37	AP29	SODT_A2	
38	AN32	SODT_A1	
39	AP30	SODT_A0	
40	AL29	SDQS_A4#	
	F15	**RSV**	**XOR Chain #2 Output**

Table 15-16. DDR2 XOR Chain #3

Pin Count	Ball #	DDR2 Signal Name	Comments
1	W26	SDQ_B62	
2	U26	SDQ_B63	
3	V28	SDQ_B58	
4	V29	SDQ_B59	
5	W29	SDQ_B57	
6	W31	SDM_B7	
7	AA29	SDQ_B61	
8	AA28	SDQ_B56	
9	Y26	SDQ_B60	
10	W27	SDQS_B7	
11	AD32	RSV	
12	AB31	SDQS_B6	
13	AB27	SDQ_B55	
14	AE31	SDQ_B52	
15	AC26	SDQ_B50	
16	AE27	SDQ_B49	
17	AE29	SDQ_B53	
18	AF27	SDQ_B48	
19	AB26	SDQ_B51	
20	AC28	SDQ_B54	
21	AD24	SDM_B6	
22	AP34	SCS_B2#	
23	AD29	SCLK_B5#	
24	AE25	SCLK_B2#	
25	AE26	SCLK_B2	
26	AN34	SCS_B3#	
27	AN33	SCS_B0#	
28	AM34	SCS_B1#	
29	AK34	SODT_B3	
30	AL34	SODT_B1	
31	AL35	SODT_B2	
32	AM33	SODT_B0	
33	AF28	SDQ_B43	
34	AK32	SDQ_B40	
35	AH31	SDM_B5	
36	AK33	SDQ_B45	
37	AJ31	SDQ_B41	
38	AG27	SDQ_B47	
39	AJ29	SDQ_B44	
40	AG31	SDQ_B42	
41	AH28	SDQS_B5	
42	AL33	SMA_B13	
43	AJ25	SDQ_B39	
44	AL25	SDQ_B38	
45	AJ26	SDQ_B35	
46	AL26	SDQ_B34	
47	AF23	SDQ_B36	
48	AF25	SDQ_B33	
	C15	**MTYPE**	**XOR Chain #3 Output**

Table 15-17. DDR2 XOR Chain #4

Pin Count	Ball #	DDR2 Signal Name	Comments
1	U35	SDQS_A7#	
2	AA35	SDQS_A6#	
3	AC34	SCLK_A2	
4	AG33	SDQS_A5#	
5	AP32	SCS_A1#	
6	AN31	SCS_A3#	
7	AM30	SDQS_A4	
8	AK31	SDQ_A35	
9	AH27	SDQ_A36	
10	AK29	SDM_A4	
11	AJ28	SDQ_A33	
12	AL30	SDQ_A39	
13	AL31	SDQ_A34	
14	AN30	SDQ_A38	
15	AL27	SDQ_A37	
16	AK27	SDQ_A32	
17	AN29	SCAS_A#	
18	AN28	SWE_A#	
19	AR28	SCS_A2#	
20	AN27	SBS_A1	
21	AP27	SRAS_A#	
22	AR27	SBS_A0	
23	AP25	SCLK_A0#	
24	AN26	SCLK_A0	
25	AN25	SCLK_A3	
26	AM24	SCLK_A3#	
27	AL24	SMA_A2	
28	AM27	SMA_A10	
29	AP26	SMA_A0	
30	AP31	SMA_A13	
31	AR24	SMA_A1	
32	AR23	SMA_A4	
33	AP23	SMA_A3	
34	AN23	SMA_A6	
35	AN22	SMA_A8	
36	AF17	SDQS_A3	
37	AH18	SDQ_A27	
38	AF19	SDQ_A26	
39	AJ17	SDQ_A25	
40	AL17	SDQ_A24	
41	AF16	SDQ_A29	
42	AN18	SCKE_A2	
43	AR7	SDQS_A2#	
44	AM3	SCLK_A1#	
45	AL2	SDQS_A1#	
46	AG2	SDQS_A0#	
	A16	**EXP_SLR**	**XOR Chain #4 Output**

Table 15-18. DDR2 XOR Chain #5

Pin Count	Ball #	DDR2 Signal Name	Comments
1	Y28	SDQS_B7#	
2	AC30	SDQS_B6#	
3	AD28	SCLK_B5	
4	AG30	SDQ_B46	
5	AH30	SDQS_B5#	
6	AG24	SDM_B4	
7	AD23	SDQ_B37	
8	AF24	SDQ_B32	
9	AG26	SDQS_B4#	
10	AF20	SDQS_B3#	
11	AE22	SDQ_B30	
12	AL18	SDQ_B29	
13	AK19	SDQ_B24	
14	AG20	SDM_B3	
15	AD21	SDQ_B27	
16	AF22	SDQ_B31	
17	AH21	SDQ_B26	
18	AD18	SDQ_B28	
19	AH19	SDQ_B25	
20	AK22	SCLK_B3#	
21	AG23	SCLK_B0#	
22	AH22	SCLK_B0	
23	AN17	SRAS_B#	
24	AP18	SCAS_B#	
25	AP17	SWE_B#	
26	AR16	SBS_B0	
27	AN16	SBS_B1	
28	AN15	SMA_B2	
29	AM15	SMA_B0	
30	AP15	SMA_B10	
31	AR15	SMA_B1	
32	AL15	SMA_B3	
33	AP14	SMA_B4	
34	AP10	SCKE_B0	
35	AL14	SDQS_B2#	
36	AL9	SCLK_B1#	
37	AH10	SDQS_B1#	
38	AL4	SDQS_B0#	
	B15	**RSV**	**XOR Chain #5 Output**

Table 15-19. DDR2 XOR Chain #6

Pin Count	Ball #	DDR2 Signal Name	Comments
1	AG17	SDQS_A3#	
2	AH16	SDM_A3	
3	AE19	SDQ_A31	
4	AD17	SDQ_A30	
5	AK16	SDQ_A28	
6	AM18	SCKE_A1	
7	AM21	SMA_A11	
8	AN21	SMA_A9	
9	AP22	SMA_A5	
10	AN20	SBS_A2	
11	AP21	SMA_A7	
12	AR20	SMA_A12	
13	AP19	SCKE_A0	
14	AR19	SCKE_A3	
15	AP7	SDQS_A2	
16	AP9	SDQ_A18	
17	AN9	SDQ_A19	
18	AR8	SDQ_A23	
19	AN8	SDQ_A22	
20	AN7	SDM_A2	
21	AP6	SDQ_A17	
22	AR5	SDQ_A16	
23	AP5	SDQ_A21	
24	AN5	SDQ_A20	
25	AN2	SCLK_A4#	
26	AN3	SCLK_A4	
27	AM2	SCLK_A1	
28	AP4	SDQ_A11	
29	AP3	SDQ_A15	
30	AP2	SDQ_A14	
31	AN4	SDQ_A10	
32	AK3	SDQ_A9	
33	AK2	SDQ_A8	
34	AJ3	SDQ_A13	
35	AJ1	SDQ_A12	
36	AL1	SDM_A1	
37	AL3	SDQS_A1	
38	AG1	SDQS_A0	
39	AG3	SDQ_A6	
40	AF2	SDM_A0	
41	AH2	SDQ_A7	
42	AH3	SDQ_A2	
43	AJ2	SDQ_A3	
44	AF3	SDQ_A1	
45	AE3	SDQ_A0	
46	AE2	SDQ_A4	
47	AE1	SDQ_A5	
	C14	**RSV**	**XOR Chain #6 Output**

Table 15-20. DDR2 XOR Chain #7

Pin Count	Ball #	DDR2 Signal Name	Comments
1	AH25	SDQS_B4	
2	AD20	SDQS_B3	
3	AL23	SCLK_B3	
4	AP13	SMA_B6	
5	AR12	SMA_B9	
6	AN13	SMA_B8	
7	AL12	SMA_B7	
8	AR11	SMA_B12	
9	AP11	SMA_B11	
10	AN11	SBS_B2	
11	AM12	SMA_B5	
12	AR9	SCKE_B2	
13	AN10	SCKE_B1	
14	AM9	SCKE_B3	
15	AD15	SDQ_B19	
16	AD14	SDQ_B18	
17	AG14	SDQ_B22	
18	AH13	SDM_B2	
19	AH12	SDQ_B17	
20	AF14	SDQ_B23	
21	AD12	SDQ_B20	
22	AF13	SDQ_B16	
23	AE13	SDQ_B21	
24	AK13	SDQS_B2	
25	AL11	SCLK_B4#	
26	AJ11	SCLK_B4	
27	AK9	SCLK_B1	
28	AL8	SDQ_B9	
29	AL7	SDQ_B13	
30	AJ7	SDQ_B12	
31	AJ8	SDQ_B8	
32	AF11	SDQ_B10	
33	AG11	SDQ_B15	
34	AG10	SDQ_B14	
35	AH9	SDM_B1	
36	AE11	SDQ_B11	
37	AK10	SDQS_B1	
38	AK5	SDQS_B0	
39	AG9	SDQ_B4	
40	AH7	SDQ_B5	
41	AJ6	SDQ_B1	
42	AL6	SDQ_B2	
43	AN6	SDQ_B3	
44	AL5	SDQ_B6	
45	AJ5	SDM_B0	
46	AH4	SDQ_B0	
47	AM5	SDQ_B7	
	K15	**RSV**	**XOR Chain #7 Output**

Table 15-21. DDR2 XOR Chain #8

Pin Count	Ball #	DDR2 Signal Name	Comments
1	F11	EXP_RXN0	For SDVO interface signal name, see ballout table.
2	C9	EXP_TXN0	For SDVO interface signal name, see ballout table.
3	H11	EXP_RXN1	For SDVO interface signal name, see ballout table.
4	A8	EXP_TXN1	For SDVO interface signal name, see ballout table.
5	E9	EXP_RXN2	For SDVO interface signal name, see ballout table.
6	C7	EXP_TXN2	For SDVO interface signal name, see ballout table.
7	E7	EXP_RXN3	For SDVO interface signal name, see ballout table.
8	A6	EXP_TXN3	For SDVO interface signal name, see ballout table.
9	B4	EXP_RXN4	For SDVO interface signal name, see ballout table.
10	C5	EXP_TXN4	For SDVO interface signal name, see ballout table.
11	E5	EXP_RXN5	For SDVO interface signal name, see ballout table.
12	D2	EXP_TXN5	For SDVO interface signal name, see ballout table.
13	G5	EXP_RXN6	For SDVO interface signal name, see ballout table.
14	F3	EXP_TXN6	For SDVO interface signal name, see ballout table.
15	H7	EXP_RXN7	For SDVO interface signal name, see ballout table.
16	G1	EXP_TXN7	For SDVO interface signal name, see ballout table.
17	J5	EXP_RXN8	For SDVO interface signal name, see ballout table.
18	H3	EXP_TXN8	For SDVO interface signal name, see ballout table.
19	K7	EXP_RXN9	For SDVO interface signal name, see ballout table.
20	J1	EXP_TXN9	For SDVO interface signal name, see ballout table.
21	L5	EXP_RXN10	For SDVO interface signal name, see ballout table.
22	K3	EXP_TXN10	For SDVO interface signal name, see ballout table.
23	R10	EXP_RXN11	For SDVO interface signal name, see ballout table.
24	L1	EXP_TXN11	For SDVO interface signal name, see ballout table.
25	M7	EXP_RXN12	For SDVO interface signal name, see ballout table.
26	M3	EXP_TXN12	For SDVO interface signal name, see ballout table.
27	N5	EXP_RXN13	For SDVO interface signal name, see ballout table.
28	N1	EXP_TXN13	For SDVO interface signal name, see ballout table.
29	P8	EXP_RXN14	For SDVO interface signal name, see ballout table.
30	P3	EXP_TXN14	For SDVO interface signal name, see ballout table.
31	R5	EXP_RXN15	For SDVO interface signal name, see ballout table.
32	R1	EXP_TXN15	For SDVO interface signal name, see ballout table.
33	E11	EXP_RXP0	For SDVO interface signal name, see ballout table.
34	C10	EXP_TXP0	For SDVO interface signal name, see ballout table.
35	J11	EXP_RXP1	For SDVO interface signal name, see ballout table.
36	A9	EXP_TXP1	For SDVO interface signal name, see ballout table.
37	F9	EXP_RXP2	For SDVO interface signal name, see ballout table.
38	C8	EXP_TXP2	For SDVO interface signal name, see ballout table.
39	F7	EXP_RXP3	For SDVO interface signal name, see ballout table.
40	A7	EXP_TXP3	For SDVO interface signal name, see ballout table.
41	B3	EXP_RXP4	For SDVO interface signal name, see ballout table.
42	C6	EXP_TXP4	For SDVO interface signal name, see ballout table.
43	D5	EXP_RXP5	For SDVO interface signal name, see ballout table.
44	C2	EXP_TXP5	For SDVO interface signal name, see ballout table.
45	G6	EXP_RXP6	For SDVO interface signal name, see ballout table.

Pin Count	Ball #	DDR2 Signal Name	Comments
46	E3	EXP_TXP6	For SDVO interface signal name, see ballout table.
47	H8	EXP_RXP7	For SDVO interface signal name, see ballout table.
48	F1	EXP_TXP7	For SDVO interface signal name, see ballout table.
49	J6	EXP_RXP8	For SDVO interface signal name, see ballout table.
50	G3	EXP_TXP8	For SDVO interface signal name, see ballout table.
51	K8	EXP_RXP9	For SDVO interface signal name, see ballout table.
52	H1	EXP_TXP9	For SDVO interface signal name, see ballout table.
53	L6	EXP_RXP10	For SDVO interface signal name, see ballout table.
54	J3	EXP_TXP10	For SDVO interface signal name, see ballout table.
55	P10	EXP_RXP11	For SDVO interface signal name, see ballout table.
56	K1	EXP_TXP11	For SDVO interface signal name, see ballout table.
57	M8	EXP_RXP12	For SDVO interface signal name, see ballout table.
58	L3	EXP_TXP12	For SDVO interface signal name, see ballout table.
59	N6	EXP_RXP13	For SDVO interface signal name, see ballout table.
60	M1	EXP_TXP13	For SDVO interface signal name, see ballout table.
61	P7	EXP_RXP14	For SDVO interface signal name, see ballout table.
62	N3	EXP_TXP14	For SDVO interface signal name, see ballout table.
63	R6	EXP_RXP15	For SDVO interface signal name, see ballout table.
64	P1	EXP_TXP15	For SDVO interface signal name, see ballout table.
	H16	**BSEL0**	**XOR Chain #8 Output**

Table 15-22. DDR2 XOR Chain #9

Pin Count	Ball #	DDR2 Signal Name	Comments
1	U6	DMI_RXN0	
2	U5	DMI_RXP0	
3	T3	DMI_TXN0	
4	R3	DMI_TXP0	
5	T8	DMI_RXN1	
6	T9	DMI_RXP1	
7	U1	DMI_TXN1	
8	T1	DMI_TXP1	
9	V8	DMI_RXN2	
10	V7	DMI_RXP2	
11	V3	DMI_TXN2	
12	U3	DMI_TXP2	
13	U10	DMI_RXN3	
14	V10	DMI_RXP3	
15	W5	DMI_TXN3	
16	V5	DMI_TXP3	
	E15	**BSEL1**	**XOR Chain #9 Output**

15.7 PADs Excluded from XOR Mode(s)

A large number of pads do not support XOR testing. The majority of the pads that fall into this category are analog related pins (see Table 15-23).

Table 15-23. XOR Pad Exclusion List

PCI Express*	Host Interface	System Memory	Misc
GCLKN	HCLKN	SRCOMP1	DREFCLKN
GCLKP	HCLKP	SRCOMP0	DREFCLKP
EXP_COMPO	HRCOMP	SMVREF1	BLUE
EXP_COMPI	HSCOMP	SMVREF0	BLUE#
	HVREF	SOCOMP1	GREEN
	HSWING	SOCOMP0	GREEN#
		SM_SLEWOUT1	RED
		SM_SLEWOUT0	RED#
		SM_SLEWIN1	RSTIN#
		SM_SLEWIN0	HSYNC
			VSYNC
			REFSET

§