

DATA SHEET

MB2541

Dual octal buffer line driver (3-State)

Product specification
Supersedes data of 1993 Aug 18
IC23 Data Handbook

1998 Jan 16

16-bit buffer/line drivers (3-State)

MB2541

FEATURES

- Two 8-bit bus interfaces
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffers sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Inputs are disabled during 3-State mode

DESCRIPTION

The MB2541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2541 has two 8-bit buffers that are ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA.

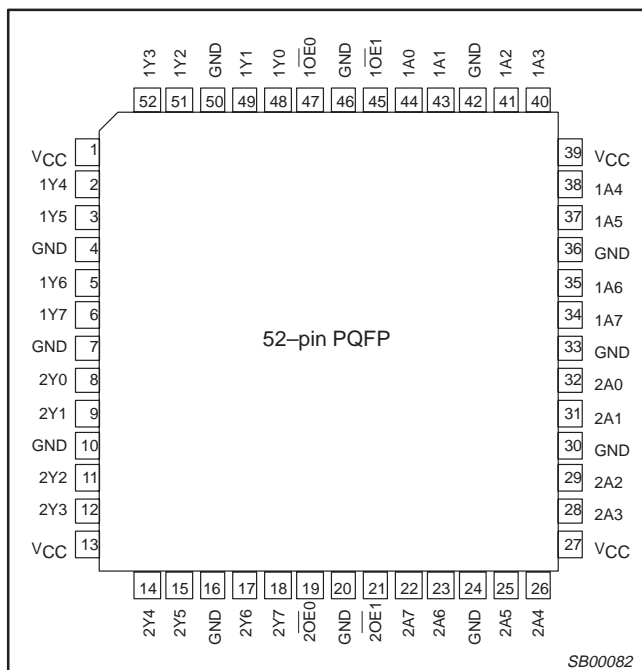
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nlx to nYx	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	3.0 3.1	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	65	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
52-pin plastic Quad Flat Pack	-40°C to $+85^{\circ}\text{C}$	MB2541 BB	MB2541 BB	SOT379-1

PIN CONFIGURATION



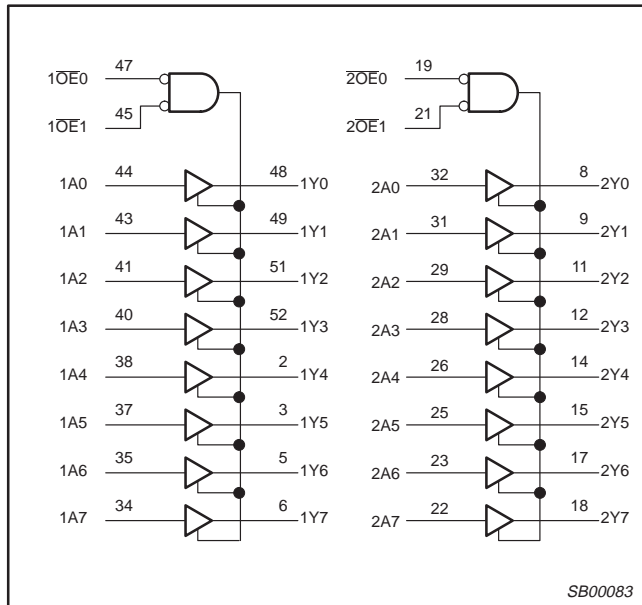
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
44, 43, 41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 26, 25, 23, 22	1A0 – 1A7 2A0 – 2A7	Data inputs
48, 49, 51, 52, 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18	1Y0 – 1Y7, 2Y0 – 2Y7	Data outputs
47, 45, 19, 21	$\overline{1OE0}$, $\overline{1OE1}$, $\overline{2OE0}$, $\overline{2OE1}$	Output enables
4, 7, 10, 16, 20, 24, 30, 33, 36, 42, 46, 50	GND	Ground (0V)
1, 13, 27, 39	V_{CC}	Positive supply voltage

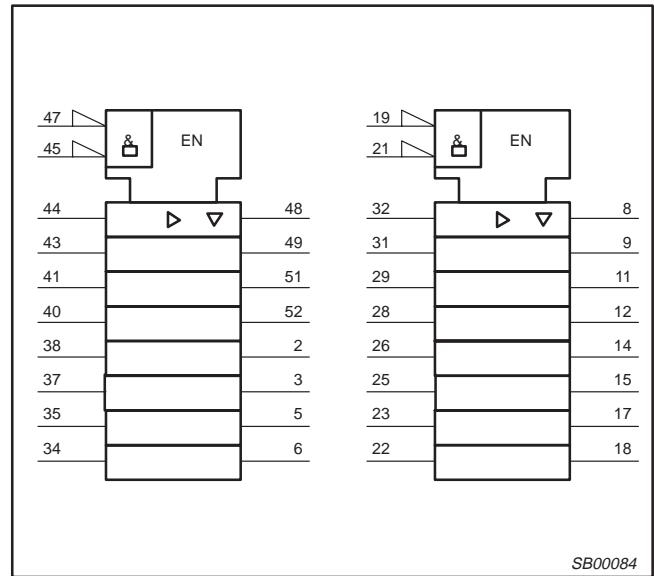
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LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS
nOE0	nOE1	nIx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	$V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 4.5\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL} \text{ or } V_{IH}$	2.5	2.9		2.5		V
		$V_{CC} = 5.0\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL} \text{ or } V_{IH}$	3.0	3.4		3.0		V
		$V_{CC} = 4.5\text{V}; I_{OH} = -32\text{mA}; V_I = V_{IL} \text{ or } V_{IH}$	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.5\text{V}; I_{OL} = 64\text{mA}; V_I = V_{IL} \text{ or } V_{IH}$		0.42	0.55		0.55	V
I_I	Input leakage current	$V_{CC} = 5.5\text{V}; V_I = \text{GND or } 5.5\text{V}$		± 0.01	± 1.0		± 1.0	μA
I_{OFF}	Power-off leakage current	$V_{CC} = 0.0\text{V}; V_O \text{ or } V_I \leq 4.5\text{V}$		± 5.0	± 100		± 100	μA
I_{PU}/I_{PD}	Power-up/down 3-State output current	$V_{CC} = 2.0\text{V}; V_O = 0.5\text{V}; V_I = \text{GND or } V_{CC}; V_{OE} = V_{CC}$		± 5.0	± 50		± 50	μA
I_{OZH}	3-State output High current	$V_{CC} = 5.5\text{V}; V_O = 2.7\text{V}; V_I = V_{IL} \text{ or } V_{IH}$		5.0	50		50	μA
I_{OZL}	3-State output Low current	$V_{CC} = 5.5\text{V}; V_O = 0.5\text{V}; V_I = V_{IL} \text{ or } V_{IH}$		-5.0	-50		-50	μA
I_{CEX}	Output high leakage current	$V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND or } V_{CC}$		5.0	50		50	μA
I_O	Output current ¹	$V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$	-50	-70	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	$V_{CC} = 5.5\text{V}; \text{Outputs High, } V_I = \text{GND or } V_{CC}$		65	250		250	μA
I_{CCL}		$V_{CC} = 5.5\text{V}; \text{Outputs Low, } V_I = \text{GND or } V_{CC}$		48	60		60	mA
I_{CCZ}		$V_{CC} = 5.5\text{V}; \text{Outputs 3-State; } V_I = \text{GND or } V_{CC}$		65	250		250	μA
ΔI_{CC}	Additional supply current per input pin ²	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

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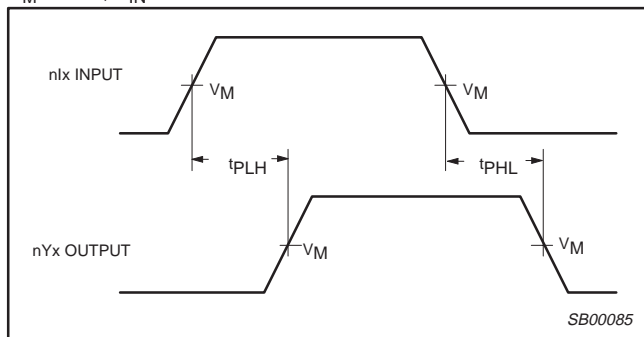
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

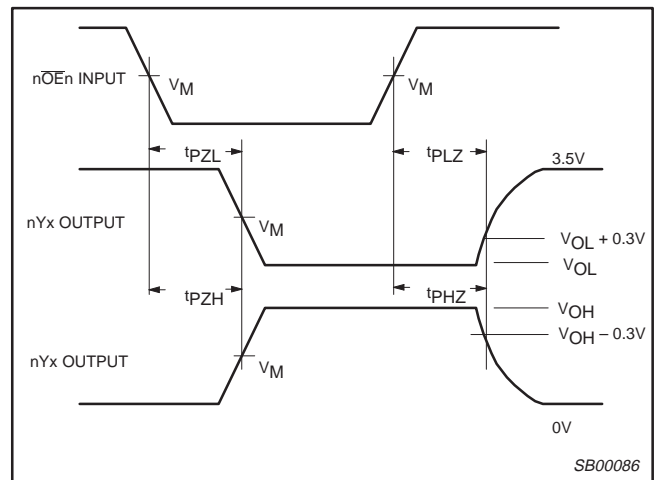
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nIx to nYx	1	1.2 1.2	3.0 3.1	4.5 4.5	1.2 1.2	5.1 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.1	3.6 4.7	5.2 6.1	1.3 2.1	5.8 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.8 1.7	4.3 4.0	6.2 5.4	1.8 1.7	6.8 5.9	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

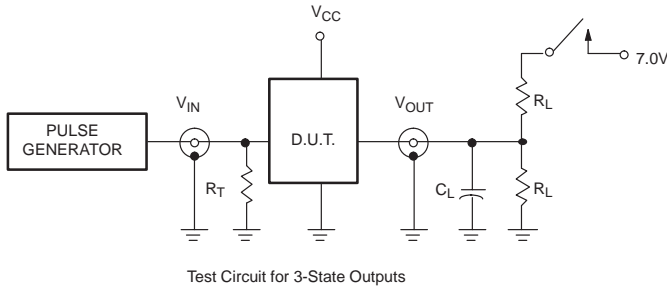


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

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TEST CIRCUIT AND WAVEFORMS



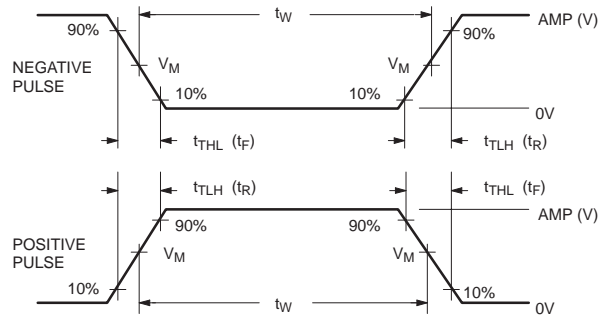
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{pZL}	closed
All other	open

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



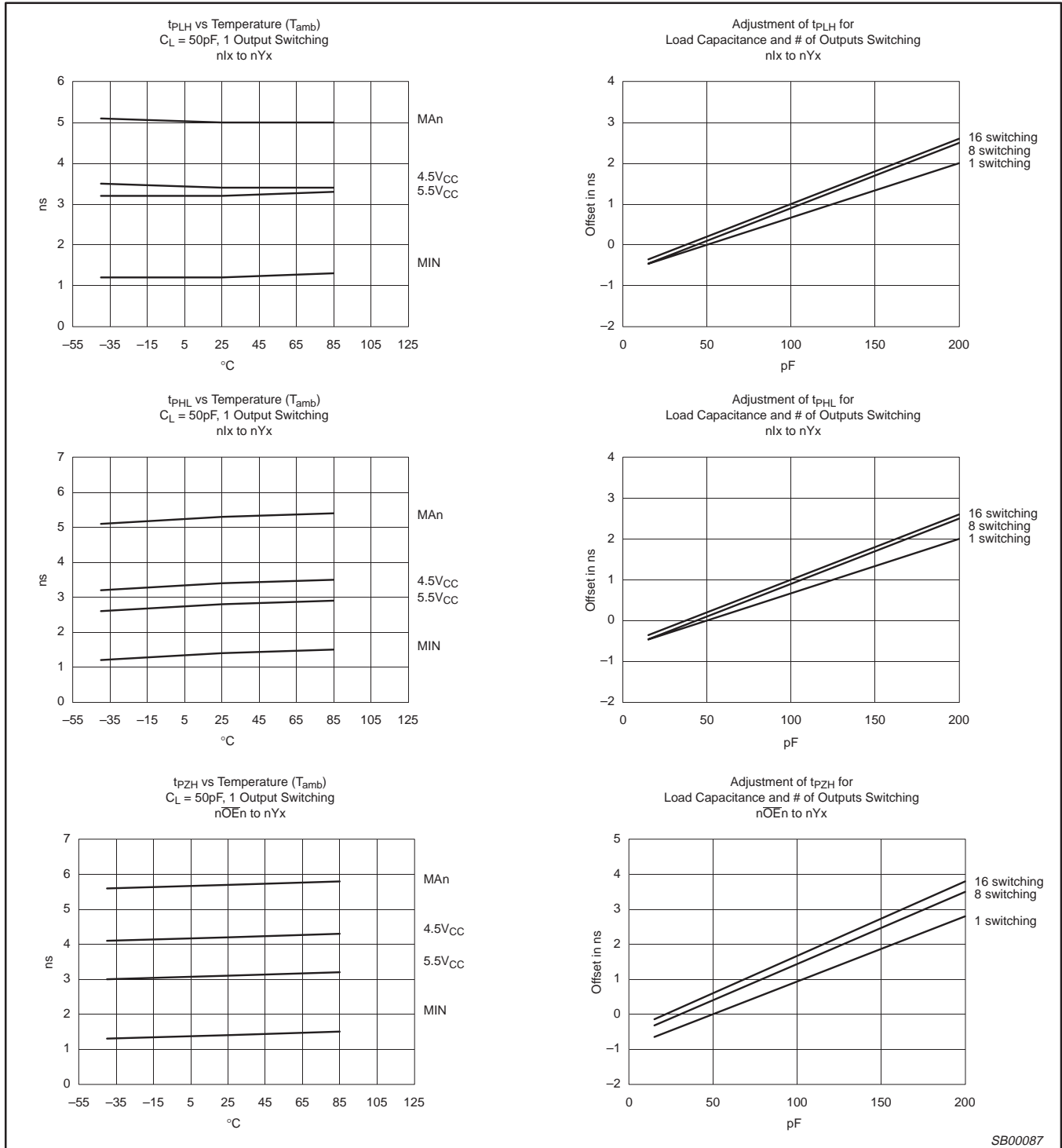
$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_r	t_f
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

SB00010

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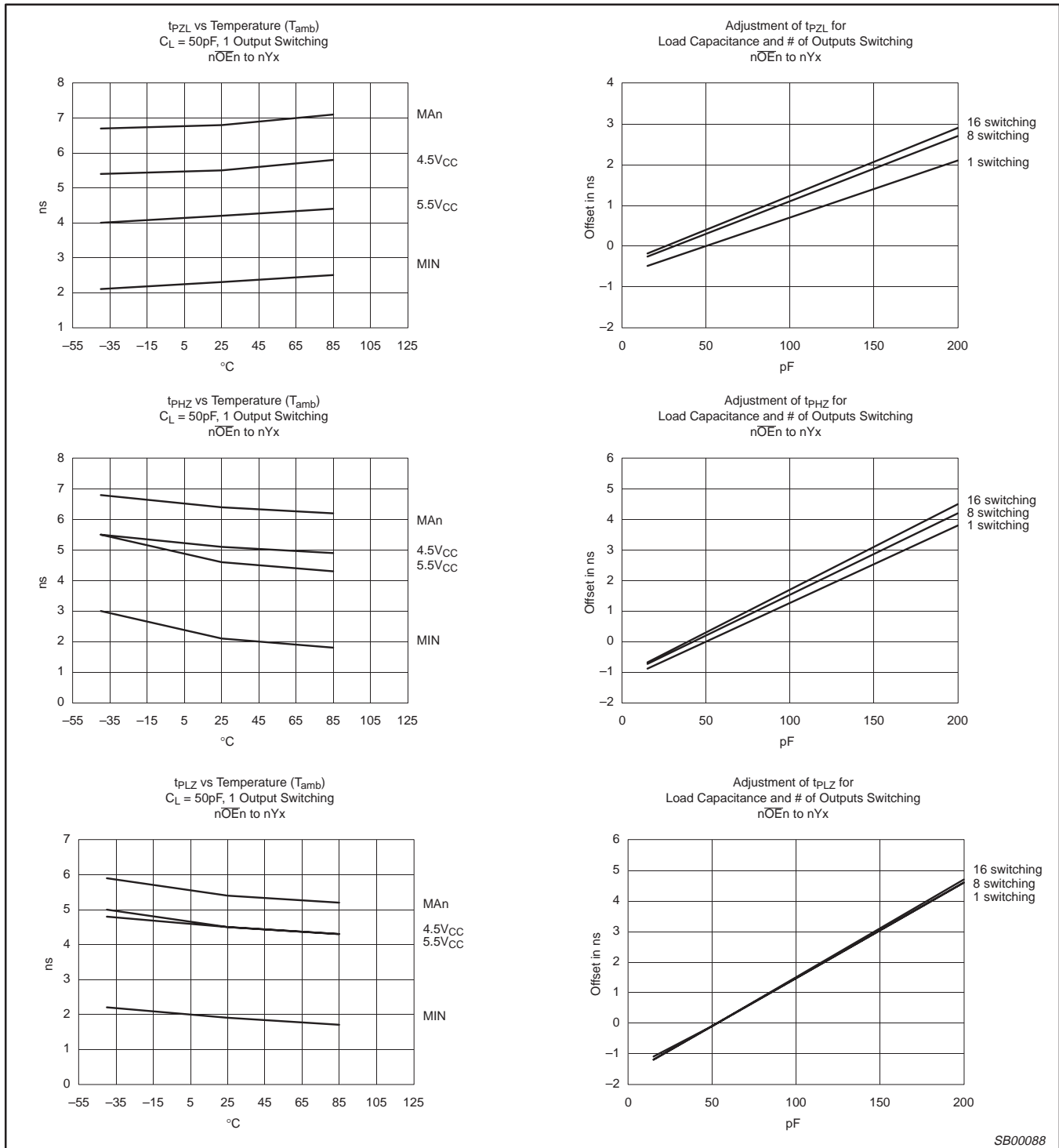
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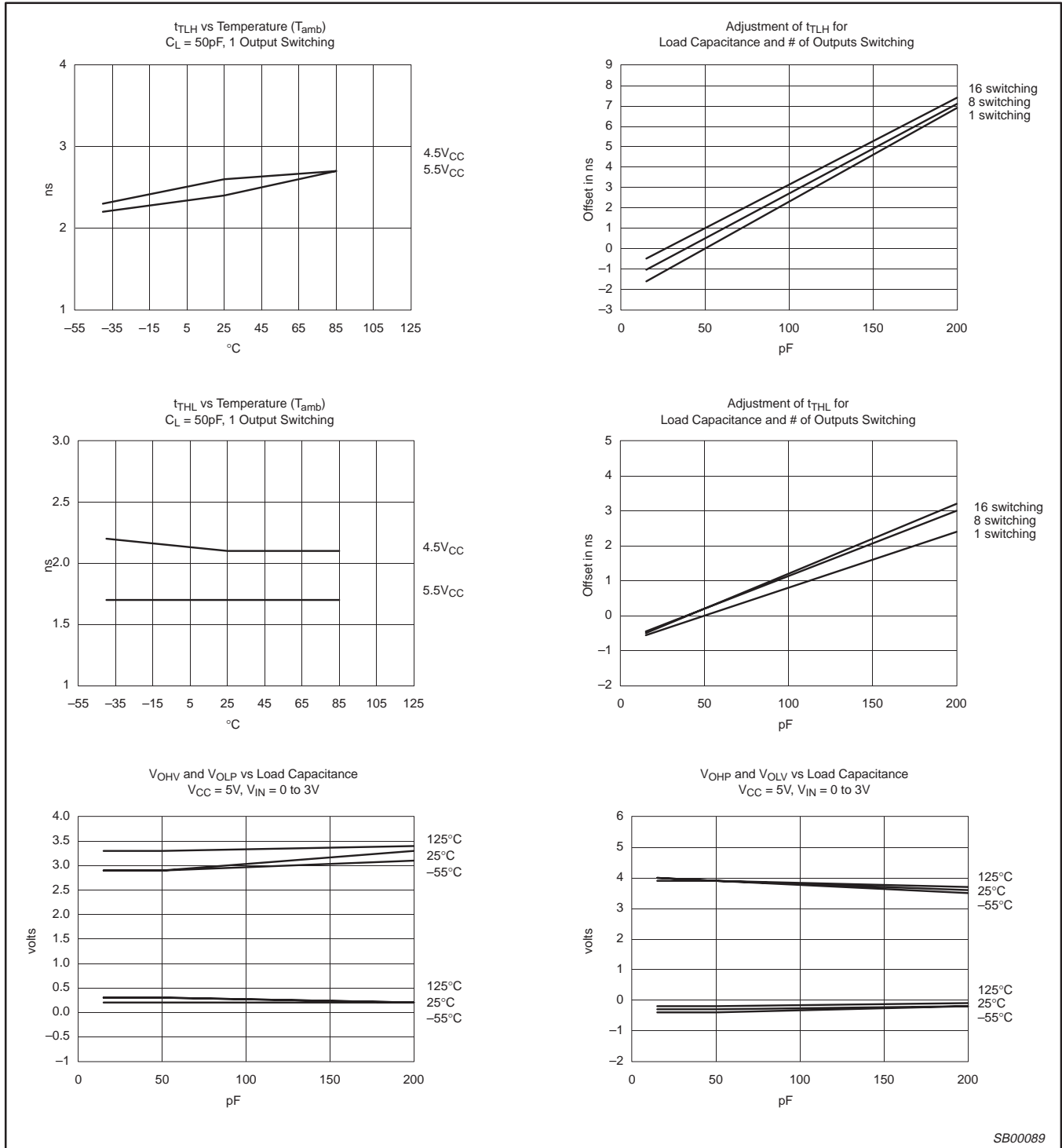
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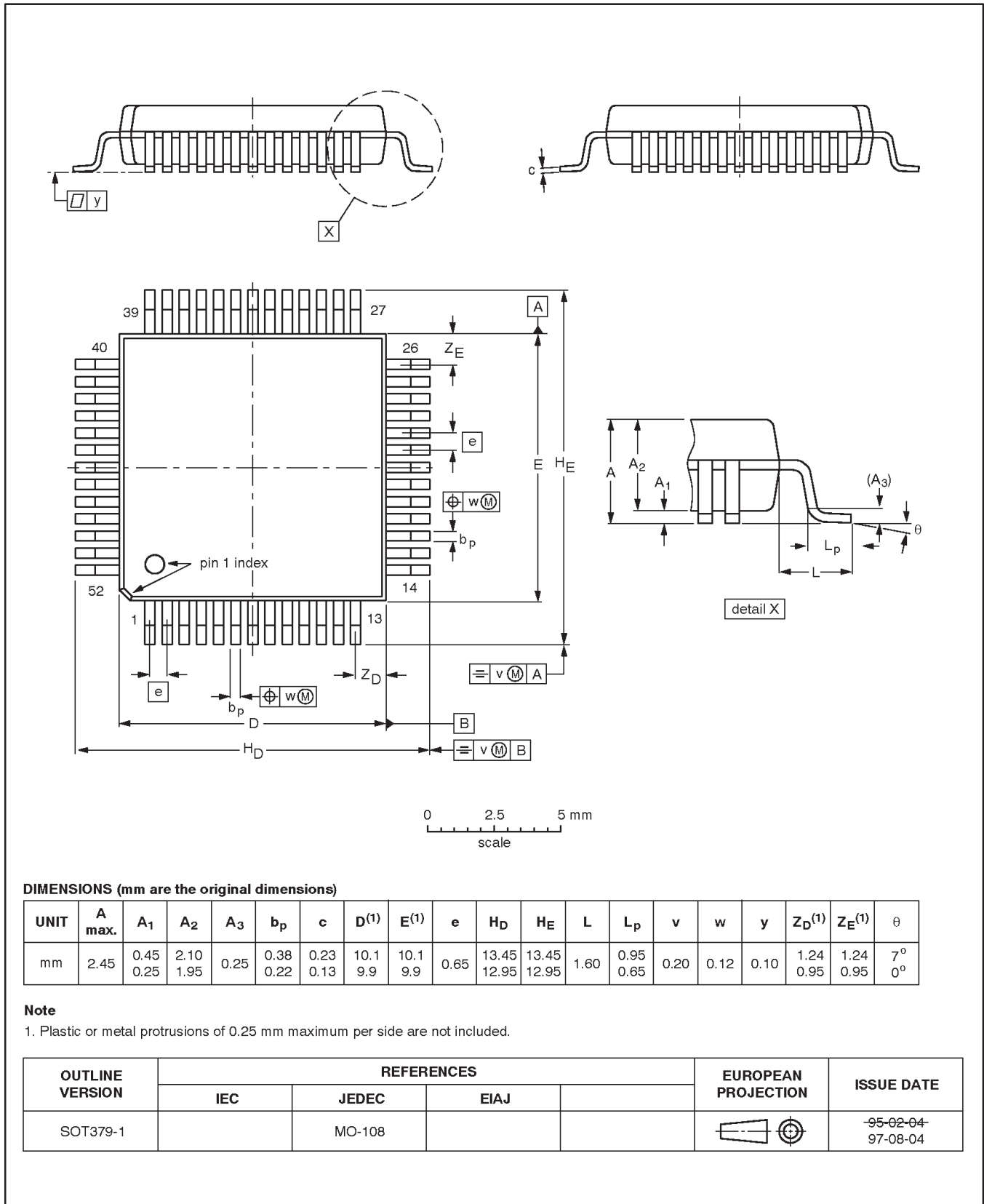
SB00089

Dual octal buffer line driver (3-State)

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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



Dual octal buffer line driver (3-State)

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NOTES

Dual octal buffer line driver (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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