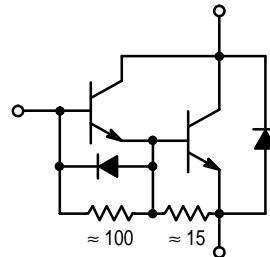


MJ10023

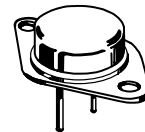
Designer's™ Data Sheet
SWITCHMODE Series
NPN Silicon Power Darlington
Transistor with Base-Emitter
Speedup Diode

The MJ10023 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 150 ns Inductive Fall Time @ 25°C (Typ)
 - 300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range – 65 to + 200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



40 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
400 VOLTS
250 WATTS



CASE 197A-05
TO-204AE (TO-3)

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V _{CEO}	400	Vdc
Collector-Emitter Voltage	V _{CEV}	600	Vdc
Emitter Base Voltage	V _{EB}	80	Vdc
Collector Current — Continuous	I _C	40	Adc
— Peak (1)	I _{CM}	80	
Base Current — Continuous	I _B	20	Adc
— Peak (1)	I _{BM}	40	
Total Power Dissipation @ T _C = 25°C	P _D	250	Watts
@ T _C = 100°C		143	
Derate above 25°C		1.43	W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MJ10023

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I _C = 100 mA, I _B = 0)	V _{CEO(sus)}	400	—	—	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEV}	—	—	0.25 5.0	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V _{EB} = 2.0 V, I _C = 0)	I _{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	I _{S/b}			See Figure 13	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 14	

ON CHARACTERISTICS (1)

DC Current Gain (I _C = 10 Adc, V _{CE} = 5.0 V)	h _{FE}	50	—	600	—
Collector–Emitter Saturation Voltage (I _C = 20 Adc, I _B = 1.0 Adc) (I _C = 40 Adc, I _B = 5.0 Adc) (I _C = 20 Adc, I _B = 10 Adc, T _C = 100°C)	V _{CE(sat)}	—	—	2.2 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I _C = 20 Adc, I _B = 1.2 Adc) (I _C = 20 Adc, I _B = 1.2 Adc, T _C = 100°C)	V _{BE(sat)}	—	—	2.5 2.5	Vdc
Diode Forward Voltage (I _F = 20 Adc)	V _f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1.0 kHz)	C _{ob}	150	—	600	pF
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SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 20 A, I _{B1} = 1.0 Adc, V _{BE(off)} = 5.0 V, t _p = 50 μs, Duty Cycle ≤ 2.0%)	t _d	—	0.03	0.2	μs
Rise Time		t _r	—	0.4	1.2	μs
Storage Time		t _s	—	0.9	2.5	μs
Fall Time		t _f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _{CM} = 20 A, V _{CEM} = 250 V, I _{B1} = 1.0 A, V _{BE(off)} = 5 V, T _C = 100°C)	t _{sv}	—	1.9	4.4	μs
Crossover Time		t _c	—	0.6	2.0	μs
Fall Time		t _{fi}	—	0.3	—	μs
Storage Time	(I _{CM} = 20 A, V _{CEM} = 250 V, I _{B1} = 1.0 A, V _{BE(off)} = 5 V, T _C = 25°C)	t _{sv}	—	1.0	—	μs
Crossover Time		t _c	—	0.3	—	μs
Fall Time		t _{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

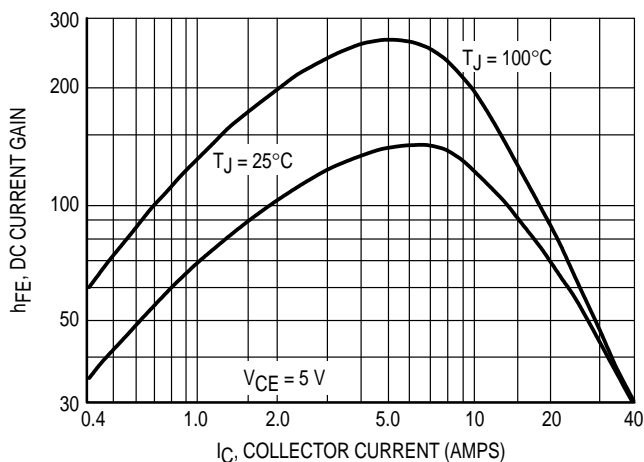


Figure 1. DC Current Gain

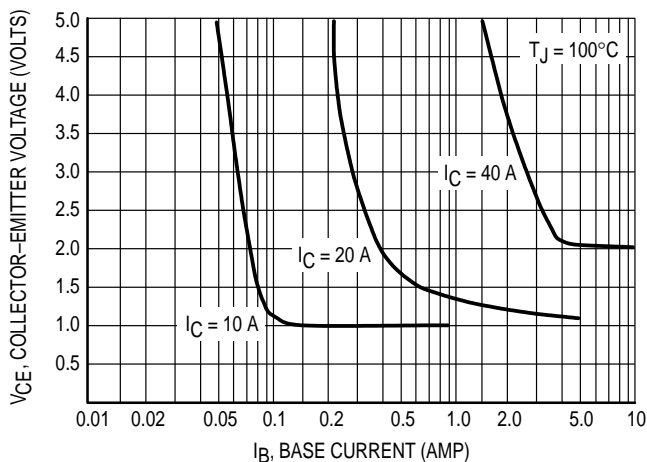


Figure 2. Collector Saturation Region

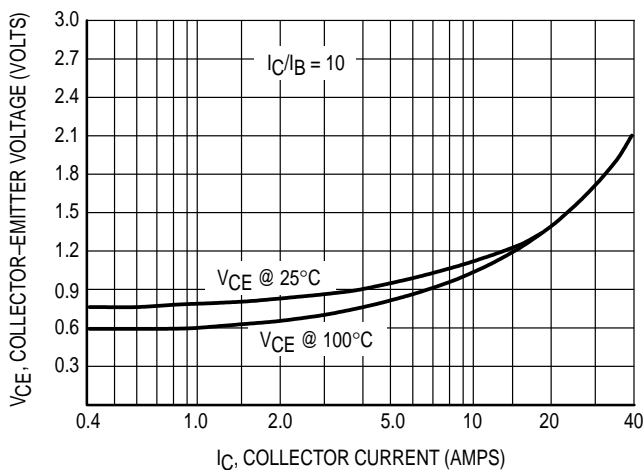


Figure 3. Collector-Emitter Saturation Voltage

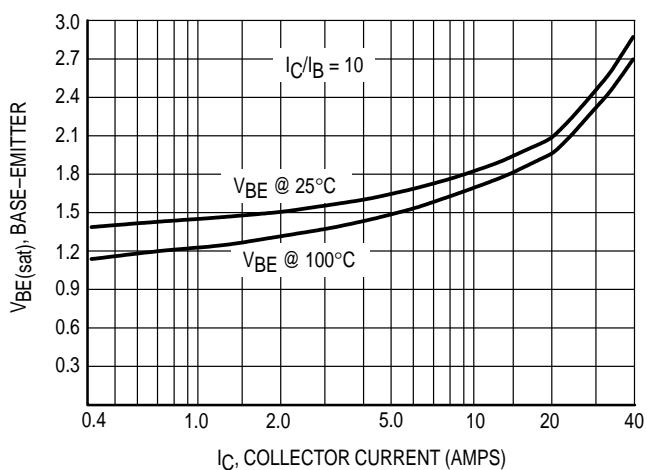


Figure 4. Base-Emitter Saturation Voltage

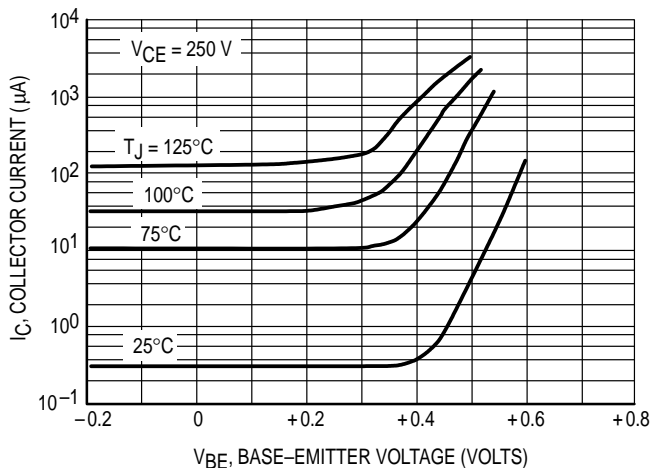


Figure 5. Collector Cutoff Region

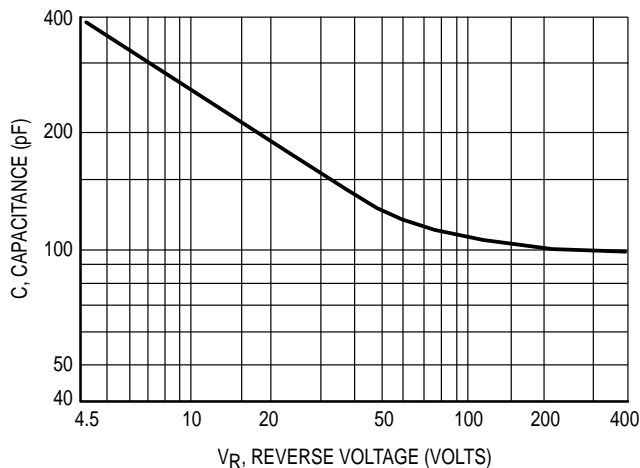


Figure 6. C_{Ob} , Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	V _{CEO(sus)}	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain I_C = 100 mA</p>	<p>INDUCTIVE TEST CIRCUIT</p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p>TURN-ON TIME</p> <p>I_{B1} adjusted to obtain the forced h_{FE} desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	L _{coil} = 10 mH, V _{CC} = 10 V R _{coil} = 0.7 Ω V _{clamp} = V _{CEO(sus)}	L _{coil} = 180 μH R _{coil} = 0.05 Ω V _{CC} = 20 V	V _{CC} = 250 V R _L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	<p>OUTPUT WAVEFORMS</p> <p>t₁ Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>	

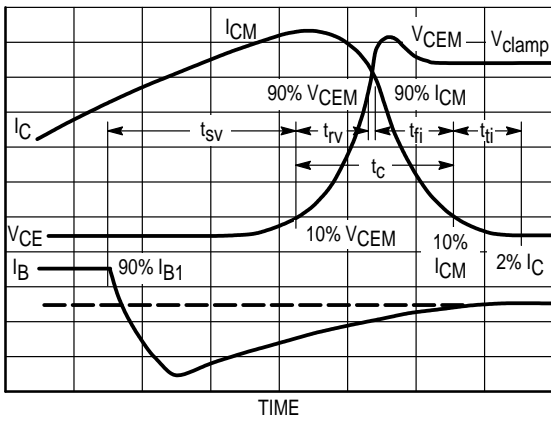


Figure 7. Inductive Switching Measurements

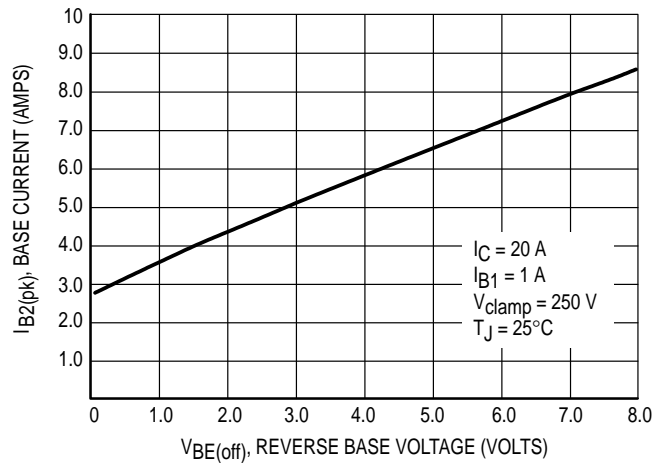


Figure 8. Typical Peak Reverse Base Current

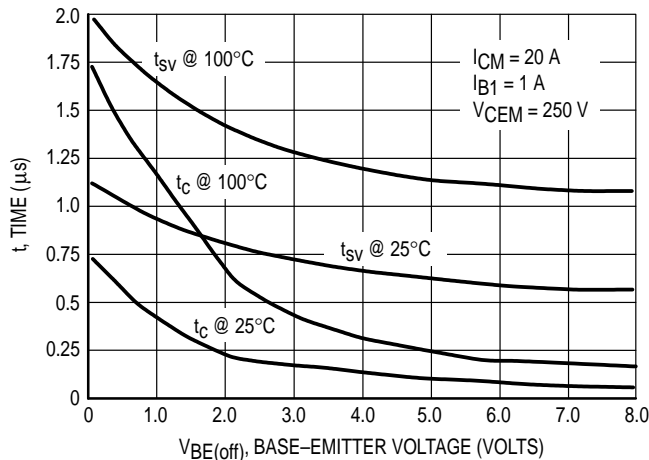


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
- t_{RV} = Voltage Rise Time, 10–90% V_{CEM}
- t_{fi} = Current Fall Time, 90–10% I_{CM}
- t_{ti} = Current Tail, 10–2% I_{CM}
- t_C = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is

shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \cong t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

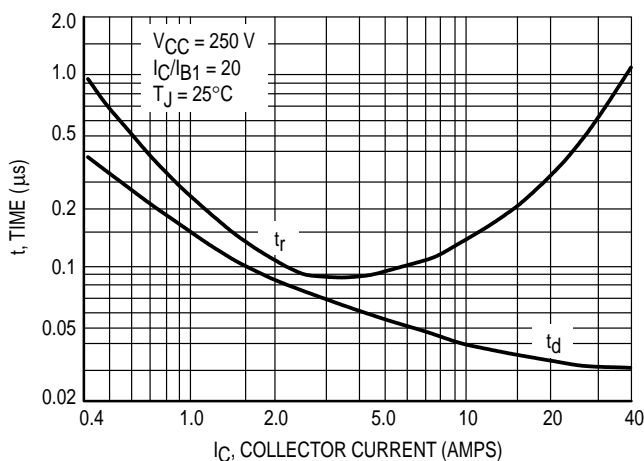


Figure 10. Typical Turn-On Switching Times

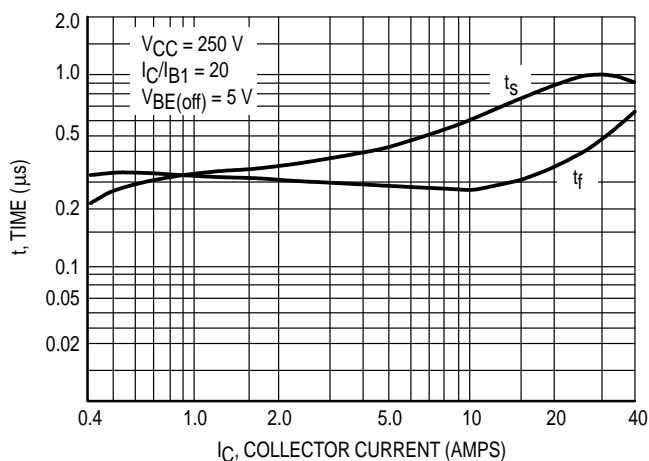


Figure 11. Typical Turn-Off Switching Times

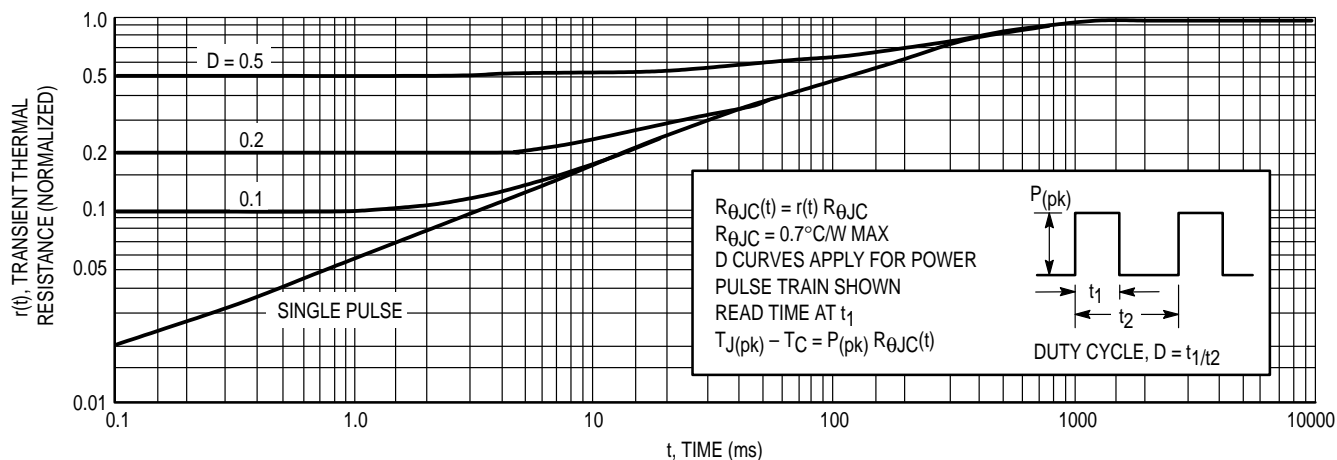


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

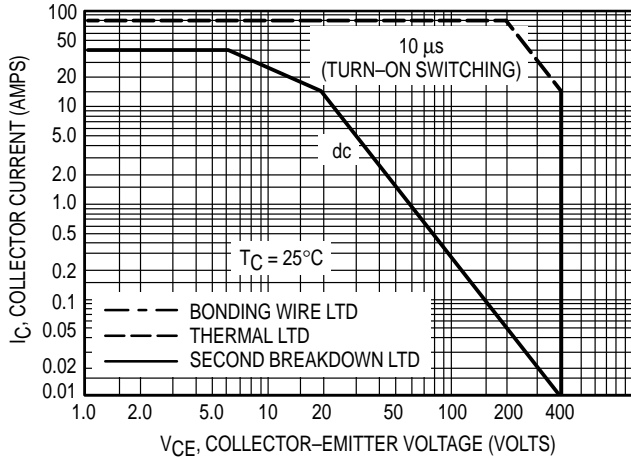


Figure 13. Maximum Forward Bias Safe Operating Area

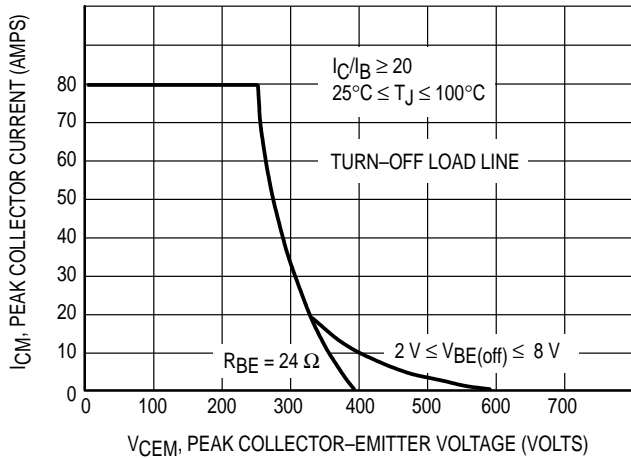


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

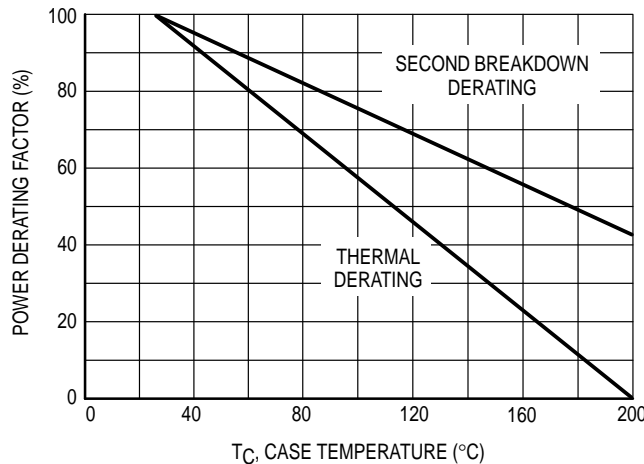
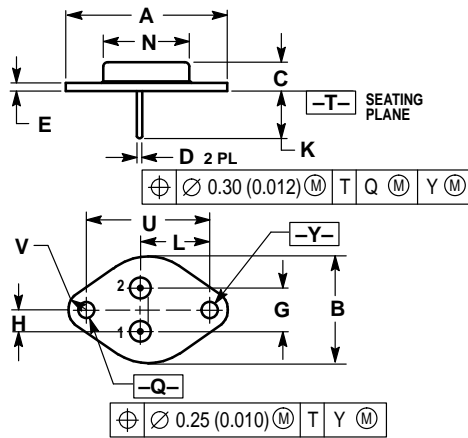


Figure 15. Power Derating

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
 PIN 1: BASE
 2: EMITTER
 CASE: COLLECTOR

**CASE 197A-05
 TO-204AE (TO-3)
 ISSUE J**

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