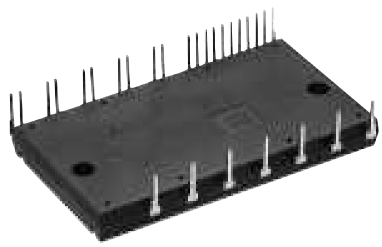
PS22052

TRANSFER-MOLD TYPE
INSULATED TYPE

PS22052



INTEGRATED POWER FUNCTIONS

1200V/5A low-loss 4th generation IGBT inverter bridge for 3 phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

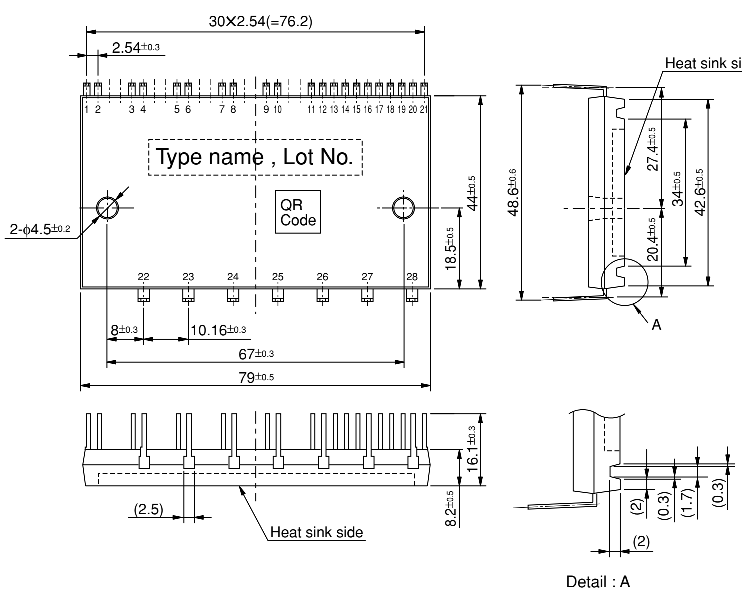
- For upper-leg IGBTS :Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTS : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible (High active logic).

APPLICATION

AC400V 0.2kW~0.4kW inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



1. VUFS	22. P
2. VUFB	23. U
3. VP1	24. V
4. UP	25. W
5. VVFS	26. NU
6. VVFB	27. NV
7. VP1	28. NW
8. VP	
9. VWFS	
10. VWFB	
11. VP1	
12. VPC	
13. WP	
14. VN1	
15. VNC	
16. CIN	
17. CFO	
18. FO	
19. UN	
20. VN	
21. WN	

All external terminals are treated with lead free solder (ingredient : Sn-Cu) plating.

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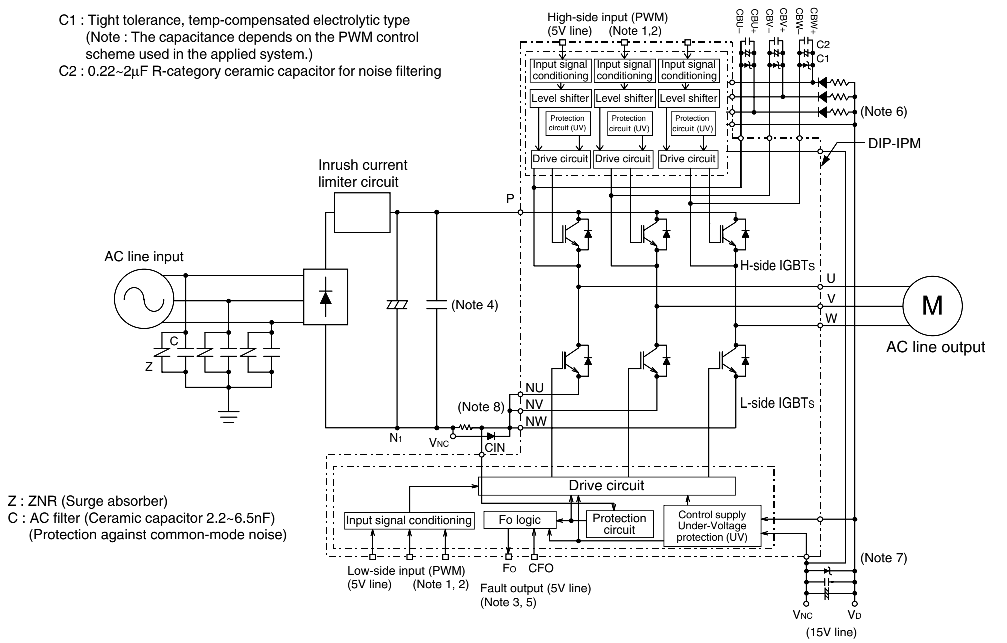
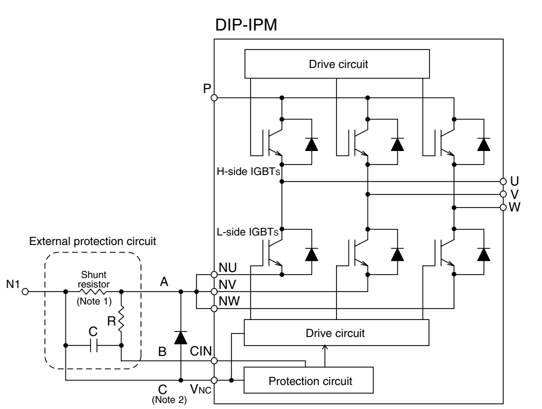
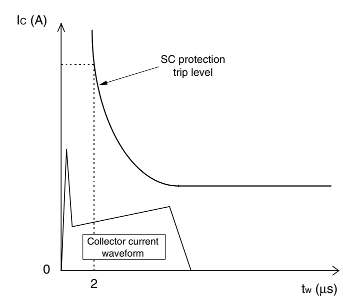
Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)



Note1: To prevent input signals oscillation, an RC coupling at each input terminal is recommended.
2: By virtue of integrating HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
3: Fo output is open drain type. The signal line should be pulled up to the positive side of a 5V supply with an approximate 10kΩ resistor.
4: The wiring between the power DC-link capacitor and the P/N1 terminals should be as short as possible to protect DIP-IPM against catastrophic high surge voltage. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to mount closely to the P and N1 terminals.
5: Fo output pulse width (t_{FO}) should be determined by connecting external capacitor between CFO and V_{NC} terminals. (Example : t_{FO}=2.4ms(typ.) at C_{FO}=22nF)
6: High voltage (1200V or more) and fast recovery type (less than 100ns) diodes should be used for the bootstrap circuit.
7: It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
8: To prevent LVIC from surge destruction, it is recommended to mount a fast recovery type diode between V_{NC} and NU, NV, NW terminals.

Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT





Note1: In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0µs.
2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) with a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output.
Since the SC fault may be repetitive, it is recommended to stop the system and check the fault, when the Fo signal is received.

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MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	900	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	1000	V
V_{CES}	Collector-emitter voltage		1200	V
$\pm I_C$	Each IGBT collector current	T_C = 25°C	5	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C = 25°C, less than 1ms	10	A
P_C	Collector dissipation	T_C = 25°C, per 1 chip	38.3	W
T_j	Junction temperature	(Note 1)	–20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_C \le$ 100°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \le$ 125°C (@ $T_C \le$ 100°C).

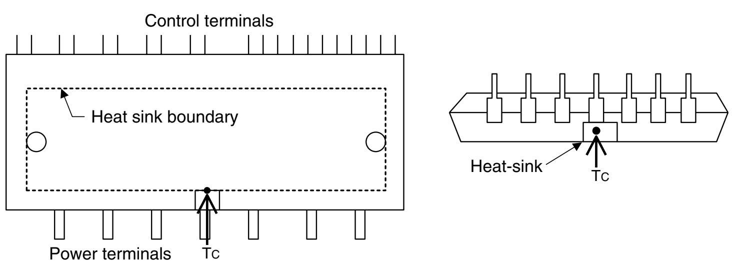
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	–0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	–0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	–0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short circuit protection capability)	V_D = 13.5~16.5V, Inverter part T_j = 125°C, non-repetitive, less than 2 μs	800	V
T_C	Module case operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	V_{rms}

Note 2 : T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
$R_{th(j-c)Q}$	Junction to case thermal resistance	Inverter IGBT part (per 1/6 module)	—	—	2.61	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	—	—	3.18	°C/W
$R_{th(c-f)}$	Contact thermal resistance (Note 3)	Case to fin, (per 1 module) thermal grease applied	—	—	0.047	°C/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100µm~+200µm on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB}$ = 15V, V_{IN} = 5V, I_C = 5A	T_j = 25°C	—	2.7	3.4	V
			T_j = 125°C	—	2.5	3.2	
V_{EC}	FWDi forward voltage	$-I_C$ = 5A, V_{IN} = 0V		—	2.4	2.9	V
t_{on}	Switching times	V_{CC} = 600V, $V_D = V_{DB}$ = 15V, I_C = 5A, T_j = 125°C, $V_{IN} = 0 \leftrightarrow 5V$, Inductive load (upper-lower arm)		0.8	1.5	2.2	µs
t_{rr}				—	0.2	—	µs
$t_{c(on)}$				—	0.4	0.7	µs
t_{off}				—	2.8	3.8	µs
$t_{c(off)}$				—	0.4	0.7	µs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
I_D	Circuit current	$V_D = V_{DB}$ = 15V, V_{IN} = 5V	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	—	—	3.70	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	1.30	mA
		$V_D = V_{DB}$ = 15V, V_{IN} = 0V	Total of V_{P1}-V_{PC}, V_{N1}-V_{NC}	—	—	3.50	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	1.30	mA
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O circuit pull-up to 5V with 10kΩ		4.9	—	—	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		—	—	1.10	V
$V_{SC(ref)}$	Short circuit trip level	T_j = 25°C, V_D = 15V (Note 4)		0.43	0.48	0.53	V
I_{IN}	Input current	V_{IN} = 5V		0.7	1.5	2.0	mA
UV_{DBt}	Supply circuit under-voltage protection	$T_j \leq 125°C$	Trip level	10.0	—	12.0	V
UV_{DBr}			Reset level	10.5	—	12.5	V
UV_{Dt}			Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V
t_{FO}	Fault output pulse width	C_{FO} = 22nF (Note 5)		1.6	2.4	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}		2.0	3.0	4.2	V
$V_{th(off)}$	OFF threshold voltage			0.8	1.4	2.0	V

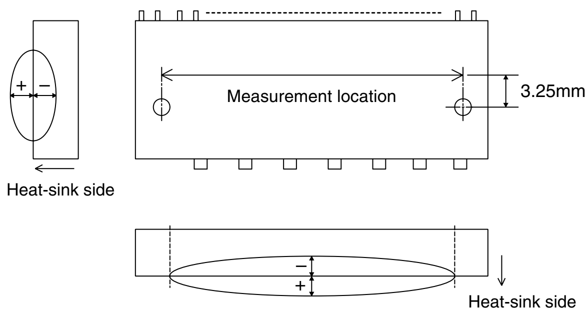
Note 4 : Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 1.7 times device current rating.

5 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 9.3 \times 10^{-6} \times t_{FO}$ [F].

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw : M4	Recommended 1.18 N·m	0.98	—	1.47	N·m
Weight			—	77	—	g
Heat-sink flatness		(Note 6)	–50	—	100	µm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW		350	600	800	V
V_D	Control supply voltage	Applied between V_{P1}-V_{PC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}		13.5	15.0	16.5	V
ΔV_D, ΔV_{DB}	Control supply variation			–1	—	1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal, $T_C \le 100°C$		3.3	—	—	µs
f_{PWM}	PWM input frequency	$T_C \le 100°C$, $T_j \le 125°C$		—	—	15	kHz
I_O	Output r.m.s. current	V_{CC} = 600V, V_D = 15V, f_C = 15kHz P.F = 0.8, sinusoidal PWM $T_j \le 125°C$, $T_C \le 100°C$ (Note 7)		—	—	1.8	Arms
PWIN(on)	Minimum input pulse width	(Note 8)		1.5	—	—	µs
PWIN(off)		$350 \le V_{CC} \le 800V$, $13.5 \le V_D \le 16.5V$, $13.5 \le V_{DB} \le 16.5V$, $-20°C \le T_C \le 100°C$, N line wiring inductance less than 10nH (Note 9)	$I_C \le 5A$	2.6	—	—	
			$5 < I_C \le 8.5A$	2.8	—	—	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		–5.0	—	5.0	V

Note 7 : The output r.m.s. current value depends on the actual application conditions.
8 : DIP-IPM might not make response to the input on signal with pulse width less than PWIN (on).
9 : DIP-IPM might not make response or work properly if the input off signal pulse width is less than PWIN (off).

Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

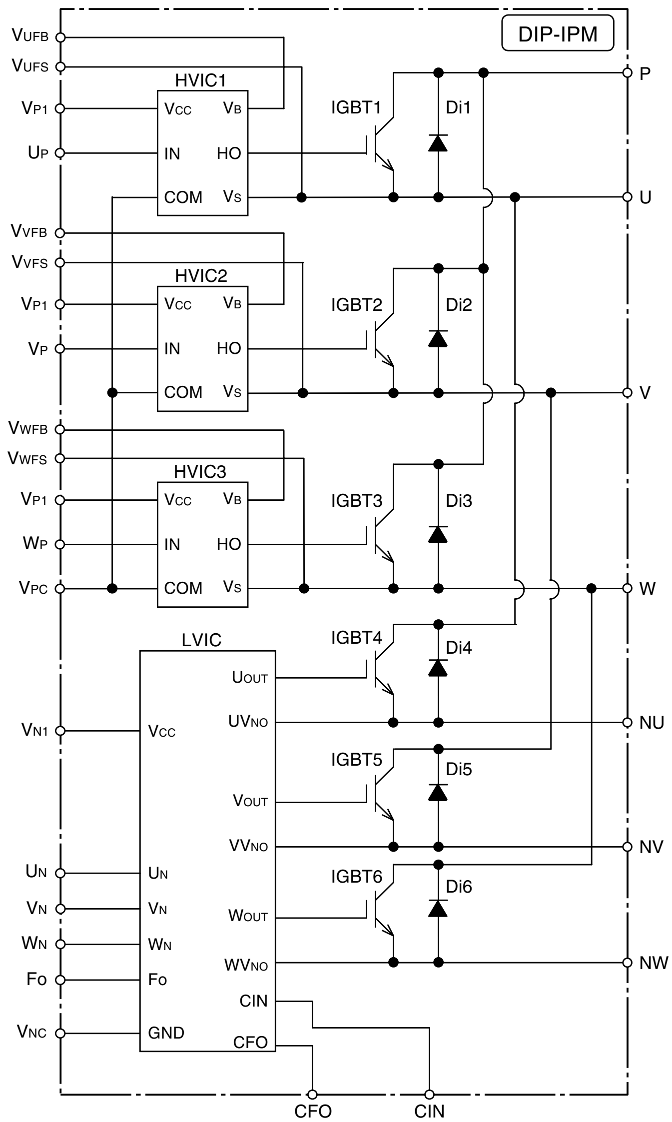


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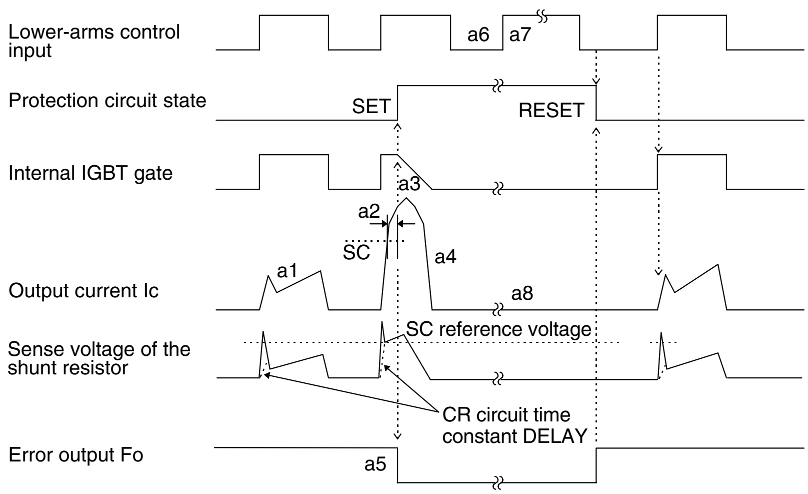
Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

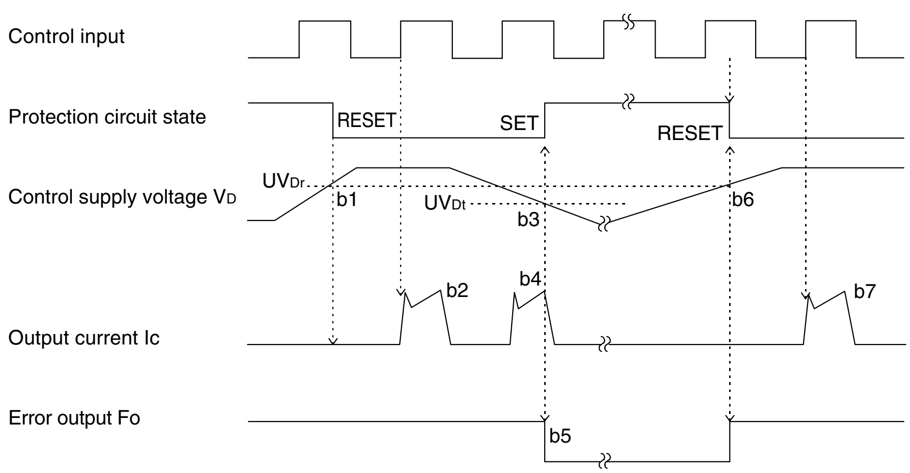
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. FO output with a fixed pulse width determined by the external capacitor CFO.
a6. Input = "L" : IGBT OFF
a7. Input = "H" :
a8. IGBT OFF state in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UVD)

b1. Control supply voltage rising : After the voltage level reaches UVDr, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip (UVDt).
b4. IGBT OFF in spite of control input condition.
b5. FO keeps output during the UV period, however, FO pulse is not less than the fixed width for very short UV interval.
b6. Under voltage reset (UVDr).
b7. Normal operation : IGBT ON and carrying current.



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[C] Under-Voltage Protection (Upper-side, UV_{DB})

c1. Control supply voltage rises : After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip (UV_{DBt}).
c4. IGBT OFF in spite of control input signal level, but there is no F_O signal output.
c5. Under voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.

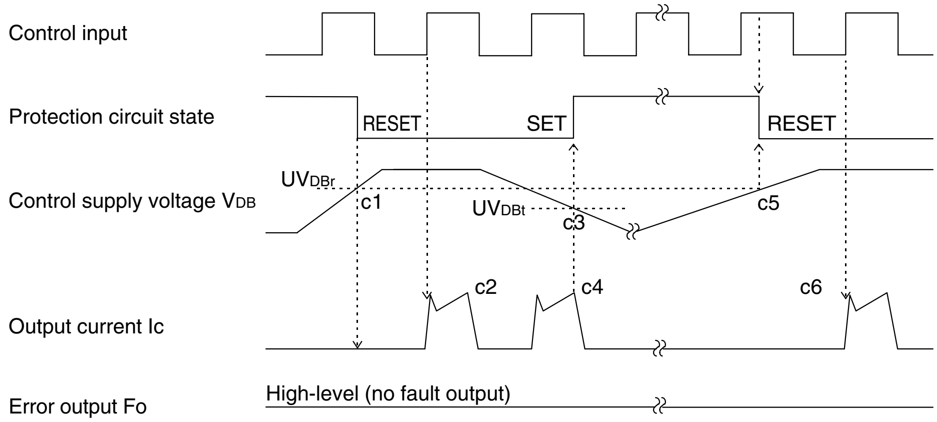
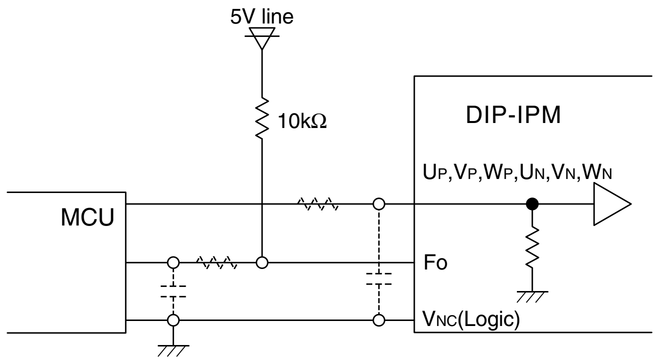
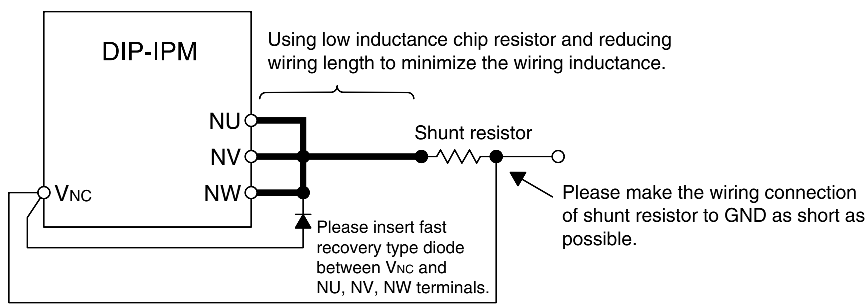


Fig. 6 MCU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using a external filtering resistor, pay attention to the turn-on threshold voltage requirement.

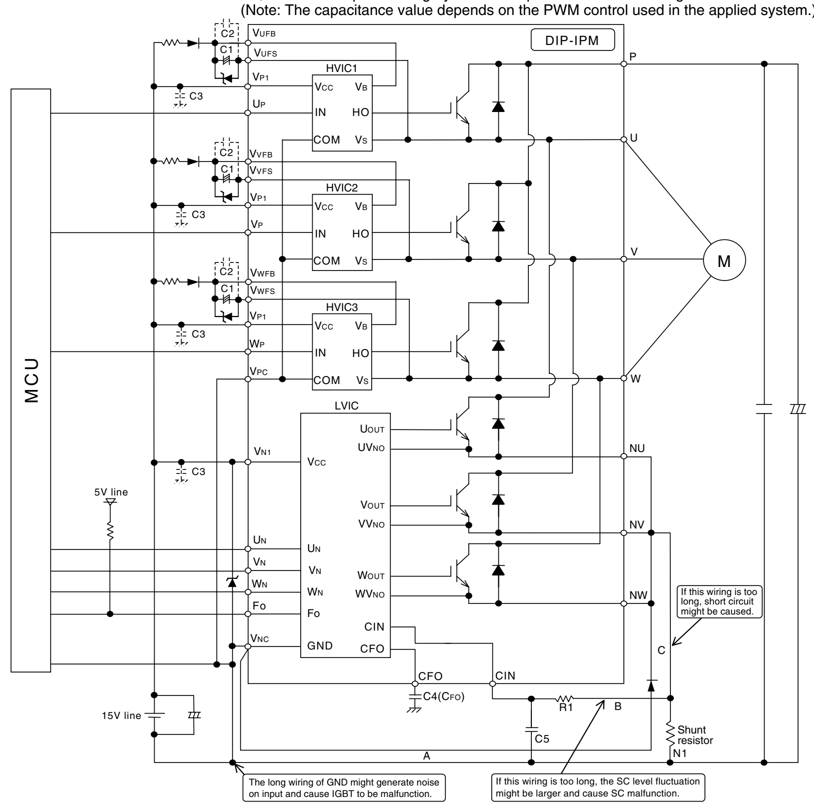
Fig. 7 WIRING CONNECTION WITH 1 SHUNT RESISTOR



For 3 shunt resistors connection, please refer to Fig.9.

Fig. 8 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT WITH 1 SHUNT RESISTOR

C1:Tight tolerance temp-compensated electrolytic type
C2,C3: 0.1~0.22µF R-category ceramic capacitor for noise filtering.
(Note: The capacitance value depends on the PWM control used in the applied system.)



Note 1 : To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

2: By virtue of integrating HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.

3: Fo output is open drain type. The signal line should be pulled up to the positive side of a 5V supply with an approximate 10kΩ resistor.

4: Fo output pulse width (t_{FO}) should be determined by connecting external capacitor C4 between CFO and V_{NC} terminals. (Example : t_{FO}=2.4ms(typ.) at C_{FO}=22nF)

5: Input signal is High-Active type. There is a 2.5kΩ (Min.) resistor inside IC to pull down each input signal line to GND. When employing RC coupling circuits at each input, set up RC couple such that input signal agree with turn-off/turn-on threshold voltage.

6: To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

7: The time constant R5C1 of the protection circuit should be selected in the range of 1.5~2µs. SC interrupting time might vary with the wiring pattern.

8: All capacitors should be mounted as close to the terminals of the DIP-IPM as possible.

9: To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Generally a 0.1~0.22µF snubber between the P&N1 terminals is recommended.

10: It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

11: To prevent LVIC from surge destruction, it is recommended to mount a fast recovery type diode between V_{NC} and NU, NV, NW terminals.

Fig. 9 EXAMPLE OF EXTERNAL PROTECTION CIRCUIT WITH 3 SHUNT RESISTORS