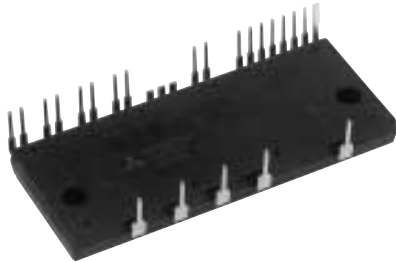


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INTEGRATED POWER FUNCTIONS

- Single phase AC input, DC output IGBT/FWD converter bridge
- 600V, 20Arms (Input current)

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

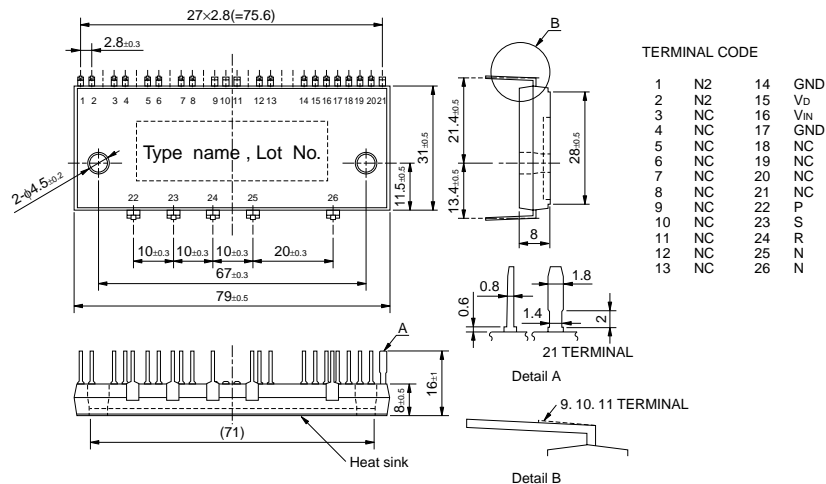
- IGBTs driver circuit
- Control supply under-voltage (UV) protection
- Input interface : 5~15V line CMOS/TTL compatible, Schmitt Trigger receiver circuit (Active high)

APPLICATION

AC100~200V Active-Converter for PFC (Power Factor Correction), of Air-conditioner and so on.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

MAIN CIRCUIT PART

Symbol	Parameter	Conditions	Ratings	Unit
V_i	Supply Voltage	Applied between : S-R	264	V_{rms}
$V_{i(surge)}$	Supply Voltage (surge)	Applied between : S-R, Surge value, Non-operating	500	V
V_o	Output Voltage	Applied between : P-N	450	V
$V_{o(surge)}$	Output Voltage (surge)	Applied between : P-N, Surge value, Non-operating	500	V
V_{CES}	Collector-Emitter Voltage	—	600	V
V_{RRM}	Repetitive Peak Reverse Voltage	—	600	V
I_i	Input Current (100% Load)	$T_c \leq +90^\circ\text{C}$, $V_i = 200\text{V}$, $V_o = 300\text{V}$, $f_{PWM} = 20\text{kHz}$	20	Arms
$I_{i(125\%)}$	Input Current (125% Load)	$T_c \leq +90^\circ\text{C}$, $V_i = 200\text{V}$, $V_o = 300\text{V}$, $f_{PWM} = 20\text{kHz}$, 1 min Non-repetitive	25	Arms
I^2t	I^2t for Fu sing	Value for 1msec of Surge Current	120	A^2s
T_j	Junction Temperature	(Note 1)	-20~+125	$^\circ\text{C}$

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-PFC is 150°C (@ $T_c \leq 100^\circ\text{C}$) however, to ensure safe operation of the DIP-PFC, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C}$ (@ $T_c \leq 100^\circ\text{C}$).

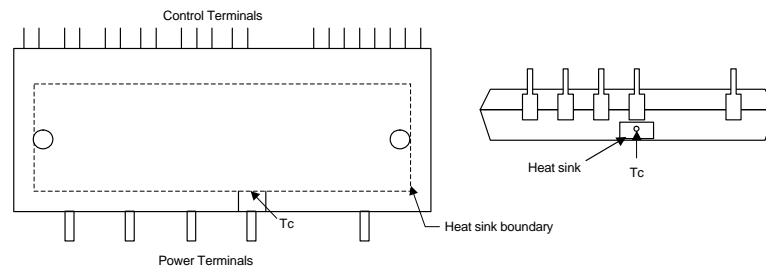
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between : V_D -GND	20	V
V_{IN}	Control input voltage	Applied between : V_{IN} -GND	0- $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
T_c	Module case operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V_{rms}

Note 2 : T_c MEASUREMENT POINT



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Rth(j-c)Q	Junction to case thermal resistance	Inverter IGBT part	—	—	1.55	°C/W
Rth(j-c)F		Inverter FWDi part	—	—	1.90	°C/W
Rth(c-f)	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.067	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
VCE(sat)	Collector-emitter saturation voltage	V _D = 15V, V _{IN} = 5V, I _C = 50A	—	1.8	2.4	V
V _F	Forward voltage	I _F = 50A	—	2.1	2.6	V
t _{on}	Switching times	V _{CC} = 300V, V _D = 15V I _C = 30A, T _j = 125°C, V _{IN} = 5V ↔ 0V Inductive load	—	0.29	—	μs
t _{rr}			—	0.13	—	μs
t _{c(on)}			—	0.15	—	μs
t _{off}			—	0.46	—	μs
t _{c(off)}			—	0.17	—	μs
I _{CES}	Collector-emitter cut-off current	V _{CE} = 600V	T _j = 25°C		1	mA
			T _j = 125°C		10	
I _R	Reverse current	V _R = 600V	T _j = 25°C		1	mA
			T _j = 125°C		10	
I _{rr}	FWDi reverse recovery current	V _{CC} = 300V, V _D = 15V, I _C = 30A, T _j = 25°C	—	13	—	A

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _D	Control supply voltage	Applied between : V _D -GND	13.5	15.0	16.5	V	
I _D	Circuit current	Applied between : V _D = 15V, V _{IN} = 5V V _D -GND	—	0.8	3.0	mA	
		V _D = 15V, V _{IN} = 0V	—	0.7	3.0		
I _{IN}	Control input current	V _D = 15V, V _{IN} = 5V	—	0.3	0.45	mA	
V _{th(on)}	ON threshold voltage	Applied between : V _{IN} -GND	—	3.0	3.7	V	
V _{th(off)}	OFF threshold voltage		1.3	2.0	—	V	
U _{VDt}	Supply circuit under-voltage protection	T _j ≤ 125°C	Trip level		10.3	12.5	V
U _{VDr}			Reset level		10.8	—	13.0

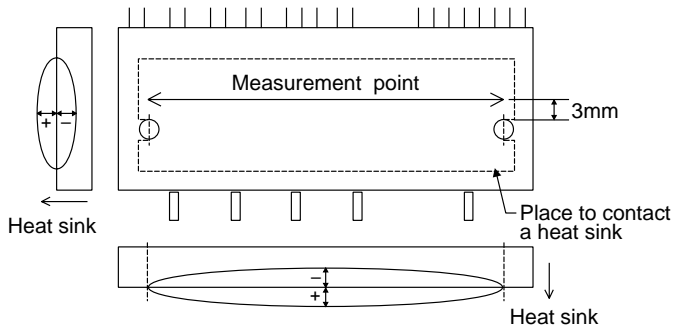
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MECHANICAL CHARACTERISTICS AND RATINGS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting screw : M4	0.98	1.18	1.47	N·m
—	Weight		—	54	—	g
—	Heat-sink flatness	(Note 3)	-50	—	100	μm

Note 3: Measurement point of heat-sink flatness



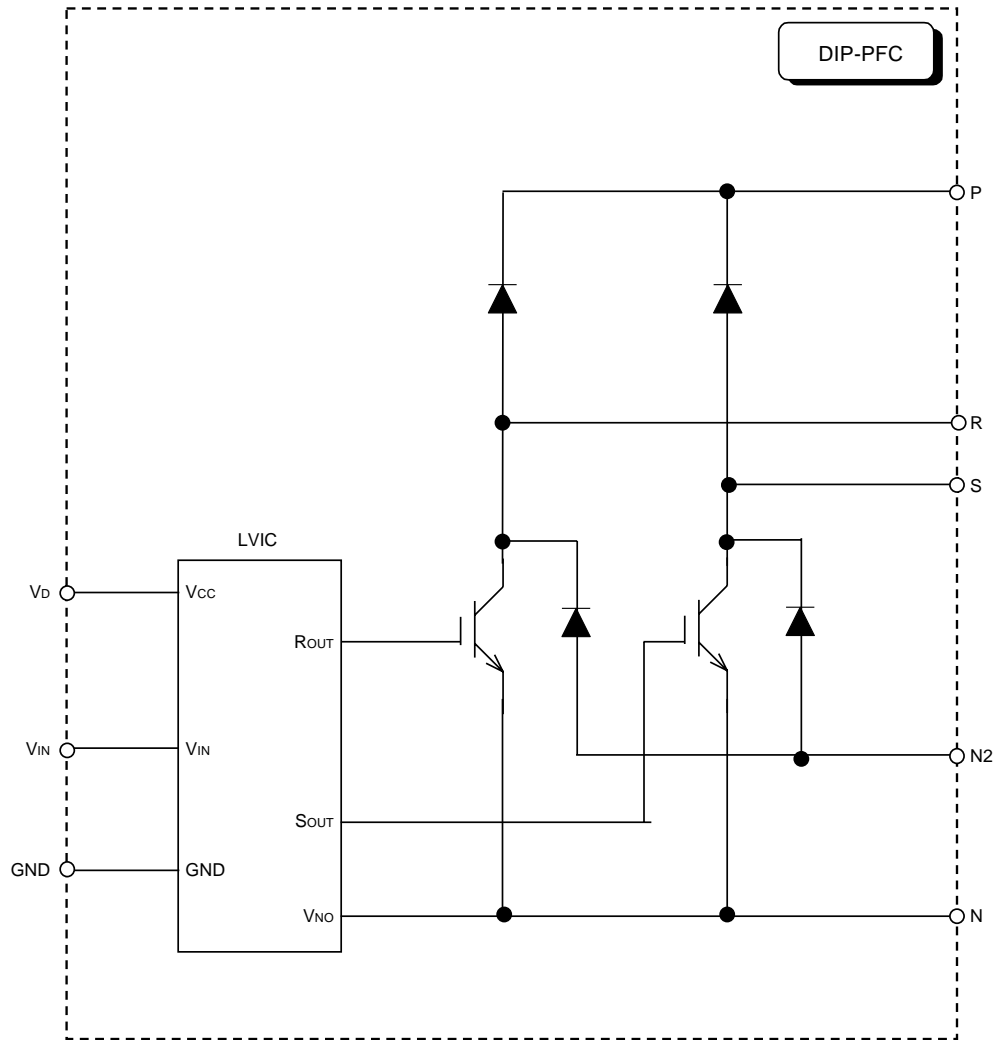
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_i	Supply voltage	Applied between : S-R	90	—	264	V _{rms}
V_D	Control supply voltage	Applied between : VD-GND	13.5	15.0	16.5	V
ΔV_D	Control supply variation		-1	—	1	V/μs
f_{PWM}	PWM input frequency	$T_c \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$	—	20	—	kHz
$V_{IN(on)}$	Input ON threshold voltage	Applied between : VIN-GND	4.0~ V_D			V
$V_{IN(off)}$	Input OFF threshold voltage		0~1.0			V

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Fig. 2 THE DIP-PFC INTERNAL CIRCUIT



DIP-PFC Wiring Guidelines

Because DIP-PFC switches large current at a very high speed, considerable large surge voltage is generated easily between P and N terminals. Please pay attention to the following items:

- The area of P-Co-N shown in Fig. 3 should be as small as possible because the rectangle shaped switching current flows on this route. In addition, please add a bypass condenser Co' with good frequency response such as a polypropylene film condenser closely to the P and N terminals.
- The two IGBT emitters are connected to the VNO terminal of LVIC inside the DIP-PFC. If the internal wiring inductance shown as $L1$ and $L2$ in Fig. 4 is too large, large surge voltage will be generated by di/dt . Especially, the lower the temperature, the faster the switching speed, therefore the larger the di/dt . This surge voltage applies to the VNO and N terminals, which is possible to destruct LVIC.
- In order to suppress the surge voltage, the external wiring method shown in Fig. 4 is recommended. To reduce the parasitic wiring inductance, the wiring of the external terminals of N(N-1) and N(N-2) should be made as short as possible.
- Please mount a fast clamp diode (EG01Y@Sanken) between N and control GND terminals to prevent control GND potential variation from the minus voltage of N terminal.

Fig. 3 DIP-PFC INTERFACE

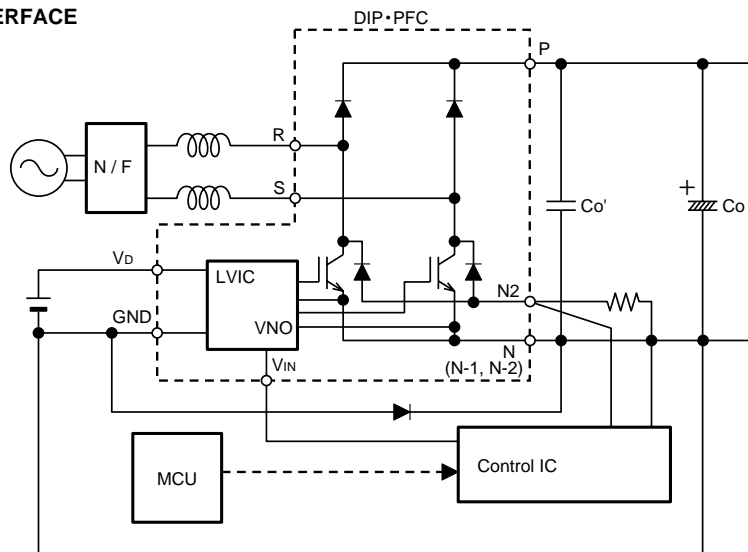


Fig. 4 RECOMMENDED WIRING METHOD

