USING INTELLIGENT POWER MODULES

6.0 Introduction to Intelligent Power Modules (IPM)

Mitsubishi Intelligent Power Modules (IPMs) are advanced hybrid power devices that combine high speed, low loss IGBTs with optimized gate drive and protection circuitry. Highly effective over-current and short-circuit protection is realized through the use of advanced current sense IGBT chips that allow continuous monitoring of power device current. System reliability is further enhanced by the IPM's integrated over temperature and under voltage lock out protection. Compact, automatically assembled Intelligent Power Modules are designed to reduce system size, cost, and time to market. Mitsubishi Electric introduced the first full line of Intelligent Power Modules in November, 1991. Continuous improvements in power chip, packaging, and control circuit technology have lead to the IPM lineup shown in Table 6.1.

6.0.1 Third Generation Intelligent Power Modules

Mitsubishi third generation intelligent power module family shown in Table 6.1 represents the industries most complete line of IPMs. Since their original introduction in 1993 the series has been expanded to include 36 types with ratings ranging from 10A 600V to 800A 1200V. The power semiconductors used in these modules are based on the field proven H-Series IGBT and diode processes. In Table 6.1 the third generation family has been divided into two groups, the "Low Profile Series" and "High Power Series" based on the packaging technology that is used. The third generation IPM has been optimized for minimum switching losses in order to meet industry demands for acoustically noiseless inverters with carrier frequencies up to 20kHz. The built in gate drive and protection has been carefully designed to minimize the components required for the user supplied interface circuit.

6.0.2 V-Series High Power IPMs

The V-Series IPM was developed in order to address newly emerging industry requirements for higher reliability, lower cost and reduced EMI. By utilizing the low inductance packaging technology developed for the U-Series IGBT module (described in Section 4.1.5) combined with an advanced super soft freewheel diode and optimized gate drive and protection circuits the V-Series IPM family achieves improved performance at reduced cost. The detailed descriptions of IPM operation and interface requirements presented in Sections 6.1 through 6.8 apply to V-Series as well as third generation IPMs. The only exception being that V-Series IPMs have a unified short circuit protection function that takes the place of the separate short circuit and over current functions described in Sections 6.4.4 and 6.4.5. The unified protection was made

Table 6.1 Mitsubishi Intelligent Power Modules

Type Number	Amps	Power Circuit
Third Generation Low Profile Series - 600V		
PM10CSJ060	10	Six IGBTs
PM15CSJ060	15	Six IGBTs
PM20CSJ060	20	Six IGBTs
PM30CSJ060	30	Six IGBTs
PM50RSK060	50	Six IGBTs + Brake ckt.
PM75RSK060	75	Six IGBTs + Brake ckt.
Third Generation Low Profile Series - 1200V		
PM10CZF120	10	Six IGBTs
PM10RSH120	10	Six IGBTs + Brake ckt.
PM15CZF120	15	Six IGBTs
PM15RSH120	15	Six IGBTs + Brake ckt.
PM25RSK120	25	Six IGBTs + Brake ckt.
Third Generation High Power Series - 600V		
PM75RSA060	75	Six IGBTs + Brake ckt.
PM100CSA060	100	Six IGBTs
PM100RSA060	100	Six IGBTs + Brake ckt.
PM150CSA060	150	Six IGBTs
PM150RSA060	150	Six IGBTs + Brake ckt.
PM200CSA060	200	Six IGBTs
PM200RSA060	200	Six IGBTs + Brake ckt.
PM200DSA060	200	Two IGBTs: Half Bridge
PM300DSA060	300	Two IGBTs: Half Bridge
PM400DAS060	400	Two IGBTs: Half Bridge
PM600DSA060	600	Two IGBTs: Half Bridge
PM800HSA060	800	One IGBT

Type Number	Amps	Power Circuit
Third Generation High Power Series - 1200V		
PM25RSB120	25	Six IGBTs + Brake ckt.
PM50RSA120	50	Six IGBTs + Brake ckt.
PM75CSA120	75	Six IGBTs
PM75DSA120	75	Two IGBTs: Half Bridge
PM100CSA120	100	Six IGBTs
PM100DSA120	100	Two IGBTs: Half Bridge
PM150DSA120	150	Two IGBTs: Half Bridge
PM200DSA120	200	Two IGBTs: Half Bridge
PM300DSA120	300	Two IGBTs: Half Bridge
PM400HSA120	400	Two IGBTs: Half Bridge
PM600HSA120	600	One IGBT
PM800HSA120	800	One IGBT
V-Series High Power - 600V		
PM75RVA060	75	Six IGBTs + Brake ckt.
PM100CVA060	100	Six IGBTs
PM150CVA060	150	Six IGBTs
PM200CVA060	200	Six IGBTs
PM300CVA060	300	Six IGBTs
PM400DVA060	400	Two IGBTs: Half Bridge
PM600DVA060	600	Two IGBTs: Half Bridge
V-Series High Power - 1200V		
PM50RVA120	50	Six IGBTs + Brake ckt.
PM75CVA120	75	Six IGBTs
PM100CVA120	100	Six IGBTs
PM150CVA120	150	Six IGBTs
PM200DVA120	200	Two IGBTs: Half Bridge
PM300DVA120	300	Two IGBTs: Half Bridge

possible by an advanced RTC (Real Time Control) current clamping circuit that eliminates the need for the over current protection function. In V-Series IPMs a unified short circuit protection with a delay to avoid unwanted operation replaces the over current and short circuit modes of the third generation devices.

6.1 Structure of Intelligent Power Modules

Mitsubishi Intelligent Power Modules utilize many of the same field proven module packaging technologies used in Mitsubishi IGBT modules. Cost effective implementation of the built in gate drive and protection circuits over a wide range of current ratings was achieved using two different packaging techniques. Low power devices use a multilayer epoxy isolation system while medium and high power devices use ceramic isolation. These packaging technologies are described in more detail in Sections 6.1.1 and 6.1.2. IPM are available in four power circuit configurations, single (H), dual (D), six pack (C), and seven pack (R). Table 6.1 indicates the power circuit of each IPM and Figure 6.1 shows the power circuit configurations.

6.1.1 Multilayer Epoxy Construction

Low power IPM (10-50A, 600V and 10-15A, 1200V) use a multilayer epoxy based isolation system. In this system, alternate layers of copper and epoxy are used to create a shielded printed circuit directly on the aluminum base plate. Power chips and gate control circuit components are soldered directly to the substrate eliminating the need for a separate printed circuit board and ceramic isolation materials. Modules constructed using this technique are easily identified by their extremely low profile packages. This package design is ideally suited for consumer and industrial applications where low cost and compact size are important. Figure 6.2 shows a cross section of this type of IPM package. Figure 6.3 is a PM20CSJ060 20A, 600V IPM.

Figure 6.1 Power Circuit Configuration

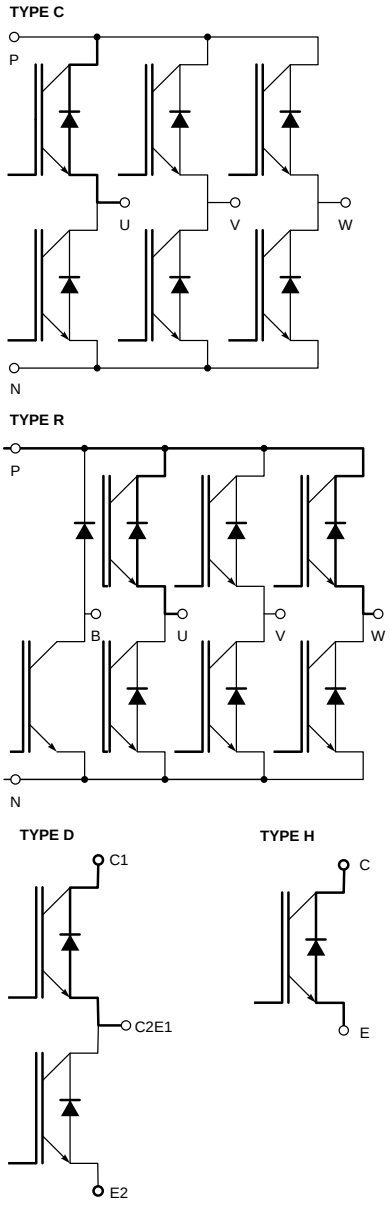
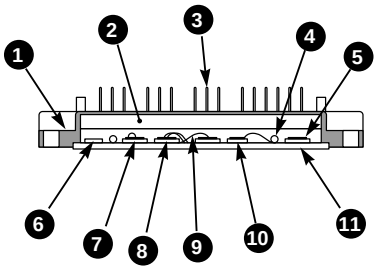
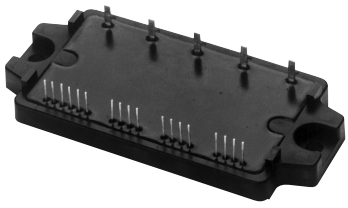


Figure 6.2 Multi-Layer Epoxy Construction



1. Case
2. Epoxy Resin
3. Input Signal Terminal
4. SMT Resistor
5. Gate Control IC
6. SMT Capacitor
7. IGBT Chip
8. Free-wheel Diode Chip
9. Bond Wire
10. Copper Block
11. Baseplate with Epoxy Based Isolation

Figure 6.3 PM20CSJ060



6.1.2 Ceramic Isolation Construction

Higher power IPMs are constructed using ceramic isolation material. A direct bond copper process in which copper patterns are bonded directly to the ceramic substrate without the use of solder is used in these modules. This substrate provides the improved thermal characteristics and greater current carrying capabilities that are needed in these higher power devices. Gate drive and control circuits are contained on a separate PCB mounted directly above the power devices. The PCB is a multilayer construction with special shield layers for EMI noise immunity. Figure 6.4 shows the structure of a ceramic isolated Intelligent Power Module. Figure 6.5 is a PM75RSA060 75 A, 600V IPM.

Figure 6.4 Ceramic Isolation Construction

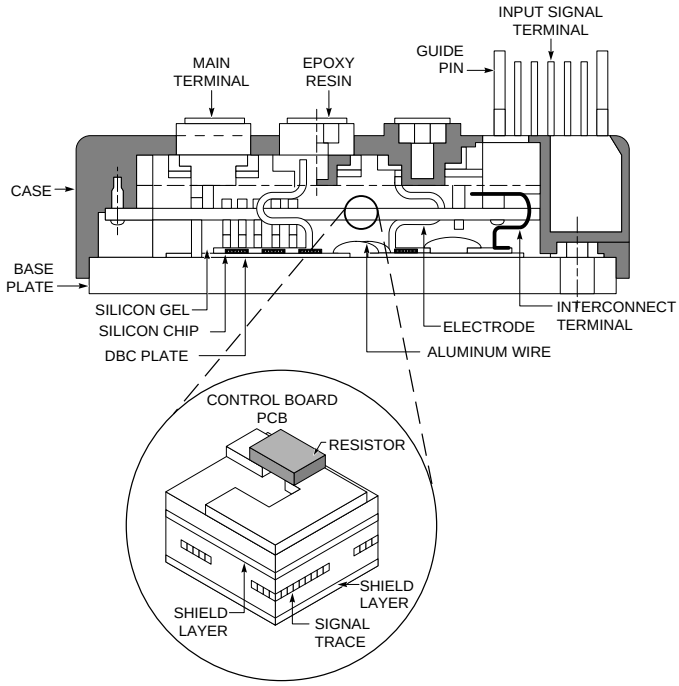
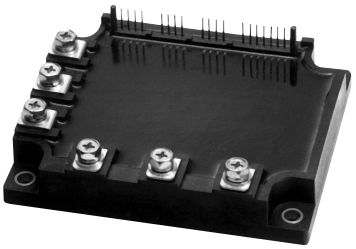


Figure 6.5 PM75RSA060



6.1.3 V-Series IPM Construction

V-Series IPMs are similar to the ceramic isolated types described in Section 6.1.2 except that an insert molded case similar to the U-Series IGBT is used. Like the U-Series IGBT described in Section 4.1.5, the V-Series IPM has lower internal inductance and improved power cycle durability. Figure 6.6 is a cross section drawing showing the construction of the V-Series IPM. The insert molded case makes the V-Series IPM is easier to manufacture and lower in cost. Figure 6.7 shows a PM150CVA120 which is a 150A 1200V V-Series IPM.

6.1.4 Advantages of Intelligent Power Module

IPM (Intelligent Power Module) products were designed and developed to provide advantages to Customers by reducing design, development, and manufacturing costs as well as providing improvement in system performance and reliability over conventional IGBTs. Design and development effort is simplified and successful drive coordination is assured by the integration of the drive and protection circuitry directly into the IPM. Reduced time to market is only one of the additional benefits of using an IPM. Others include increased system reliability through automated IPM assembly and test and reduction in the number of components that must be purchased, stored, and assembled. Often the system size can be reduced through smaller heatsink requirements as a result of lower on-state and switching losses. All IPMs use the same standardized gate control interface with logic level control circuits allowing extension of the product line without additional drive circuit design. Finally, the ability of the IPM to self protect in fault situations reduce the chance of device destruction during development testing as well as in field stress situations.

6.2 IPM Ratings and Characteristics

IPM datasheets are divided into three sections:

- Maximum Ratings
- Characteristics (electrical, thermal, mechanical)
- Recommended Operating Conditions

The limits given as maximum rating must not be exceeded under any circumstances, otherwise destruction of the IPM may result.

Key parameters needed for system design are indicated as electrical, thermal, and mechanical characteristics.

The given recommended operating conditions and application circuits should be considered as a preferable design guideline fitting most applications.

Figure 6.6 V-Series IPM Construction

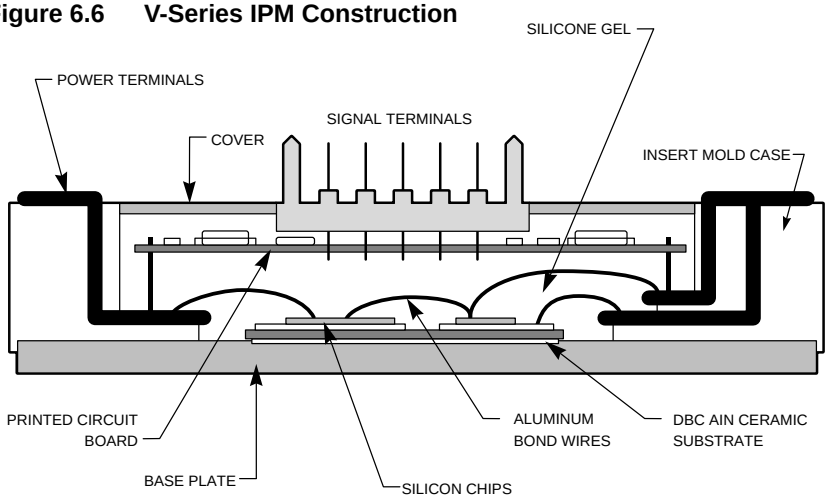
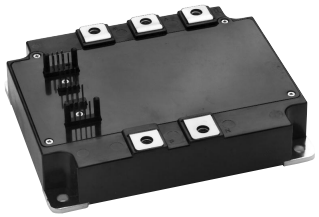


Figure 6.7 PM150CVA120



6.2.1 Maximum Ratings

Symbol	Parameter	Definition
Inverter Part		
V_{CC}	Supply Voltage	Maximum DC bus voltage applied between P-N
V_{CES}	Collector-Emitter Voltage	Maximum off-state collector-emitter voltage at applied control input off signal
$\pm I_C$	Collector-Current	Maximum DC collector and FWDi current @ $T_j \leq 150°C$
$\pm I_{CP}$	Collector-Current (peak)	Maximum peak collector and FWDi current @ $T_j \leq 150°C$
P_C	Collector Dissipation	Maximum power dissipation per IGBT switch at $T_j = 25°C$
T_j	Junction Temperature	Range of IGBT junction temperature during operation
Brake Part		
$V_{R(DC)}$	FWDi Reverse Voltage	Maximum reverse voltage of FWDi
I_F	FWDi Forward Current	Maximum FWDi DC current at $T_j \leq 150°C$
Control Part		
V_D	Supply Voltage	Maximum control supply voltage
V_{CIN}	Input Voltage	Maximum voltage between input (I) and ground (C) pins
V_{FO}	Fault Output Supply Voltage	Maximum voltage between fault output (FO) and ground (C) pins
I_{FO}	Fault Output Current	Maximum sink current of fault output (FO) pin
Total System		
$V_{CC(prot)}$	Supply Voltage Protected by OC & SC	Maximum DC bus voltage applied between P-N with guaranteed OC and SC protection
T_C	Module Case Operating Temperature	Range of allowable case temperature at specified reference point during operation
T_{stg}	Storage Temperature	Range of allowable ambient temperature without voltage or current
V_{iso}	Isolation Voltage	Maximum isolation voltage (AC 60Hz 1 min.) between baseplate and module terminals (all main and signal terminals externally shorted together)

6.2.2 Thermal Resistance

Symbol	Parameter	Definition
$R_{th(j-c)}$	Junction to Case Thermal Resistance	Maximum value of thermal resistance between junction and case per switch
$R_{th(c-f)}$	Contact Thermal Resistance	Maximum value of thermal resistance between case and fin (heatsink) per IGBT/FWDi pair with thermal grease applied according to mounting recommendations

6.2.3 Electrical Characteristics

Symbol	Parameter	Definition
Inverter and Brake Part		
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage	IGBT on-state voltage at rated collector current under specified conditions
V_{EC}	FWDi Forward Voltage	FWDi forward voltage at rated current under specified conditions
t_{on}	Turn-On Time	
t_{rr}	FWDi Recovery Time	Inductive load switching times under rated conditions
$t_{c(on)}$	Turn-On Crossover Time	(See Figure 6.10)
t_{off}	Turn-Off Time	
$t_{c(off)}$	Turn-Off Crossover Time	
I_{CES}	Collector-Emitter Cutoff	Collector-Emitter current in off-state at $V_{CE} = V_{CES}$ under specified conditions

6.2.3 Electrical Characteristics (continued)

Symbol	Parameter	Definition
Control Part		
V_D	Supply Voltage	Range of allowable control supply voltage in switching operation
I_D	Circuit Current	Control supply current in stand-by mode
$V_{CIN(on)}$	Input ON-Voltage	A voltage applied between input (I) and ground (C) pins less than this value will turn on the IPM
$V_{CIN(off)}$	Input OFF-Voltage	A voltage applied between input (I) and ground (C) pins higher than this value will turn off the IPM
f_{PWM}	PWM Input Frequency	Range of PWM frequency for VVVF inverter operations
t_{dead}	Arm Shoot Through Blocking Time	Time delay required between high and low side input off/on signals to prevent an arm shoot through
OC	Over-Current Trip Level	Collector that will activate the over-current protection
SC	Short-Circuit Trip Level	Collector current that will activate the short-circuit protection
$t_{off(OC)}$	Over-Current Delay Time	Time delay after collector current exceeds OC trip level until OC protection is activated
OT	Over-Temperature Trip Level	Baseplate temperature that will activate the over-temperature protection
OT_r	Over-Temperature Reset Level	Temperature that the baseplate must fall below to reset an over-temperature fault
UV	Control Supply Undervoltage Trip Level	Control supply voltage below this value will activate the undervoltage protection
UV_r	Control Supply Undervoltage Reset Level	Control supply voltage that must exceed to reset an undervoltage fault
$I_{FO(H)}$	Fault Output Inactive Current	Fault output sink current when no fault has occurred
$I_{FO(L)}$	Fault Output Active Current	Fault Output sink current when a fault has occurred
t_{FO}	Fault Output Pulsed Width	Duration of the generated fault output pulse
V_{SXR}	SXR Terminal Output Voltage	Regulated power supply voltage on SXR terminal for driving the external optocoupler

6.2.4 Recommended Operation Conditions

Symbol	Parameter	Definition
V_{CC}	Main Supply Voltage	Recommended DC bus voltage range
V_D	Control Supply Voltage	Recommended control supply voltage range
$V_{CIN(on)}$	Input ON-Voltage	Recommended input voltage range to turn on the IPM
$V_{CIN(off)}$	Input OFF-Voltage	Recommended input voltage range to turn off the IPM
f_{PWM}	PWM Input Frequency	Recommended range of PWM carrier frequency using the recommended application circuit
t_{DEAD}	Arm Shoot Through Blocking Time	Recommended time delay between high and low side off/on signals to the optocouplers using the recommended application circuit

6.2.5 Test Circuits and Conditions

The following test circuits are used to evaluate the IPM characteristics.

1. V_{CE}(sat) and V_{EC}

   To ensure specified junction temperature, T_j, measurements of V_{CE}(sat) and V_{EC} must be performed as low duty factor pulsed tests. (See Figures 6.8 and 6.9)

Figure 6.8 V_{CE}(sat) Test

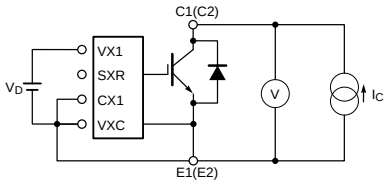
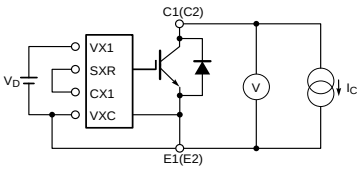


Figure 6.9 V_{EC} Test



2. Half-Bridge Test Circuit and Switching Time Definitions.

   Figure 6.10 shows the standard half-bridge test circuit and switching waveforms. Switching times and FWDi recovery characteristics are defined as shown in this figure.

3. Overcurrent and Short-Circuit Test

   I_{trip} levels and timing specifications in short circuit and overcurrent are defined as shown in Figure 6.11. By using a fixed load resistance the supply voltage, V_{CC}, is gradually increased until OC and SC trip levels are reached.

Precautions:

A. Before applying any main bus voltage, V_{CC}, the input terminals should be pulled up by resistors to their corresponding control supply (or SXR) pin, each input signal should be kept in OFF state, and the control supply should be provided. After this, the specified ON and OFF level for each input signal should be applied. The control supply should also be applied to the non-operating arm of the module under test and inputs of these arms should be kept to their OFF state.

B. When performing OC and SC tests the applied voltage, V_{CC}, must be less than $V_{CC(prot)}$ and the turn-off surge voltage spike must not be allowed to rise above the V_{CES} rating of the device. (These tests must not be attempted using a curve tracer.)

Figure 6.10 Half-Bridge Test Circuit and Switching Time Definitions

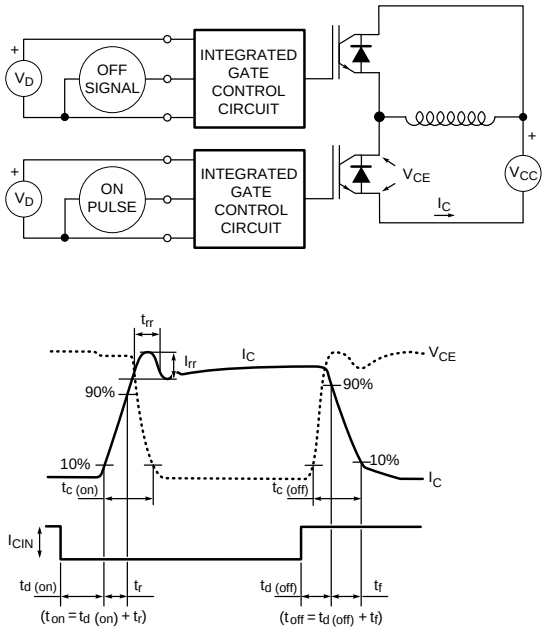
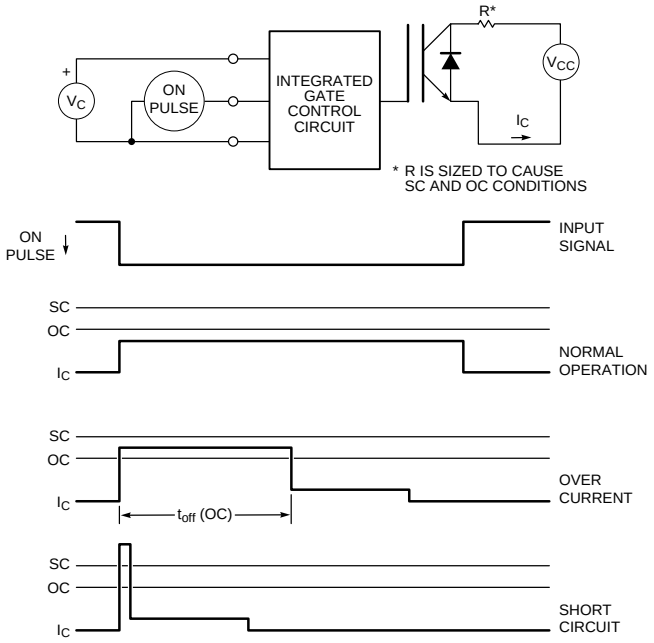


Figure 6.11 Over-Current and Short-Circuit Test Circuit



6.3 Area of Safe Operation for Intelligent Power Modules

The IPMs built-in gate drive and protection circuits protect it from many of the operating modes that would violate the Safe Operation Area (SOA) of non-intelligent IGBT modules. A conventional SOA definition that characterizes all possible combinations of voltage, current, and time that would cause power device failure is not required. In order to define the SOA for IPMs, the power device capability and control circuit operation must both be considered. The resulting easy to use short circuit and switching SOA definitions for Intelligent Power Modules are summarized
in this section.

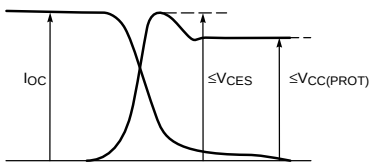
6.3.1 Switching SOA

Switching or turn-off SOA is normally defined in terms of the maximum allowable simultaneous voltage and current during repetitive turn-off switching operations. In the case of the IPM the built-in gate drive eliminates many of the dangerous combinations of voltage and current that are caused by improper gate drive. In addition, the maximum operating current is limited by the over current protection circuit. Given these constraints the switching SOA can be defined using the waveform shown in Figure 6.12. This waveform shows that the IPM will operate safely as long as the DC bus voltage is below the data sheet $V_{CC(prot)}$ specification, the turn-off transient voltage across C-E terminals of each IPM switch is maintained below the V_{CES} specification, T_j is less than 125°C, and the control power supply voltage is between 13.5V and 16.5V. In this waveform I_{OC} is the maximum current that the IPM will allow without causing an Over Current (OC) fault to occur. In other words, it is just below the OC trip level. This waveform defines the worst case for hard turn-off operations because the IPM will initiate a controlled slow shutdown for currents higher than the OC
trip level.

6.3.2 Short Circuit SOA

The waveform in Figure 6.13 depicts typical short circuit operation. The standard test condition uses a minimum impedance short circuit which causes the maximum short circuit current to flow in the device. In this test, the short circuit current (I_{SC}) is limited only by the device characteristics. The IPM is guaranteed to survive non-repetitive short circuit and over current conditions as long as the initial DC bus voltage is less than the $V_{CC(prot)}$ specification, all transient voltages across C-E terminals of each IPM switch are maintained less than the V_{CES} specification, T_j is less than 125°C, and the control supply voltage is between 13.5V and 16.5V.

Figure 6.12 Turn-Off Waveform



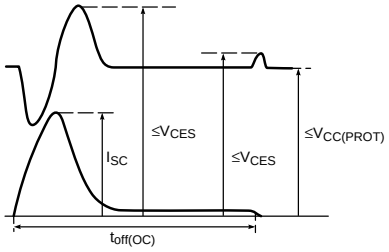
The waveform shown depicts the controlled slow shutdown that is used by the IPM in order to help minimize transient voltages.

Note:
The condition $V_{CE} \leq V_{CES}$ has to be carefully checked for each IPM switch. For easing the design another rating is given on the data sheets, $V_{CC(surge)}$, i.e., the maximum allowable switching surge voltage applied between the P and N terminals.

6.3.3 Active Region SOA

Like most IGBTs, the IGBTs used in the IPM are not suitable for linear or active region operation. Normally device capabilities in this mode of operation are described in terms of FBSOA (Forward Biased Safe Operating Area). The IPM's internal gate drive forces the IGBT to operate with a gate voltage of either zero for the off state or the control supply voltage (V_D) for the on state. The IPMs under-voltage lock out prevents any possibility of active or linear operation by automatically turning the power device off if V_D drops to a level
that could cause desaturation of the IGBT.

Figure 6.13 Short-Circuit Operation



6.4. IPM Self Protection

6.4.1 Self Protection Features

IPM (Intelligent Power Modules) have sophisticated built-in protection circuits that prevent the power devices from being damaged should the system malfunction or be over stressed. Our design and applications engineers have developed fault detection and shut down schemes that allow maximum utilization of power device capability without compromising reliability. Control supply under-voltage, over-temperature, over-current, and short-circuit protection are all provided by the IPM's internal gate control circuits. A fault output signal is provided to alert the system controller if any of the protection circuits are activated. Figure 6.14 is a block diagram showing the IPMs internally integrated functions. This diagram also shows the isolated interface circuits and control power supply that must be provided by the user. The internal gate control circuit requires only a simple +15V DC supply. Specially designed gate drive circuits eliminate the need for a negative supply to off bias the IGBT. The IPM control input is designed to interface with optocoupled transistors with a minimum of external components. The operation and timing of each protection feature is described in Sections 6.4.2 through 6.4.5.

6.4.2 Control Supply Under-Voltage Lock-Out

The Intelligent Power Module's internal control circuits operate from an isolated 15V DC supply. If, for any reason, the voltage of this supply drops below the specified under-voltage trip level (UV_t), the power devices will be turned off and a fault signal will be generated. Small glitches less than the specified t_{dUV} in length will not affect the operation of the control circuitry and will be ignored by the under-voltage protection circuit. In order for normal operation to resume, the supply voltage must exceed the under-voltage reset level (UV_r). Operation of the under-voltage protection circuit will also occur during power up and power down of the control supply. This operation is normal and the system controller's program should take the fault output delay (t_{fo}) into account. Figure 6.15 is a timing diagram showing the operation of the under-voltage lock-out protection circuit. In this diagram an active low input signal is applied to the input pin of the IPM by the system controller. The effects of control supply power up, power down and failure on the power device gate drive and fault output are shown.

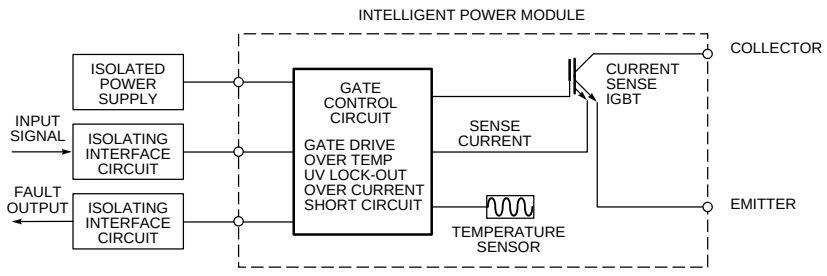
Caution:

1. Application of the main bus voltage at a rate greater than 20V/µs before the control power supply is on and stabilized may cause destruction of the power devices.
2. Voltage ripple on the control power supply with dv/dt in excess of 5V/µs may cause a false trip of the UV lock-out.

6.4.3 Over-Temperature Protection

The Intelligent Power Module has a temperature sensor mounted on the isolating base plate near the IGBT chips. If the temperature of the base plate exceeds the over-temperature trip level (OT) the IPMs internal control circuit will protect the power devices by disabling the gate drive and ignoring the control input signal until the over temperature condition has subsided. In six and seven pack modules all three low side devices will be turned off and a low side fault signal will be generated. High side switches are unaffected and can still be turned on and off by the system controller. Similarly, in dual type modules only the low side device is disabled. The fault output will remain as long as the over-temperature condition exists. When the temperature falls below the over-temperature reset level (OT_r), and the control input is high (off-state) the power device will be enabled and normal operation will resume at the next low (on) input signal. Figure 6.16 is a timing diagram showing the operation of the over-

Figure 6.14 IPM Functional Diagram



temperature protection circuit. The over temperature function provides effective protection against overloads and cooling system failures in most applications. However, it does not guarantee that the maximum junction temperature rating of the IGBT chip will never be exceeded. In cases of abnormally high losses such as failure of the system controller to properly regulate current or excessively high switching frequency it is possible for IGBT chip to exceed $T_{j(max)}$ before the base plate reaches the OT trip level.

Caution:
Tripping of the over-temperature protection is an indication of stressful operation. Repetitive tripping should be avoided.

6.4.4 Over-Current Protection

The IPM uses current sense IGBT chips to continuously monitor power device current. If the current though the Intelligent Power Module exceeds the specified overcurrent trip level (OC) for a period longer than $t_{off(OC)}$ the IPMs internal control circuit will protect the power device by disabling the gate drive and generating a fault output signal. The timing of the over-current protection is shown in Figure 6.17. The $t_{off(OC)}$ delay is implemented in order to avoid tripping of the OC protection on short pulses of current above the OC level that are not dangerous for the power device. When an over-current is detected a controlled shutdown is initiated and a fault output is generated. The controlled shutdown lowers the turn-off di/dt which helps to control transient voltages that can occur during shut down from high fault currents. Most Intelligent Modules use the two step shutdown depicted in Figure 6.17. In the two step shutdown, the gate voltage is reduced to an intermediate voltage causing the current through the device to drop slowly to a low level. Then, about 5µs later, the gate voltage is reduced to zero completing the shut down. Some of the large six and seven pack IPMs use an active ramp of gate voltage to achieve the desired reduction in turn off di/dt under high fault currents. The oscillographs in Figure 6.18 illustrate

Figure 6.15 Operation of Under-Voltage Lockout

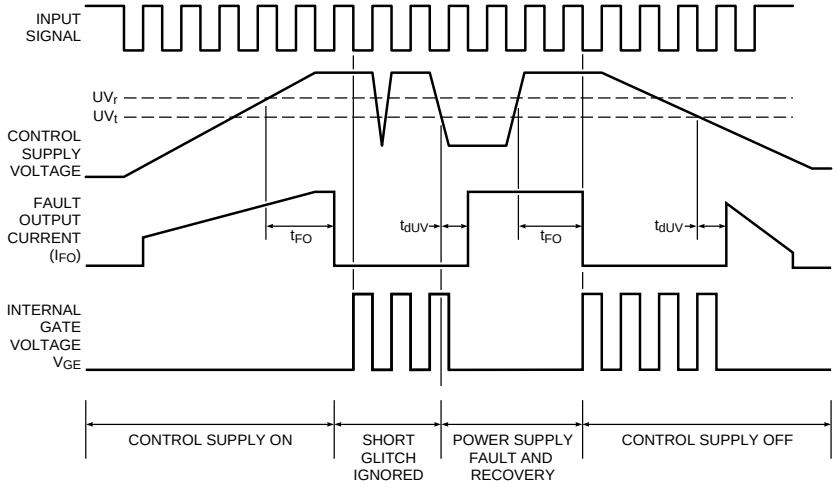
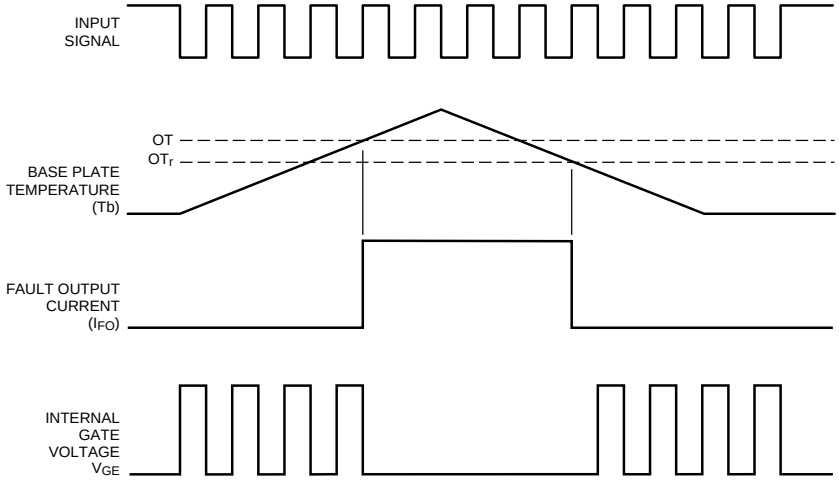


Figure 6.16 Operation of Over-Temperature



the effect of the controlled shutdown (for obtaining the oscillograph in “A”
the internal soft shutdown was intentionally deactivated). The IPM uses actual device current measurement to detect all types of over current conditions. Even resistive and inductive shorts to ground that are often missed by conventional desaturation and bus current sensing protection schemes will be detected by the IPMs current sense IGBTs.

Note:
V-Series IPMs do not have an over- current protection function. Instead a unified short circuit protection function that has a delay like the over current protection described in this section is used.

Figure 6.17 Operation of Over-Current and Short-Circuit Protection

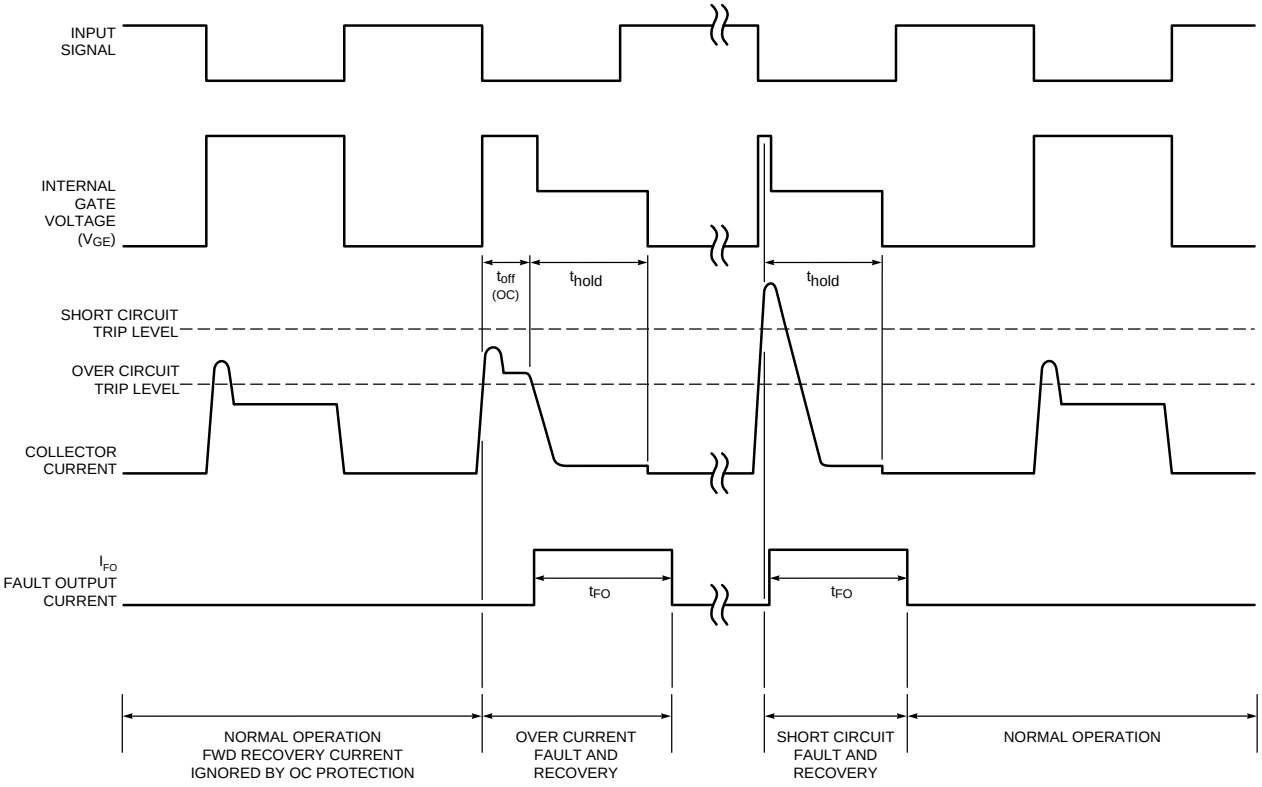
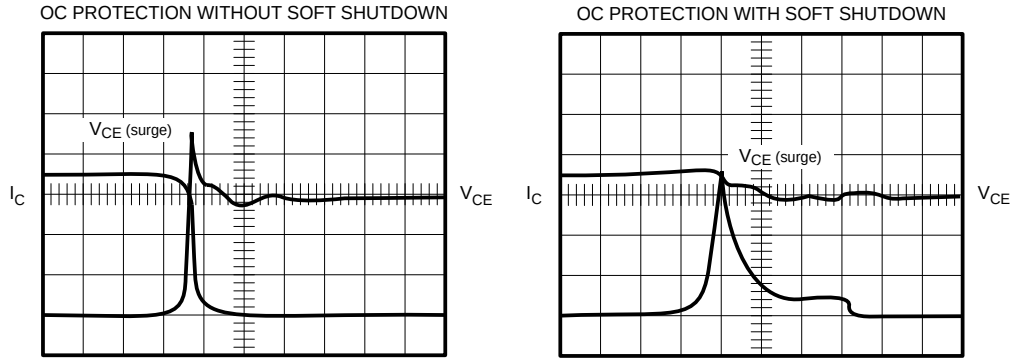


Figure 6.18 OC Operation of PM200DSA060 (I_C: 100A/div; 100V/div; t: 1μs/div)



6.4.5 Short Circuit Protection

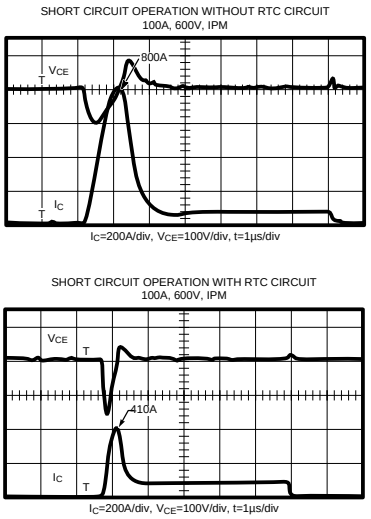
If a load short circuit occurs or the system controller malfunctions causing a shoot through, the IPMs built in short circuit protection will prevent the IGBTs from being damaged. When the current, through the IGBT exceeds the short circuit trip level (SC), an immediate controlled shutdown is initiated and a fault output is generated. The same controlled shutdown techniques used in the over current protection are used to help control transient voltages during short circuit shut down. The short circuit protection provided by the IPM uses actual current measurement to detect dangerous conditions. This type of protection is faster and more reliable than conventional out-of-saturation protection schemes. Figure 6.17 is a timing diagram showing the operation of the short circuit protection.

To reduce the response time between SC detection and SC shutdown, a real time current control circuit (RTC) has been adopted. The RTC bypasses all but the final stage of the IGBT driver in SC operation thereby reducing the response time to less than 100ns. The oscillographs in Figure 6.19 illustrate the effectiveness of the RTC technique by comparing short circuit operation of second generation IPM (without RTC) and third generation IPM (with RTC).
A significant improvement can be seen as the power stress is much lower as the time in short circuit and the magnitude of the short circuit current are substantially reduced.

Note:
The short circuit protection in V-Series IPMs has a delay similar to the third generation over current protection function described in 6.4.4. The need for a quick trip has been eliminated through the use of a new advanced RTC circuit.

Caution:
1. Tripping of the over current and short circuit protection indicates stressful operation of the IGBT. Repetitive tripping must be avoided.
2. High surge voltages can occur during emergency shutdown. Low inductance buswork and snubbers are recommended.

Figure 6.19 Waveforms Showing the Effect of the RTC Circuit



6.5 IPM Selection

There are two key areas that must be coordinated for proper selection of an IPM for a particular inverter application. These are peak current coordination to the IPM overcurrent trip level and proper thermal design to ensure that peak junction temperature is always less than the maximum junction temperature rating (150°C) and that the baseplate temperature remains below the over-temperature trip level.

6.5.1 Coordination of OC Trip

Peak current is addressed by reference to the power rating of the motor. Tables 6.2, 6.3 and 6.4 give recommended IPM types derived from the OC trip level and the peak motor current requirement based on several assumptions for the inverter and motor operation regarding efficiency, power factor, maximum overload, and current ripple. For the purposes of this table, the maximum motor current is taken from the NEC table. This already includes the motor efficiency and power factor appropriate to the particular motor size. Peak inverter current is then calculated using this RMS current, a 200% overload requirement, and a 20% ripple factor. An IPM is then selected which has a minimum overcurrent trip level that is above this calculated peak operating requirement.

Table 6.2 Motor Rating vs. OC Protection (230 VAC Line)

	Current			
Motor Rating (HP)	NEC Current Rating A(RMS)$^{\tau}$	Inverter Peak Current (A)*	Applicable IPM	Minimum OC Trip (A)
0.5	2.0	6.8	PM10CSJ060	12
0.75	2.8	9.5	PM10CSJ060	12
1	3.6	12.2	PM15CSJ060	18
1.5	5.2	17.6	PM15CSJ060	18
2	6.8	23	PM20CSJ060	28
3	9.6	32	PM30CSJ060, PM30RSF060	39
5	15.2	52	PM50RSA060, PM50RSK060	65
7.5	22	75	PM75RSA060, PM75RSK060	115
10	28	95	PM75RSA060, PM75RSK060	115
15	42	143	PM100CSA060, PM100RSA060	158
20	54	183	PM150CSA060, PM150RSA060	210
25	68	231	PM200CSA060, PM200RSA060, PM200DSA060 x3	310
30	80	271	PM200CSA060, PM200RSA060, PM200DSA060 x3	310
40	104	353	PM300DSA060 x3	390
50	130	441	PM400DSA060 x3	500
60	154	523	PM600DSA060 x3	740
75	192	652	PM600DSA060 x3	740
100	256	869	PM800HSA060 x6	1000

τ - From NEC Table 430-150
* - Inverter peak current is based on 200% overload requirement and a 20% current ripple factor.

Table 6.3 Motor Rating vs. OC Protection (460 VAC Line)

	Current			
Motor Rating (HP)	NEC Current Rating A(RMS)$^{\tau}$	Inverter Peak Current (A)*	Applicable IPM	Minimum OC Trip (A)
0.5	1.0	3.4	PM10RSH120, PM10CZF120	15
0.75	1.4	4.8	PM10RSH120, PM10CZF120	15
1	1.8	6.1	PM10RSH120, PM10CZF120	15
1.5	2.6	8.8	PM10RSH120, PM10CZF120	15
2	3.4	12	PM10RSH120, PM10CZF120	15
3	4.8	16	PM15RSH120, PM15CZF120	22
5	7.6	26	PM25RSB120, PM25RSK120	32
7.5	11	37	PM50RSA120	59
10	14	48	PM50RSA120	59
15	21	71	PM75CSA120, PM75DSA120 x3	105
20	27	92	PM75CSA120, PM75DSA120 x3	105
25	34	115	PM100CSA120, PM100DSA120 x3	145
30	40	136	PM100CSA120, PM100DSA120 x3	145
40	52	176	PM150DSA120 x3	200
50	65	221	PM200DSA120 x3	240
60	77	261	PM300DSA120 x3	380
75	96	326	PM300DSA120 x3	380
100	124	421	PM400HSA120 x6	480
125	156	529	PM600HSA120 x6	740
150	180	611	PM600HSA120 x6	740
200	240	815	PM800HSA120 x6	1060
250	300	1020	PM800HSA120 x6	1060

τ - From NEC Table 430-150
* - Inverter peak current is based on 200% overload requirement and a 20% current ripple factor.

Table 6.4 Motor Rating vs. SC Protection for V-Series IPMs

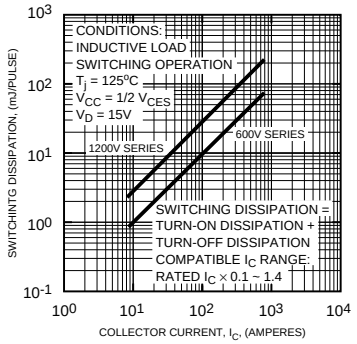
Motor Rating (HP)	Current: NEC Current Rating A(RMS)$^{\tau}$	Current: Inverter Peak Current (A)*	Applicable IPM	Minimum SC Trip (A)
240VAC Line				
10	28	95	PM75RVA060	115
15	42	143	PM100CVA060	158
20	54	183	PM150CVA060	210
30	80	271	PM200CVA060	310
40	104	353	PM300CVA060	396
50	130	441	PM400DVA060	650
75	192	652	PM600DVA060	1000
460VAC Line				
10	14	48	PM50RVA120	59
20	27	92	PM75CVA120	105
30	40	136	PM100CVA120	145
40	52	176	PM150CVA120	200
50	65	221	PM200DVA120	240
75	96	326	PM300DVA120	380

τ - From NEC Table 430-150
* - Inverter peak current is based on 200% overload requirement and a 20% current ripple factor.

6.5.2 Estimating Losses

Once the coordination of the OC trip with the application requirements has been established the next step is determining the cooling system requirements. Section 3.4 provides a general description of the methodology for loss estimation and thermal system design. Figure 6.20 shows the total switching energy ($E_{SW(on)}$+$E_{SW(off)}$) versus I_C for all third generation IPMs. Figure 6.21 shows total switching energy versus I_C for V-Series IPMs. A detailed explanation of these curves and their use can be found in Section 3.4.1. Figures 6.22 through 6.34 show simulation results calculating total power loss (switching and conduction) per arm in a sinusoidal output PWM inverter application using V-Series IPMs.

Figure 6.20 Switching Energy vs. I_C for Third Generation IPMs



APPLICABLE TYPES: THIRD-GENERATION IPM
PM200DSA060, PM300DSA060, PM400DSA060, PM600DSA060,
PM75DSA120, PM100DSA120, PM150DSA120, PM200DSA120,
PM300DSA120, PM100CSA060, PM150CSA060, PM200CSA060,
PM75CSA120, PM100CSA120, PM10CSJ060, PM15CSJ060,
PM20CSJ060, PM300CSJ060, PM30RSF060, PM50RSA060,
PM50RSK060, PM75RSA060, PM100RSA060, PM150RSA060,
PM10RSH120, PM15RSH120, PM25RSB120, PM50RSA120

Figure 6.21

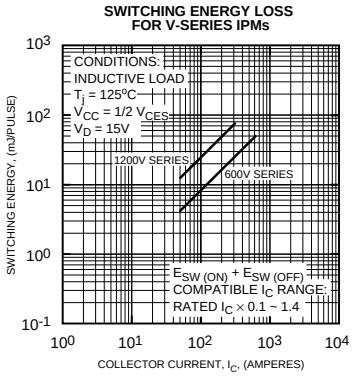


Figure 6.22 Power Loss Simulation of PM75RVA060 (Typ.)

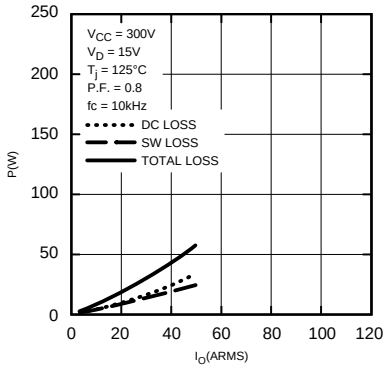


Figure 6.23 Power Loss Simulation of PM100CVA060 (Typ.)

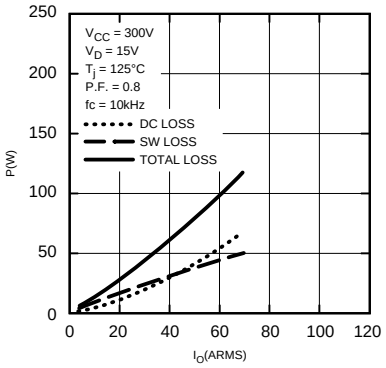


Figure 6.24 Power Loss Simulation of PM150CVA060 (Typ.)

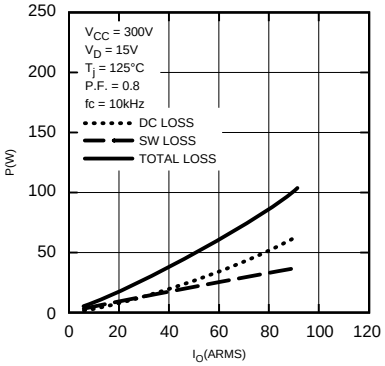


Figure 6.25 Power Loss Simulation of PM200CVA060 (Typ.)

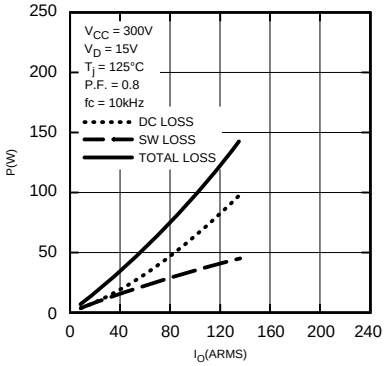


Figure 6.26 Power Loss Simulation of PM300CVA060 (Typ.)

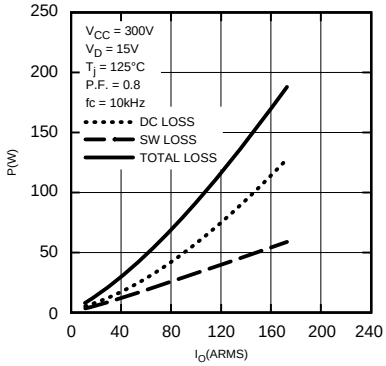


Figure 6.27 Power Loss Simulation of PM400DVA060 (Typ.)

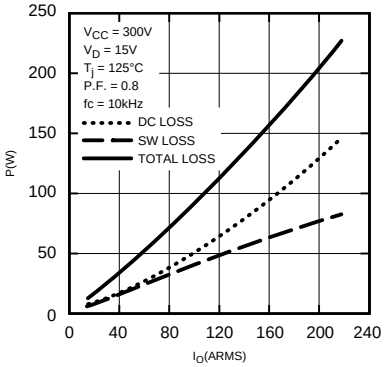


Figure 6.28 Power Loss Simulation of PM600DVA060 (Typ.)

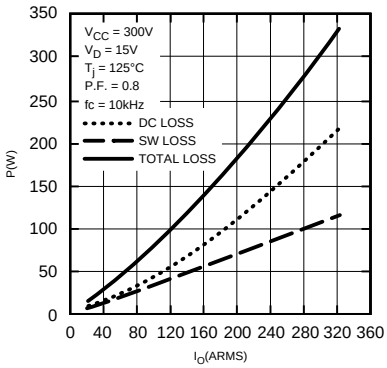


Figure 6.29 Power Loss Simulation of PM50RVA120 (Typ.)

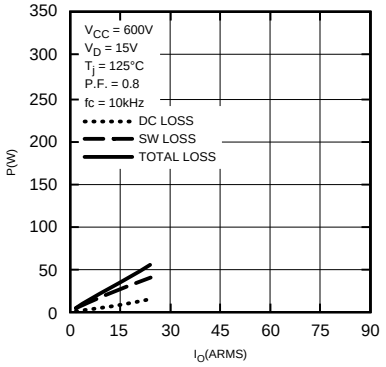


Figure 6.30 Power Loss Simulation of PM75RVA1200 (Typ.)

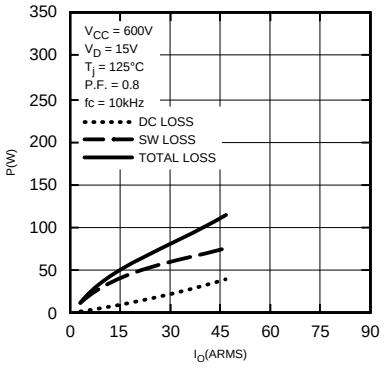


Figure 6.31 Power Loss Simulation of PM100CVA120 (Typ.)

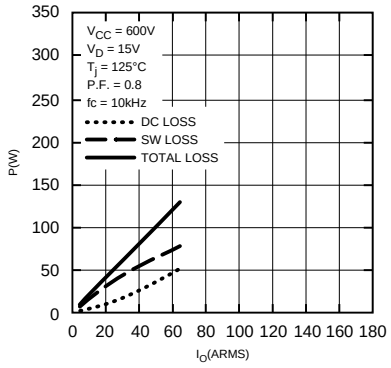


Figure 6.32 Power Loss Simulation of PM150CVA120 (Typ.)

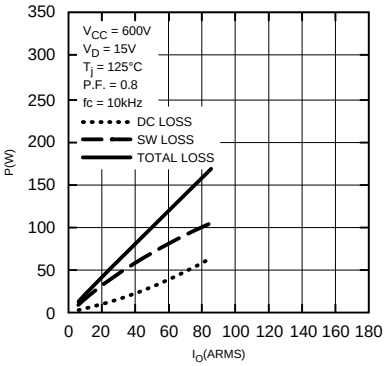


Figure 6.33 Power Loss Simulation of PM200DVA120 (Typ.)

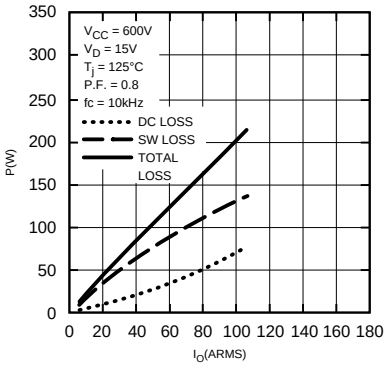
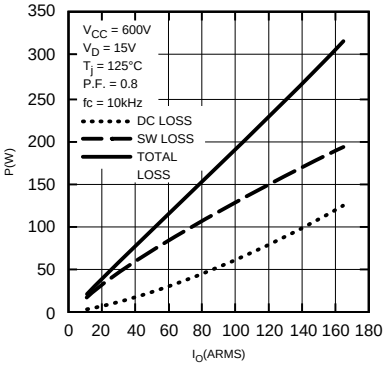


Figure 6.34 Power Loss Simulation of PM300DVA120 (Typ.)



6.6 Controlling the Intelligent Power Module

IPM (Intelligent Power Modules) are easy to operate. The integrated drive and protection circuits require only an isolated power supply and a low level on/off control signal. A fault output is provided for monitoring the operation of the modules internal protection circuits.

6.6.1 The Control Power Supply

Depending on the power circuit configuration of the module one, two, or four isolated power supplies are required by the IPMs internal drive and protection circuits. In high power 3-phase inverters using single or dual type IPMs it is good practice to use six isolated power supplies. In these high current applications each low side device must have its own isolated control power supply in order to avoid ground loop noise problems. The control supplies should be regulated to 15V +/-10% in order to avoid over-voltage damage or false tripping of the under-voltage protection. The supplies should have an isolation voltage rating of at least two times the IPM's V_{CES} rating (i.e. V_{iso} = 2400V for 1200V module). The current that must be supplied by the control power supply is the sum of the quiescent current needed to power the internal control circuits and the current required to drive the IGBT gate.

Table 6.5 summarizes the typical and maximum control power supply current requirements for

third generation Intelligent Power Modules. Table 6.6 summarizes control supply requirements for V-Series IPMs. These tables give control circuit currents for the quiescent (not switching) state and for 20kHz switching. This data is provided in order to help the user design appropriately sized control power supplies.

Power requirements for operating frequencies other than 20kHz can be determined by scaling the frequency dependent portion of the control circuit current. For example, to determine the maximum control circuit current for a PM300DSA120 operating at 7kHz the maximum quiescent control circuit current is subtracted from the maximum 20kHz control circuit current:

70mA – 30mA = 40mA

40mA is the frequency dependent portion of the control circuit current for 20kHz operation. For 7kHz operation the frequency dependent portion is:

40mA x (7kHz ÷ 20kHz) = 14mA

To get the total control power supply current required, the quiescent current must be added back:

30mA + 14mA = 44mA

44mA is the maximum control circuit current required for a PM300DSA120 operating at 7kHz.

Capacitive coupling between primary and secondary sides of isolated control supplies must be minimized as parasitic capacitances in excess of 100pF can cause noise that may trigger

Table 6.5 Control Power Requirements for Third Generation IPMs (V_D = 15V, Duty = 50%) ma

	N Side				P Side (Each Supply)			
	DC		20kHz		DC		20kHz	
Type Name	Typ.	Max	Typ.	Max.	Typ.	Max.	Typ.	Max.
600V Series								
PM10CSJ060	18	25	23	32	7	10	8	12
PM15CSJ060	18	25	23	32	7	10	8	12
PM20CSJ060	18	25	24	34	7	10	8	12
PM30CSJ060	18	25	24	34	7	10	9	13
PM100CSA060	40	55	78	100	13	18	25	34
PM150CSA060	40	55	80	110	13	18	25	38
PM200CSA060	40	55	85	120	13	18	27	40
PM30RSF060	25	30	32	45	7	10	9	13
PM50RSA060	44	60	70	100	13	18	23	32
PM50RSK060	44	60	70	100	13	18	23	32
PM75RSA060	44	60	75	100	13	18	24	35
PM100RSA060	44	60	78	105	13	18	25	36
PM150RSA060	52	72	72	113	13	18	26	38
PM200RSA060	52	72	85	115	13	18	26	40
PM200DSA060	19	26	30	42	19	26	30	42
PM300DSA060	19	26	35	48	19	26	35	48
PM400DSA060	23	30	40	60	23	30	40	60
PM600DSA060	23	30	50	70	23	30	50	70
PM800HSA060	23	30	50	70	–	–	–	–
1200V SERIES								
PM10RSH120	25	35	31	44	7	10	9	13
PM10CZF120	18	25			7	10	9	13
PM15RSH120	25	35	32	45	7	10	9	13
PM15CZF120	18	25			7	10	9	13
PM25RSB120	44	60	60	83	13	18	18	25
PM25RSK120	44	60	60	83	13	18	18	25
PM50RSA120	44	60	65	90	13	18	19	27
PM75CSA120	44	60	60	83	13	18	20	28
PM100CSA120	40	55	75	104	13	18	25	35
PM75DSA120	13	20	20	28	13	20	20	28
PM100DSA120	19	26	30	42	19	26	30	42
PM150DSA120	19	26	35	48	19	26	35	48
PM200DSA120	23	30	48	67	23	30	48	67
PM300DSA120	23	30	50	70	23	30	50	70
PM400HSA120	23	30	60	90	–	–	–	–
PM600JSA120	23	30	60	90	–	–	–	–
PM800HSA120	30	40	–	–	–	–	–	–

Table 6.6 V-Series IPM Control Power Supply Current

Type Name	N Side				P Side (Each Supply)			
	DC		20kHz		DC		20kHz	
	Typ.	Max	Typ.	Max.	Typ.	Max.	Typ.	Max.
600V Series								
PM75RVA060	44	60	72	94	13	18	21	27
PM100CVA060	40	55	68	88	13	18	22	29
PM150CVA060	40	55	72	94	13	18	23	30
PM200CVA060	40	55	84	110	13	18	28	36
PM300CVA060	52	72	130	170	17	24	43	56
PM400DVA060	23	30	56	73	23	30	56	73
PM600DVA060	23	30	56	73	23	30	56	73
1200V SERIES								
PM50RVA120	44	60	73	95	13	18	21	27
PM75CVA120	40	55	70	92	13	18	24	31
PM100CVA120	40	55	80	104	13	18	26	34
PM150CVA120	72	100	128	166	24	34	42	55
PM200DVA120	37	48	52	68	37	48	52	68
PM300DVA120	37	48	52	68	37	48	52	68

the control circuits. An electrolytic or tantalum decoupling capacitor should be connected across the control power supply at the IPMs terminals. This capacitor will help to filter common noise on the control power supply and provide the high pulse currents required by the IPMs internal gate drive circuits. Isolated control power supplies can be created using a variety of techniques. Control power can be derived from the main input line using either a switching power supply with multiple outputs or a line frequency transformer with multiple secondaries. Control power supplies can also be derived from the main logic power supply using DC-to-DC converters. Using a compact DC-to-DC converter for each isolated supply can help to simplify the interface circuit layout. A distributed DC-to-DC converter in which a single oscillator is used to drive several small isolation transformers can provide the layout advantages of separate DC-to-DC converters at a lower cost.

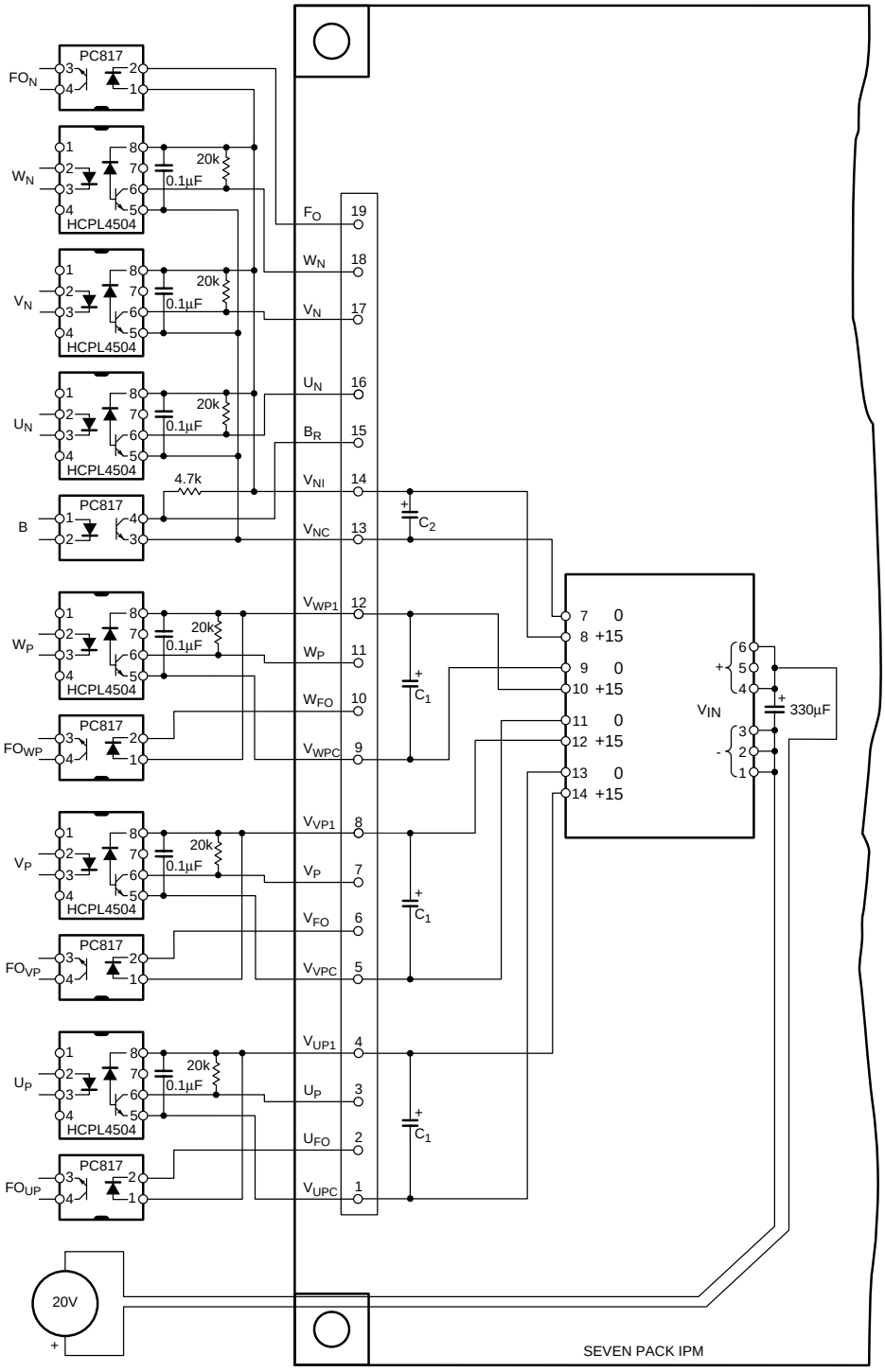
In order to simplify the design of the required isolated power supplies, Mitsubishi has developed two DC-to-DC converter modules to work with the IPMs. The M57120L is a high input voltage step down converter. When supplied with 113 to 400VDC the M57120L will produce a regulated 20VDC output. The 20VDC can then be connected to the M57140-01 to produce four isolated 15VDC outputs to power the IPMs control circuits. The M57140-01 can also be used as a stand alone unit if 20VDC is available from another source such as the main logic power supply. Figure 6.35 shows an isolated interface circuit for a seven pack IPM using M57140-01. Figure 6.36 shows a complete high input voltage isolated power supply circuit for a dual type intelligent power module.

Caution:
Using bootstrap techniques is not recommended because the voltage ripple on VD may cause a false trip of the undervoltage protection in certain inverter PWM modes.

6.6.2 Interface Circuit Requirements

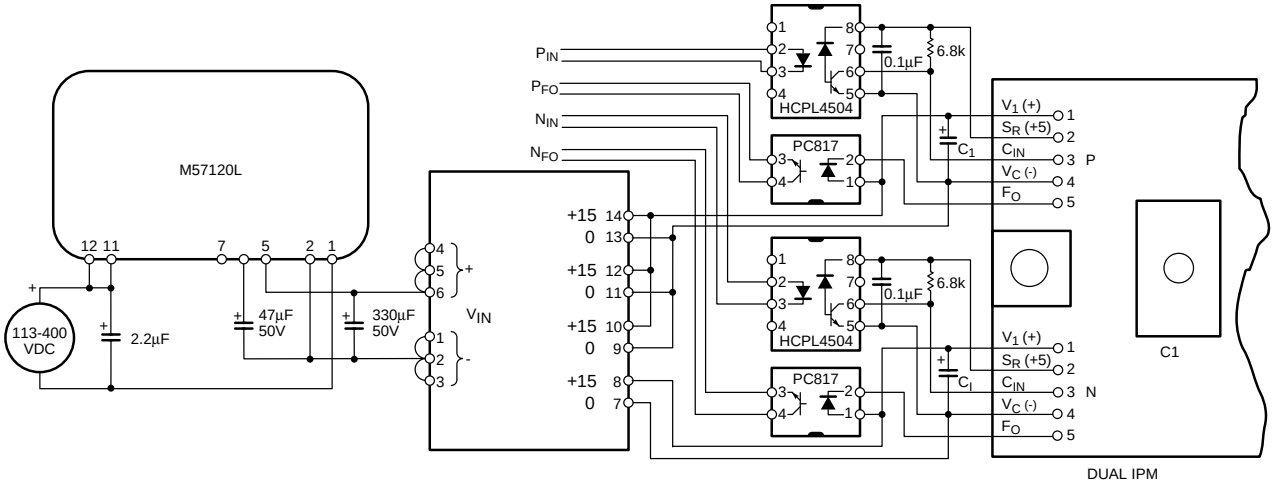
The IGBT power switches in the IPM are controlled by a low level input signal. The active low control input will keep the power devices off when it is held high. Typically the input pin of the IPM is pulled high with a resistor connected to the positive side of the control power supply. An ON signal is then generated by pulling the control input low. The fault output is an open collector with its maximum sink current internally limited. When a fault condition occurs the open collector device turns on allowing the fault output to sink current from the positive side of the control supply. Fault and on/off control signals are usually transferred to and from the system controller using isolating interface circuits. Isolating interfaces allow high and low side control signals to be referenced to a common logic level. The isolation is usually provided by optocouplers. However, fiber optics, pulse transformers, or level shifting circuits could be used. The most important consideration in interface circuit design is layout. Shielding and careful routing of printed circuit wiring is necessary in order to avoid coupling of dv/dt noise into control circuits. Parasitic capacitance between high side

Figure 6.35 Isolated Interface Circuit for Seven-Pack IPMs



NOTE: FOR C1 AND C2 SEE SECTION 6.6.3

Figure 6.36 Isolated Interface Circuit for Dual Intelligent Power Modules



interface circuits, high and low side interface circuits, or primary and secondary sides of the isolating devices can cause noise problems. Careful layout of control power supply and isolating circuit wiring is necessary. The following is a list of guidelines that should be followed when designing interface circuits. Figure 6.37 shows an example interface circuit layout for dual type IPMs. Figure 6.38 shows an example interface circuit layout for a V-Series IPMs.The shielding and printed circuit routing techniques used in this example are intended to illustrate a typical application of the layout guidelines.

INTERFACE CIRCUIT LAYOUT GUIDELINES

I. Maintain maximum interface isolation. Avoid routing printed circuit board traces from primary and secondary sides of the isolation device near to or above and below each other. Any layout that increases the primary to secondary capacitance of the isolating interface can cause noise problems.

II. Maintain maximum control power supply isolation. Avoid routing printed circuit board traces from UP, VP, WP, and N side supplies near to each other. High dv/dts exist between these supplies and noise will be coupled through parasitic capacitances. If isolated power supplies are derived from a common transformer interwinding capacitance should be minimized.

III. Keep printed circuit board traces between the interface circuit and IPM short. Long traces have a tendency to pick up noise from other parts of the circuit.

IV. Use recommended decoupling capacitors for power supplies and optocouplers. Fast switching IGBT power circuits generate dv/dt and di/dt noise. Every precaution should be taken to protect the control circuits from coupled noise.

V. Use shielding. Printed circuit board shield layers are helpful for controlling coupled dv/dt noise. Figure 6.37 shows an example of how the primary and secondary sides of the isolating interface can be shielded.

VI. High speed optocouplers with high common mode rejection (CMR) should be used for signal input:

t_{PLH},t_{PHL} < 0.8µs
CMR > 10kV/µs
@ V_{CM} = 1500V

Appropriate optocoupler types are HCPL 4503, HCPL 4504 (Hewlett Packard) and PS2041 (NEC). Usually high speed optos require a 0.1µF decoupling capacitor close to the opto.

VII. Select the control input pull-up resistor with a low enough value to avoid noise pick-up by the high impedance IPM input and with a high enough value that the high speed optotransistor can still pull the IPM safely below the recommended maximum $V_{CIN(on)}$.

Figure 6.37 Interface Circuit Layout Example for Dual IPMs

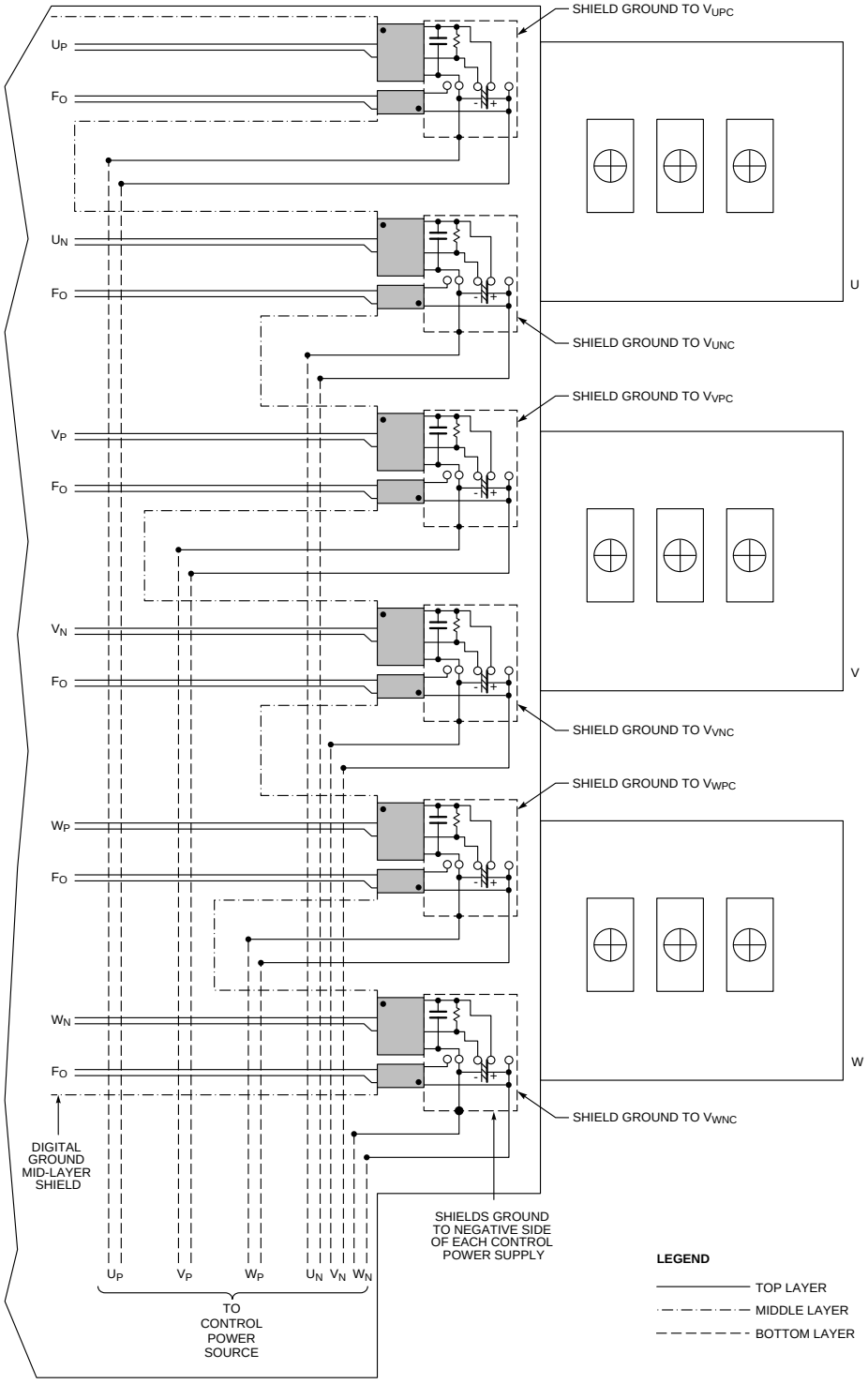
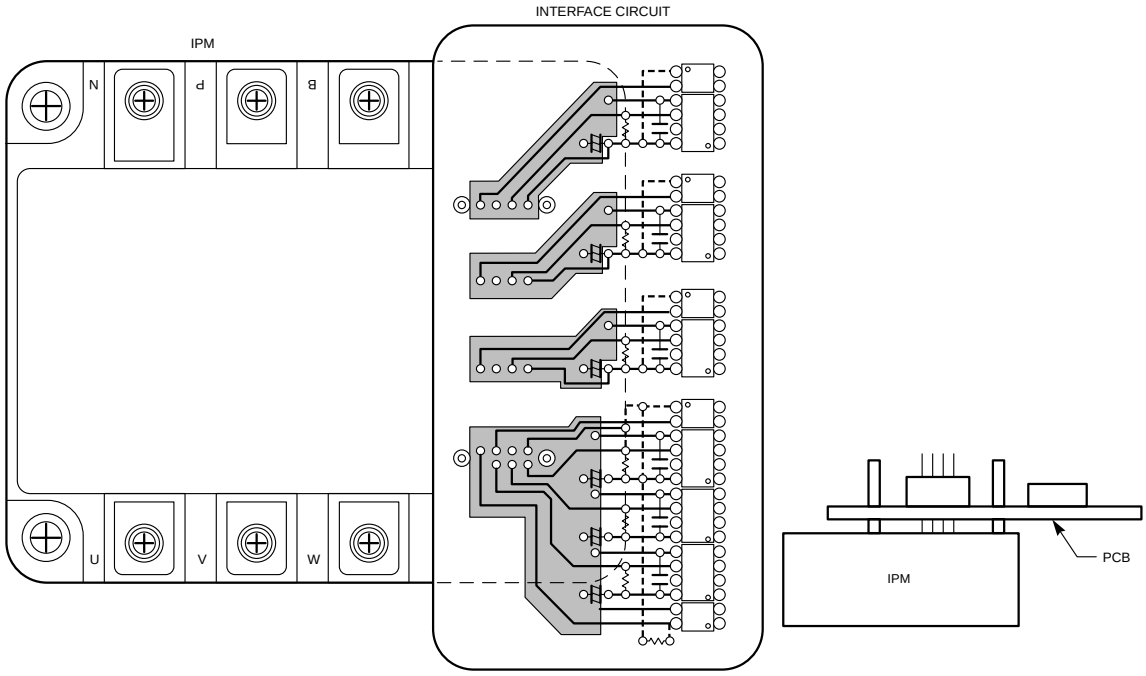


Figure 6.38 Interface Circuit Layout for a V-Series IPMs



VIII. If some IPM switches are not used in actual application their control power supply must still be applied. The related signal input terminals should be pulled up by resistors to the control power supply (V_D or V_{SXR}) to keep the unused switches safely in off-state.

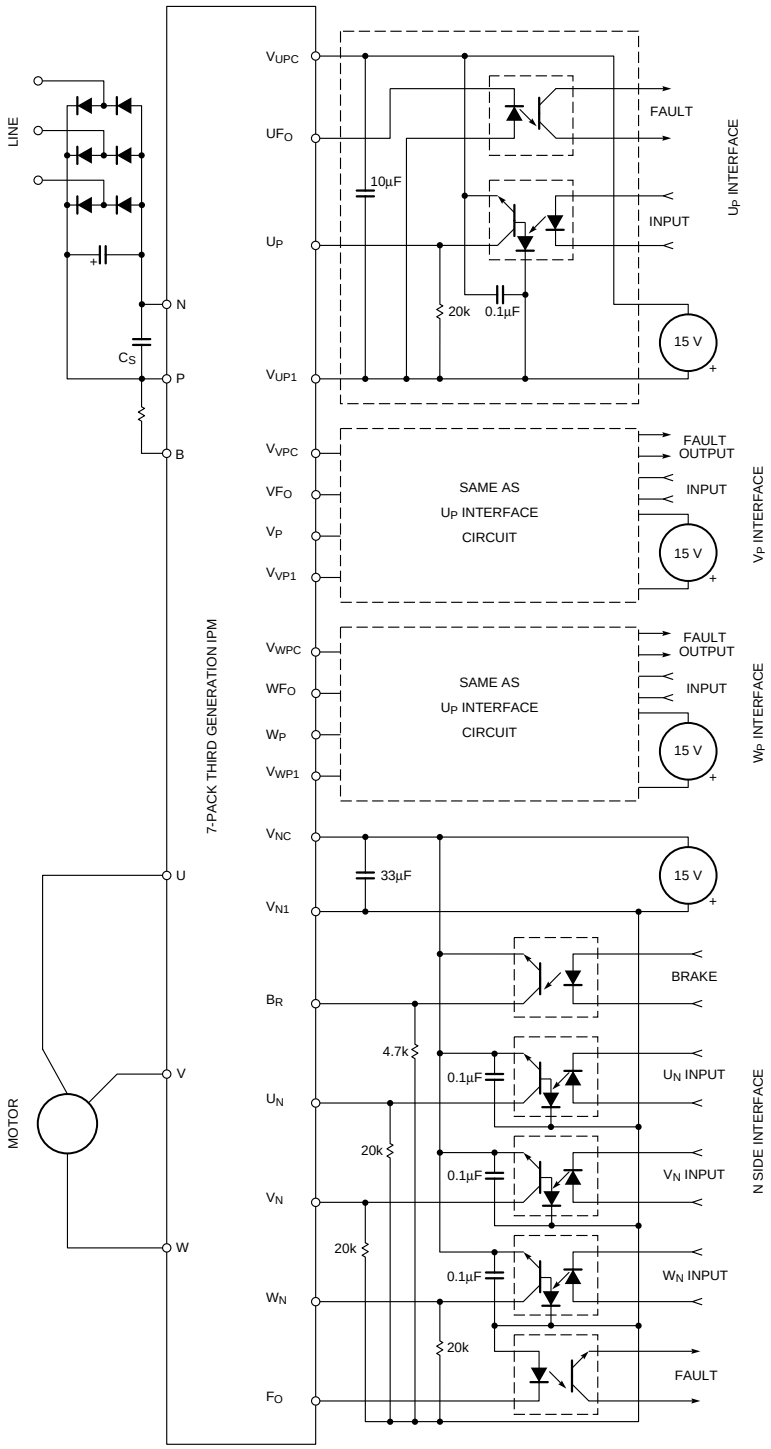
IX. Unused fault outputs must be tied high in order to avoid noise pick up and unwanted activation of internal protection circuits. Unused fault outputs should be connected directly to the +15V of local isolated control power supply.

6.6.3 Example Interface Circuits

IPM (Intelligent Power Modules) are designed to use optocoupled transistors for control input and fault output interfaces. In most applications optocouplers will provide a simple and inexpensive isolated interface to the system controller. Figures 6.39 through 6.43 show example interface circuits for the four IPM power circuit configurations. These circuits use two types of optocoupled transistors. The control input on/off signals are transferred from the system controller using high speed optocoupled transistors. Usually high speed optos require a 0.1µF film or ceramic decoupling capacitor connected near their V_{CC} and GND pins. The value of the control input pull up resistor is selected low enough to avoid noise pick up by the high impedance input and high enough so that the high speed optotransistor with its relatively low current transfer ratio can still pull the input low enough to assure turn on. The circuits shown use a Hewlett Packard HCPL-4504 optotransistor. This opto was chosen mainly for its high common mode transient immunity of 15,000V/µs. For reliable operation in IGBT power circuits optocouplers should have a minimum common mode noise immunity of 10,000 V/µs. Low speed optocoupled transistors can be used for the fault output and brake input. Slow optos have the added advantages of lower cost and higher current transfer ratios. The example interface circuits use a Sharp PC817 low speed optocoupled transistor for the transfer of brake and fault signals. Like most low speed optos the PC817 does not have internal shielding. Some switching noise will be coupled through the opto. An RC filter with a time constant of about 10ms can be added to the opto's output to remove this noise. The IPMs 1.5ms long fault output signal will be almost unaffected by the addition of this filter. When designing interface circuits always follow the interface circuit layout guidelines given in Section 6.6.2.

USING INTELLIGENT POWER MODULES

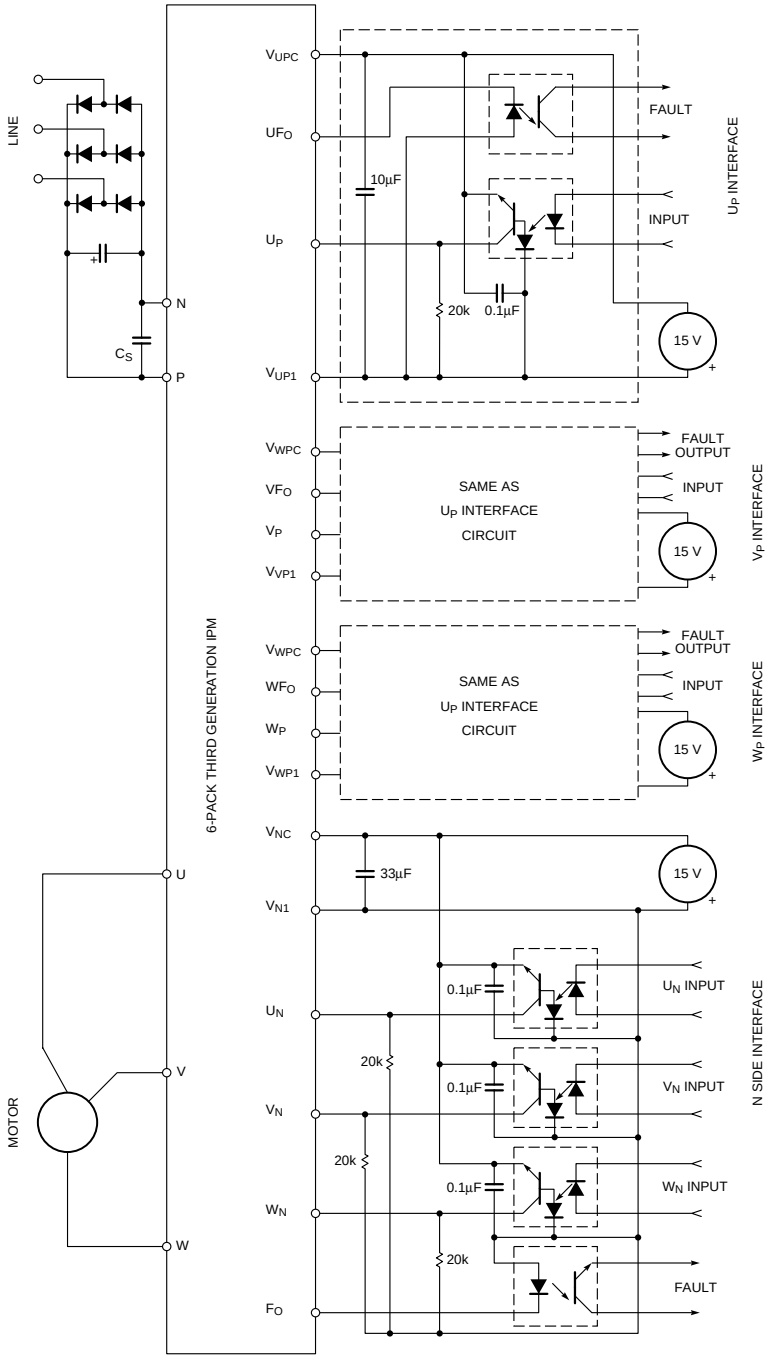
Figure 6.39 Interface Circuit for Seven-Pack IPMs



Applicable Types	Rated Current (Amps)	Decoupling Capacitor (C_S)
600V Modules		
PM30RSF060	30	0.3µF
PM50RSK060	55	0.47µF
PM50RSA060	50	0.47µF
PM75RSA060, PM75RSK060, PM75RVA060	75	1.0µF
PM100RSA060	100	1.0µF
PM150RSA060	150	1.5µF
PM200RSA060	200	2.0µF
1200V Modules		
PM10RSH120	10	0.1µF
PM15RSH120	15	0.1µF
PM25RSB120, PM25RSK120	25	0.22µF
PM50RSA120, PM50RVA120	50	0.47µF

NOTE: If high side fault outputs are not used, they must be connected to the +15V of the local power supply.

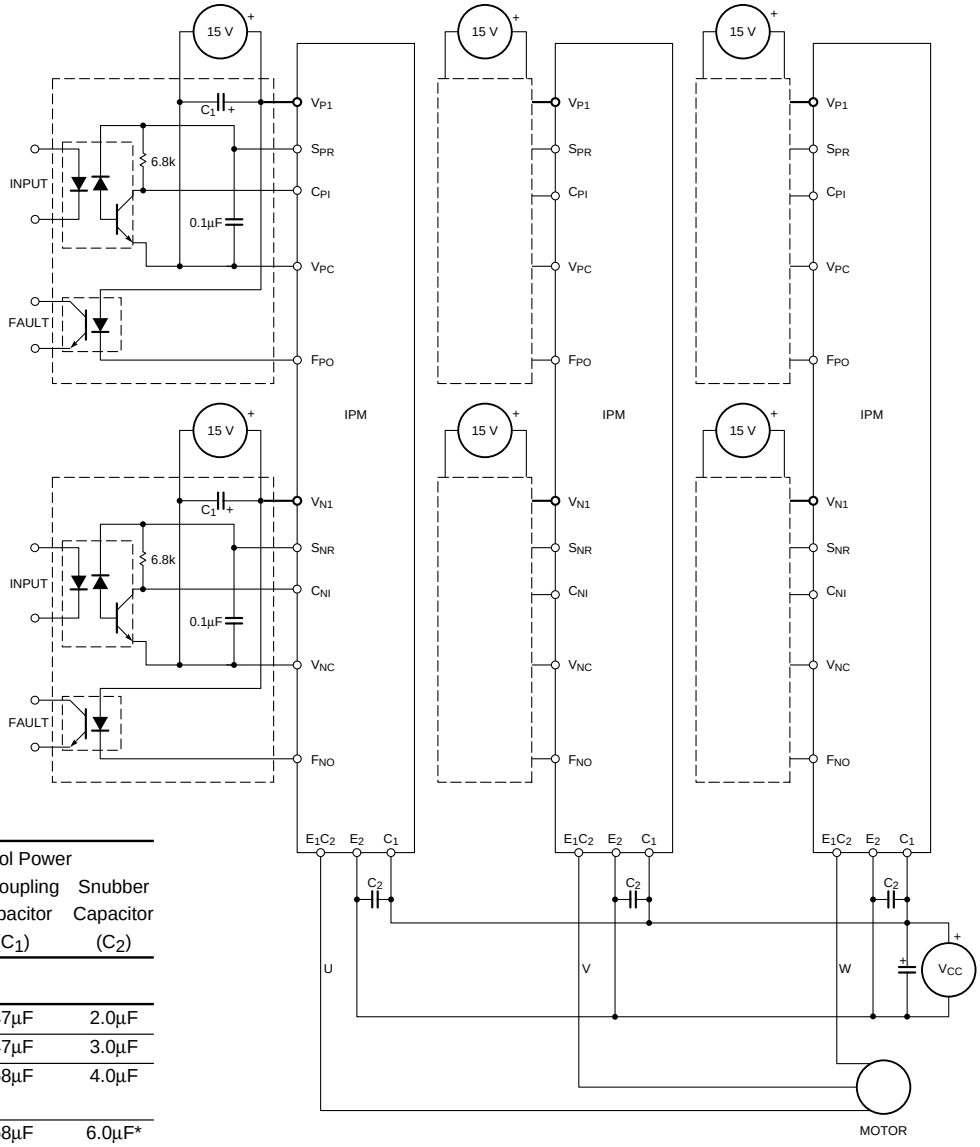
Figure 6.40 Interface Circuit for Six-Pack IPMs



Applicable Types	Rated Current (Amps)	Decoupling Capacitor (C_S)
600V Modules		
PM10CSJ060	10	0.1μF
PM15CSJ060	15	0.1μF
PM20CSJ060	20	0.1μF
PM30CSJ060	30	0.3μF
PM100CSA060, PM100CVA060	100	1.0μF
PM150CSA060, PM150CVA060	150	1.5μF
PM200CSA060, PM200CVA060	200	2.2μF
PM300CVA060	300	3.0μF
1200V Modules		
PM75CSA120, PM75CVA120	75	1.0μF
PM100CSA120, PM100CVA120	100	1.0μF
PM150CVA120	150	1.5μF

NOTE: Unused fault outputs must be connected to the +15V of the local control supply.

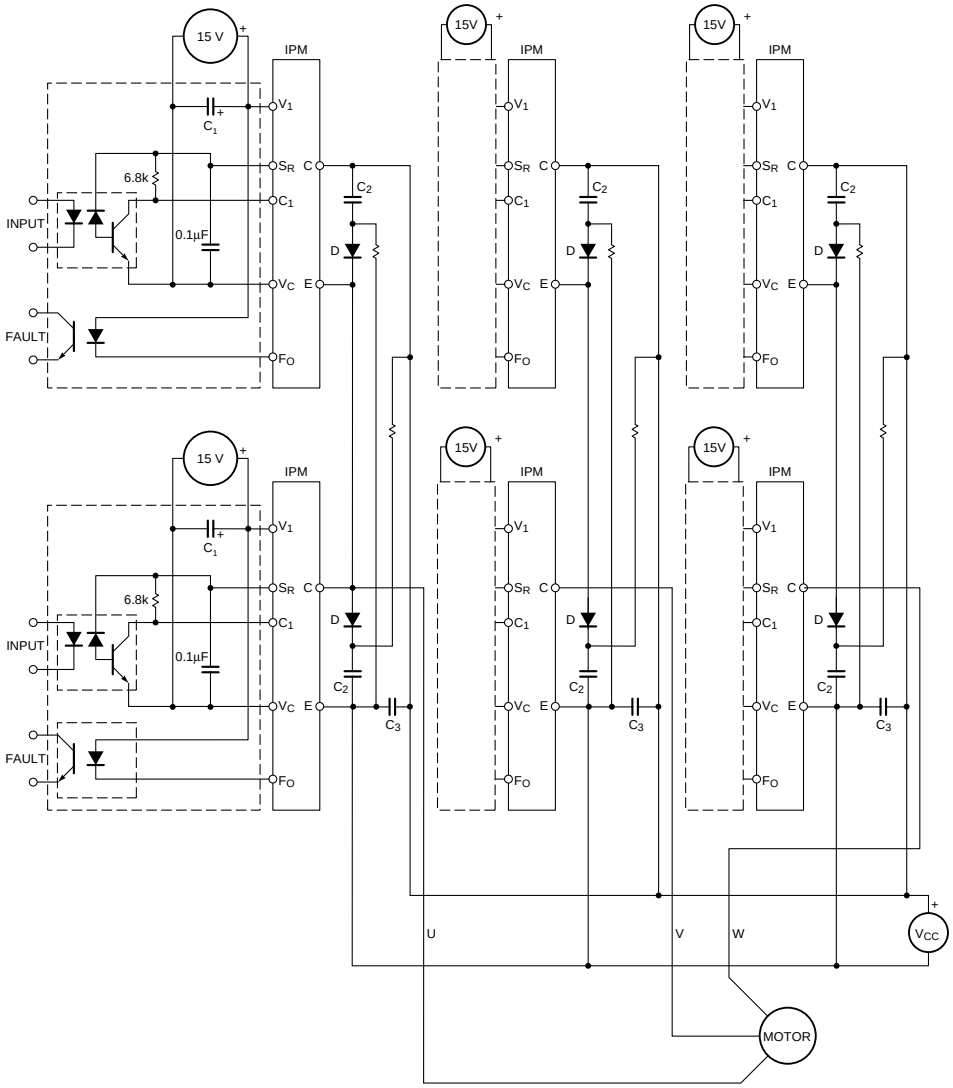
Figure 6.41 Interface Circuit for Dual IPMs



Applicable Types	Rated Current (Amps)	Control Power Decoupling Capacitor (C_1)	Control Power Snubber Capacitor (C_2)
600V Modules			
PM200DSA060	200	47μF	2.0μF
PM300DSA060	300	47μF	3.0μF
PM400DSA060, PM400DVA060	400	68μF	4.0μF
PM600DSA060, PM600DVA060	600	68μF	6.0μF*
1200V Modules			
PM75DSA120	75	22μF	0.68μF
PM100DSA120	100	47μF	1.5μF
PM150DSA120	150	47μF	2.0μF
PM200DSA120, PM200DVA120	200	68μF	3.0μF
PM300DSA120, PM300DVA120	300	68μF	5.0μF

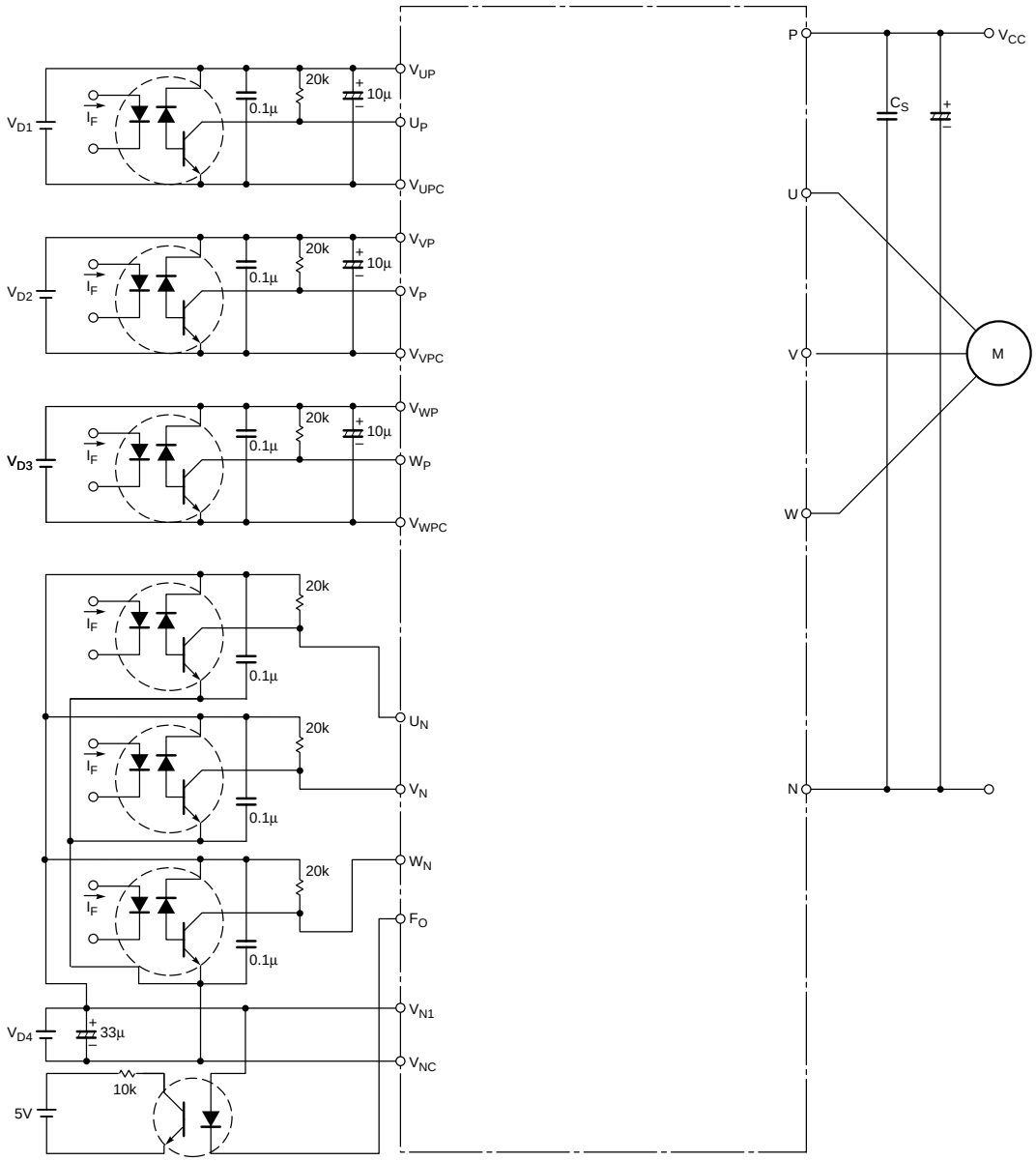
*Depending on maximum DC link voltage and main circuit layout, an RCDi clamp may be needed. (see Section 3.3)

Figure 6.42 Interface Circuit for Single IPMs



Applicable Types	Rated Current (Amps)	Control Power Decoupling Capacitor (C_1)	Snubber Capacitor (C_2)	Main Bus Decoupling Capacitor (C_3)	Snubber Diode
600V Modules					
PM800HSA060	800	68μF	3.0μF	6.0μF	RM50HG-12S (2 pc. parallel)
1200V Modules					
PM400HSA120	400	68μF	1.5μF	4.0μF	RM25HG-24S
PM600HSA120	600	68μF	2.0μF	6.0μF	RM25HG -24S (2 pc. parallel)
PM800HSA120	800	68μF	3.0μF	6.0μF	RM25HG-24S (3 pc. parallel)

Figure 6.43 Interface Circuit for PM10CZF120 and PM15CZF120

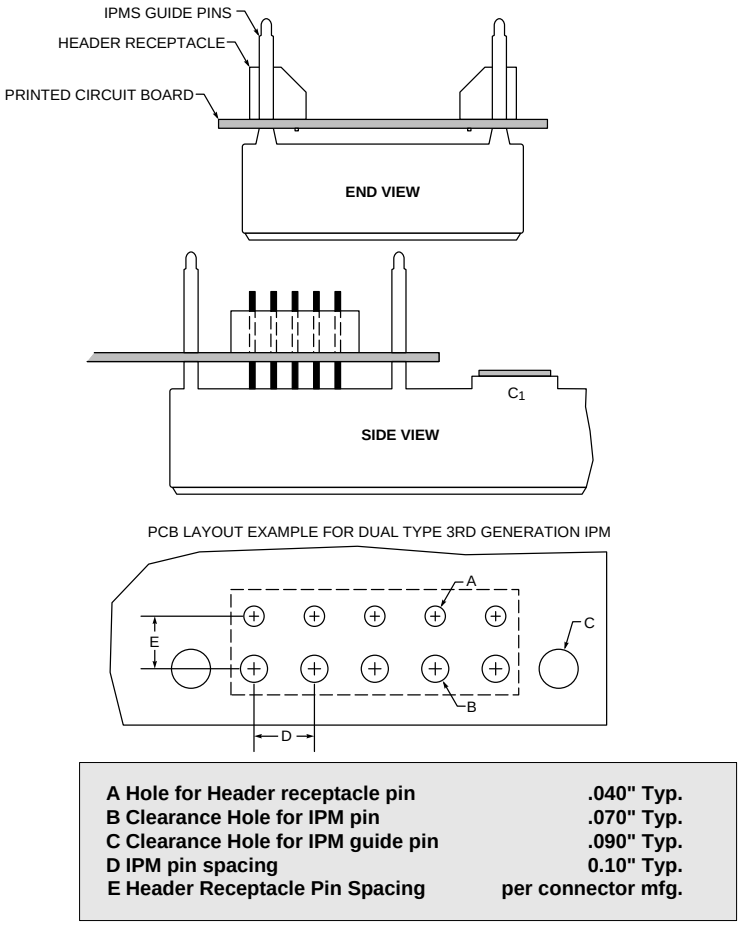


6.6.4 Connecting the Interface Circuit

The input pins of Mitsubishi Intelligent Power Modules are designed to be connected directly to a printed circuit board. Noise pick up can be minimized by building the interface circuit on the PCB near the input pins of the module. Low power modules have tin plated control and power pins that are designed to be soldered directly to the PCB. Higher power modules have gold plated pins that are designed to be connected to the PCB using an inverse mounted header receptacle. An example of this connection for a dual type IPM is shown in Figure 6.44. This connection technique can also be adapted to large six and seven pack modules. Table 6.7 shows the suggested connection method and connector for each Third Generation IPM.

Table 6.8 shows the suggested connection method and connector for V-Series IPMs. Figure 6.45 shows the PCB layout for V-Series six and seven pack connector.

Figure 6.44 Connection of the Interface Circuit



A Hole for Header receptacle pin	**.040" Typ.**
B Clearance Hole for IPM pin	**.070" Typ.**
C Clearance Hole for IPM guide pin	**.090" Typ.**
D IPM pin spacing	**0.10" Typ.**
E Header Receptacle Pin Spacing	**per connector mfg.**

Table 6.7 Third Generation IPM Connection Methods

Third Generation Intelligent Power Module Type	Connection Method
PM10CSJ060, PM15CSJ060, PM20CSJ060, PM30CSJ060, PM30RSF060, PM50RSK060, PM10RSH120, PM15RSH120	Solder to PCB
PM50RSA060, PM75RSA060, PM100CSA060, PM100RSA060, PM150CSA060, PM150RSA060, PM200CSA060, PM25RSB120, PM50RSA120, PM75CSA120, PM100CSA120	31 Position 2mm Inverse Header Receptacle Hirose P/N: DF10-31S-2DSA (59)
PM200DSA060, PM300DSA060, PM400DSA060, PM600DSA060, PM75DSA120, PM100DSA120, PM150DSA120, PM200DSA120, PM300DSA120, PM400HSA120, PM600HSA120	5 Position 2.54mm (0.1") Inverse Header Receptacle Method P/N: 1000-205-2105 Hirose P/N: MDF7-5S-2.54DSA

6.6.5 Dead Time (t_{dead})

In order to prevent arm shoot through a dead time between high and low side input ON signals is required to be included in the system control logic. Two different values are specified on the datasheet:

A. t_{dead} measured directly on the IPM input terminals

B. t_{dead} related to optocoupler input signals using the recommended application circuit

The specified type B dead time is related to standard high speed optocouplers. (See Section 6.6.2) By using specially selected optocouplers with narrow distribution of switching times the required type B dead time could be reduced.

6.6.6 Using the Fault Signal

In order to keep the interface circuits simple the IPM uses a single on/off output to alert the system controller of all fault conditions. The system controller can easily determine whether the fault signal was caused by an over temperature or over current/short circuit by examining its duration. Short circuit and over current condition fault signals will be t_{FO} (nominal 1.5ms) in duration. An over temperature fault signal will be much longer. The over temperature fault starts when the base plate temperature exceeds the OT level and does not reset until the base plate cools below the OT_r level. Typically this takes tens of seconds.

Note:
Unused fault outputs must be properly terminated by connecting them to the +15V on the local control power supply. Failure to properly terminate unused fault outputs may result in unexpected tripping of the modules internal protection.

Figure 6.45 PCB Layout for V-Series Connector

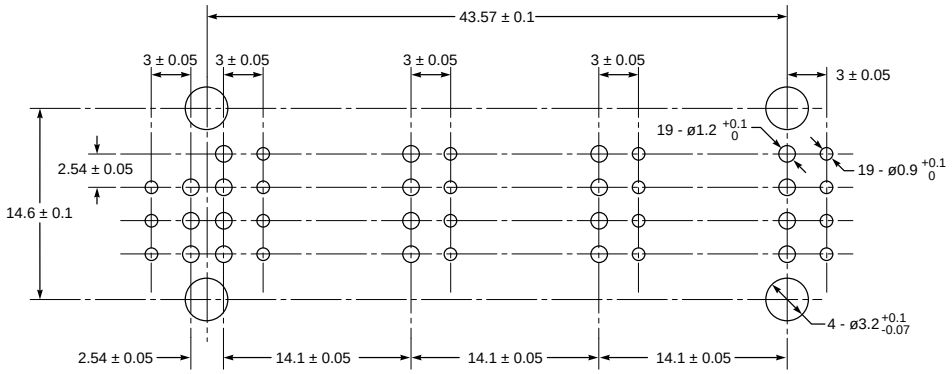


Table 6.8 V-Series IPM Connection Methods

V-Series Intelligent Power Module Type	Connection Method
PM75RVA060, PM100CVA060, PM150CVA060, PM200CVA060, PM300CVA060, PM50RVA120, PM75CVA120, PM100CVA120, PM150CVA120	19 Position, 0.1" Compound Inverse Header Receptacle, Hirose Part # MDF92-19S-2.54DSA
PM400DVA060, PM600DVA060, PM200DVA120, PM300DVA120	5 Position, 0.1" (2.54mm) Inverse Header Receptacle, Hirose Part # MDF7-5S-2.54DSA

6.7 IPM Inverter Example

The IPMs integrated intelligence greatly simplifies inverter design. The built in protection circuits allow maximum utilization of power device capability without compromising reliability. Figure 6.46 shows a complete inverter constructed using dual type IPMs. Input common mode noise filtering and MOV surge suppression helps to protect the input rectifier and IPMs from line transients. The main power bus is constructed using laminated plates in order to minimize parasitic inductance. Low inductance bus designs are covered in more detail in Sections 3.2 and 3.3. An example of the mechanical layout of the inverter is shown in Figure 6.47. The IPMs must be mounted on a heatsink with suitable cooling capabilities. Thermal design and power loss estimation is covered in Section 3.4. Mitsubishi offers a complete line-up of diode modules that are ideal for use as the input bridge in inverter applications.

Figure 6.46 IPM Inverter System

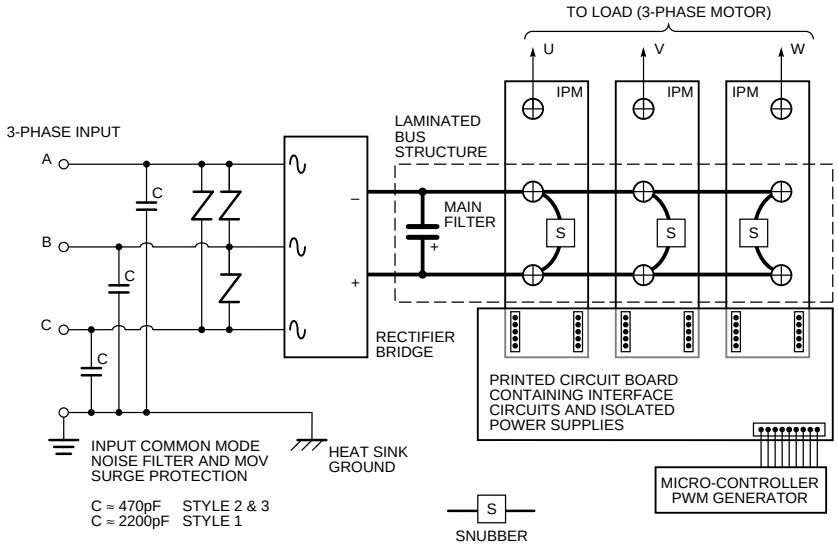
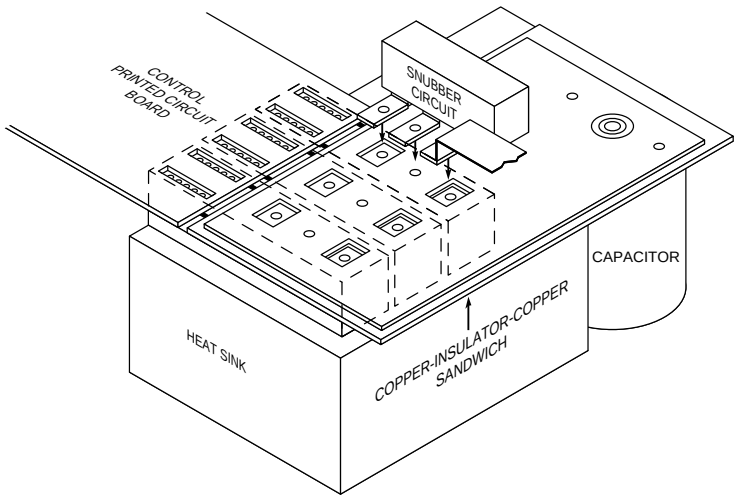


Figure 6.47 Power Circuit Layout for IPMs



6.8 Handling Precautions for Intelligent Power Modules

Electrical Considerations:

I. Apply proper control voltages and input signals before static testing.

II. Carefully check wiring of control voltage sources and input signals. Miswiring may destroy the integrated gate control circuit.

III. When measuring leakage current always ramp the curve tracer voltage up from zero. Ramp voltage back down before disconnecting the device. Never apply a voltage greater than the V_{CES} rating of the device.

IV. When measuring saturation voltage low inductance test fixtures must be used. Inductive surge voltages can exceed device ratings.

Mechanical Considerations:

I. Avoid mechanical shock. The module uses ceramic isolation that can be cracked if the module is dropped.

II. Do not bend the power terminals. Lifting or twisting the power terminals may cause stress cracks in the copper.

III. Do not over torque terminal or mounting screws. Maximum torque specifications are provided in device data sheets.

IV. Avoid uneven mounting stress. A heatsink with a flatness of 0.001"/1" or better is recommended. Avoid one sided tightening stress. Figure 6.48 shows the recommended torquing order for mounting screws. Uneven mounting can cause the modules ceramic isolation to crack.

Thermal Considerations:

I. Do not put the module on a hot plate. Externally heating the module's base plate at a rate greater than 15°C/min. will cause thermal stress that may damage the module.

II. When soldering to the signal pins and fast on terminals avoid excessive heat. The soldering time and temperature should not exceed 230°C for 5 seconds.

III. Maximize base plate to heatsink contact area for good heat transfer. Use a thermal interface compound such as white silicon grease. The heatsink should have a surface finish of 64 microinches or less.

Figure 6.48 Mounting Screws Torque Order