M59MR032C
M59MR032D

32 Mbit (2Mb x16, Mux I/O, Dual Bank, Burst)
1.8V Supply Flash Memory

- SUPPLY VOLTAGE
  - V_{DD} = V_{DDQ} = 1.65V to 2.0V for Program, Erase and Read
  - V_{PP} = 12V for fast Program (optional)
- MULTIPLEXED ADDRESS/DATA
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Configurable Burst mode Read
  - Page mode Read (4 Words Page)
  - Random Access: 100ns
- PROGRAMMING TIME
  - 10µs by Word typical
  - Double Word Programming Option
- MEMORY BLOCKS
  - Dual Bank Memory Array: 8 Mbit - 24 Mbit
  - Parameter Blocks (Top or Bottom location)
- DUAL BANK OPERATIONS
  - Read within one Bank while Program or Erase within the other
  - No delay between Read and Write operations
- BLOCK PROTECTION/UNPROTECTION
  - All Blocks protected at Power-up
  - Any combination of Blocks can be protected
- COMMON FLASH INTERFACE (CFI)
- 64 bit SECURITY CODE
- ERASE SUSPEND and RESUME MODES
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M59MR032C: A4h
  - Bottom Device Code, M59MR032D: A5h

LFBGA54 (ZC)
10 x 4 ball array

µBGA46 (GC)
10 x 4 ball array

Figure 1. Logic Diagram

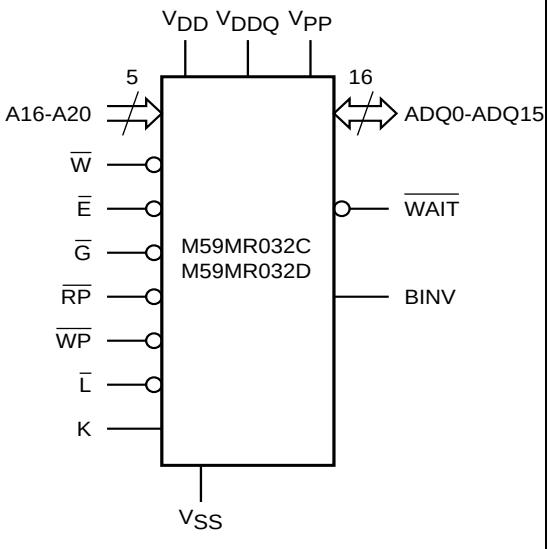


Figure 2. LFBGA Connections (Top view through package)

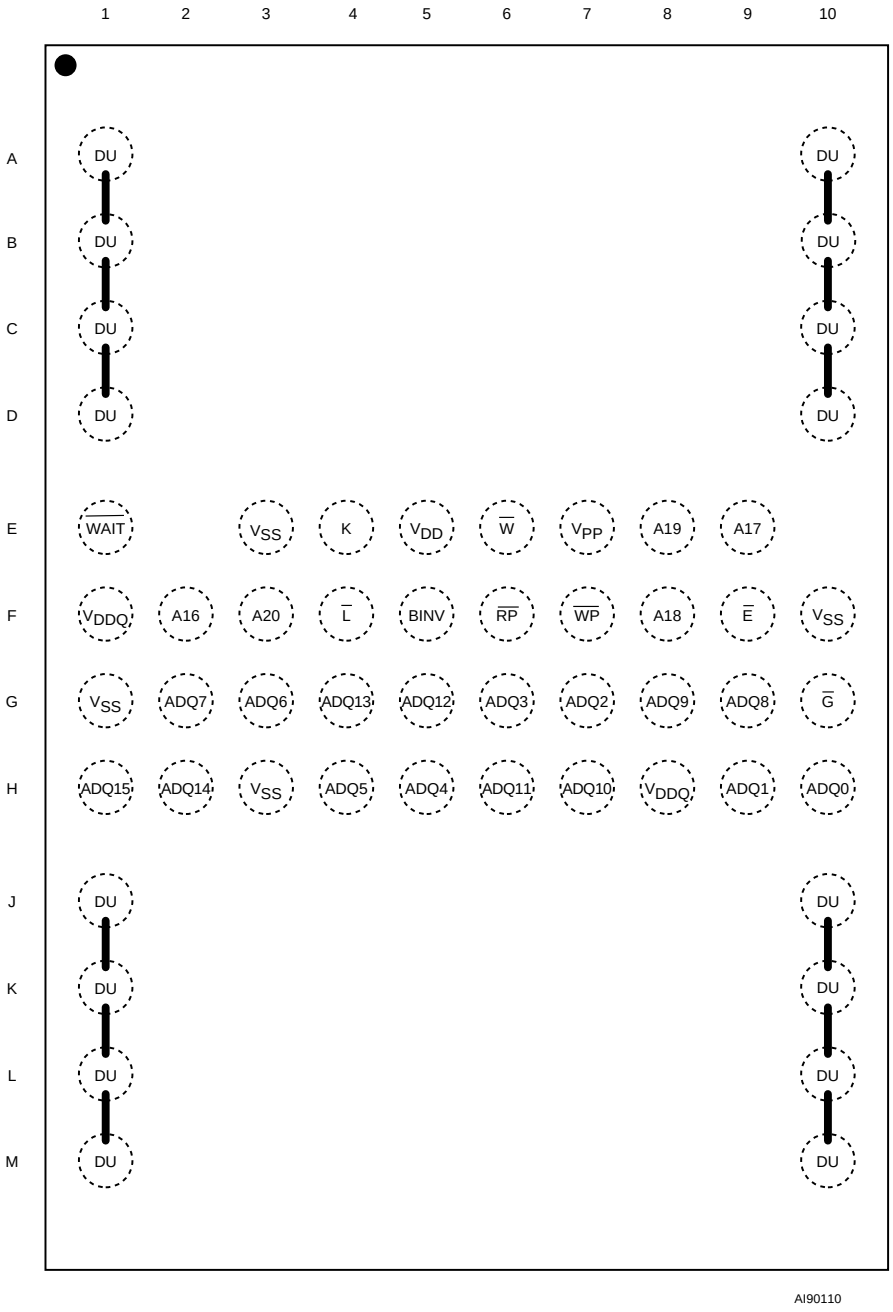


Figure 3. µBGA Connections (Top view through package)

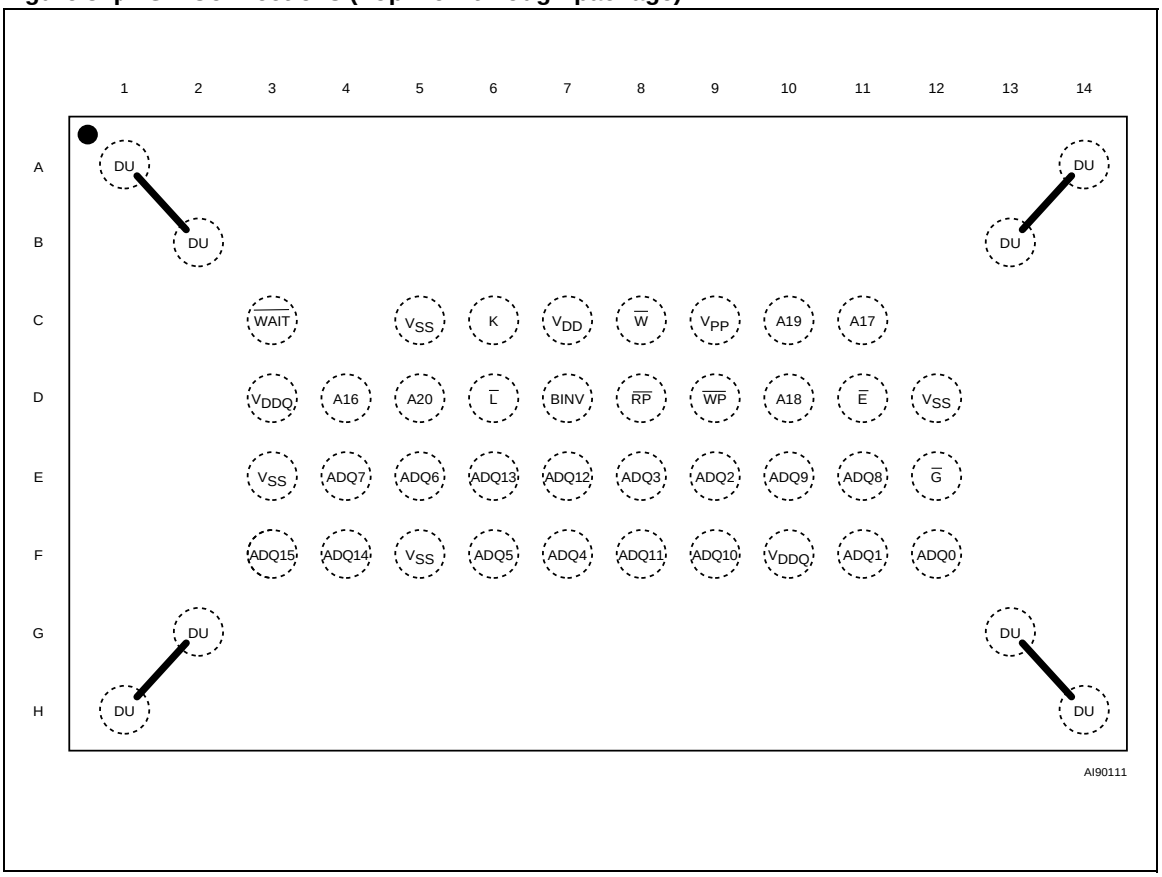


Table 1. Signal Names

A16-A20	Address Inputs
ADQ0-ADQ15	Data Input/Outputs or Address Inputs, Command Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power-down
$\overline{WP}$	Write Protect
K	Burst Clock
$\overline{L}$	Latch Enable
$\overline{WAIT}$	Wait Data in Burst Mode
BINV	Bus Invert
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
DU	Don't Use as Internally Connected

DESCRIPTION

The M59MR032 is a 32 Mbit non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.0V V_{DD} supply for the circuitry. For Program and Erase operations the necessary high voltages are generated internally. The device supports synchronous burst read and asynchronous page mode read from all the blocks of the memory array; at power-up the device is configured for page mode read. In synchronous burst mode, a new data is output at each clock cycle for frequencies up to 54MHz.

The array matrix organization allows each block to be erased and reprogrammed without affecting other blocks. All blocks are protected against programming and erase at Power-up. Blocks can be unprotected to make changes in the application and then reprotected.

Instructions for Read/Reset, Auto Select, Write Configuration Register, Programming, Block Erase, Bank Erase, Erase Suspend, Erase Resume, Block Protect, Block Unprotect, Block Locking, CFI Query, are written to the memory through a Command Interface (C.I.) using standard microprocessor write timings.

The memory is offered in LFBGA54 and µBGA46, 0.5 mm ball pitch packages and it is supplied with all the bits erased (set to '1').

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 155	°C
V_{IO} (3)	Input or Output Voltage	–0.5 to V_{DDQ}+0.5	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.5 to 2.7	V
V_{PP}	Program Voltage	–0.5 to 13	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

Organization

The M59MR032 is organized as 2Mbit by 16 bits. The first sixteen address lines are multiplexed with the Data Input/Output signals on the multiplexed address/data bus ADQ0-ADQ15. The remaining address lines A16-A20 are the MSB addresses. Memory control is provided by Chip Enable $\overline{E}$, Output Enable $\overline{G}$ and Write Enable $\overline{W}$ inputs.

The clock K input synchronizes the memory to the microprocessor during burst read.

Reset $\overline{RP}$ is used to reset all the memory circuitry and to set the chip in power-down mode if this function is enabled by a proper setting of the Configuration Register. Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.). Status Register data output on ADQ7 provides a Data Polling signal, ADQ6 and ADQ2 provide Toggle signals and ADQ5 provides error bit to indicate the state of the P/E.C operations. $\overline{WAIT}$ output indicates to the microprocessor the status of the memory during the burst mode operations.

Memory Blocks

The device features asymmetrically blocked architecture. M59MR032 has an array of 71 blocks and is divided into two banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible into Bank B or vice versa. The memory also features an erase suspend allowing to read or program in another block within the same bank. Once suspended the erase can be resumed. The Bank Size and Sectorization are summarized in Table 8. Parameter Blocks are located at the top of the memory address space for the M59MR032C, and at the bottom for the M59MR032D. The memory maps are shown in Tables 4, 5, 6 and 7.

The Program and Erase operations are managed automatically by the P/E.C. Block protection against Program or Erase provides additional data security. Instructions are provided to protect or unprotect any block in the application. A second register locks the protection status while $\overline{WP}$ is low (see Block Locking description). All blocks are protected and unlocked at Power-up.

Table 3. Bank Size and Sectorization

	Bank Size	Parameter Blocks	Main Blocks
Bank A	8 Mbit	8 blocks of 4 KWord	15 blocks of 32 KWord
Bank B	24 Mbit	-	48 blocks of 32 KWord

Table 4. Bank A, Top Boot Block Addresses M59MR032C

#	Size (KWord)	Address Range
22	4	1FF000h-1FFFFFh
21	4	1FE000h-1FEFFFh
20	4	1FD000h-1FDFFFh
19	4	1FC000h-1FCFFFh
18	4	1FB000h-1FBFFFh
17	4	1FA000h-1FAFFFh
16	4	1F9000h-1F9FFFh
15	4	1F8000h-1F8FFFh
14	32	1F0000h-1F7FFFh
13	32	1E8000h-1EFFFFh
12	32	1E0000h-1E7FFFh
11	32	1D8000h-1DFFFFh
10	32	1D0000h-1D7FFFh
9	32	1C8000h-1CFFFFh
8	32	1C0000h-1C7FFFh
7	32	1B8000h-1BFFFFh
6	32	1B0000h-1B7FFFh
5	32	1A8000h-1AFFFFh
4	32	1A0000h-1A7FFFh
3	32	198000h-19FFFFh
2	32	190000h-197FFFh
1	32	188000h-18FFFFh
0	32	180000h-187FFFh

Table 5. Bank B, Top Boot Block Addresses M59MR032C

#	Size (KWord)	Address Range
47	32	178000h-17FFFFh
46	32	170000h-177FFFh
45	32	168000h-16FFFFh
44	32	160000h-167FFFh
43	32	158000h-15FFFFh
42	32	150000h-157FFFh
41	32	148000h-14FFFFh
40	32	140000h-147FFFh
39	32	138000h-13FFFFh
38	32	130000h-137FFFh
37	32	128000h-12FFFFh
36	32	120000h-127FFFh
35	32	118000h-11FFFFh
34	32	110000h-117FFFh
33	32	108000h-10FFFFh
32	32	100000h-107FFFh
31	32	0F8000h-0FFFFFh
30	32	0F0000h-0F7FFFh
29	32	0E8000h-0EFFFFh
28	32	0E0000h-0E7FFFh
27	32	0D8000h-0DFFFFh
26	32	0D0000h-0D7FFFh
25	32	0C8000h-0CFFFFh
24	32	0C0000h-0C7FFFh
23	32	0B8000h-0BFFFFh
22	32	0B0000h-0B7FFFh
21	32	0A8000h-0AFFFFh
20	32	0A0000h-0A7FFFh
19	32	098000h-09FFFFh
18	32	090000h-097FFFh
17	32	088000h-08FFFFh
16	32	080000h-087FFFh
15	32	078000h-07FFFFh
14	32	070000h-077FFFh
13	32	068000h-06FFFFh
12	32	060000h-067FFFh
11	32	058000h-05FFFFh
10	32	050000h-057FFFh
9	32	048000h-04FFFFh
8	32	040000h-047FFFh
7	32	038000h-03FFFFh
6	32	030000h-037FFFh
5	32	028000h-02FFFFh
4	32	020000h-027FFFh
3	32	018000h-01FFFFh
2	32	010000h-017FFFh
1	32	008000h-00FFFFh
0	32	000000h-007FFFh

Table 6. Bank B, Bottom Boot Block Addresses M59MR032D

#	Size (KWord)	Address Range
47	32	1F8000h-1FFFFFh
46	32	1F0000h-1F7FFFh
45	32	1E8000h-1EFFFFh
44	32	1E0000h-1E7FFFh
43	32	1D8000h-1DFFFFh
42	32	1D0000h-1D7FFFh
41	32	1C8000h-1CFFFFh
40	32	1C0000h-1C7FFFh
39	32	1B8000h-1BFFFFh
38	32	1B0000h-1B7FFFh
37	32	1A8000h-1AFFFFh
36	32	1A0000h-1A7FFFh
35	32	198000h-19FFFFh
34	32	190000h-197FFFh
33	32	188000h-18FFFFh
32	32	180000h-187FFFh
31	32	178000h-17FFFFh
30	32	170000h-177FFFh
29	32	168000h-16FFFFh
28	32	160000h-167FFFh
27	32	158000h-15FFFFh
26	32	150000h-157FFFh
25	32	148000h-14FFFFh
24	32	140000h-147FFFh
23	32	138000h-13FFFFh
22	32	130000h-137FFFh
21	32	128000h-12FFFFh
20	32	120000h-127FFFh
19	32	118000h-11FFFFh
18	32	110000h-117FFFh
17	32	108000h-10FFFFh
16	32	100000h-107FFFh
15	32	0F8000h-0FFFFFh
14	32	0F0000h-0F7FFFh
13	32	0E8000h-0EFFFFh
12	32	0E0000h-0E7FFFh
11	32	0D8000h-0DFFFFh
10	32	0D0000h-0D7FFFh
9	32	0C8000h-0CFFFFh
8	32	0C0000h-0C7FFFh
7	32	0B8000h-0BFFFFh
6	32	0B0000h-0B7FFFh
5	32	0A8000h-0AFFFFh
4	32	0A0000h-0A7FFFh
3	32	098000h-09FFFFh
2	32	090000h-097FFFh
1	32	088000h-08FFFFh
0	32	080000h-087FFFh

Table 7. Bank A, Bottom Boot Block Addresses M59MR032D

#	Size (KWord)	Address Range
22	32	078000h-07FFFFh
21	32	070000h-077FFFh
20	32	068000h-06FFFFh
19	32	060000h-067FFFh
18	32	058000h-05FFFFh
17	32	050000h-057FFFh
16	32	048000h-04FFFFh
15	32	040000h-047FFFh
14	32	038000h-03FFFFh
13	32	030000h-037FFFh
12	32	028000h-02FFFFh
11	32	020000h-027FFFh
10	32	018000h-01FFFFh
9	32	010000h-017FFFh
8	32	008000h-00FFFFh
7	4	007000h-007FFFh
6	4	006000h-006FFFh
5	4	005000h-005FFFh
4	4	004000h-004FFFh
3	4	003000h-003FFFh
2	4	002000h-002FFFh
1	4	001000h-001FFFh
0	4	000000h-000FFFh

SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs or Data Input/Output (ADQ0-ADQ15). When Chip Enable $\overline{E}$ is at V_{IL} and Output Enable $\overline{G}$ is at V_{IH} the multiplexed address/data bus is used to input addresses for the memory array, data to be programmed in the memory array or commands to be written to the C.I. The address inputs for the memory array are latched on the rising edge of Latch Enable L. The address latch is transparent when L is at V_{IL}. Both input data and commands are latched on the rising edge of Write Enable $\overline{W}$. When Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} the address/data bus outputs data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection status the Configuration Register status or the Status Register Data Polling bit ADQ7, the Toggle Bits ADQ6 and ADQ2, the Error bit ADQ5. The address/data bus is high impedance when the chip is deselected, Output Enable $\overline{G}$ is at V_{IH}, or $\overline{RP}$ is at V_{IL}.

Address Inputs (A16-A20). The five MSB addresses of the memory array are latched on the rising edge of Latch Enable L.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ at V_{IH} deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at V_{IL}.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ is at V_{IH} the outputs are High impedance.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Data latches. Data are latched on the rising edge of $\overline{W}$.

Write Protect ($\overline{WP}$). This input gives an additional hardware protection level against program or erase when pulled at V_{IL}, as described in the Block Lock instruction description.

Reset/Power-down Input ($\overline{RP}$). The $\overline{RP}$ input provides hardware reset of the memory, and/or Power-down functions, depending on the Configuration Register status. Reset/Power-down of the memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPH}. When the reset pulse is given, if the memory is in Read, Erase Suspend Read or Standby, it will output new valid data in t_{PHQ7V1} after the rising edge of $\overline{RP}$. If the memory is in Erase or Program modes, the operation will be aborted and the reset recovery will take a maximum of t_{PLQ7V}. The memory will recover from Power-down (when enabled) in t_{PHQ7V2} after the rising edge of $\overline{RP}$. Exit from Reset/Power-down changes the contents of the configuration register bits 14 and 15, setting the memory in asynchronous page mode read and power save function disabled. All blocks are protected and unlocked after a Reset/Power-down. See Tables 29, 31 and Figure 14.

Latch Enable (L). L latches the address bits ADQ0-ADQ15 and A16-A20 on its rising edge. The address latch is transparent when L is at V_{IL} and it is inhibited when L is at V_{IH}.

Clock (K). The clock input synchronizes the memory to the microcontroller during burst mode read operation; the address is latched on a K edge (rising or falling, according to the configuration settings) when L is at V_{IL}. K is don't care during asynchronous page mode read and in write operations.

Wait ($\overline{WAIT}$). $\overline{WAIT}$ is an output signal used during burst mode read, indicating whether the data on the output bus are valid or a wait state must be inserted. This output is high impedance when $\overline{E}$ or $\overline{G}$ are high or $\overline{RP}$ is at V_{IL}, and can be configured to be active during the wait cycle or one clock cycle in advance.

Bus Invert (BINV). BINV is an input/output signal used to reduce the amount of power needed to switch the external address/data bus. The power saving is achieved by inverting the data output on ADQ0-ADQ15 every time this gives an advantage in terms of number of toggling bits. In burst mode read, each new data output from the memory is compared with the previous data. If the number of transitions required on the data bus is in excess of 8, the data is inverted and the BINV signal will be driven by the memory at V_{OH} to inform the receiving system that data must be inverted before any further processing. By doing so, the actual transitions on the data bus will be less than 8. In a similar way, when a command is given, BINV may be driven by the system at V_{IH} to inform the memory that the data must be inverted.Like the other input/output pins, BINV is high impedance when the chip is deselected, output enable $\overline{G}$ is at V_{IH} or $\overline{RP}$ is at V_{IL}; when used as an input, BINV must follow the same setup and hold timings of the data inputs.

V_{DD} and V_{DDQ} Supply Voltage (1.65V to 2.0V). The main power supply for all operations (Read, Program and Erase). V_{DD} and V_{DDQ} must be at the same voltage.

V_{PP} Program Supply Voltage (12V). V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin; if V_{PP} is kept in a low voltage range (0 to 2V) V_{PP} is seen as a control input, and the current absorption is limited to 5µA (0.2µA typical). In this case with $V_{PP} = V_{IL}$ we obtain an absolute protection against program or erase; with $V_{PP} = V_{PP1}$ these functions are enabled. V_{PP} value is only sampled during program or erase write cycles; a change in its value after the operation has been started does not have any effect and program or erase are carried on regularly. If V_{PP} is used in the 11.4V to 12.6V range (V_{PP2}) then the pin acts as a power supply. This supply voltage must remain stable as long as program or erase are finished. In read mode the current sunk is less then 0.5mA, while during program and erase operations the current may increase up to 10mA.

V_{SS} Ground. V_{SS} is the reference for all the voltage measurements.

DEVICE OPERATIONS

The following operations can be performed using the appropriate bus cycles: Address Latch, Read Array (Random, and Page Modes), Write command, Output Disable, Standby, Reset/Power-down and Block Locking. See Table 8.

Address Latch. In asynchronous operation, the address is latched on the rising edge of $\overline{L}$ input; in burst mode, the address is latched either by $\overline{L}$ going high or with a rising/falling edge of K, depending on the clock configuration.

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the CFI, the Block Protection Status, the Configuration Register status and the Security Code.

Read operation of the Memory Array may be performed in asynchronous page mode or synchronous burst mode. In asynchronous page mode data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by ADQ0 and ADQ1 address inputs.

According to the device configuration the following Read operations: Electronic Signature - Status Register - CFI - Block Protection Status - Configuration Register Status - Security Code must be accessed as asynchronous read or as single synchronous burst mode (see Figure 4). Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be at V_{IL} in order to read the output of the memory.

Table 8. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{WP}$	ADQ0-ADQ15
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{IH}	Hi-Z
Reset / Power-down	X	X	X	V_{IL}	V_{IH}	Hi-Z
Block Locking	V_{IL}	X	X	V_{IH}	V_{IL}	X

Note: 1. X = Don't care.

Table 9. Read Electronic Signature (AS and Read CFI instructions) (1)

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0-A7	A8-A20	Data
Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	00h	Don't Care	0020h
Device Code	M59MR032C	V_{IL}	V_{IL}	V_{IH}	01h	Don't Care	00A4h
	M59MR032D	V_{IL}	V_{IL}	V_{IH}	01h	Don't Care	00A5h

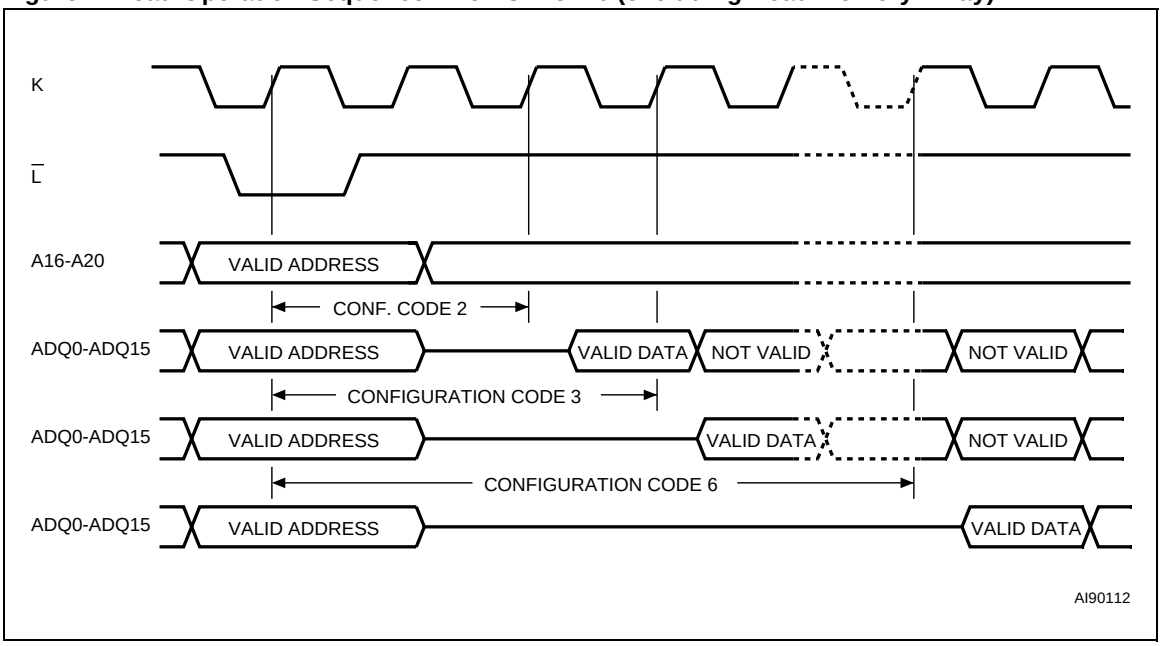
Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.

Table 10. Read Block Protection (AS and Read CFI instructions) (1)

Block Status	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0-A7	A8-A11	A12-A20	Data
Protected and unlocked	V_{IL}	V_{IL}	V_{IH}	02h	Don't Care	Block Address	0001
Unprotected and unlocked	V_{IL}	V_{IL}	V_{IH}	02h	Don't Care	Block Address	0000
Protected and locked	V_{IL}	V_{IL}	V_{IH}	02h	Don't Care	Block Address	0003
Unprotected and locked (2)	V_{IL}	V_{IL}	V_{IH}	02h	Don't Care	Block Address	0002

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. A locked block can be unprotected only with $\overline{WP}$ at V_{IH}.

Figure 4. Read Operation Sequence when CR15 = 0 (excluding Read Memory Array)



Burst Read. The device also supports a burst read. In this mode, an address is first latched on the rising edge of $\overline{L}$ or K (or falling edge of K, according to configuration settings); after a configurable delay of 2 to 6 clock cycles a new data is output at each clock cycle. The burst sequence may be configured for linear or interleaved order and for a length of 4, 8 words or for continuous burst mode.

A $\overline{WAIT}$ signal may be asserted to indicate to the system that an output delay will occur.

This delay will depend on the starting address of the burst sequence; the worst case delay will occur when the sequence is crossing a 32 word boundary and the starting address was at the end of a four word boundary. See the Write Configuration Register (CR) Instruction for more details on all the possible settings for the synchronous burst read.

Write. Write operations are used to give Instruction Commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at V_{IL} with Output Enable $\overline{G}$ at V_{IH}. Addresses are latched on the rising edge of $\overline{L}$. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first. Noise pulses of less than 5ns typical on $\overline{E}$, $\overline{W}$ and $\overline{G}$ signals do not start a write cycle. Write operations are asynchronous and clock is ignored during write.

Dual Bank Operations. The Dual Bank allows to read data from one bank of memory while a program or erase operation is in progress in the other bank of the memory. Read and Write cycles can be initiated for simultaneous operations in different banks without any delay. Status Register during Program or Erase must be monitored using an address within the bank being modified.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is at V_{IH} with Write Enable $\overline{W}$ at V_{IH}.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is at V_{IH} and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Standby. When in Read mode, after 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus. The automatic standby feature is not available when the device is configured for synchronous burst mode.

Power-down. The memory is in Power-down when the Configuration Register is set for Power-down and $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the Power-down level, and Outputs are in high impedance, independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Block Locking. Any combination of blocks can be temporarily protected against Program or Erase by setting the lock register and pulling $\overline{WP}$ to V_{IL} (see Block Lock instruction).

INSTRUCTIONS AND COMMANDS

Seventeen instructions are defined (see Table 17), and the internal P/E.C. automatically handles all timing and verification of the Program and Erase operations. The Status Register Data Polling, Toggle, Error bits can be read at any time, during programming or erase, to monitor the progress of the operation.

Instructions, made up of one or more commands written in cycles, can be given to the Program/ Erase Controller through a Command Interface (C.I.). The C.I. latches commands written to the memory. Commands are made of address and data sequences. Two Coded Cycles unlock the Command Interface. They are followed by an input command or a confirmation command. The Coded Sequence consists of writing the data AAh at the address 555h during the first cycle and the data 55h at the address 2AAh during the second cycle.

Instructions are composed of up to six cycles. The first two cycles input a Coded Sequence to the Command Interface which is common to all instructions (see Table 17). The third cycle inputs the instruction set-up command. Subsequent cycles output the addressed data, Electronic Signature, Block Protection, Configuration Register Status or CFI Query for Read operations. In order to give additional data protection, the instructions for Block Erase and Bank Erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For a Double Word Programming instruction, the fourth and fifth command cycles input the address and data to be programmed. For a Block Erase and Bank Erase instructions, the fourth and fifth cycles input a further Coded Sequence before the Erase confirm command on the sixth cycle. Any combination of blocks of the same memory bank can be erased. Erasure of a memory block may be suspended, in order to read data from another block or to program data in another block, and then resumed. When power is first applied the command interface is reset to Read Array.

Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to ensure maximum data security.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded Cycles. Subsequent read operations will read the memory array addressed and output the data read. The Reset command does not affect the configuration of unprotected blocks and the Configuration Register status. Read/Reset Instruction is ignored when program or erase is in progress.

CFI Query (RCFI) Instruction. Common Flash Interface Query mode is entered writing 98h at address 55h. The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. Tables 19, 20, 21 and 22 show the addresses used to retrieve each data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number, organized by word, is written starting at address 81h. This area can be accessed only in read mode by the final user and there are no ways of changing the code after it has been written by ST. Write a read instruction (RD) to return to Read Array mode.

Table 11. Commands

Hex Code	Command
00h	Bypass Reset
10h	Bank Erase Confirm
20h	Unlock Bypass
30h	Block Erase Resume/Confirm
40h	Double Word Program
60h	Block Protect, or Block Unprotect, or Block Lock, or Write Configuration Register
80h	Set-up Erase
90h	Read Electronic Signature, or Block Protection Status, or Configuration Register Status
98h	CFI Query
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Auto Select (AS) Instruction. This instruction uses two Coded Cycles followed by one write cycle giving the command 90h to address 555h for command set-up. A subsequent read will output the Manufacturer or the Device Code (Electronic Signature), the Block Protection status or the Configuration Register status depending on the levels of ADQ0 and ADQ1 (see Tables 9, 10 and 11).

The Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of M59MR032. The Manufacturer Code is output when the address lines ADQ0 and ADQ1 are at V_{IL}, the Device Code is output when ADQ0 is at V_{IH} with ADQ1 at V_{IL}.

The codes are output on ADQ0-ADQ7 with ADQ8-ADQ15 at 00h. The AS instruction also allows the access to the Block Protection Status. After giving the AS instruction, ADQ0 is set to V_{IL} with ADQ1 at V_{IH}, while A12-A20 define the address of the block to be verified (see Table 10). The AS Instruction finally allows the access to the Configuration Register status if both ADQ0 and ADQ1 are set to V_{IH}; refer to Table 12 for configuration register description.

A reset command puts the device in Read Array mode.

Write Configuration Register (CR) Instruction. This instruction uses two Coded Cycles followed by one write cycle giving the command 60h to address 555h. A further write cycle giving the command 03h writes the contents of address bits ADQ0-ADQ15 to bits CR15-CR0 of the configuration register. At Power-up the Configuration Register is set to asynchronous Read mode, Power-down disabled and bus invert (power save function) disabled.

A description of the effects of each configuration bit is given in Table 12.

Table 12. Read Configuration Register (AS and Read CFI instructions)

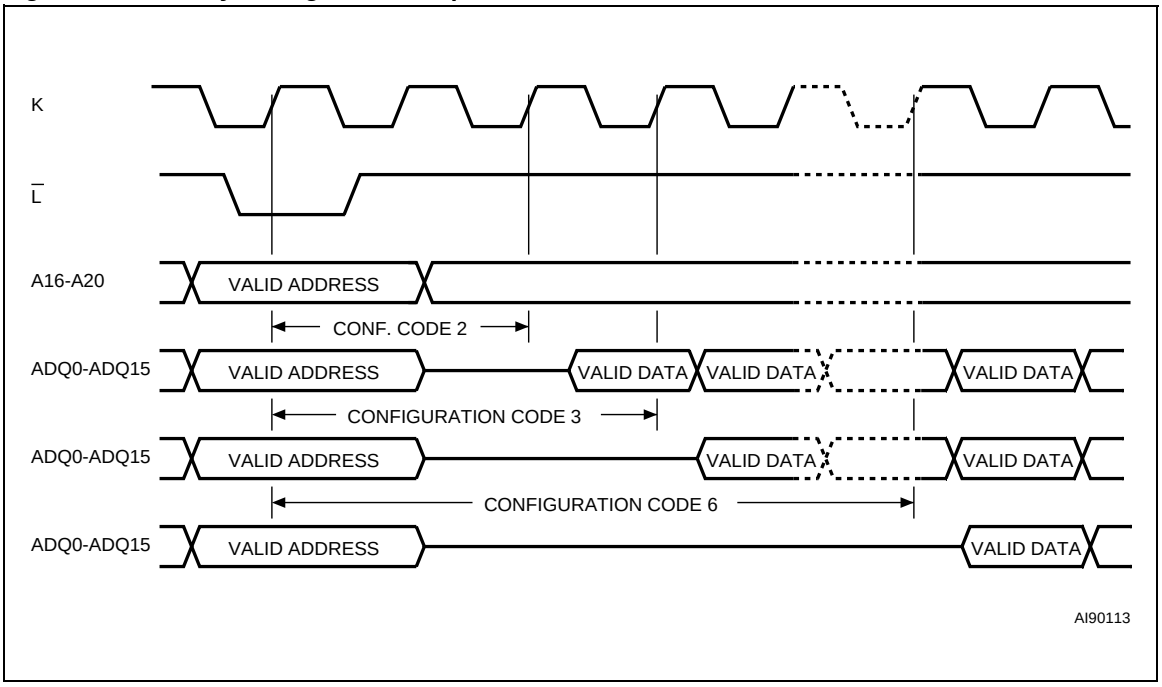
Configuration Register	Function
CR15	Read mode 0 = Burst mode read 1 = Page mode read (default)
CR14	Bus Invert configuration (power save) 0 = disabled (default) 1 = enabled
CR13-CR11	X-Latency 010 = 2 clock latency 011 = 3 clock latency 100 = 4 clock latency 101 = 5 clock latency 110 = 6 clock latency
CR10	Power-down configuration 0 = power-down disabled (default) 1 = power-down enabled
CR9	Data hold configuration 0 = data output at every clock cycle 1 = data output every 2 clock cycles
CR8	Wait configuration 0 = $\overline{\text{WAIT}}$ is active during wait state 1 = $\overline{\text{WAIT}}$ is active one data cycle before wait state
CR7	Burst order configuration 0 = Interleaved 1 = Linear
CR6	Clock configuration 0 = Address latched and data output on the falling clock edge. 1 = Address latched and data output on the rising clock edge.
CR5-CR3	Reserved
CR2-CR0	Burst length 001 = 4 word burst length 010 = 8 word burst length 111 = Continuous burst mode (requires CR7 = 1)

Table 13. X-Latency Configuration

Configuration Code	Input Frequency	
	100ns	120ns
2	25MHz	20MHz
3	40MHz	30MHz
4	54MHz	40MHz
5 (1)	66MHz	50MHz
6 (1)	–	60MHz

Note: 1. Configuration codes 5 and 6 may be used only in conjunction with configuration bit CR9 set at "1" (one data every 2 clock cycles).

Figure 5. X-Latency Configuration Sequence



– **Read mode (CR15).** The device supports an asynchronous page mode and a synchronous burst mode. In asynchronous page mode, the default at power-up, data is internally read and stored in a buffer of 4 words selected by ADQ0 and ADQ1 address inputs. In synchronous burst mode, the device latches the starting address and then outputs a sequence of data which depends on the configuration register settings.

– **Bus Invert configuration (CR14).** This register bit is used to enable the BINV pin functionality. BINV functionality depends upon configuration bits CR14 and CR15 (see Table 12 for configuration bits definition) as shown in Table 14.

As output pin BINV is active only when enabled (CR14 = 1) in Read Array burst mode (CR15 = 0).

As input pin BINV is active only when enabled (CR14 = 1). BINV is ignored when ADQ0-ADQ15 lines are used as address inputs (addresses must not be inverted).

Table 14. BINV Configuration Bits

CR15	CR14	BINV	
		IN	OUT
0	0	X	0
0	1	Active	Active
1	0	X	0
1	1	Active	0

Table 15. Burst Order and Length Configuration

Starting Address	4 Words		8 Words		Continuous Burst
	Linear	Interleaved	Linear	Interleaved	
0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5...
1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6...
2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7...
3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8...
...					
7	7-4-5-6	7-6-5-4	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11...
...					
28					28-29-30-31-32...
29					29-30-31-WAIT-32...
30					30-31-WAIT-WAIT-32...
31					31-WAIT-WAIT-WAIT-32...

– **X-Latency (CR13-CR11).** These configuration bits define the number of clock cycles elapsing from $\overline{L}$ going low to valid data available in burst mode. The correspondence between X-Latency settings and the sustainable clock frequencies is given in Table 13 and Figure 5.

– **Power-down configuration (CR10).** The $\overline{RP}$ pin may be configured to give a very low power consumption when driven low (power-down state). In power-down the I_{CC} supply current is reduced to a typical figure of 2µA; if this function is disabled (default at power-up) the $\overline{RP}$ pin causes only a reset of the device and the supply current is the stand-by value. The recovery time after a $\overline{RP}$ pulse is significantly longer (50µs vs. 150ns) when power-down is enabled.

– **Data hold configuration (CR9).** In burst mode this register bit determines if a new data is output at each clock cycle or every 2 clock cycles.

– **Wait configuration (CR8).** In burst mode $\overline{WAIT}$ indicates whether the data on the output bus are valid or a wait state must be inserted. The configuration bit determines if $\overline{WAIT}$ will be asserted one clock cycle before the wait state or during the wait state (see Figure 10).

– **Burst order configuration (CR7).** See Table 15 for burst order and length.

– **Clock configuration (CR6).** In burst mode determines if address is latched and data is output on the rising or falling edge of the clock.

– **Burst length (CR2-CR0).** In burst mode determines the number of words output by the memory. It is possible to have 4 words, 8 words or a continuous burst mode, in which all the words in bank A or bank B are read sequentially. In continuous burst mode the burst sequence is interrupted at the end of each of the two banks or when a suspended block is reached. In continuous burst mode it may happen that the memory will stop the data output flow for a few clock cycles; this event is signaled by $\overline{WAIT}$ going low until the output flow is resumed. The initial address determines if the output delay will occur as well as its duration. If the starting address is aligned to a four word boundary no wait states will be needed. If the starting address is shifted by 1,2 or 3 positions from the four word boundary, $\overline{WAIT}$ will be asserted for 1,2 or 3 clock cycles (2,4, 6 cycles if CR9 is set at “1”) when the burst sequence is crossing the first 32 word boundary. $\overline{WAIT}$ will be asserted only once during a continuous burst access. See also Table 15.

Enter Bypass Mode (EBY) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 20h to address 555h for mode set-up. Once in Bypass mode, the device will accept the Exit Bypass (XBY) and Program or Double Word Program in Bypass mode (PGBY, DPGBY) commands. The Bypass mode allows to reduce the overall programming time when large memory arrays need to be programmed.

Exit Bypass Mode (XBY) Instruction. This instruction uses two write cycles. The first inputs to the memory the command 90h and the second inputs the Exit Bypass mode confirm (00h). After the XBY instruction, the device resets to Read Memory Array mode.

Table 16. Protection States (1)

Current State (2) ($\overline{WP}$, ADQ1, ADQ0)	Program/Erase Allowed	Next State After Event (3)			
		Protect	Unprotect	Lock	$\overline{WP}$ transition
100	yes	101	100	111	000
101	no	101	100	111	001
110	yes	111	110	111	011
111	no	111	110	111	011
000	yes	001	000	011	100
001	no	001	000	011	101
011	no	011	011	011	111 or 110 (4)

Note: 1. All blocks are protected at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
2. Current state and Next state gives the protection status of a block. The protection status is defined by the write protect pin and by ADQ1 (= 1 for a locked block) and ADQ0 (= 1 for a protected block) as read in the Autoselect instruction with A1 = V_{IH} and A0 = V_{IL}.
3. Next state is the protection status of a block after a Protect or Unprotect or Lock command has been issued or after $\overline{WP}$ has changed its logic value.
4. A $\overline{WP}$ transition to V_{IH} on a locked block will restore the previous ADQ0 value, giving a 111 or 110.

Program in Bypass Mode (PGBY) Instruction. This instruction uses two write cycles. The Program command A0h is written to any Address on the first cycle and the second write cycle latches the Address on the rising edge of $\overline{L}$ and the Data to be written on the rising edge of $\overline{W}$ and starts the P/E.C. Read operations within the same bank output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. The content of the memory cell is not changed if the user write '1' in place of '0' and no error occurs. Status bits ADQ6 and ADQ7 determine if programming is ongoing and ADQ5 allows verification of any possible error.

Program (PG) Instruction. This instruction uses four write cycles. The Program command A0h is written to address 555h on the third cycle after two Coded Cycles. A fourth write operation latches the Address and the Data to be written and starts the P/E.C. Read operations within the same bank output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. The content of the memory cell is not changed if the user write '1' in place of '0' and no error occurs. Status bits ADQ6 and ADQ7 determine if programming is on-going and ADQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend.

Double Word Program (DPG) Instruction. This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel. High voltage (11.4V to 12.6V) on V_{PP} pin is required. This instruction uses five write cycles. The double word program command 40h is written to address 555h on the third cycle after two Coded Cycles. A fourth write cycle latches the address and data to be written to the first location. A fifth write cycle latches the new data to be written to the second location and starts the P/E.C.. Note that the two locations must have the same address except for the address bit A0. The Double Word Program can be executed in Bypass mode (DPGBY) to skip the two coded cycles at the beginning of each command.

Block Protect (BP), Block Unprotect (BU), Block Lock (BL) Instructions. All blocks are protected and unlocked at power-up. Each block of the array has two levels of protection against program or erase operation. The first level is set by the Block Protect instruction; a protected block cannot be programmed or erased until a Block Unprotect instruction is given for that block. A second level of protection is set by the Block Lock instruction, and requires the use of the $\overline{WP}$ pin, according to the following scheme:

– when $\overline{WP}$ is at V_{IH}, the Lock status is overridden and all blocks can be protected or unprotected;
– when $\overline{WP}$ is at V_{IL}, Lock status is enabled; the locked blocks are protected, regardless of their previous protect state, and protection status cannot be changed. Blocks that are not locked can still change their protection status, and program or erase accordingly;

– the lock status is cleared for all blocks at power-up or pulling $\overline{RP}$ at V_{IL} for at least t_{PLPH}. The protection and lock status can be monitored for each block using the Autoselect (AS) instruction. Protected blocks will output a '1' on ADQ0 and locked blocks will output a '1' on ADQ1.

After a pulse of $\overline{RP}$ of at least t_{PLPH} all blocks are protected and unlocked.

Refer to Table 16 for a list of the protection states.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 555h on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles and an address within the block to be erased is given and latched into the memory.

Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. All blocks must belong to the same bank of memory; if a new block belonging to the other bank is given, the operation is aborted. The erase will start after an erase timeout period of 100µs. Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of ADQ3, if ADQ3 is '0' the Block Erase Command has been given and the timeout is running, if ADQ3 is '1', the timeout has expired and the P/E.C. is erasing the Block(s). If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before erasing to FFh. Read operations within the same bank, after the sixth rising edge of $\overline{W}$ or $\overline{E}$, output the status register bits.

During the execution of the erase by the P/E.C., the memory accepts only the Erase Suspend ES instruction; the Read/Reset RD instruction is accepted during the 100µs time-out period. Data Polling bit ADQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit ADQ6 toggles during the erase operation, and stops when erase is completed.

After completion the Status Register bit ADQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit ADQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the P/E.C.

Bank Erase (BKE) Instruction. This instruction uses six write cycles and is used to erase all the blocks belonging to the selected bank. The Erase Set-up command 80h is written to address 555h on the third cycle after the two Coded cycles. The Bank Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles at an address within the selected bank. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing it to FFh. Read operations within the same bank after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the Status Register bits. During the execution of the erase by the P/E.C., Data Polling bit ADQ7 returns '0', then '1' on completion. The Toggle bit ADQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit ADQ5 returns '1' if there has been an Erase Failure.

Erase Suspend (ES) Instruction. In a dual bank memory the Erase Suspend instruction is used to read data within the bank where erase is in progress. It is also possible to program data in blocks not being erased.

The Erase Suspend instruction consists of writing the command B0h without any specific address. No Coded Cycles are required. Erase suspend is accepted only during the Block Erase instruction execution. The Toggle bit ADQ6 stops toggling when the P/E.C. is suspended within 15µs after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output ADQ2 toggling and ADQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions. A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in ADQ6 toggling when the data is being programmed.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at an address within the bank being erased and without any Coded Cycle.

Table 17. Instructions (1,2)

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.
RD (4)	Read/Reset Memory Array	1+	**Addr.** (3)	X	Read Memory Array until a new write cycle is initiated.				
			Data	F0h					
		3+	**Addr.**	555h	2AAh	555h	Read Memory Array until a new write cycle is initiated.		
			Data	AAh	55h	F0h			
RCFI	CFI Query	1+	**Addr.**	55h	Read CFI data until a new write cycle is initiated.				
			Data	98h					
AS (4)	Auto Select	3+	**Addr.**	555h	2AAh	555h	Read electronic Signature or Block Protection or Configuration Register Status until a new cycle is initiated.		
			Data	AAh	55h	90h			
CR	Configuration Register Write	4	**Addr.**	555h	2AAh	555h	Configura-tion Data		
			Data	AAh	55h	60h	03h		
PG	Program	4	**Addr.**	555h	2AAh	555h	Program Address	Read Data Polling or Toggle Bit until Program completes.	
			Data	AAh	55h	A0h	Program Data		
DPG	Double Word Program	5	**Addr.**	555h	2AAh	555h	Program Address 1	Program Address 2	Note 6, 7
			Data	AAh	55h	40h	Program Data 1	Program Data 2	
EBY	Enter Bypass Mode	3	**Addr.**	555h	2AAh	555h			
			Data	AAh	55h	20h			
XBY	Exit Bypass Mode	2	**Addr.**	X	X				
			Data	90h	00h				
PGBY	Program in Bypass Mode	2	**Addr.**	X	Program Address	Read Data Polling or Toggle Bit until Program completes.			
			Data	A0h	Program Data				
DPGBY	Double Word Program in Bypass Mode	3	**Addr.**	X	Program Address 1	Program Address 2	Note 6, 7		
			Data	40h	Program Data 1	Program Data 2			
BP	Block Protect	4	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	01h		
BU	Block Unprotect	1	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	D0h		

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.
BL	Block Lock	4	**Addr.**	555h	2AAh	555h	Block Address		
			Data	AAh	55h	60h	2Fh		
BE	Block Erase	6+	**Addr.**	555h	2AAh	555h	555h	2AAh	Block Address
			Data	AAh	55h	80h	AAh	55h	30h
BKE	Bank Erase	6	**Addr.**	555h	2AAh	555h	555h	2AAh	Bank Address
			Data	AAh	55h	80h	AAh	55h	10h
ES	Erase Suspend	1	**Addr.** (3)	X	Read until Toggle stops, then read all the data needed from any Blocks not being erased then Resume Erase.				
			Data	B0h					
ER	Erase Resume	1	**Addr.**	Bank Address	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time				
			Data	30h					

Note: 1. Commands not interpreted in this table will default to read array mode.
2. For Coded cycles address inputs A11-A20 are don't care.
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.
6. Program Address 1 and Program Address 2 must be consecutive addresses differing only for address bit A0.
7. High voltage on V_{PP} (11.4V to 12.6V) is required for the proper execution of the Double Word Program instruction.

STATUS REGISTER BITS

P/E.C. status is indicated during execution by Data Polling on ADQ7, detection of Toggle on ADQ6 and ADQ2, or Error on ADQ5 bits. Any read attempt within the Bank being modified and during Program or Erase command execution will automatically output these five Status Register bits. The P/E.C. automatically sets bits ADQ2, ADQ5, ADQ6 and ADQ7. Other bits (ADQ0, ADQ1 and ADQ4) are reserved for future use and should be masked (see Table 18). Read attempts within the bank not being modified will output array data.

Toggle bits ADQ6 and ADQ2 are affected by $\overline{G}$ and/or $\overline{E}$ cycles regardless of the bank in which these cycles refer to. This means that toggle bits are in a state that depends on the amount of accesses to both banks and not only to the bank where erasing or programming is on going. Status Register Bits must be accessed according to the device configuration (see Figure 4).

Data Polling Bit (ADQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on ADQ7. In case of a double word program operation, the complement is done on ADQ7 of the last word written to the command interface, i.e. the data written in the fifth cycle. During Erase operation, it outputs a '0'. After completion of the operation, ADQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid and only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for erase. It must be performed at the address being programmed or at an address within the block being erased. See Figure 17 for the Data Polling flowchart and Figure 15 for the Data Polling waveforms. ADQ7 will also flag the Erase Suspend mode by switching from '0' to '1' at the start of the Erase Suspend. In order to monitor ADQ7 in the Erase Suspend mode an address within a block being erased must be provided. For a Read Operation in Suspend mode, ADQ7 will output '1' if the read is attempted on a block being erased and the data value on other blocks. During Program operation in Erase Suspend Mode, ADQ7 will have the same behavior as in the normal program execution outside of the suspend mode.

Toggle Bit (ADQ6). When Programming or Erasing operations are in progress, successive attempts to read ADQ6 will output complementary data. ADQ6 will toggle following toggling of either $\overline{G}$, or $\overline{E}$ when $\overline{G}$ is at V_{IL}. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit ADQ6 is valid only during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. ADQ6 will be set to '1' if a Read operation is attempted on an Erase Suspend block. When erase is suspended ADQ6 will toggle during programming operations in a block different from the block in Erase Suspend. Either $\overline{E}$ or $\overline{G}$ toggling will cause ADQ6 to toggle. See Figure 18 for Toggle Bit flowchart and Figure 16 for Toggle Bit waveforms.

Toggle Bit (ADQ2). This toggle bit, together with ADQ6, can be used to determine the device status during the Erase operations. During Erase Suspend a read from a block being erased will cause ADQ2 to toggle. A read from a block not being erased will output data. ADQ2 will be set to '1' during program operation. After erase completion and if the error bit ADQ5 is set to '1', ADQ2 will toggle if the faulty block is addressed.

Error Bit (ADQ5). This bit is set to '1' by the P/E.C. when there is a failure of programming or block erase, that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occurred or to which the programmed data belongs, must be discarded. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0'.

Erase Timer Bit (ADQ3). This bit is set to '0' by the P/E.C. when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, ADQ3 returns to '1', in the range of 80µs to 120µs.

Table 18. Status Register Bits (1)

	Status		DQ7 (2)	DQ6	DQ5	DQ3	DQ2 (2)
In Progress	Program		$\overline{DQ7}$	Toggle	0	N/A	1
	Block Erase Timeout		0	Toggle	0	0	N/A
	Block/Chip Erase		0	Toggle	0	1	N/A
	Erase Suspend Mode	Erase Suspended Block	1	1	0	N/A	Toggle
		Non Erase Suspended Block	Automatic return to reading array data				
	Programming during Erase Suspend		$\overline{DQ7}$	Toggle	0	N/A	1
Successfully/ Completed	Word Program		Automatic return to reading array data				
	Block/Chip Erase						
Exceeded Time Limit	Word Program		$\overline{DQ7}$	Toggle	1	N/A	1
	Block/Chip Erase		0	Toggle	1	1	Toggle is failed, block is addressed
	Program in Suspend		$\overline{DQ7}$	Toggle	1	N/A	1

Note: 1. Status Register bits do not consider BINV.
2. DQ7 and DQ2 require a valid address when reading status information.

POWER CONSUMPTION

Power-down

The memory provides Reset/Power-down control input $\overline{RP}$. The Power-down function can be activated only if the relevant Configuration Register bit is set to '1'. In this case, when the $\overline{RP}$ signal is pulled at V_{SS} the supply current drops to typically I_{CC2} (see Table 28), the memory is deselected and the outputs are in high impedance.If $\overline{RP}$ is pulled to V_{SS} during a Program or Erase operation, this operation is aborted in t_{PLQ7V} and the memory content is no longer valid (see Reset/Power-down input description).

Power-up

The memory Command Interface is reset on Power-up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to V_{IH} during Power-up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{W}$. At Power-up the device is configured as:

– page mode: (CR15 = 1)
– power-down disabled: (CR10 = 0)
– BINV disabled: (CR14 = 0)

and all blocks are protected and unlocked.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{DD} rails decoupled with a 0.1µF capacitor close to the V_{DD}, V_{DDQ} and V_{SS} pins. The PCB trace widths should be sufficient to carry the required V_{DD} program and erase currents.

COMMON FLASH INTERFACE (CFI)

The Common Flash Interface (CFI) specification is a JEDEC approved, standardised data structure that can be read from the Flash memory device. CFI allows a system software to query the flash device to determine various electrical and timing parameters, density information and functions supported by the device. CFI allows the system to easily interface to the Flash memory, to learn about its features and parameters, enabling the software to configure itself when necessary.

Tables 19, 20, 21, 22, 23 and 24 show the address used to retrieve each data.

The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. Tables 19, 20, 21 and 22 show the addresses used to retrieve each data. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 81h. This area can be accessed only in read mode and there are no ways of changing the code after it has been written by ST. Write a read instruction to return to Read mode. Refer to the CFI Query instruction to understand how the M59MR032 enters the CFI Query mode.

Table 19. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables 20, 21 and 22. Query data are always presented on the lowest order data outputs.

Table 20. CFI Query Identification String

Offset	Data	Description
00h	0020h	Manufacturer Code
01h	00A4h - Top 00A5h - Bottom	Device Code
02h-0Fh	reserved	Reserved
10h	0051h	Query Unique ASCII String "QRY"
11h	0052h	
12h	0059h	
13h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm
14h	0000h	
15h	offset = P = 0039h	Address for Primary Algorithm extended Query table
16h	0000h	
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)
18h	0000h	
19h	value = A = 0000h	Address for Alternate Algorithm extended Query table note: 0000h means none exists
1Ah	0000h	

Note: Query data are always presented on the lowest - order data outputs (ADQ0-ADQ7) only. ADQ8-ADQ15 are '0'.

Table 21. CFI Query System Interface Information

Offset	Data	Description
1Bh	0017h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Ch	0022h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts
1Dh	0017h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PP} pin is present
1Eh	00C0h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts Note: This value must be 0000h if no V_{PP} pin is present
1Fh	0004h	Typical timeout per single byte/word program (multi-byte program count = 1), 2^n µs (if supported; 0000h = not supported)
20h	0004h	Typical timeout for maximum-size multi-byte program or page write, 2^n µs (if supported; 0000h = not supported)
21h	000Ah	Typical timeout per individual block erase, 2^n ms (if supported; 0000h = not supported)
22h	0000h	Typical timeout for full chip erase, 2^n ms (if supported; 0000h = not supported)
23h	0004h	Maximum timeout for byte/word program, 2^n times typical (offset 1Fh) (0000h = not supported)
24h	0004h	Maximum timeout for multi-byte program or page write, 2^n times typical (offset 20h) (0000h = not supported)
25h	0004h	Maximum timeout per individual block erase, 2^n times typical (offset 21h) (0000h = not supported)
26h	0000h	Maximum timeout for chip erase, 2^n times typical (offset 22h) (0000h = not supported)

Table 22. Device Geometry Definition

Offset Word Mode	Data	Description
27h	0016h	Device Size = 2^n in number of bytes
28h	0001h	Flash Device Interface Code description: Asynchronous x16
29h	0000h	
2Ah	0000h	Maximum number of bytes in multi-byte program or page = 2^n
2Bh	0000h	
2Ch	0003h	Number of Erase Block Regions within device bit 7 to 0 = x = number of Erase Block Regions Note:1. x = 0 means no erase blocking, i.e. the device erases at once in "bulk." 2. x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128KB device (1Mb) having blocking of 16KB, 8KB, four 2KB, two 16KB, and one 64KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions. 3. By definition, symmetrically block devices have only one blocking region.
M59MR032C	M59MR032C	Erase Block Region Information
2Dh	002Fh	bit 31 to 16 = z, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128 byte block size. e.g. for 64KB block size, z = 0100h = 256 => 256 * 256 = 64K
2Eh	0000h	
2Fh	0000h	
30h	0001h	bit 15 to 0 = y, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region: e.g. y = D15-D0 = FFFFh => y+1 = 64K blocks [maximum number] y = 0 means no blocking (# blocks = y+1 = "1 block") Note: y = 0 value must be used with number of block regions of one as indicated by (x) = 0
31h	000Eh	
32h	0000h	
33h	0000h	
34h	0001h	
35h	0007h	
36h	0000h	
37h	0020h	
38h	0000h	
M59MR032D	M59MR032D	
2Dh	0007h	
2Eh	0000h	
2Fh	0020h	
30h	0000h	
31h	000Eh	
32h	0000h	
33h	0000h	
34h	0001h	
35h	002Fh	
36h	0000h	
37h	0000h	
38h	0001h	

Table 23. Primary Algorithm-Specific Extended Query Table

Offset	Data	Description
(P)h = 39h 0052h 0049h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”
(P+3)h = 3Ch	0031h	Major version number, ASCII
(P+4)h = 3Dh	0030h	Minor version number, ASCII
(P+5)h = 3Eh (P+7)h (P+8)h	00F2h 0003h 0000h 0000h	Extended Query table contents for Primary Algorithm bit 10-31 Reserved; undefined bits are ‘0’. If bit 31 is ’1’ then another 31 bit field of optional features follows at the end of the bit-30 field. bit 0 Chip Erase supported (1 = Yes, 0 = No) bit 1 Suspend Erase supported (1 = Yes, 0 = No) bit 2 Suspend Program supported (1 = Yes, 0 = No) bit 3 Legacy Lock/Unlock supported (1 = Yes, 0 = No) bit 4 Queued Erase supported (1 = Yes, 0 = No) bit 5 Instant individual block locking supported (1 = Yes, 0 = No) bit 6 Protection bits supported (1 = Yes, 0 = No) bit 7 Page-mode read supported (1 = Yes, 0 = No) bit 8 Synchronous read supported (1 = Yes, 0 = No) bit 9 Simultaneous operation supported (1 = Yes, 0 = No)
(P+9)h = 42h	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1 Reserved; undefined bits are ‘0’
(P+A)h = 43h (P+B)h	0003h 0000h	Block Protect Status Defines which bits in the Block Protect Status Register section of the Query are implemented. bit 0 Block Protect Status Register Protect/Unprotect bit active (1 = Yes, 0 = No) bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No) bit 15 to 2 Reserved for future use; undefined bits are ‘0’
(P+C)h = 45h	0018h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV
(P+D)h = 46h	00C0h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV
(P+E)h = 47h	0000h	Reserved

Table 24. Burst Read Information

Offset	Data	Description
(P+F)h = 48h	0003h	Page-mode read capability bits 0-7 'n' such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.
(P+10)h = 49h	0003h	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.
(P+11)h = 4Ah	0001h	Synchronous mode read capability configuration 1 bit 3-7 Reserved bit 0-2 'n' such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bit 0-2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.
(P+12)h = 4Bh	0002h	Synchronous mode read capability configuration 2
(P+13)h = 4Ch	0007h	Synchronous mode read capability configuration 3
(P+14)h = 4Dh	0036h	Max operating clock frequency (MHz)
(P+15)h = 4Eh	0001h	Supported handshaking signal ($\overline{WAIT}$ pin) bit 0 during synchronous read (1 = Yes, 0 = No) bit 1 during asynchronous read (1 = Yes, 0 = No)

Table 25. Security Code Area

Offset	Data	Description
81h	XXXX	64 bits: unique device number
82h	XXXX	
83h	XXXX	
84h	XXXX	

Table 26. AC Measurement Conditions

Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V_{DDQ}
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$

Figure 6. Testing Input/Output Waveforms

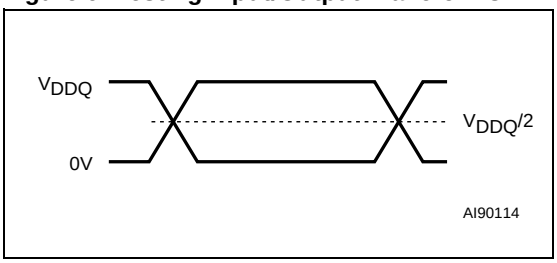


Figure 7. AC Testing Load Circuit

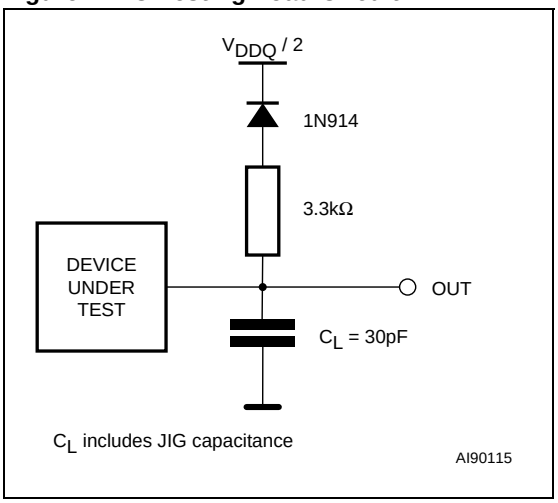


Table 27. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 28. DC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±5	µA
I_{CC1}	Supply Current (Asynchronous Read Mode)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	20	mA
	Supply Current (Synchronous Read Mode Continuous Burst)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 40MHz		20	30	mA
I_{CC2}	Supply Current (Power-down)	$\overline{RP} = V_{SS} \pm 0.2V$		2	10	µA
I_{CC3}	Supply Current (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		15	50	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Word Program, Block Erase in progress		10	20	mA
I_{CC5} (1)	Supply Current (Dual Bank)	Program/Erase in progress in one Bank, Asynchronous Read in the other Bank		20	40	mA
		Program/Erase in progress in one Bank, Synchronous Read in the other Bank		30	50	mA
I_{PP1}	V_{PP} Supply Current (Program or Erase)	V_{PP} = 12V ± 0.6V		5	10	mA
I_{PP2}	V_{PP} Supply Current (Standby or Read)	$V_{PP} \le V_{CC}$		0.2	5	µA
		V_{PP} = 12V ± 0.6V		100	400	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PP} Supply Voltage	Program, Erase	V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{PP2}	V_{PP} Supply Voltage	Double Word Program	11.4		12.6	V

Note: 1. Sampled only, not 100% tested.
2. V_{PP} may be connected to 12V power supply for a total of less than 100 hrs.

Table 29. Asynchronous Read AC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	Test Condition	M59MR032				Unit
				100		120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVLH}	t_{AVAVDH}	Address valid to Latch Enable High	$\overline{G}$ = V_{IH}	10		10		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		45		45	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{ELLH}	t_{ELAVDH}	Chip Enable Low to Latch Enable High	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		25		35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{LHAX}	t_{AVDHAX}	Latch Enable High to Address Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{LHGL}		Latch Enable High to Output Enable Low	$\overline{E}$ = V_{IL}	10		10		ns
t_{LLLH}	$t_{AVDLAVDH}$	Latch Enable Pulse Width	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{LLQV}	t_{AVDLQV}	Latch Enable Low to Output Valid (Random)	$\overline{E}$ = V_{IL}		100		120	ns
t_{LLQV1}		Latch Enable Low to Output Valid (Page)	$\overline{E}$ = V_{IL}		45		45	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 8. Asynchronous Read AC Waveforms

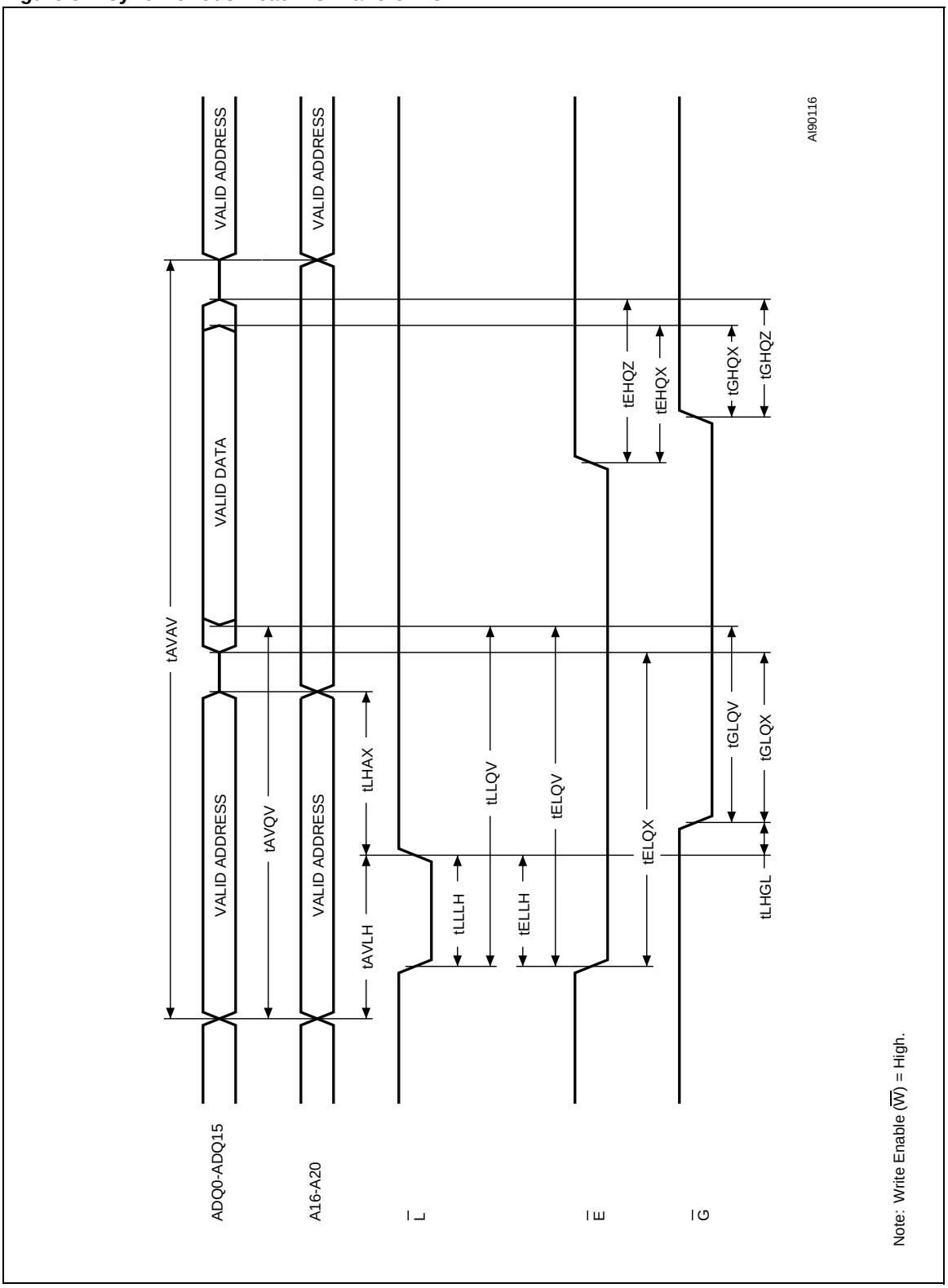


Figure 9. Page Read AC Waveforms

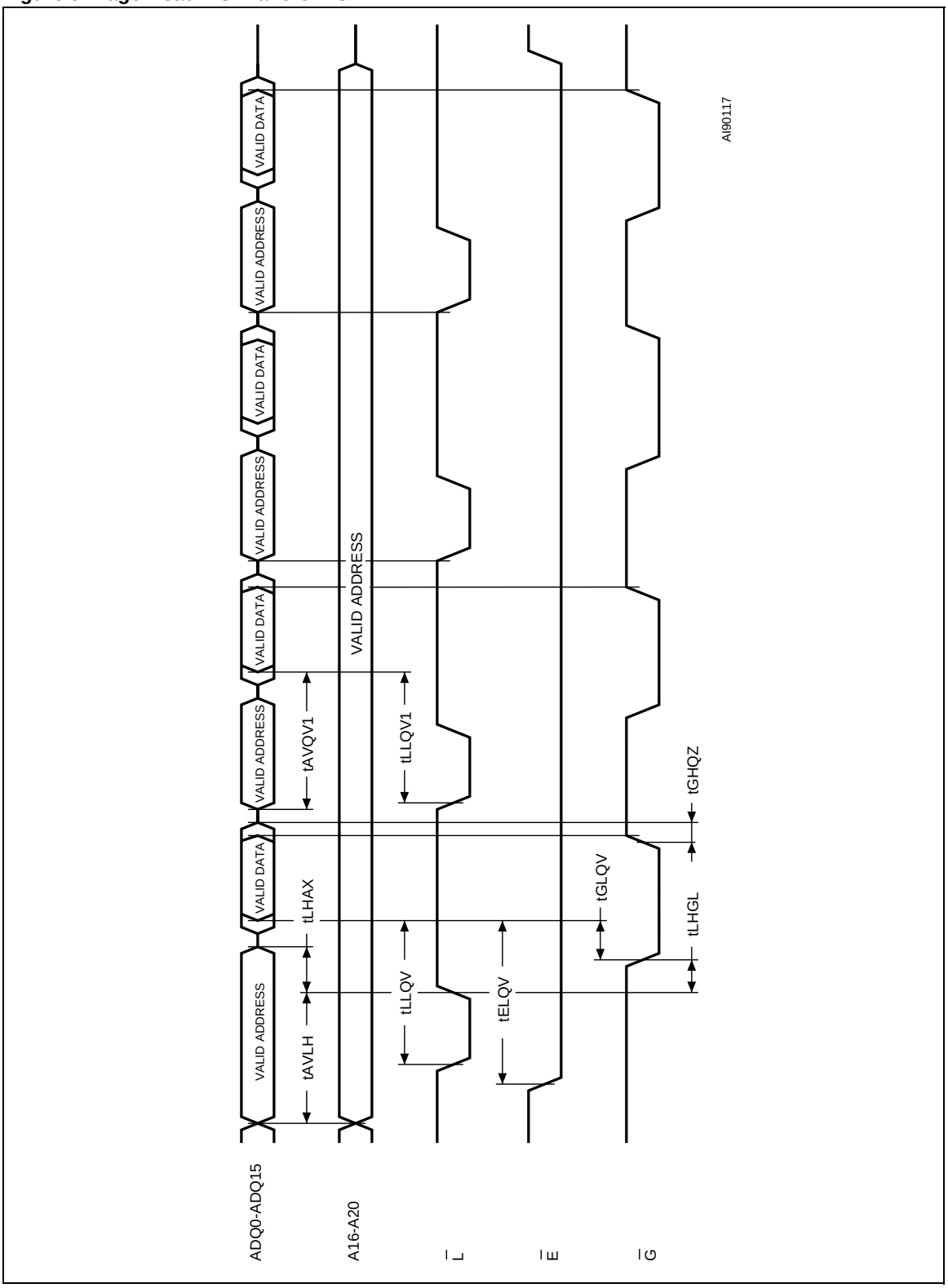
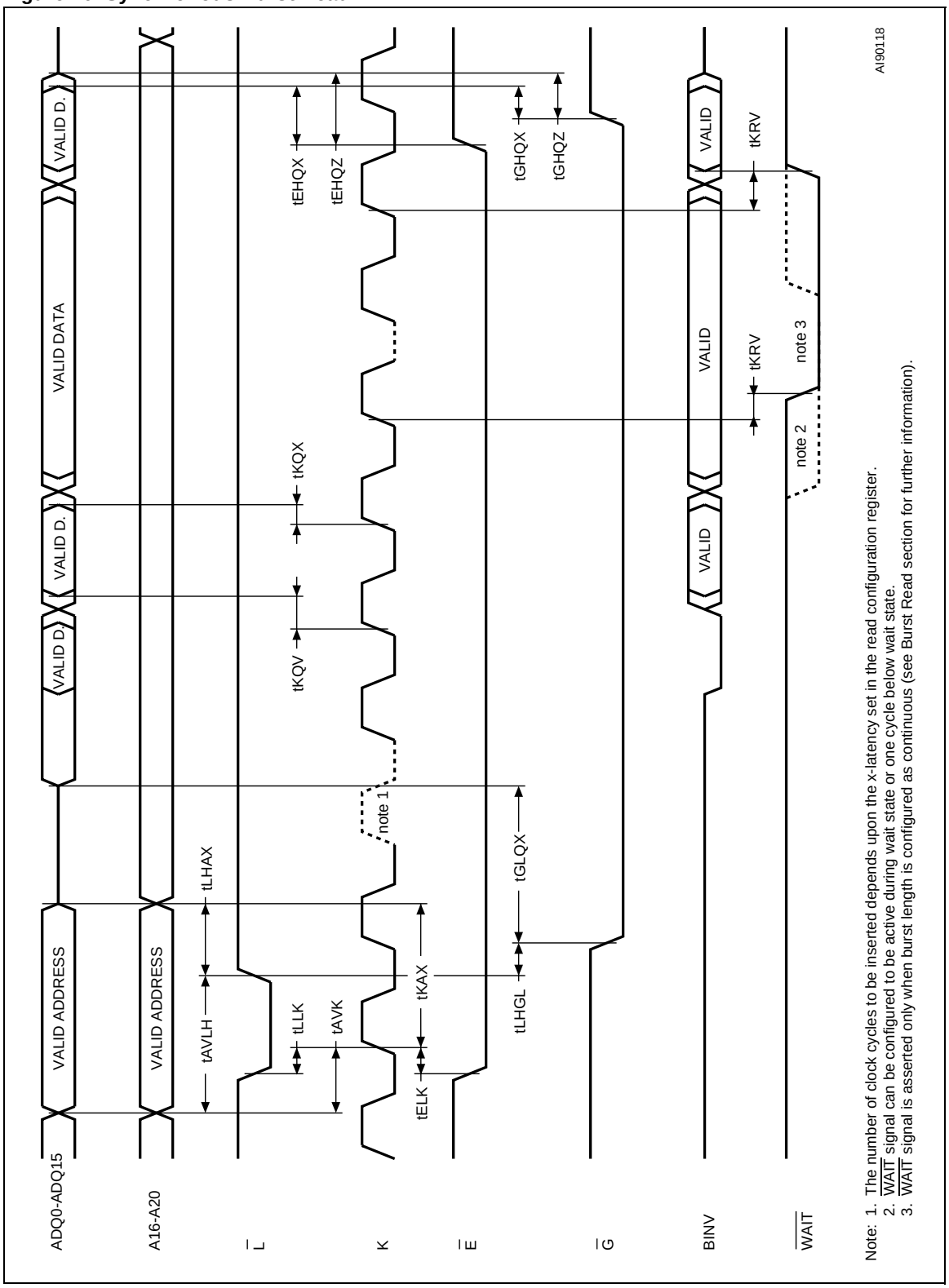


Table 30. Synchronous Burst Read AC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

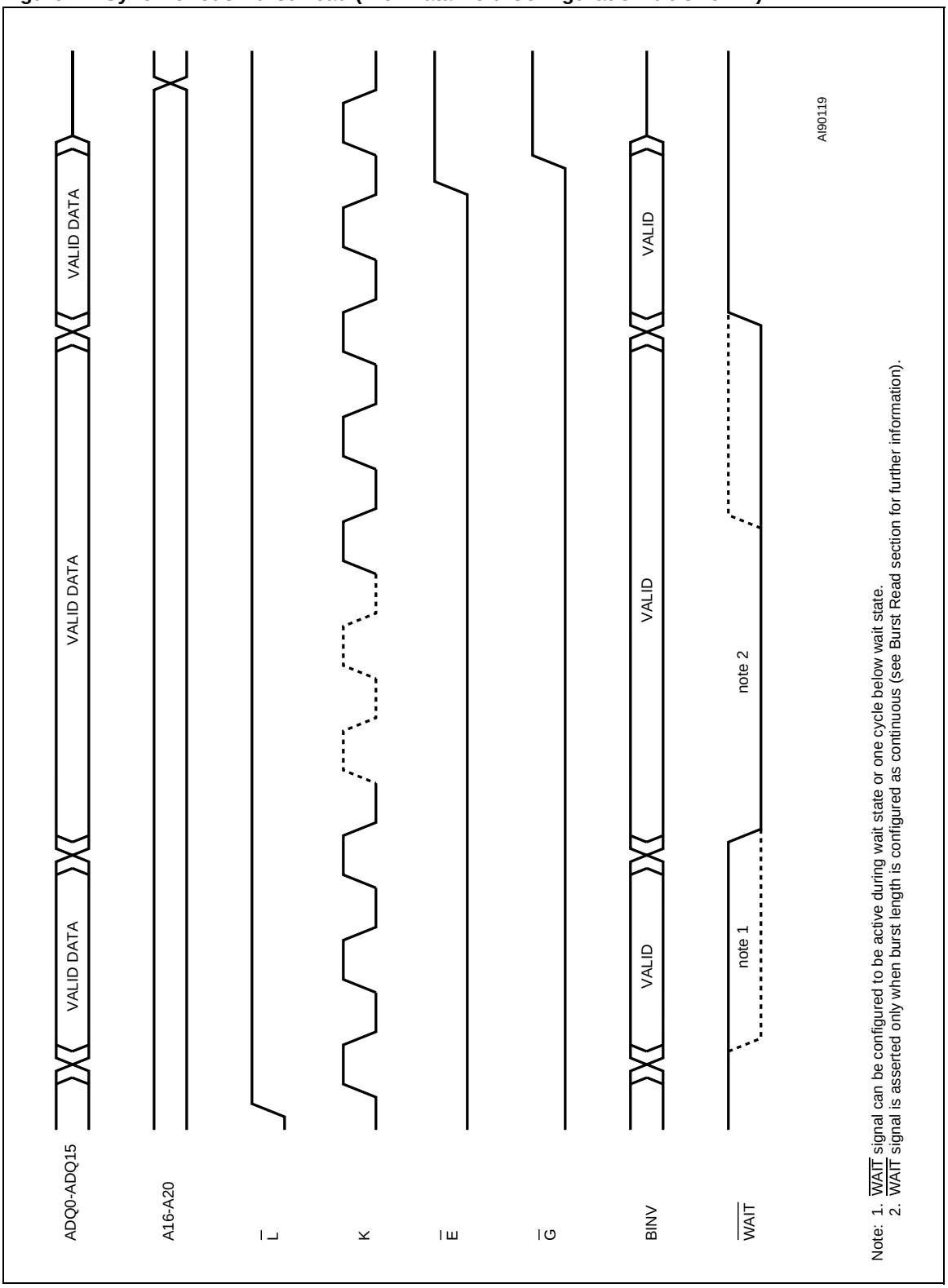
Symbol	Alt	Parameter	Test Condition	M59MR032				Unit
				100		120		
				Min	Max	Min	Max	
t_{AVK}	t_{AVCLKH}	Address Valid to Clock		7		7		ns
t_{ELK}	$t_{CELCLKH}$	Chip Enable Low to Clock		7		7		ns
t_K	t_{CLK}	Clock Period		15		16		ns
t_{KAX}	t_{CLKHAX}	Clock to Address Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{KHKL}	$t_{CLKHCLKL}$	Clock High		5		5		ns
t_{KLKH}	$t_{CLKLCLKH}$	Clock Low		5		5		ns
t_{KRV}	t_{RLCLKH}	Clock to Wait Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		14		18	ns
t_{KRX}	t_{CLKHRX}	Clock to Wait Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	4		4		ns
t_{KQV}	t_{CLKHQV}	Clock to Data Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		14		18	ns
t_{KQX}	t_{CLKHQX}	Clock to Output Transition	$\overline{E}$ = V_{IL}	4		4		ns
t_{LLK}	$t_{AVDLCLKH}$	Latch Enable Low to Clock		7		7		ns

Figure 10. Synchronous Burst Read



Note: 1. The number of clock cycles to be inserted depends upon the x-latency set in the read configuration register.
2. $\overline{WAIT}$ signal can be configured to be active during wait state or one cycle below wait state.
3. $\overline{WAIT}$ signal is asserted only when burst length is configured as continuous (see Burst Read section for further information).

Figure 11. Synchronous Burst Read (with Data Hold Configuration bit CR9 = 1)



Note: 1. WAIT signal can be configured to be active during wait state or one cycle below wait state.
2. WAIT signal is asserted only when burst length is configured as continuous (see Burst Read section for further information).

Table 31. Write AC Characteristics, Write Enable Controlled
(T_A = –40 to 85 °C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	M59MR032				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{GHLL}		Output Enable High to Latch Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	20		20		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		ns
t_{LHWH}		Latch Enable High to Write Enable High	10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		ns
t_{PLQ7V}		$\overline{RP}$ Low to Reset Complete During Program/Erase		15		15	µs
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		µs
t_{VPPHWH}		V_{PP} High to Write Enable High	200		200		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHLL}		Write Enable High to Latch Enable Low	0		0		ns
t_{WHVPPL}		Write Enable High to V_{PP} Low	200		200		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WHWPL}		Write Enable High to Write Protect Low	200		200		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{WPHWH}		Write Protect High to Write Enable High	200		200		ns

Figure 12. Write AC Waveforms, $\overline{W}$ Controlled

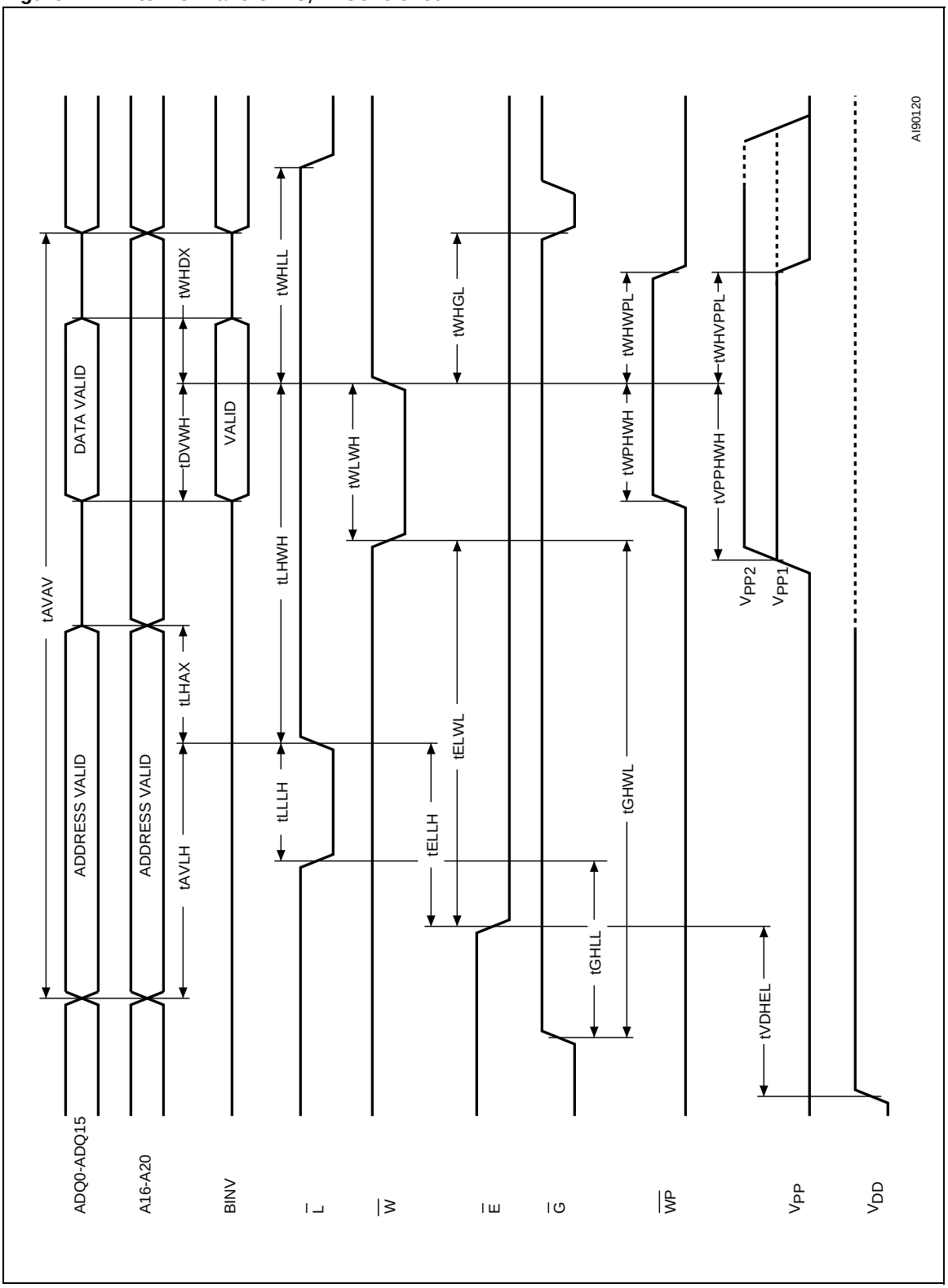


Table 32. Write AC Characteristics, Chip Enable Controlled
(T_A = –40 to 85 °C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	M59MR032				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	70		70		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		ns
t_{GHLL}		Output Enable High to Latch Enable Low	20		20		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		ns
t_{LHEH}		Latch Enable High to Chip Enable High	10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		ns
t_{PLQ7V}		$\overline{RP}$ Low to Reset Complete During Program/Erase		15		15	µs
t_{VDHWL}	t_{VCS}	V_{DD} High to Write Enable Low	50		50		µs
t_{VPPHEH}		V_{PP} High to Chip Enable High	200		200		ns
t_{EHVPPL}		Chip Enable High to V_{PP} Low	200		200		ns
t_{EHWPL}		Chip Enable High to Write Protect Low	200		200		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{WPHEH}		Write Protect High to Chip Enable High	200		200		ns

Figure 13. Write AC Waveforms, $\overline{E}$ Controlled

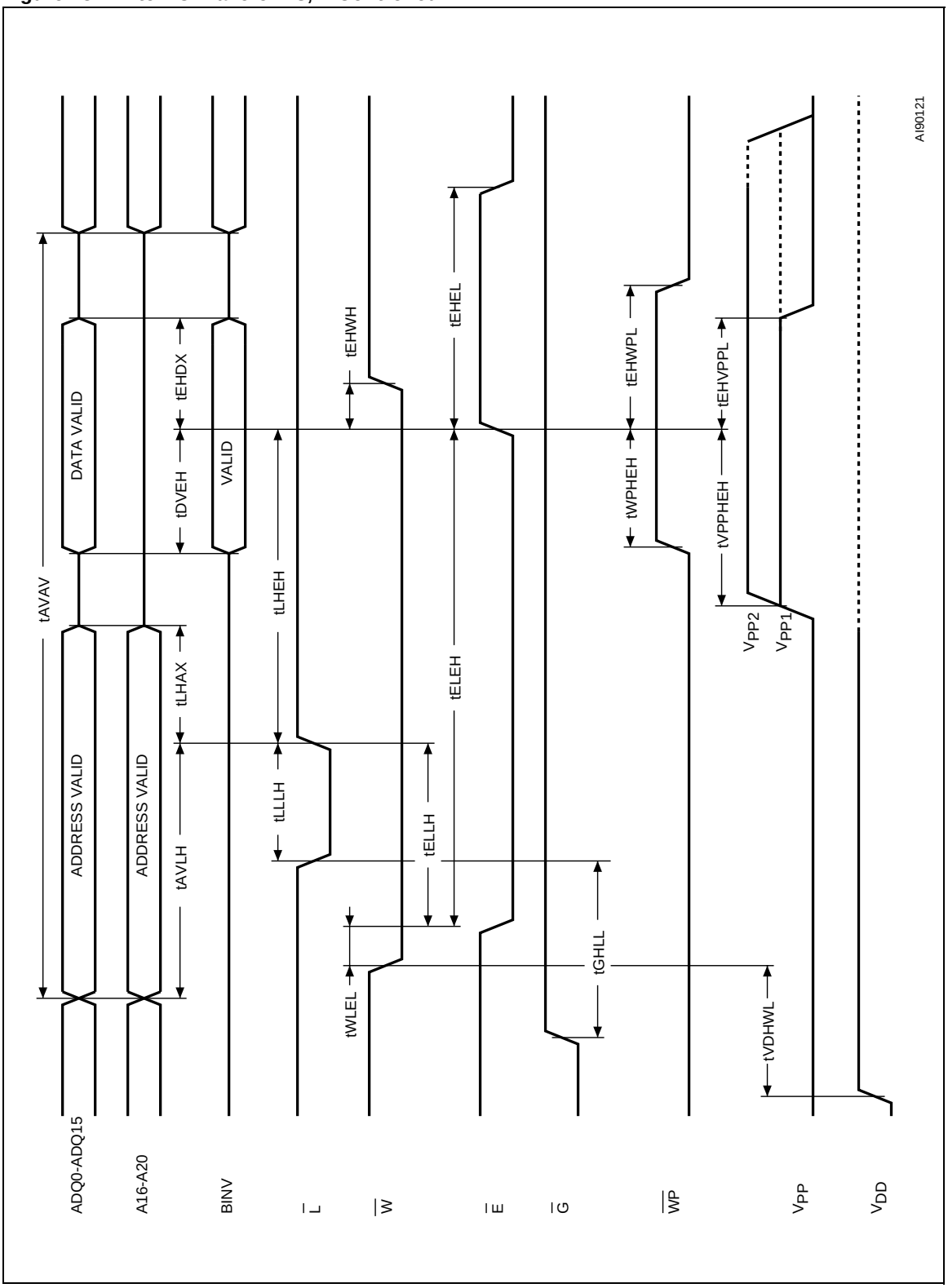


Table 33. Read and Write AC Characteristic, $\overline{RP}$ Related
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	Test Condition	M59MR032				Unit
				100		120		
				Min	Max	Min	Max	
t_{PHQ7V1}		$\overline{RP}$ High to Data Valid (Read Mode)			150		150	ns
t_{PHQ7V2}		$\overline{RP}$ High to Data Valid (Power-down enabled)			50		50	µs
t_{PLPH}	t_{RP}	$\overline{RP}$ Pulse Width		100		100		ns
t_{PLQ7V}		$\overline{RP}$ Low to Reset Complete During Program/Erase			15		15	µs

Figure 14. Read and Write AC Waveforms, $\overline{RP}$ Related

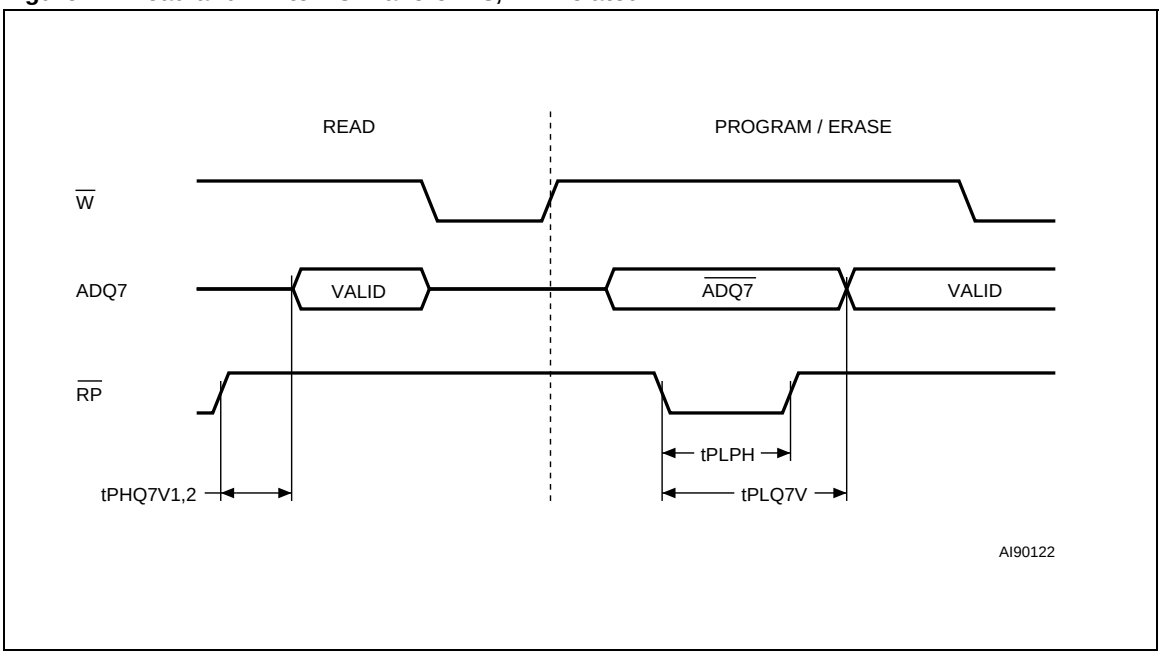


Table 34. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V, V_{PP} = V_{DD} unless otherwise specified)

Parameter	Min	Max (1)	Typ	Typical after 100k W/E Cycles	Unit
Parameter Block (4 KWord) Erase (Preprogrammed)		2.5	0.15	0.4	sec
Main Block (32 KWord) Erase (Preprogrammed)		10	1	3	sec
Bank Erase (Preprogrammed, Bank A)			2	6	sec
Bank Erase (Preprogrammed, Bank B)			10	30	sec
Chip Program (2)			20	25	sec
Chip Program (DPG, V_{PP} = 12V) (2)			10		sec
Word Program (3)		200	10	10	µs
Double Word Program		200	10	10	µs
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. Max values refer to the maximum time allowed by the internal algorithm before error bit is set. Worst case conditions program or erase should perform significantly better.
2. Excludes the time needed to execute the sequence for program instruction.
3. Same timing value if V_{PP} = 12V.

Table 35. Data Polling and Toggle Bits AC Characteristics (1)
(T_A = –40 to 85 °C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Parameter	Min	Max	Unit
t_{EHQ7V}	Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled)	10	200	µs
	Chip Enable High to DQ7 Valid (Block Erase, $\overline{E}$ Controlled)	1.0	10	sec
t_{EHQV}	Chip Enable High to Output Valid (Program)	10	200	µs
	Chip Enable High to Output Valid (Block Erase)	1.0	10	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		0	ns
t_{WHQ7V}	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10	200	µs
	Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled)	1.0	10	sec
t_{WHQV}	Write Enable High to Output Valid (Program)	10	200	µs
	Write Enable High to Output Valid (Block Erase)	1.0	10	sec

Note: 1. All other timings are defined in Read AC Characteristics table.

Figure 15. Data Polling ADQ7 AC Waveforms (when Configuration Register bit CR15 = 1)

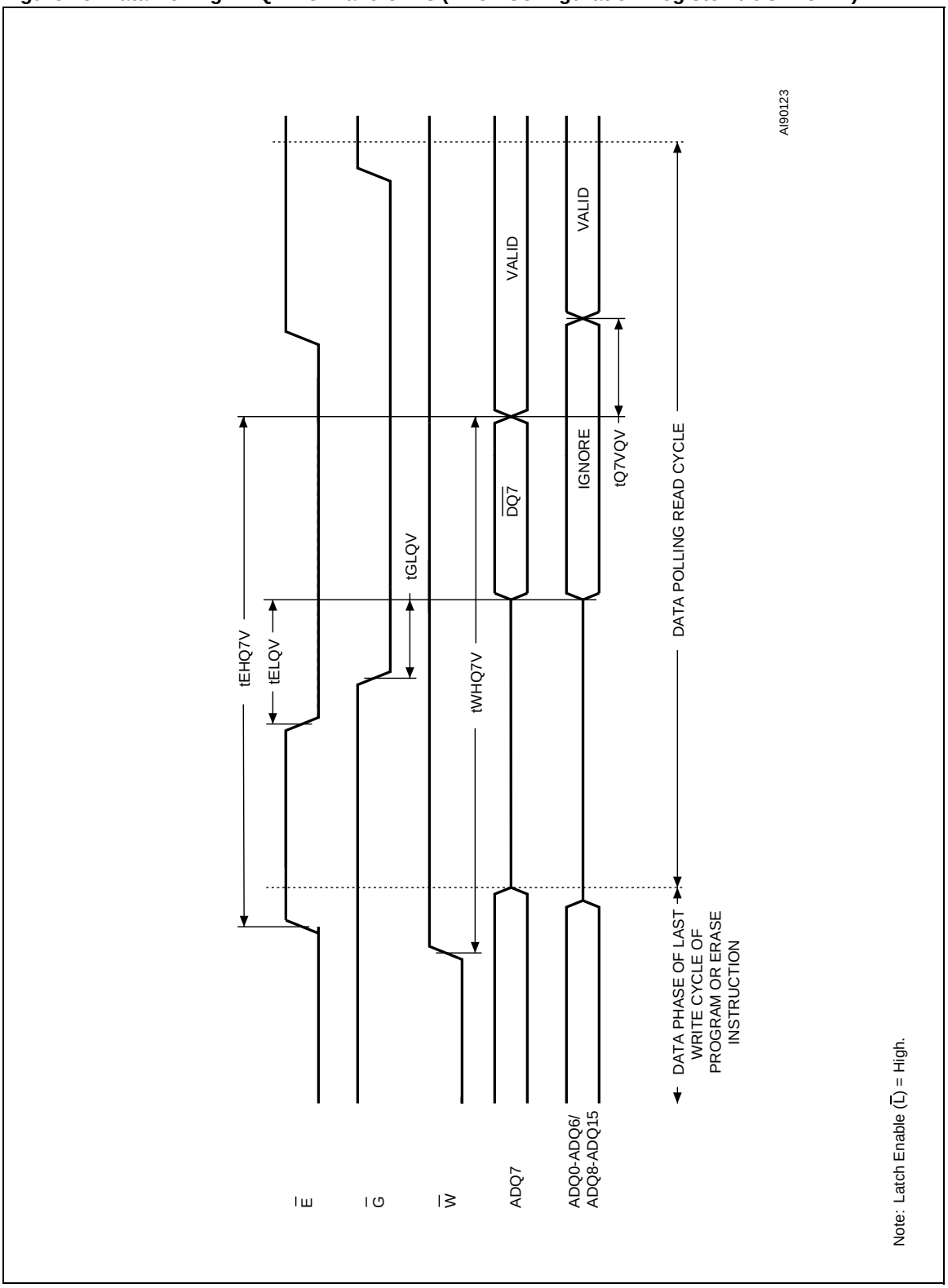


Figure 16. Data Toggle DQ6, DQ2 AC Waveforms (when Configuration Register bit CR15 = 1)

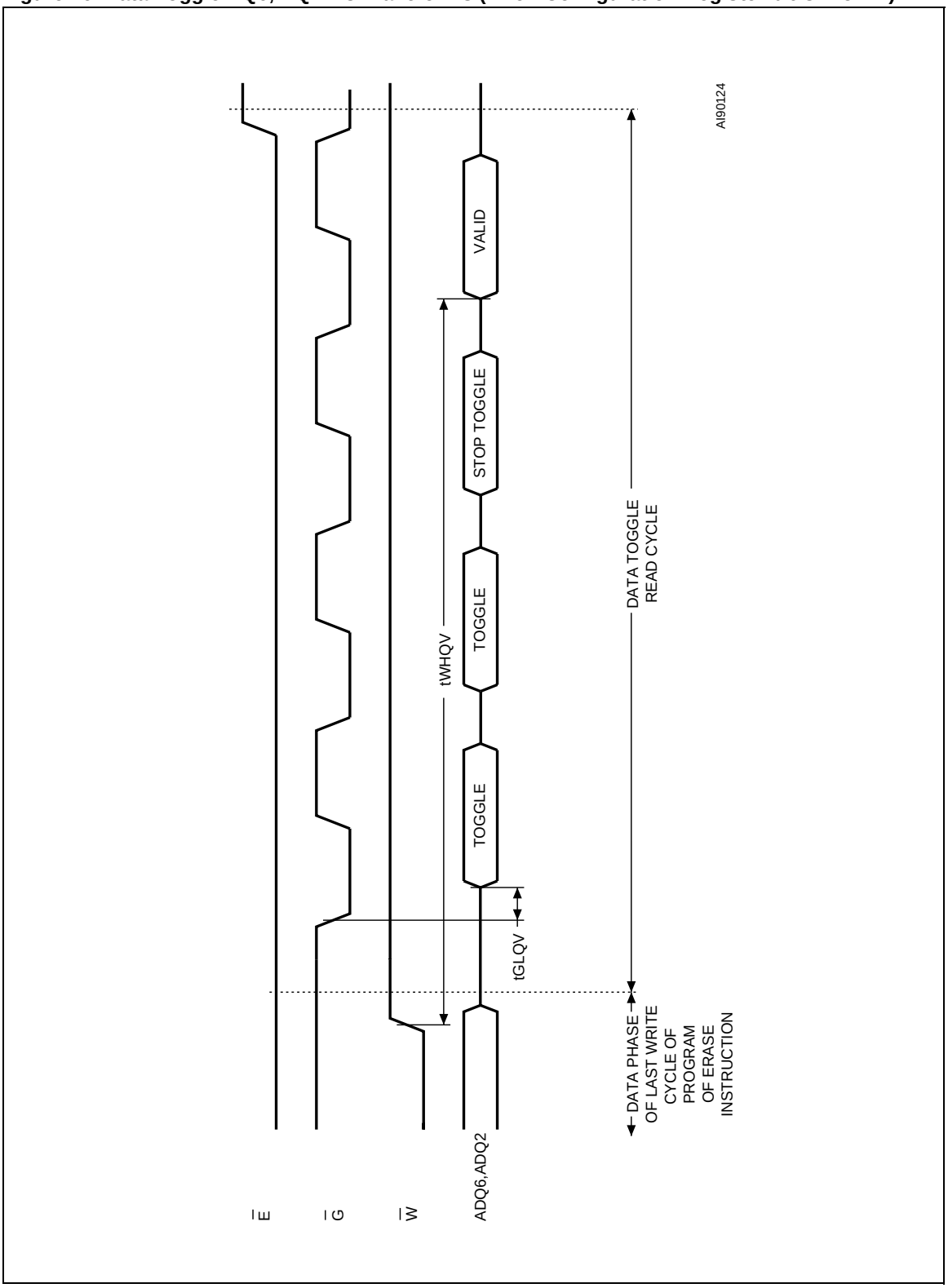


Figure 17. Data Polling Flowchart

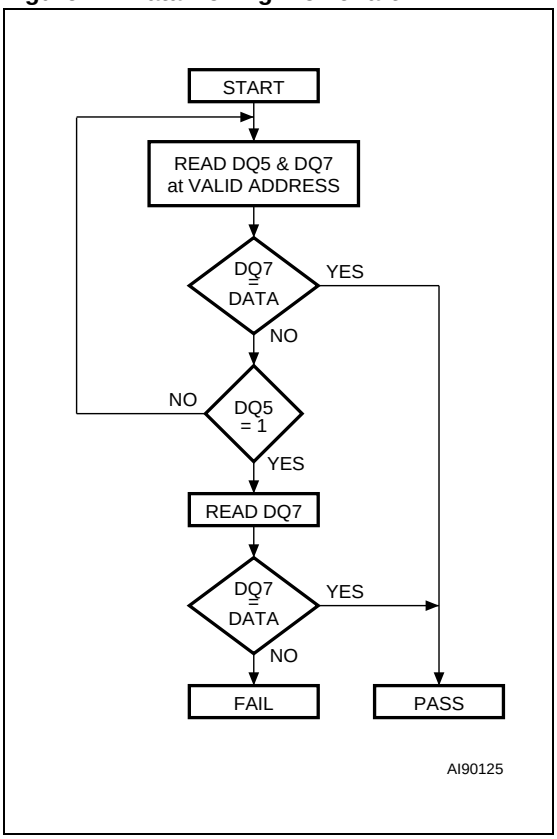


Figure 18. Data Toggle Flowchart

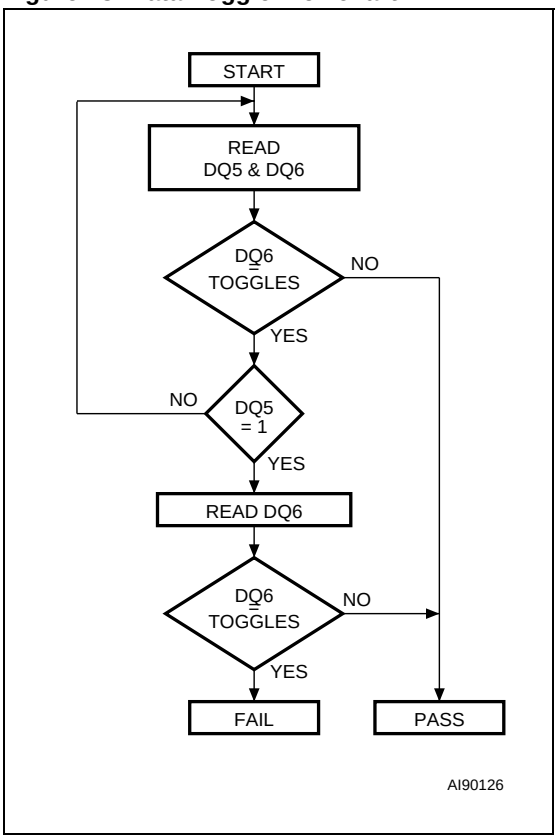


Table 36. Ordering Information Scheme

Example: M59MR032C 100 GC 6 T

Device Type
M59

Architecture
M = Multiplexed Address/Data, Dual Bank, Burst Mode

Operating Voltage
R = 1.8V

Device Function
032C = 32 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Top Boot
032D = 32 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Bottom Boot

Speed
100 = 100 ns
120 = 120 ns

Package
ZC = LFBGA54: 0.5 mm pitch
GC = µBGA46: 0.5 mm pitch

Temperature Range
6 = –40 to 85°C

Option
T = Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to '1'.

Table 37. Daisy Chain Ordering Scheme

Example: M59MR032 -GC T

Device Type
M59MR032

Daisy Chain
-GC = µBGA46: 0.5 mm pitch

Option
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

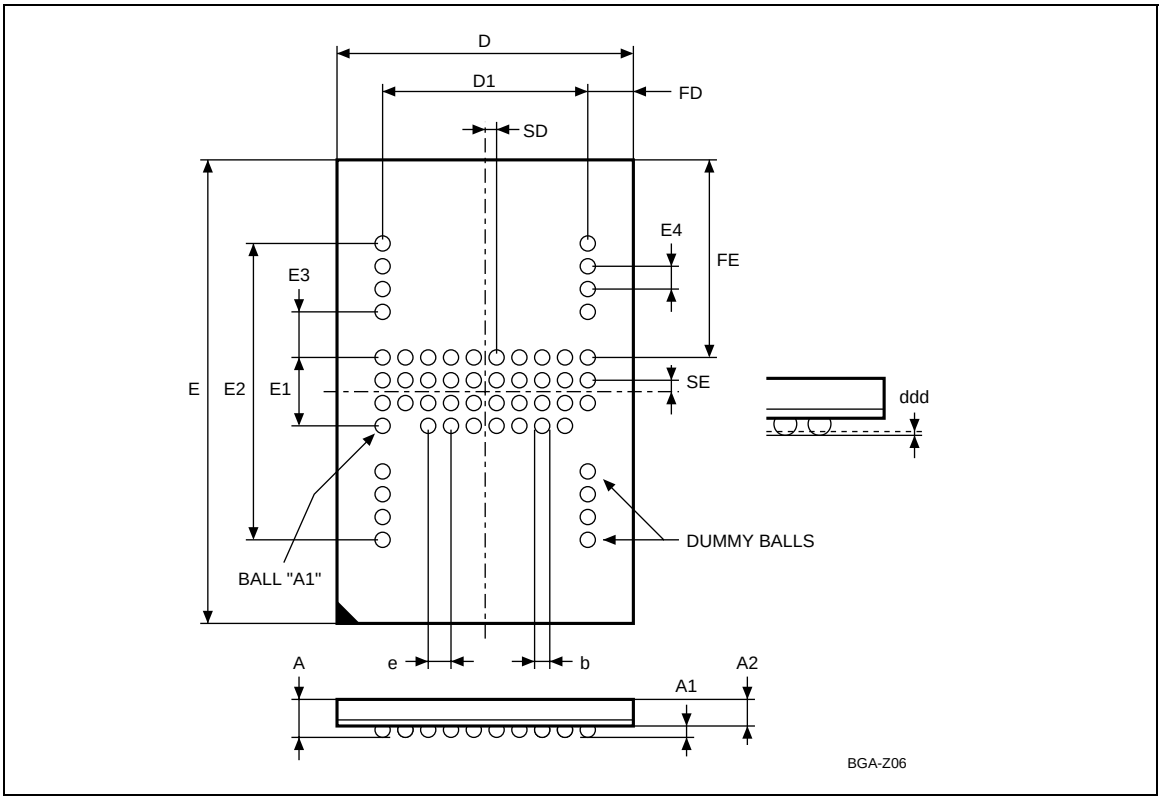
Table 38. Revision History

Date	Version	Revision Details
July 1999	-01	First Issue
12/01/99	-02	FBGA Connections change FBGA Package Mechanical Data and Outline change FBGA Daisy Chain diagrams added µBGA Package added
3/23/00	-03	Document type: from Product Preview to Preliminary Data Bus Invert (BINV) configuration bit clarification Read Operations clarification Status Register clarification LFBGA Package Mechanical Data change µBGA Package Mechanical Data change
5/17/00	-04	µBGA Package Mechanical Data change
9/26/00	-05	CFI Primary Algorithm modified CFI Burst Read modified Write AC Waveforms diagrams change (Figure 12, 13)
12/20/00	-06	Document type: from Preliminary Data to Data Sheet LFBGA Connection change (Figure 2) µBGA Connection change (Figure 3) Program Time clarification (Table 33) LFBGA Package Mechanical Data and Outline change (Table 39, Figure 19) µBGA Package Mechanical Data and Outline change (Table 40, Figure 20)
3/02/01	-07	µBGA Package Mechanical Data and Outline change (Table 40, Figure 20)
3/19/01	-08	µBGA Package Mechanical Data change (Table 40)

Table 39. LFBGA54 - 10 x 4 ball array, 0.5 mm pitch, Package Mechanical Data

		millimeters			inches	
Symbol	**Typ**	**Min**	**Max**	**Typ**	**Min**	**Max**
A	1.100	1.000	1.200	0.0433	0.0394	0.0472
A1	0.150	0.100	0.250	0.0059	0.0039	0.0098
A2	0.950	–	–	0.0374	–	–
b	0.400	0.300	0.450	0.0157	0.0118	0.0177
D	7.000	6.800	7.200	0.2756	0.2677	0.2835
D1	4.500	–	–	0.1772	–	–
ddd			0.150			0.0059
e	0.500	–	–	0.0197	–	–
E	12.000	11.800	12.200	0.4724	0.4646	0.4803
E1	1.500	–	–	0.0591	–	–
E2	6.500	–	–	0.2559	–	–
E3	1.000	–	–	0.0394	–	–
E4	0.500	–	–	0.0197	–	–
FD	1.250	–	–	0.0492	–	–
FE	5.250	–	–	0.2067	–	–
SD	0.250	–	–	0.0098	–	–
SE	0.250	–	–	0.0098	–	–

Figure 19. LFBGA54 - 10 x 4 ball array, 0.5 mm pitch, Bottom View Package Outline

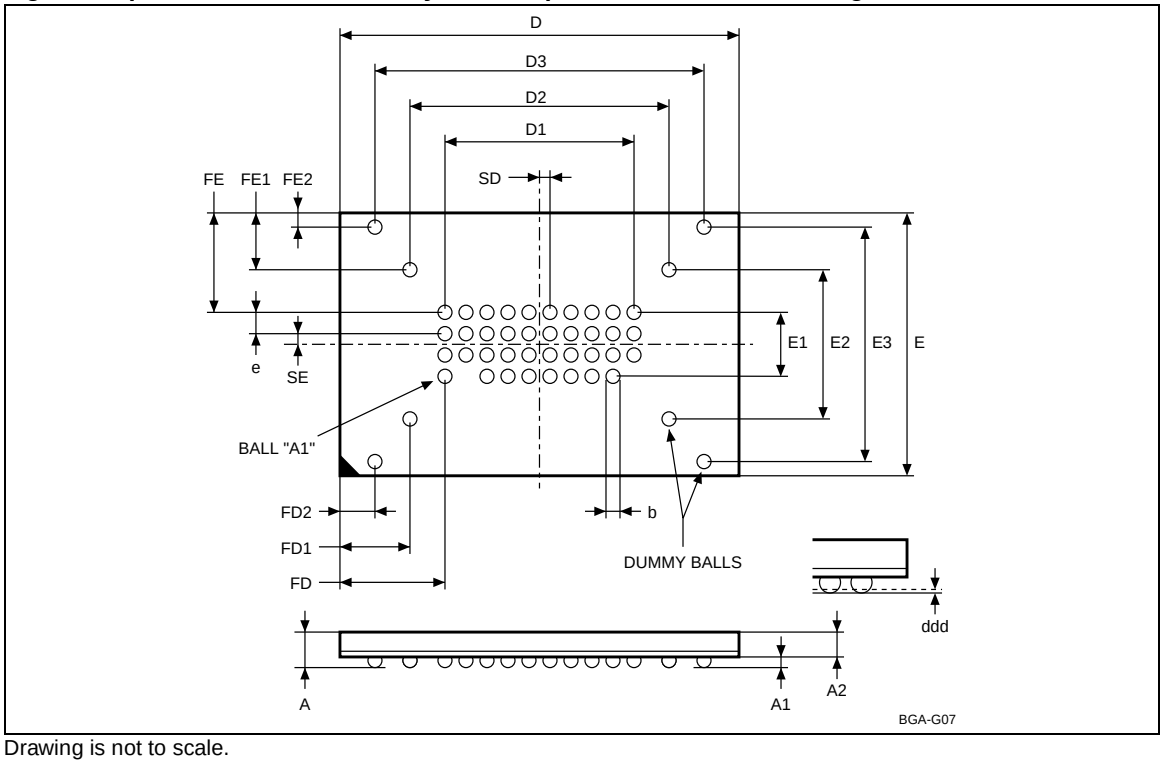


Drawing is not to scale.

Table 40. µBGA46 - 10 x 4 ball array, 0.5 mm pitch, Package Mechanical Data

		millimeters			inches	
Symbol	Typ	Min	Max	Typ	Min	Max
A			1.000			0.0394
A1		0.150			0.0059	
A2	0.700			0.0276		
b	0.320	0.250	0.400	0.0126	0.0098	0.0157
D	10.530	10.480	10.580	0.4146	0.4126	0.4165
D1	4.500	–	–	0.1772	–	–
D2	6.500	–	–	0.2559	–	–
D3	8.500	–	–	0.3346	–	–
ddd			0.080			0.0031
e	0.500	–	–	0.0197	–	–
E	6.290	6.240	6.340	0.2476	0.2457	0.2496
E1	1.500	–	–	0.0591	–	–
E2	3.500	–	–	0.1378	–	–
E3	5.500	–	–	0.2165	–	–
FD	3.015	–	–	0.1187	–	–
FD1	2.015	–	–	0.0793	–	–
FD2	1.015	–	–	0.0400	–	–
FE	2.395	–	–	0.0943	–	–
FE1	1.395	–	–	0.0549	–	–
FE2	0.395	–	–	0.0156	–	–
SD	0.250	–	–	0.0098	–	–
SE	0.250	–	–	0.0098	–	–

Figure 20. µBGA46 - 10 x 4 ball array, 0.5 mm pitch, Bottom View Package Outline



Drawing is not to scale.

Figure 21. µBGA46 Daisy Chain - Package Connections (Top view through package)

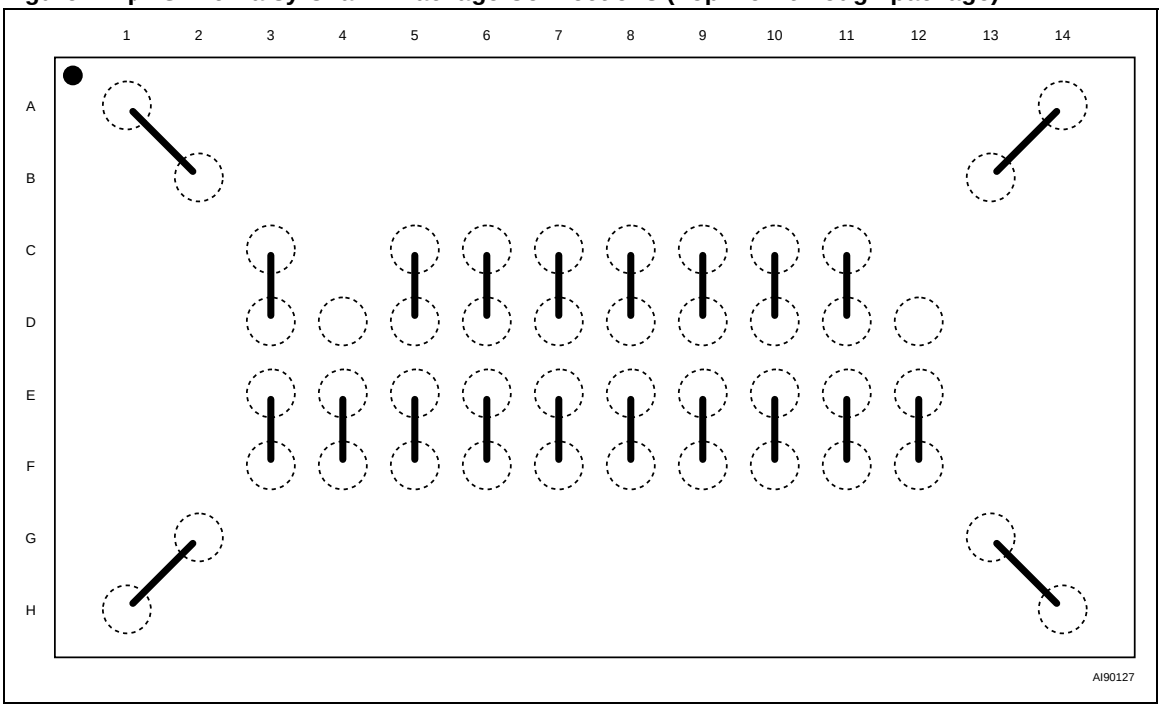


Figure 22. µBGA46 Daisy Chain - PCB Connections proposal (Top view through package)