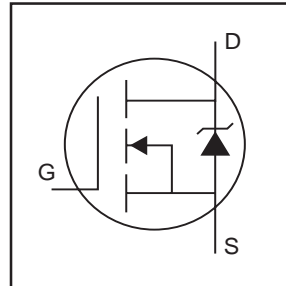


FA57SA50LC

HEXFET® Power MOSFET

- Fully Isolated Package
- Easy to Use and Parallel
- Low On-Resistance
- Dynamic dv/dt Rating
- Fully Avalanche Rated
- Simple Drive Requirements
- Low Gate Charge Device
- Low Drain to Case Capacitance
- Low Internal Inductance

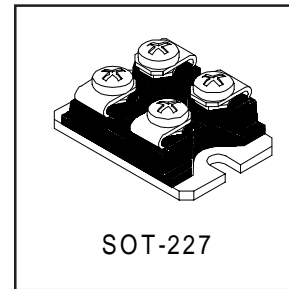


$V_{DSS} = 500V$
$R_{DS(on)} = 0.08\Omega$
$I_D = 57A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 500 watts. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	57	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	36	
I_{DM}	Pulsed Drain Current ①	228	
$P_D @ T_C = 25^\circ C$	Power Dissipation	625	W
	Linear Derating Factor	5.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	725	mJ
I_{AR}	Avalanche Current③	57	A
E_{AR}	Repetitive Avalanche Energy④	62.5	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	3.0	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T_{STG}			
V_{ISO}	Insulation Withstand Voltage (AC-RMS)	2.5	kV
	Mounting torque, M4 screw	1.3	N•m

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.20	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.05	—	

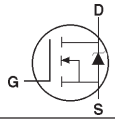
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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.62	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.08	Ω	V _{GS} = 10V, I _D = 34A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	43	—	—	S	V _{DS} = 50V, I _D = 34A
I _{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	V _{DS} = 500V, V _{GS} = 0V
		—	—	500		V _{DS} = 400V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	225	338	nC	I _D = 57A
Q _{gs}	Gate-to-Source Charge	—	51	77		V _{DS} = 400V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	98	147		V _{GS} = 10V, See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	32	—	ns	V _{DD} = 250V
t _r	Rise Time	—	152	—		I _D = 57A
t _{d(off)}	Turn-Off Delay Time	—	108	—		R _G = 2.0Ω (Internal)
t _f	Fall Time	—	118	—		R _D = 4.3Ω, See Fig. 10 ④
L _s	Internal Source Inductance	—	5.0	—	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	—	10000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1500	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	50	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	57	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	228		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 57A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	901	1351	ns	T _J = 25°C, I _F = 57A
Q _{rr}	Reverse Recovery Charge	—	15	23	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 446μH
R_G = 25Ω, I_{AS} = 57A. (See Figure 12)
- ③ I_{SD} ≤ 57A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

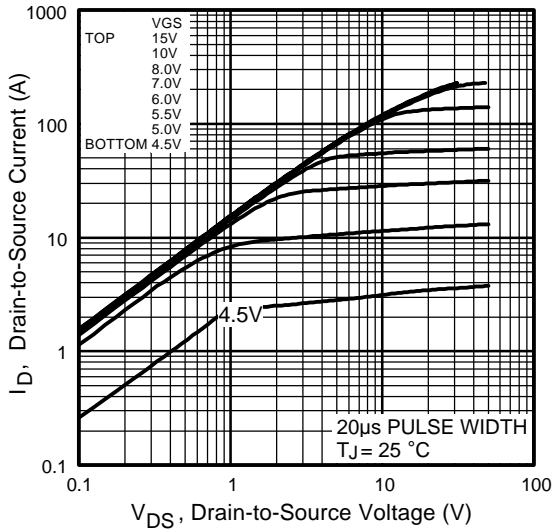


Fig 1. Typical Output Characteristics

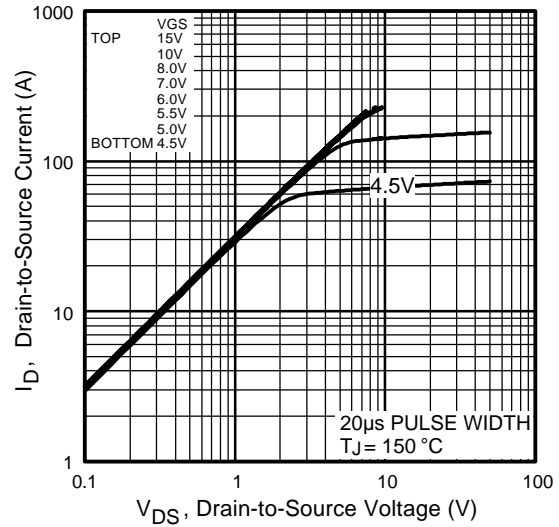


Fig 2. Typical Output Characteristics

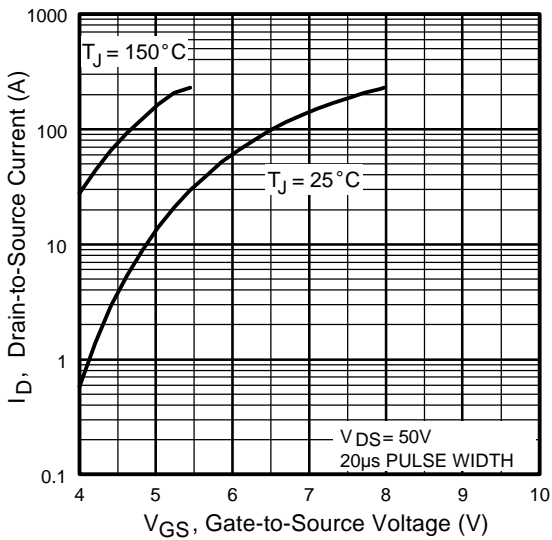


Fig 3. Typical Transfer Characteristics

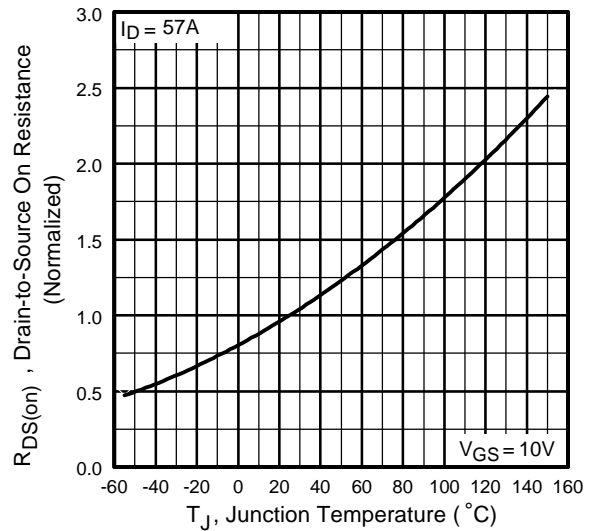


Fig 4. Normalized On-Resistance Vs. Temperature

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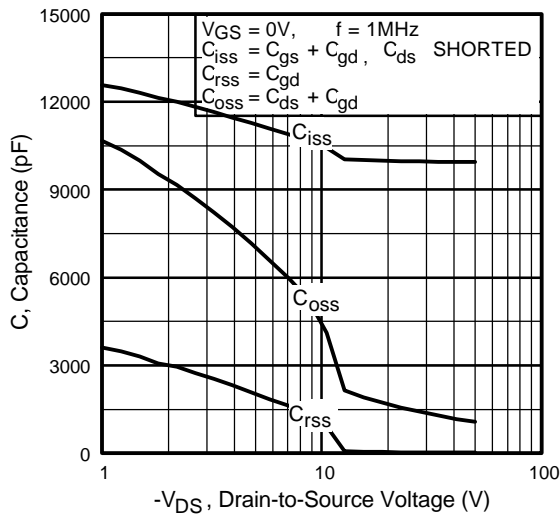


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

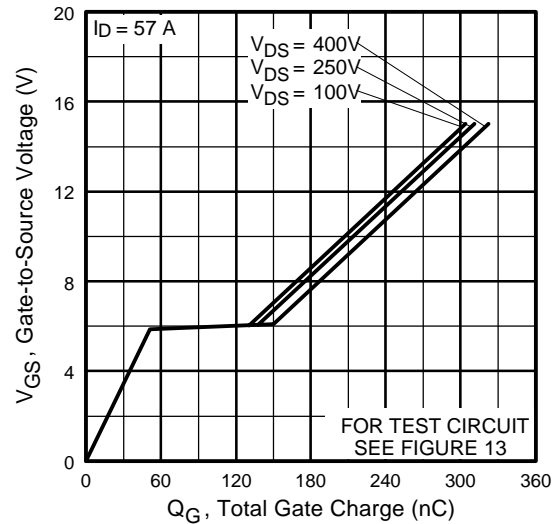


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

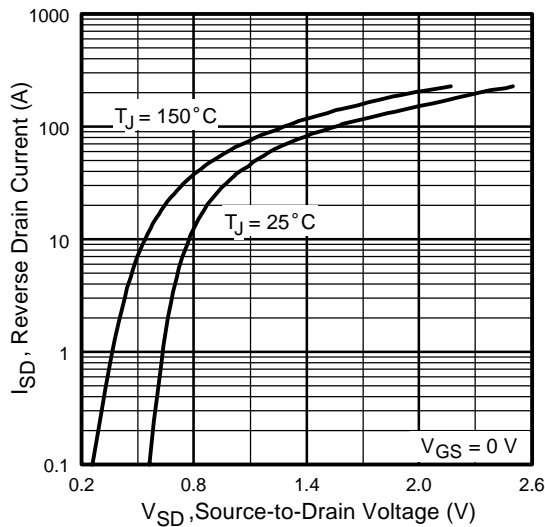


Fig 7. Typical Source-Drain Diode Forward Voltage

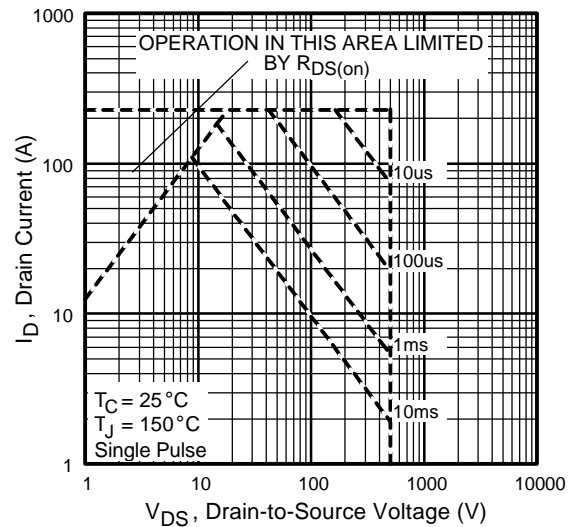


Fig 8. Maximum Safe Operating Area

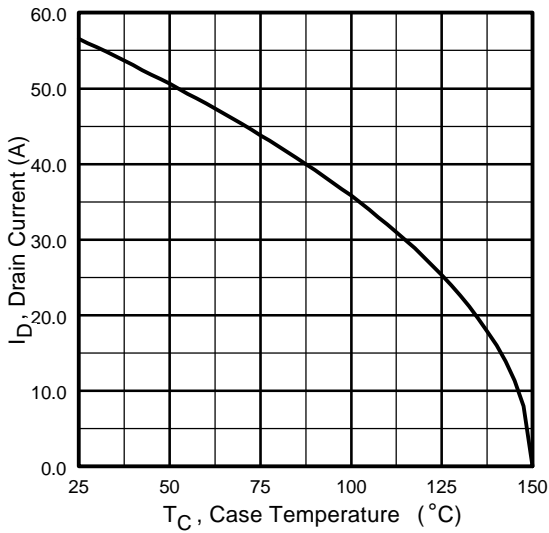


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

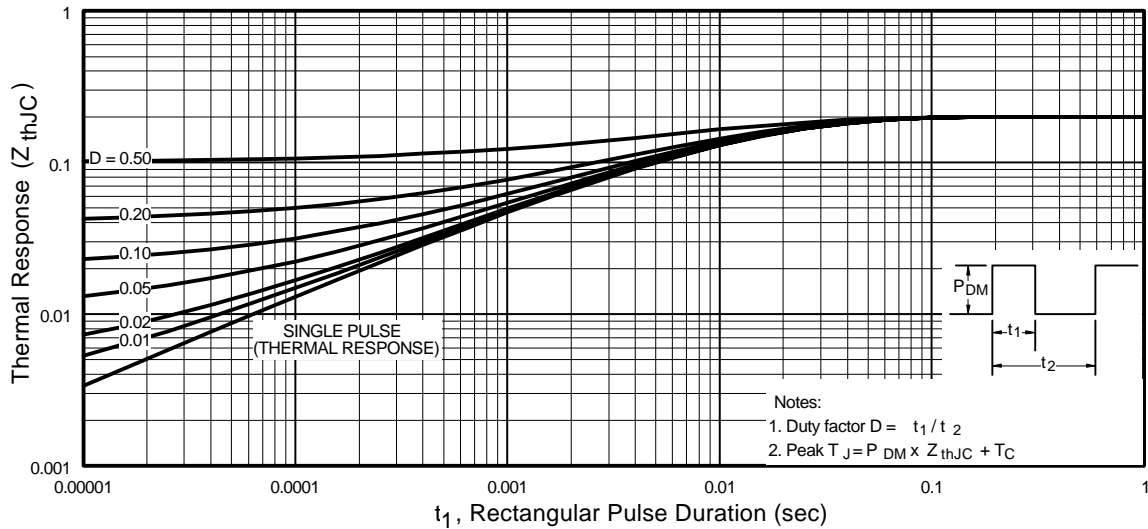


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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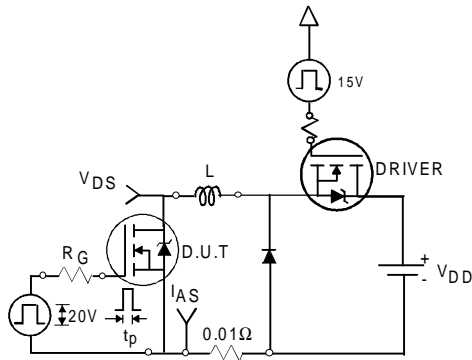


Fig 12a. Unclamped Inductive Test Circuit

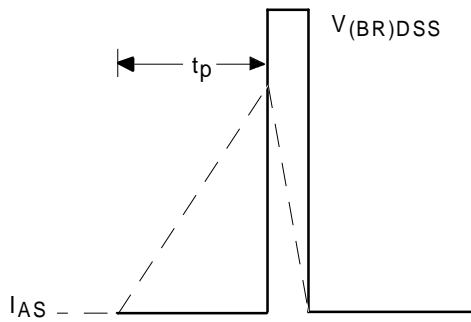


Fig 12b. Unclamped Inductive Waveforms

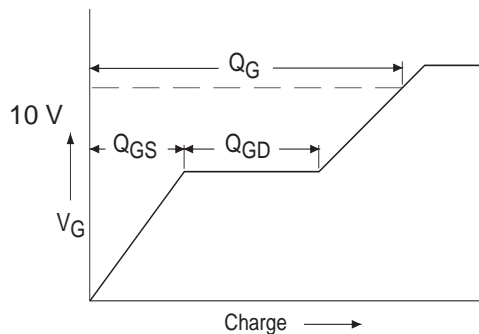


Fig 13a. Basic Gate Charge Waveform

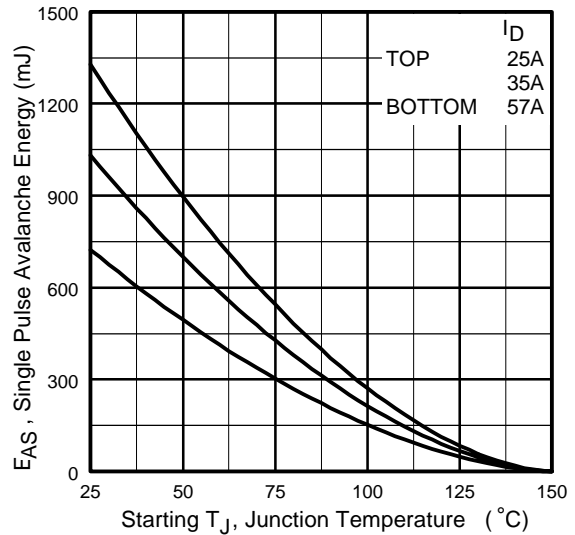


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

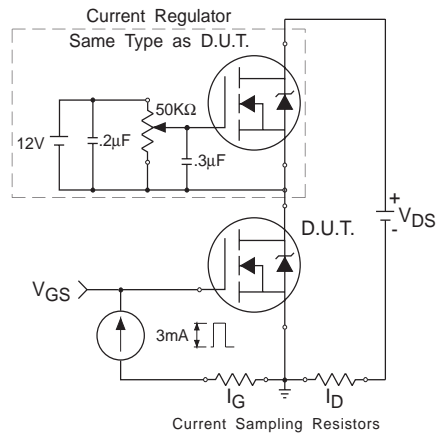
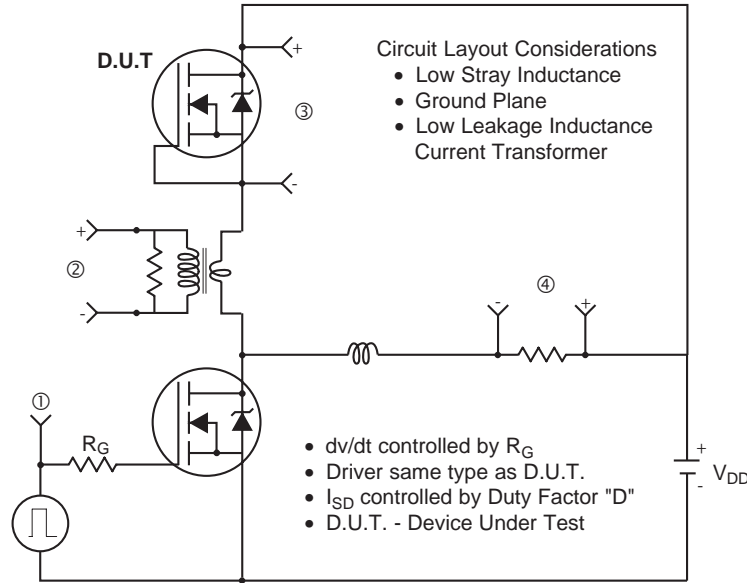


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



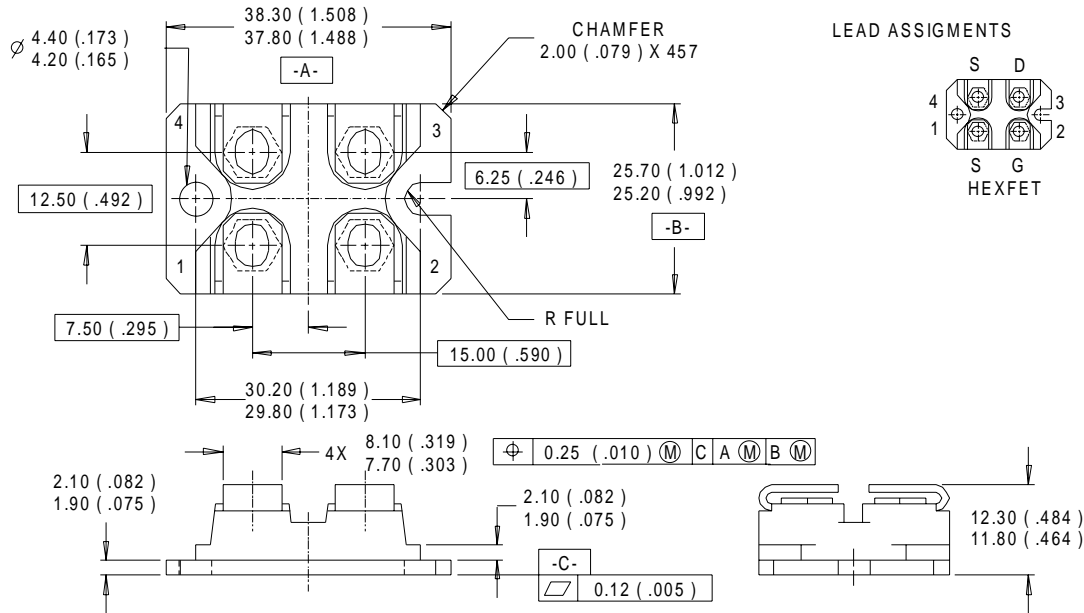
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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SOT-227 Package Details



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