

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ)
30	0.0040 @ $V_{GS} = 10$ V	25	47
	0.0048 @ $V_{GS} = 4.5$ V	23	

### FEATURES

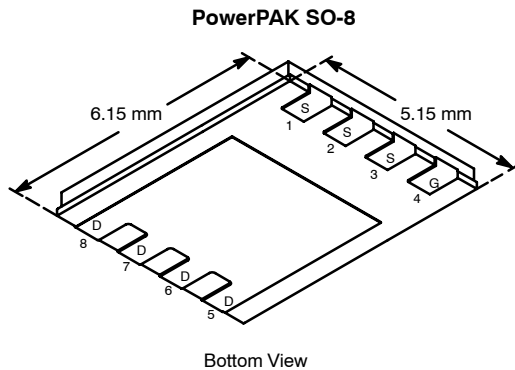
- TrenchFET® Power MOSFET
- Optimized for “Low Side” Synchronous Rectifier Operation
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100%  $R_g$  Tested



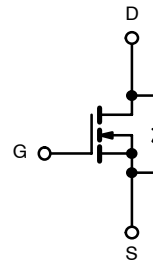
**RoHS**  
COMPLIANT  
Available

### APPLICATIONS

- DC/DC Converters
- Synchronous Rectifiers



Ordering Information: Si7886ADP-T1  
Si7886ADP-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	25	15	A
		$T_A = 70^\circ\text{C}$	20	12	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)	$I_{DM}$	60			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	4.5	1.6		
Avalanche Current	$I_{AS}$	50			
Single Pulse Avalanche Energy	$E_{AS}$	125		mJ	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	18	23	$^\circ\text{C}/\text{W}$
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.0	1.5		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

### SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)

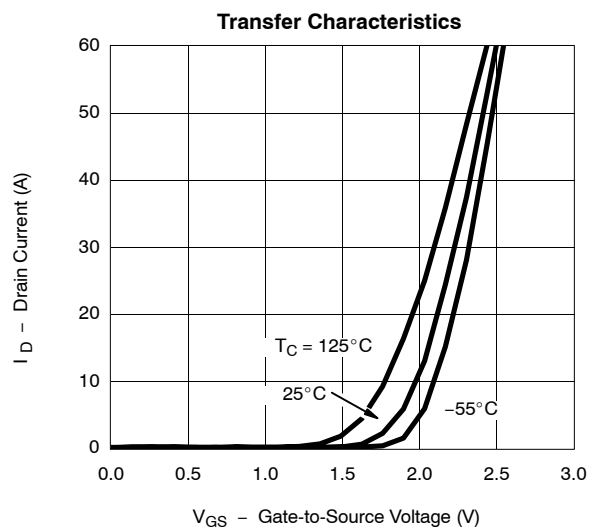
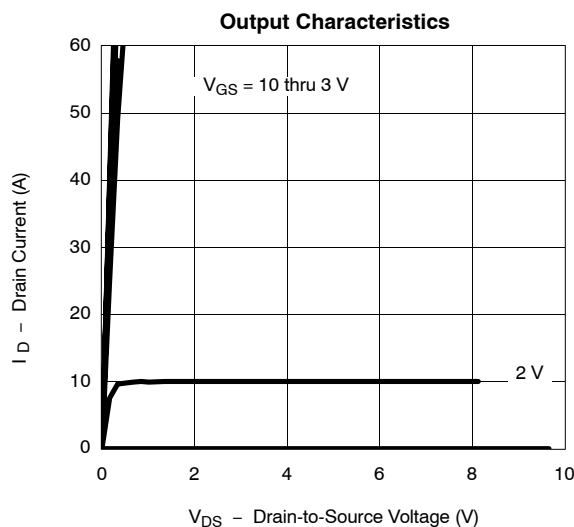
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.6	1	1.5	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		0.0032	0.0040	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 23 A		0.0037	0.0048	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		90		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.9 A, V <sub>GS</sub> = 0 V		0.7	1.1	V
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>SS</sub> = 0 V, f = 1 kHz		6450		pF
Output Capacitance	C <sub>oss</sub>			873		
Reverse Transfer Capacitance	C <sub>rss</sub>			402		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 25 A		47	60	nC
Gate-Source Charge	Q <sub>gs</sub>			12.5		
Gate-Drain Charge	Q <sub>gd</sub>			9.0		
Gate Resistance	R <sub>g</sub>		0.5	1.0	1.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 6 Ω		17	30	ns
Rise Time	t <sub>r</sub>			14	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			158	230	
Fall Time	t <sub>f</sub>			43	65	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 2.9 A, di/dt = 100 A/μs		50	

**Notes**

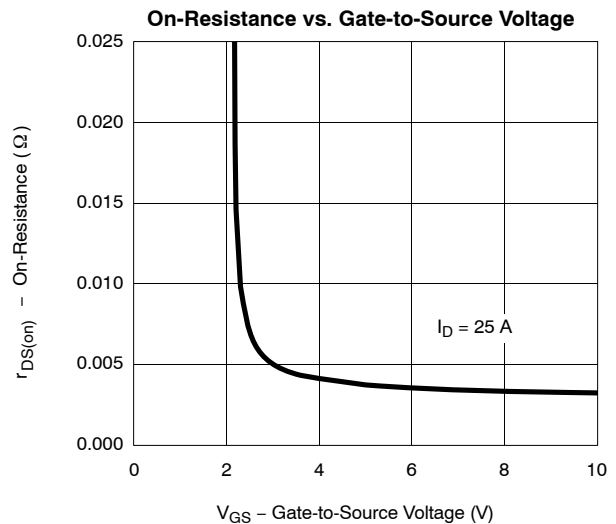
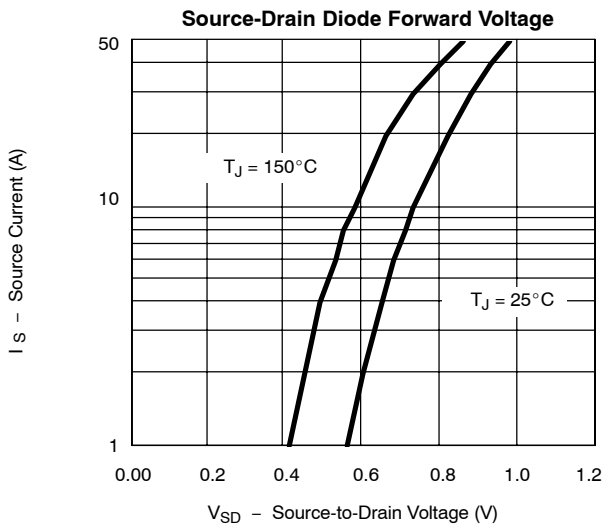
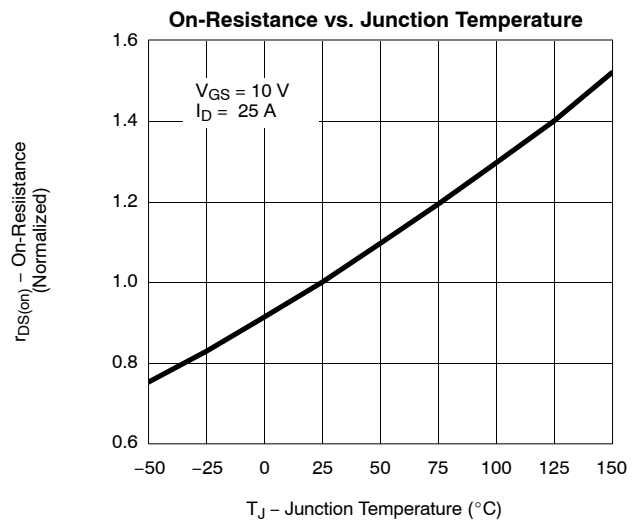
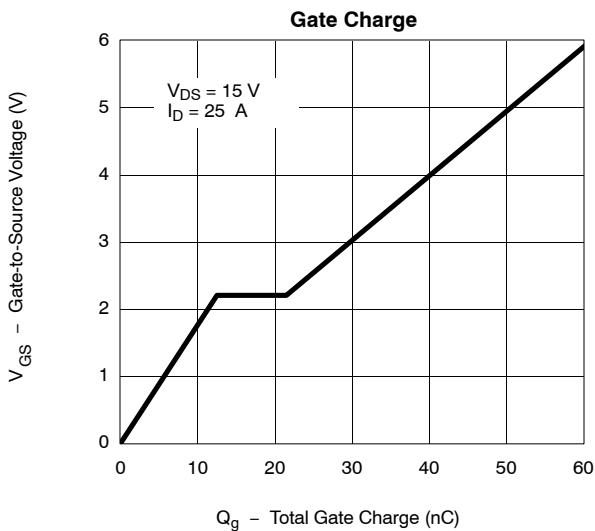
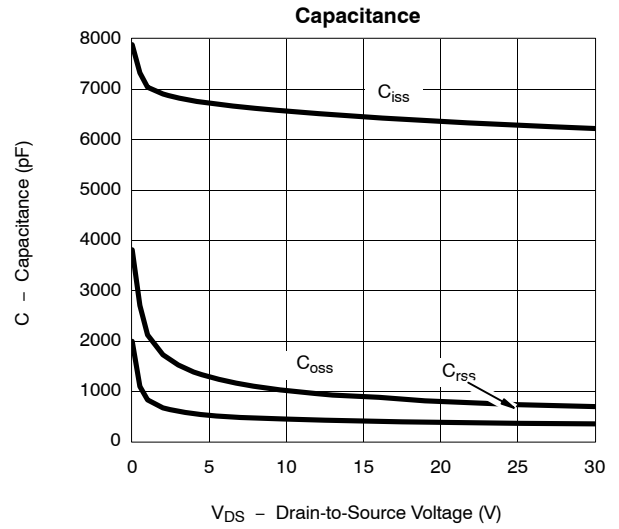
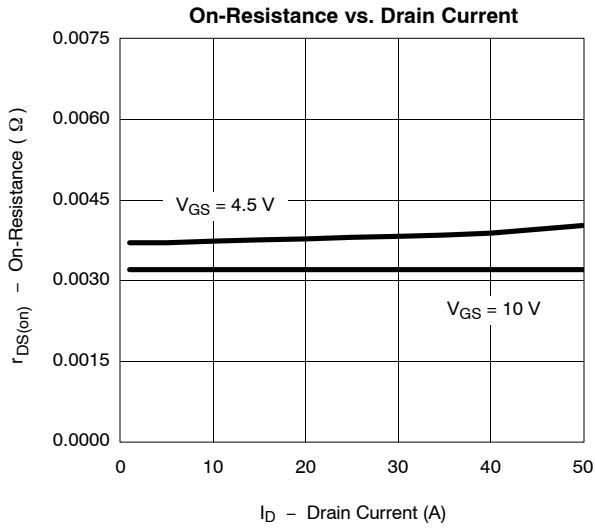
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

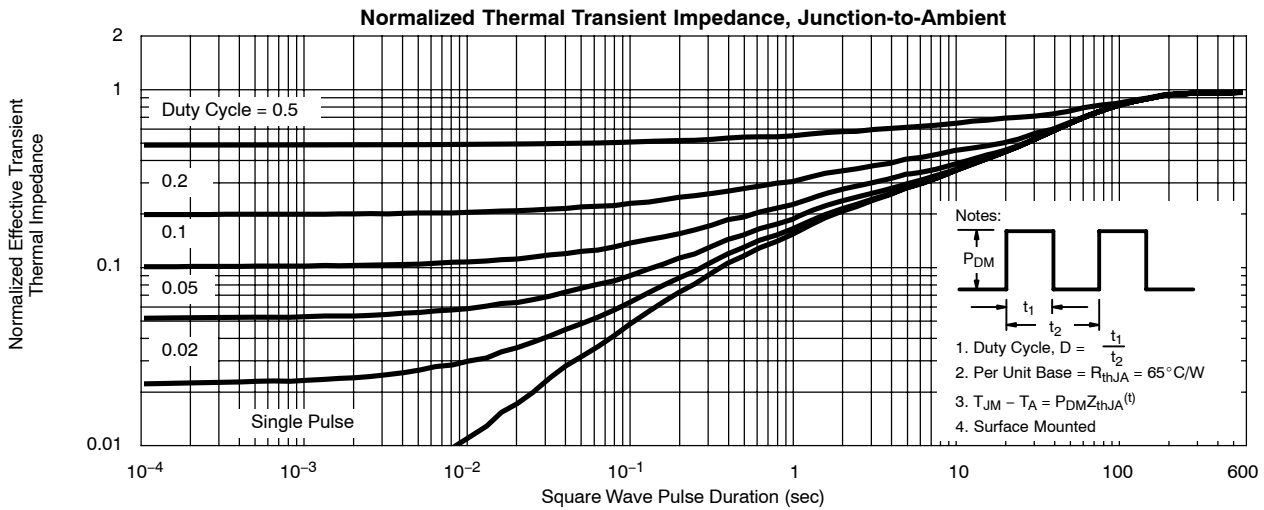
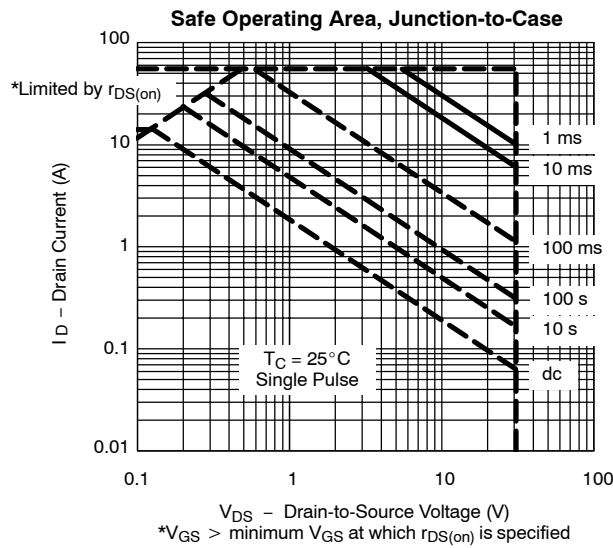
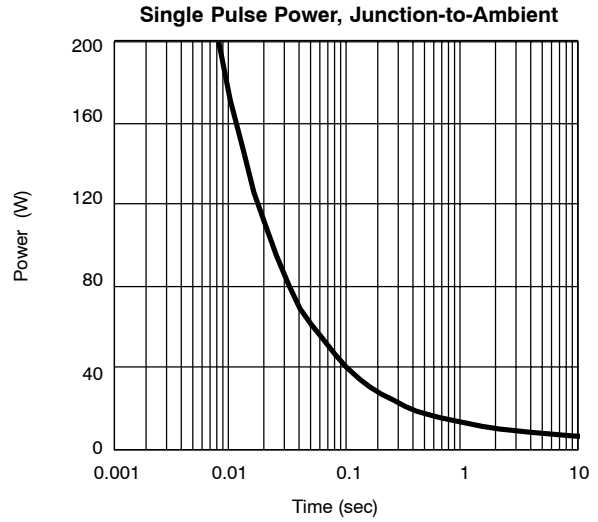
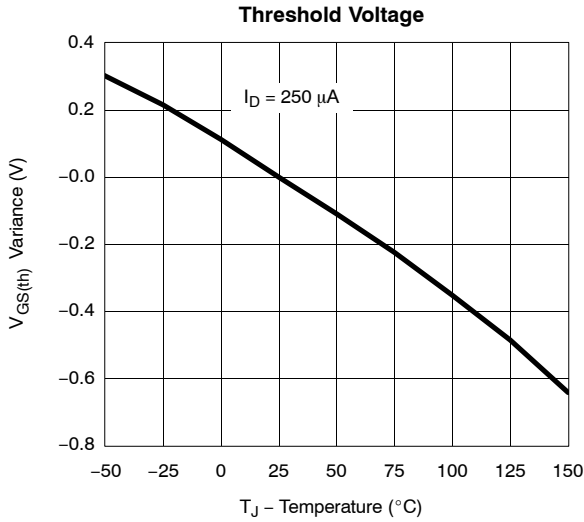
### TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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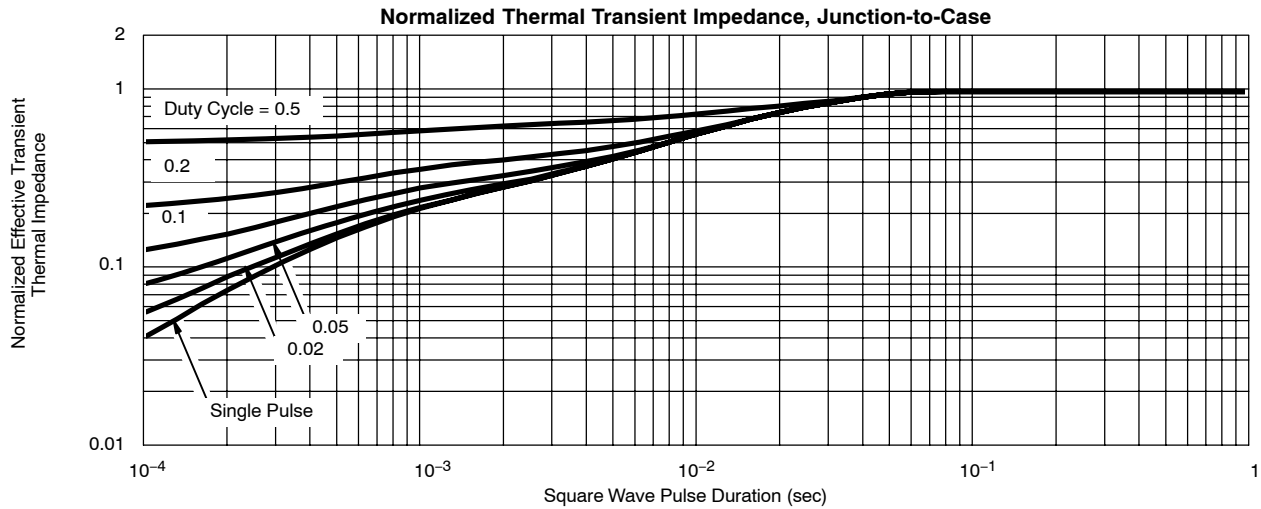


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73156>.