

## 74F164A Serial-In, Parallel-Out Shift Register

### General Description

The 74F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 74F164A is a faster version of the 74F164.

### Features

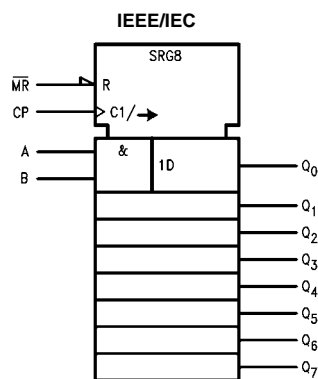
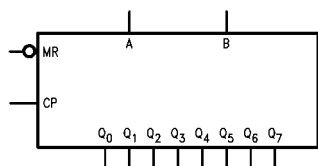
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 74F164A is a faster version of the 74F164

### Ordering Code:

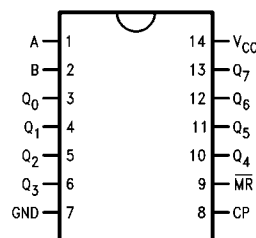
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74F164ASC    | M14A           | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| 74F164ASJ    | M14D           | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74F164APC    | N14A           | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

| Pin Names       | Description                            | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
|-----------------|--|------------------|---|
| A, B            | Data Inputs                            | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| CP              | Clock Pulse Input (Active Rising Edge) | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| $\overline{MR}$ | Master Reset Input (Active LOW)        | 1.0/1.0          | 20 $\mu$ A/-0.6 mA                              |
| $Q_0$ - $Q_7$   | Outputs                                | 50/33.3          | -1 mA/20 mA                                     |

## Functional Description

The 74F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into  $Q_0$  the logical AND of the two data inputs ( $A \cdot B$ ) that existed before the rising clock edge. A LOW level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

## Mode Select Table

| Operating Mode | Inputs          |   |   | Outputs |               |
|----------------|-----------------|---|---|---------|---------------|
|                | $\overline{MR}$ | A | B | $Q_0$   | $Q_1$ - $Q_7$ |
| Reset (Clear)  | L               | X | X | L       | L-L           |
| Shift          | H               | l | l | L       | $q_0$ - $q_6$ |
|                | H               | l | h | L       | $q_0$ - $q_6$ |
|                | H               | h | l | L       | $q_0$ - $q_6$ |
|                | H               | h | h | H       | $q_0$ - $q_6$ |

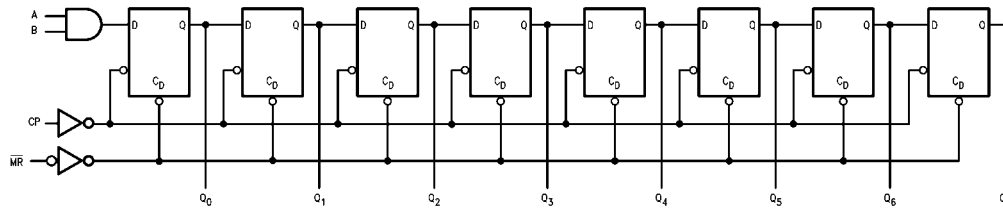
H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

X = Immaterial

$q_n$  = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 1)   | -0.5V to +7.0V                       |
| Input Current (Note 1)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Output<br>in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output  | -0.5V to V <sub>CC</sub>             |
| 3-STATE Output   | -0.5V to +5.5V                       |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)   | 4000V                                |

**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

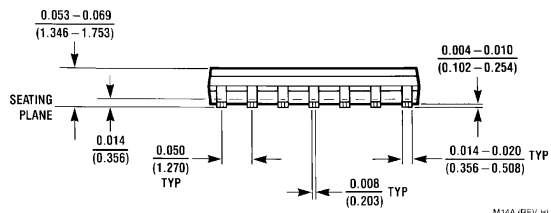
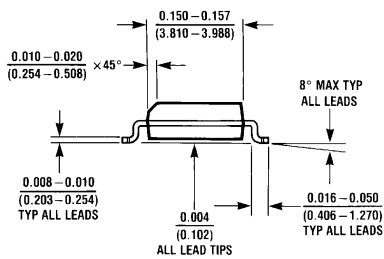
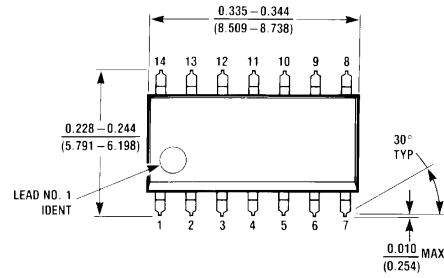
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                         | Min                                       | Typ | Max  | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|---|-----|------|-------|-----------------|--|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0                                       |     |      | V     |                 | Recognized as a HIGH Signal                          |
| V <sub>IL</sub>  | Input LOW Voltage                 |   |     | 0.8  | V     |                 | Recognized as a LOW Signal                           |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |   |     | -1.2 | V     | Min             | I <sub>IN</sub> = -18 mA                             |
| V <sub>OH</sub>  | Output HIGH Voltage               | 10% V <sub>CC</sub><br>5% V <sub>CC</sub> |     |      | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -1 mA   |
| V <sub>OL</sub>  | Output LOW Voltage                | 10% V <sub>CC</sub>                       |     | 0.5  | V     | Min             | I <sub>OL</sub> = 20 mA                              |
| I <sub>IH</sub>  | Input HIGH Current                |   |     | 5.0  | μA    | Max             | V <sub>IN</sub> = 2.7V                               |
| I <sub>BV1</sub> | Input HIGH Current Breakdown Test |   |     | 7.0  | μA    | Max             | V <sub>IN</sub> = 7.0V                               |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |   |     | 50   | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                   |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75                                      |     |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All other pins grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    |   |     | 3.75 | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All other pins grounded |
| I <sub>IL</sub>  | Input LOW Current                 |   |     | -0.6 | mA    | Max             | V <sub>IN</sub> = 0.5V                               |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -60                                       |     | -150 | mA    | Max             | V <sub>OUT</sub> = 0V                                |
| I <sub>CC</sub>  | Power Supply Current              |   | 35  | 55   | mA    | Max             | CP = HIGH<br>MR = GND, A, B = GND                    |

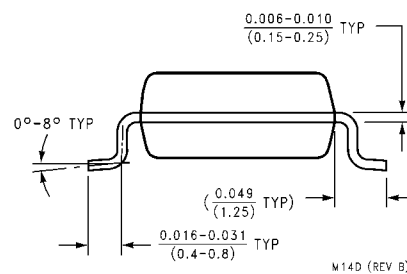
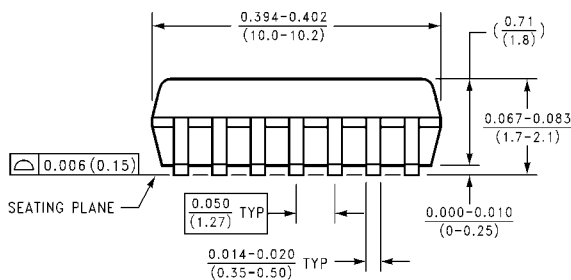
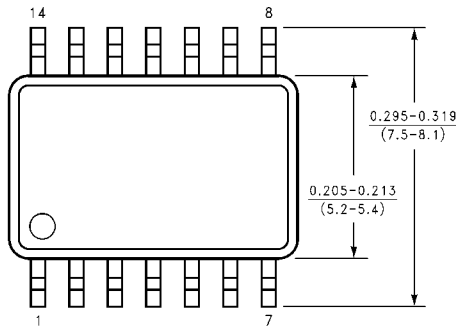
| AC Electrical Characteristics |   |   |     |  |  |   |   |       |       |
|-------------------------------|---|---|-----|--|--|---|---|-------|-------|
| Symbol                        | Parameter                                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |  | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = 5.0V<br>C <sub>L</sub> = 50 pF |   | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = 5.0V<br>C <sub>L</sub> = 50 pF |       | Units |
|                               |   | Min   | Typ | Max  | Min  | Max   | Min   | Max   |       |
| f <sub>MAX</sub>              | Maximum Clock Frequency                   | 80  | 120 |  | 60   |   | 80  |       | MHz   |
| t <sub>PLH</sub>              | Propagation Delay<br>CP to Q <sub>n</sub> | 3.0   | 4.8 | 7.5  | 2.5  | 9.0   | 3.0   | 7.5   | ns    |
| t <sub>PHL</sub>              | Propagation Delay<br>MR to Q <sub>n</sub> | 3.5   | 5.0 | 8.0  | 3.0  | 8.5   | 3.5   | 8.0   |       |
| t <sub>PHL</sub>              | Propagation Delay<br>MR to Q <sub>n</sub> | 5.0   | 7.0 | 10.0   | 4.0  | 12.5  | 5.0   | 10.5  | ns    |
| AC Operating Requirements     |   |   |     |  |  |   |   |       |       |
| Symbol                        | Parameter                                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V                           |     | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = 5.0V |  | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = 5.0V |   | Units |       |
|                               |   | Min   | Max | Min  | Max  | Min   | Max   |       |       |
| t <sub>S(H)</sub>             | Setup Time, HIGH or LOW                   | 4.5   |     | 5.5  |  | 4.5   |   | ns    |       |
| t <sub>S(L)</sub>             | A or B to CP                              | 4.0   |     | 4.0  |  | 4.0   |   |       |       |
| t <sub>H(H)</sub>             | Hold Time, HIGH or LOW                    | 1.0   |     | 1.0  |  | 1.0   |   |       |       |
| t <sub>H(L)</sub>             | A or B to CP                              | 1.0   |     | 1.0  |  | 1.0   |   | ns    |       |
| t <sub>W(H)</sub>             | CP Pulse Width                            | 4.0   |     | 4.0  |  | 4.0   |   |       |       |
| t <sub>W(L)</sub>             | HIGH or LOW                               | 7.0   |     | 7.0  |  | 7.0   |   | ns    |       |
| t <sub>W(L)</sub>             | MR Pulse Width, LOW                       | 4.0   |     | 5.0  |  | 4.0   |   | ns    |       |
| t <sub>REC</sub>              | Recovery Time<br>MR to CP                 | 5.0   |     | 6.5  |  | 5.0   |   | ns    |       |

**Physical Dimensions** inches (millimeters) unless otherwise noted



M14A (REV H)

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A**



M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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