ML2003, ML2004

Logarithmic Gain/Attenuator

Features

- Low noise: 0 dBrnc max with +24dB gain
- Low harmonic distortion: -60dB max
- Gain range: –24 to +24dB
- Resolution: 0.1dB steps
- Flat frequency response:
  ±0.05dB from .3–4 kHz
  ±0.10dB from .1-20 kHz
- Low supply current 4mA max from ±5V supplies
- TTL/CMOS compatible digital interface
- ML2003 has pin selectable serial or parallel interface; ML2004 serial interface only

General Description

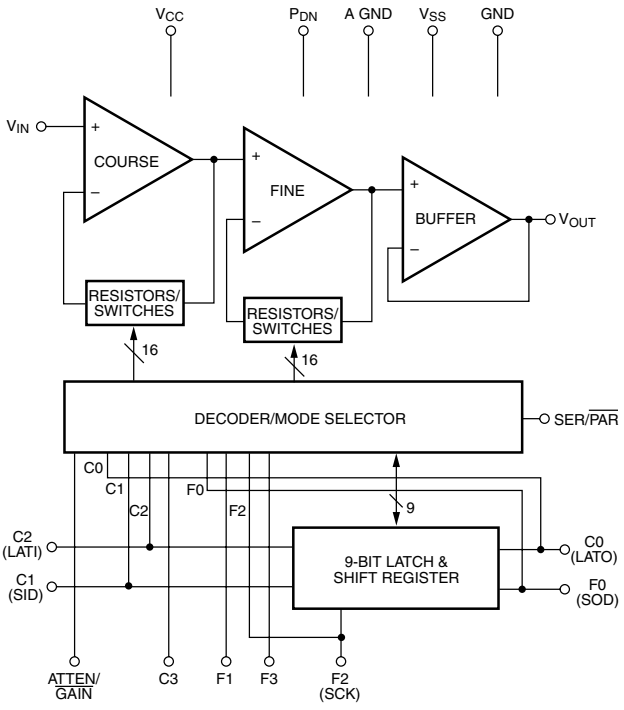
The ML2003 and ML2004 are digitally controlled logarithmic gain/attenuators with a range of –24 to +24 dB in 0.1 dB steps.

The gain settings are selected by a 9-bit digital word. The ML2003 digital interface is either parallel or serial. The ML2004 is packaged in a 14-pin DIP with a serial interface only.

Absolute gain accuracy is 0.05dB max over supply tolerance of ±10% and temperature range.

These CMOS logarithmic gain/attenuators are designed for a wide variety of applications in telecom, audio, sonar, or general purpose function generation. One specific intended application is analog telephone lines.

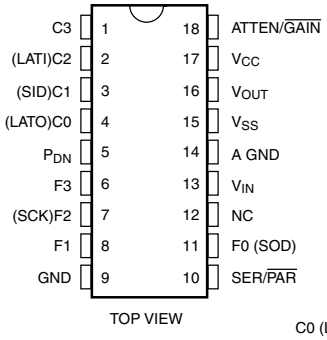
Block Diagram



NOTE: SERIAL MODE FUNCTIONS INDICATED BY PARENTHESES.

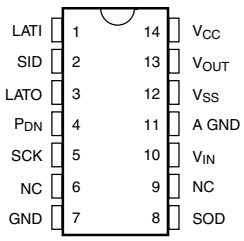
Pin Connections

ML2003
18-PIN DIP



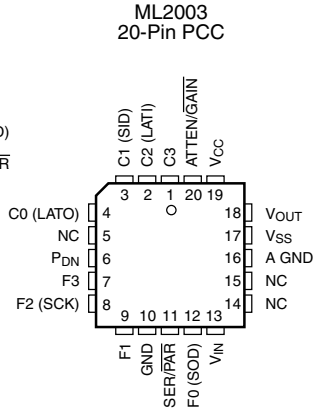
TOP VIEW

ML2004
14-PIN DIP



TOP VIEW

ML2003
20-Pin PCC



TOP VIEW

Pin Description

Name	Function
C3	In serial mode, pin is unused. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATI) C2	In serial mode, input latch clock which loads the data from the shift register into the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(SID) C1	In serial mode, serial data input that contains serial 9 bit data word which controls the gain setting. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
(LATO) C0	In serial mode, output latch clock which loads the 9 bit data word back into the shift register from the latch. In parallel mode, coarse gain select bit. Pin has internal pulldown resistor to GND.
P_{DN}	**Powerdown input**. When P_{DN} = 1, device is in powerdown mode. When P_{DN} = 0, device is in normal operation. Pin has internal pulldown resistor to GND.
F3	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
(SCK) F2	In serial mode, shift register clock which shifts the serial data on SID into the shift register on rising edges and out on SOD on falling edges. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
F1	In serial mode, pin is unused. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
GND	**Digital ground**. 0 volts. All digital inputs and outputs are referenced to this ground.
SER/$\overline{PAR}$	Serial or parallel select input. When SER/$\overline{PAR}$ = 1, device is in serial mode. When SER/$\overline{PAR}$ = 0, device is in parallel mode. Pin has internal pullup resistor to V_{CC}.
(SOD) F0	In serial mode, serial output data which is the output of the shift register. In parallel mode, fine gain select bit. Pin has internal pulldown resistor to GND.
V_{IN}	**Analog input**.
AGND	**Analog ground**. 0 volts. Analog input and output are referenced to this ground.
V_{SS}	**Negative supply**. –5 volts ±10%.
V_{OUT}	**Analog output**.
V_{CC}	**Positive supply**. +5 volts ±10%.
ATTEN/$\overline{GAIN}$	In serial mode, pin is unused. In parallel mode, attenuation/gain select bit. Pin has internal pulldown resistor to GND.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Supply Voltage V_{CC} V_{SS}		 +6.5 -6.5	 V V
AGND with respect to GND		±0.5	V
Analog Input and Output	V_{SS} –0.3V	V_{CC} +0.3	V
Digital Input and Outputs	GND –0.3	V_{CC} +0.3	V
Input Current Per Pin		±25	mA
Power Dissipation		750	mW
Storage Temperature Range	-65	+150	°C
Lead Temeperature (Soldering, 10 sec)		300	°C

Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range[2]			
ML2003CX, ML2004CX	0	70	°C
ML2003IX, ML2004IX	-40	85	°C
Supply Voltage			
V_{CC}	4	6	V
V_{SS}	-4	-6	V

Electrical Characteristics

Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0(0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4 V, C_L = 100pF or SOD.

Symbol	Parameter	Notes	Conditions	Min.	Typ.[3]	Max.	Units
Analog							
AG	Absolute gain accuracy	4	V_{IN}=8dBm, 1 kHz	-0.05		+0.05	dB
RG	Relative gain accuracy	4	100000001 000000000 000000001 All other gain settings All values referenced to 100000000 gain when ATTEN/$\overline{GAIN}$ = 1, V_{IN} =8dBm when ATTEN//$\overline{GAIN}$ =0 V_{IN} =(8dBm – Ideal Gain) in dB	-0.05 -0.05 -0.05 -0.1		+0.05 +0.05 +0.05 +0.1	dB dB dB dB
FR	Frequency response	4	300-4000 Hz 100-20,000 Hz Relative to 1 kHz	-0.05 -0.1		+0.05 +0.1	dB dB
VOS	Output Offset Voltage	4	V_{IN} = 0, +24dB gain			±100	mV
ICN	Idle Channel Noise	4 5	V_{IN} = 0, +24dB gain, C msg. Weighted V_{IN} = 0, +24dB gain, 1kHz		-6 450	0 900	dBrnc nv/√Hz
HD	Harmonic Distortion	4	V_{IN} = 8dBm gain, 1kHz Measure 2nd, 3rd harmonic relative to fundamental			-60	dB
SD	Signal to Distortion	4	V_{IN} = 8dBm, 1 kHz C msg. weighted	+60			dB
PSRR	Power Supply Rejection	4	200mVp-p, 1 kHz sine, V_{IN} = 0 on V_{CC} on V_{SS}		 -60 -60	 -40 -40	 dB dB
Z_{IN}	Input impedance, V_{IN}	4		1			Meg
V_{INR}	Input Voltage Range	4		±3.0			V
V_{OSW}	Output Voltage Swing	4		±3.0			V
Digital and DC							
V_{IL}	Digital Input Low Voltage	4				0.8	V
V_{IH}	Digital Input High Voltage	4		2.0			V
V_{OL}	Digital Output Low Voltage	4	I_{OL} = 2mA			0.4	V

Electrical Characteristics (continued)

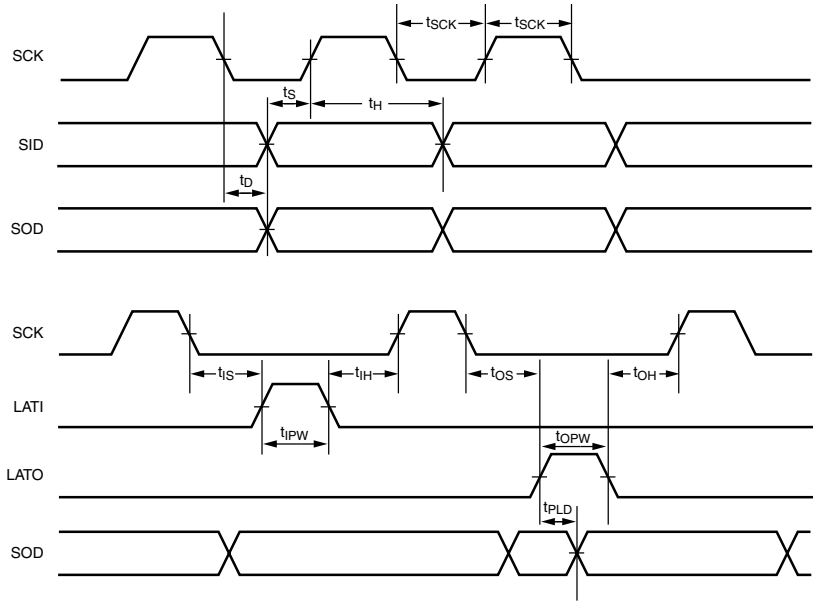
Unless otherwise specified $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ± 10%, V_{SS} = -5V ±10%, Data Word: ATTEN/$\overline{GAIN}$ = 1, Other Bits = 0(0dB Ideal Gain), C_L = 100pF, R_L = 600Ω, SCK = LATI = LATO = 0, dBm measurements use 600Ω as reference load, digital timing measured at 1.4 V, C_L = 100pF or SOD.

Symbol	Parameter	Notes	Conditions	Min.	Typ.[3]	Max.	Units
V_{OH}	Digital Output High Voltage	4	I_{OH} = -1mA	4.0			V
I_{NS}	Input Current, SER/$\overline{PAR}$	4	V_{IH} = GND	-5		-100	µA
I_{ND}	Input Current, All Digital Inputs Except SER/$\overline{PER}$	4	V_{IH} = V_{CC}	5		100	µA
I_{CC}	V_{CC} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			4	mA
I_{SS}	V_{SS} Supply Current	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}, V_{IN} = 0			-4	mA
I_{CCP}	V_{CC} Supply Current, Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			0.5	mA
I_{SSP}	V_{SS} Supply Current Powerdown Mode	4	No output load, V_{IL} = GND, V_{IH} = V_{CC}			-0.1	mA
AC Characteristics							
t_{SET}	V_{OUT} Settling Time	4	V_{IN} = 0.185V. Change gain from –24 to +24dB. Measure from LATI rising edge to when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{STEP}	V_{OUT} Step Response	4	Gain = +24dB. V_{IN} = -0.185 to +0.185V step. Measure when V_{OUT} settles to within 0.05dB of final value.			20	µs
t_{SCK}	SCK On/Off Period	4		250			ns
t_S	SID Data Setup Time	4		50			ns
t_H	SID Data Hold Time	4		50			ns
t_D	SOD Data Delay	4		0		125	ns
t_{IPW}	LATI Pulse Width	4		50			ns
t_{OPW}	LATO Pulse Width	4		50			ns
t_{IS}, t_{OS}	LATI, LATO Setup Time	4		50			ns
t_{IH}, t_{OH}	LATI, LATO Hold Time	5		50			ns
t_{PLD}	SOD Parallel Load Delay	4		0		125	ns

Notes:

1. Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.
3. Typicals are parametric norm at 25°C.
4. Parameter guaranteed and 100% production tested.
5. Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Timing Diagram



TIMING PARAMETERS ARE REFERENCED TO THE 1.4 VOLT MIDPOINT.

Figure 1. Serial Mode Timing Diagram

Typical Performance Curves

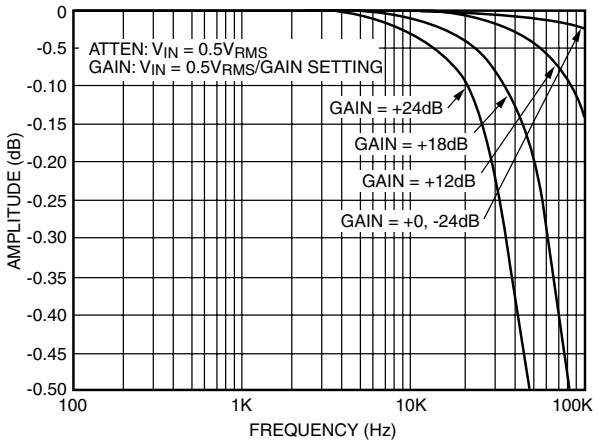


Figure 2. Amplitude vs Frequency (V_{IN}/V_{OUT} = .5V_{RMS})

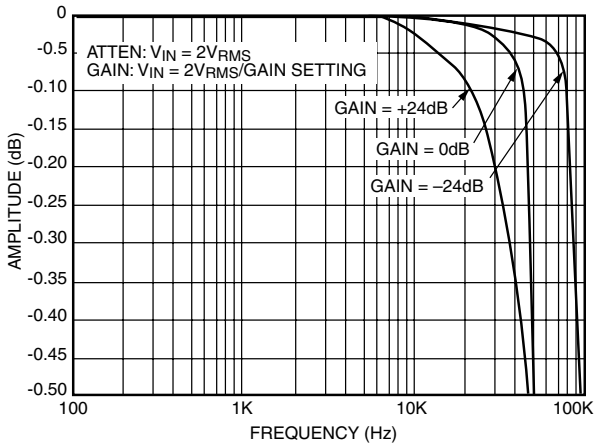


Figure 3. Amplitude vs Frequency (V_{IN}/V_{OUT} = 2V_{RMS})

Typical Performance Curves (continued)

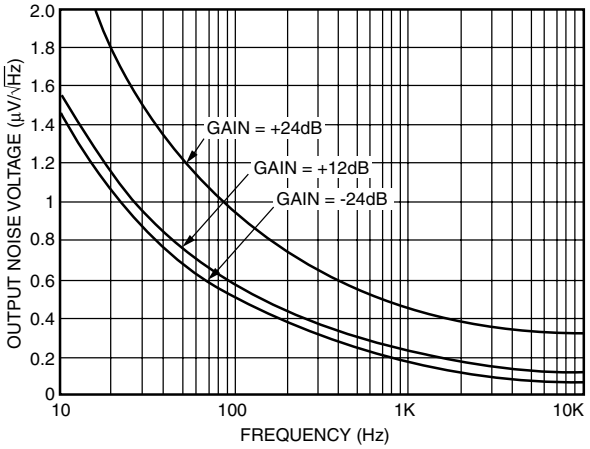


Figure 4. Output Noise Voltage vs Frequency

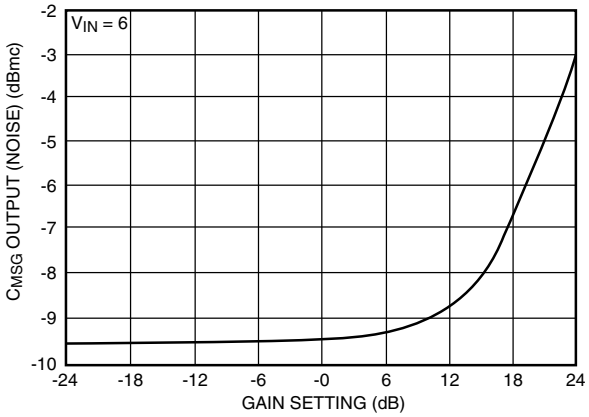


Figure 5. C_{MSG} Output Noise vs Gain Settings

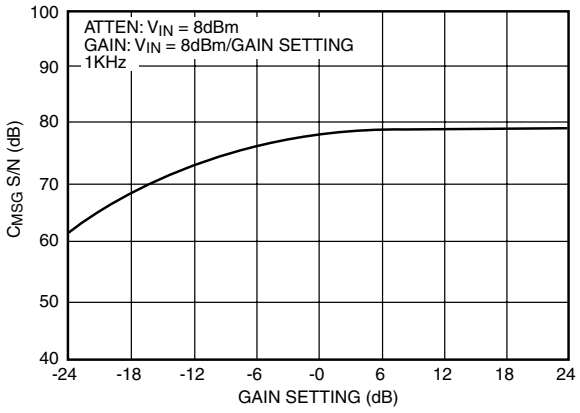


Figure 6. C_{MSG} S/N vs Gain Setting

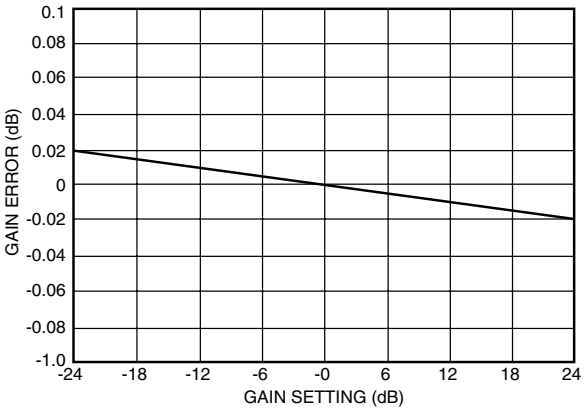


Figure 7. Gain Error vs Gain Setting

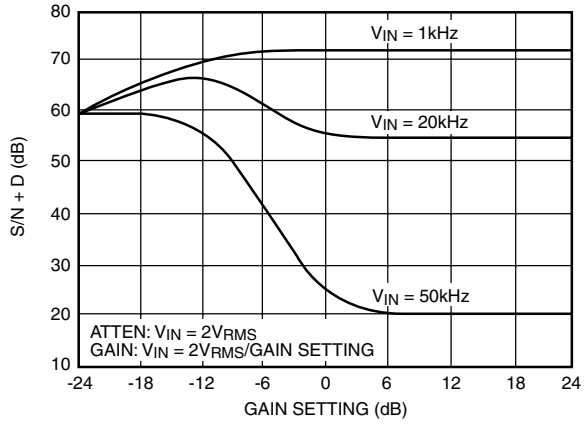


Figure 8. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = 2V_{RMS})

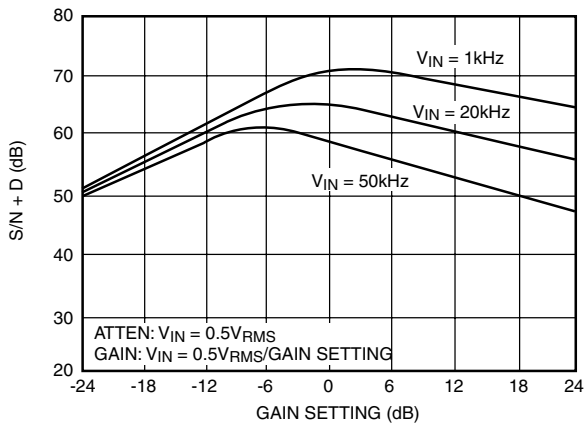


Figure 9. S/N + D vs Gain Setting (V_{IN}/V_{OUT} = 0.5V_{RMS})

Functional Description

The ML2003 consists of a coarse gain stage, a fine gain stage, an output buffer, and a serial/parallel digital interface.

Gain Stages

The analog input, V_{IN}, goes directly into the op amp input in the coarse gain stage. The coarse gain stage has a gain range of 0 to 22.5dB in 1.5dB steps.

The fine gain stage is cascaded onto the coarse section. The fine gain stage has a gain range of 0 to 1.5dB in 0.1dB steps.

In addition, both sections can be programmed for either gain or attenuation, thus doubling the effective gain range.

The logarithmic steps in each gain stage are generated by placing the input signal across a resistor string of 16 series resistors. Analog switches allow the voltage to be tapped from the resistor string at 16 points. The resistors are sized such that each output voltage is at the proper logarithimic ratio relative to the input signal at the top of the string. Attenuation is implemented by using the resistor string as a simple voltage divider, and gain is implemented by using the resistor string as a feedback resistor around an internal op amp.

Gain Settings

Since the coarse and fine gain stages are cascaded, their gains can be summed logarithmically. Thus, any gain from –24dB to +24dB in 0.1dB steps can be obtained by combining the coarse and fine gain settings to yield the desired gain setting. The relationship between the digital select bits and the corresponding analog gain values is shown in Tables 1 and 2. Note that C3-C0 selects the coarse gain, F3-F0 selects the fine gain, and ATTEN/$\overline{\text{GAIN}}$ selects either attenuation or gain.

Output Buffer

The final analog stage is the output buffer. This amplifier has internal gain of 1 and is designed to drive 600 ohms and 100pF loads. Thus, it is suitable for driving a telephone hybrid circuit directly without any external amplifier.

Power Supplies

The digital section is powered between V_{CC} and GND, or 5 volts. The analog section is powered between V_{CC} and V_{SS} and uses AGND as the reference point, or ±5 volts.

GND and AGND are totally isolated inside the device to minimize coupling from the digital section into the analog section. However, AGND and GND should be tied together physically near the device and ideally close to the common power supply ground connection.

Typically, the power supply rejection of V_{CC} and V_{SS} to the analog output is greater than –60dB at 1 kHz. If decoupling of the power supplies is still necessary in a system, V_{CC} and V_{SS} should be decoupled with respect to AGND.

Powerdown Mode

A powerdown mode can be selected with pin P_{DN}. When P_{DN} = 1, the device is powered down. In this state, the power consumption is reduced by removing power from the analog section and forcing the analog output,V_{OUT}, to a high impedance state. While the device is in powerdown mode, the digital section is still functional and the current data word remains stored in the latch when in serial mode. When P_{DN} = 0, the device is in normal operation.

Digital Section

The ML2003 can be operated with a serial or parallel interface. The SER/$\overline{\text{PAR}}$ pin selects the desired interface. When SER/$\overline{\text{PAR}}$ = 1, the serial mode is selected. When SER/$\overline{\text{PAR}}$ = 0, the parallel mode is selected. The ML2004 digital interface is serial only.

Serial Mode

Serial mode is selected by setting SER/$\overline{\text{PAR}}$ pin high. The serial interface allows the gain settings to be set from a serial data word.

The timing for the serial mode is shown in Figure 10. The serial input data, SID, is loaded into a shift register on rising edges of the shift clock, SCK. The data can be parallel loaded into a latch when the input latch signal, LATI, is high. The LATI pulse must occur when SCK is low. In this way, a new data word can be loaded into the shift register without disturbing the existing data word in the latch.

The parallel outputs of the latch control the attenuation/gain setting. The order of the data word bits in the latch is shown in Figure 11. Note that bit 0 is the first bit of the data word clocked into the shift register. Tables 1 and 2 describe how the data word programs the gain.

Table 1. Fine Gain Settings (C3-C0 = 0)

				Ideal Gain (dB)	
F3	F2	F1	F0	ATTEN/$\overline{\text{GAIN}}$ = 1	ATTEN/$\overline{\text{GAIN}}$ = 0
0	0	0	0	0	0
0	0	0	1	-.1	.1
0	0	1	0	-.2	.2
0	0	1	1	-.3	.3
0	1	0	0	-.4	.4
0	1	0	1	-.5	.5
0	1	1	0	-.6	.6
0	1	1	1	-.7	.7
1	0	0	0	-.8	.8
1	0	0	1	-.9	.9
1	0	1	0	-1.0	1.0
1	0	1	1	-1.1	1.1
1	1	0	0	-1.2	1.2
1	1	0	1	-1.3	1.3
1	1	1	0	-1.4	1.4
1	1	1	1	-1.5	1.5

Table 2. Coarse Gain Settings (F3-F0 = 0)

C3	C2	C1	C0	Ideal Gain (dB) ATTEN/$\overline{\text{GAIN}}$ = 1	Ideal Gain (dB) ATTEN/$\overline{\text{GAIN}}$ = 0
0	0	0	0	0	0
0	0	0	1	-1.5	1.5
0	0	1	0	-3.0	3.0
0	0	1	1	-4.5	4.5
0	1	0	0	-6.0	6.0
0	1	0	1	-7.5	7.5
0	1	1	0	-9.0	9.0
0	1	1	1	-10.5	10.5
1	0	0	0	-12.0	12.0
1	0	0	1	-13.5	13.5
1	0	1	0	-15.0	15.0
1	0	1	1	-16.5	16.5
1	1	0	0	-18.0	18.0
1	1	0	1	-19.5	19.5
1	1	1	0	-21.0	21.0
1	1	1	1	-22.5	22.5

The device also has the capability to read out the data word stored in the latch. This can be done by parallel loading the data from the latch back into the shift register when the latch signal, LATO, is high. The LATO pulse must occur when SCK is low. Then, the data word can be shifted out of the shift register serially to the output, SOD, on falling edges of the shift clock, SCK.

The loading and reading of the data word can be done continuously or in burst. Since the shift register and latch circuitry inside the device is static, there are no minimum frequency requirements on the clocks or data pulses. However, there is coupling (typically less than 100µV) of the digital signals into the analog section. This coupling can be minimized by clocking the data bursts in during noncritical intervals or at a frequency outside the analog frequency range.

Parallel Mode

The parallel mode is selected by setting SER/$\overline{\text{PAR}}$ pin low. The parallel interface allows the gain settings to be set with external switches or from a parallel microprocessor interface.

In parallel mode, the shift register and latch are bypassed and connections are made directly to the gain select bits with external pins ATTEN/$\overline{\text{GAIN}}$, C3-C0, and F3-F0. Tables 1 and 2 describe how these pins program the gain. The pins ATTEN/$\overline{\text{GAIN}}$, C3-C0, and F3-F0 have internal pulldown resistors to GND. The typical value of these pulldown resistors is 100kΩ.

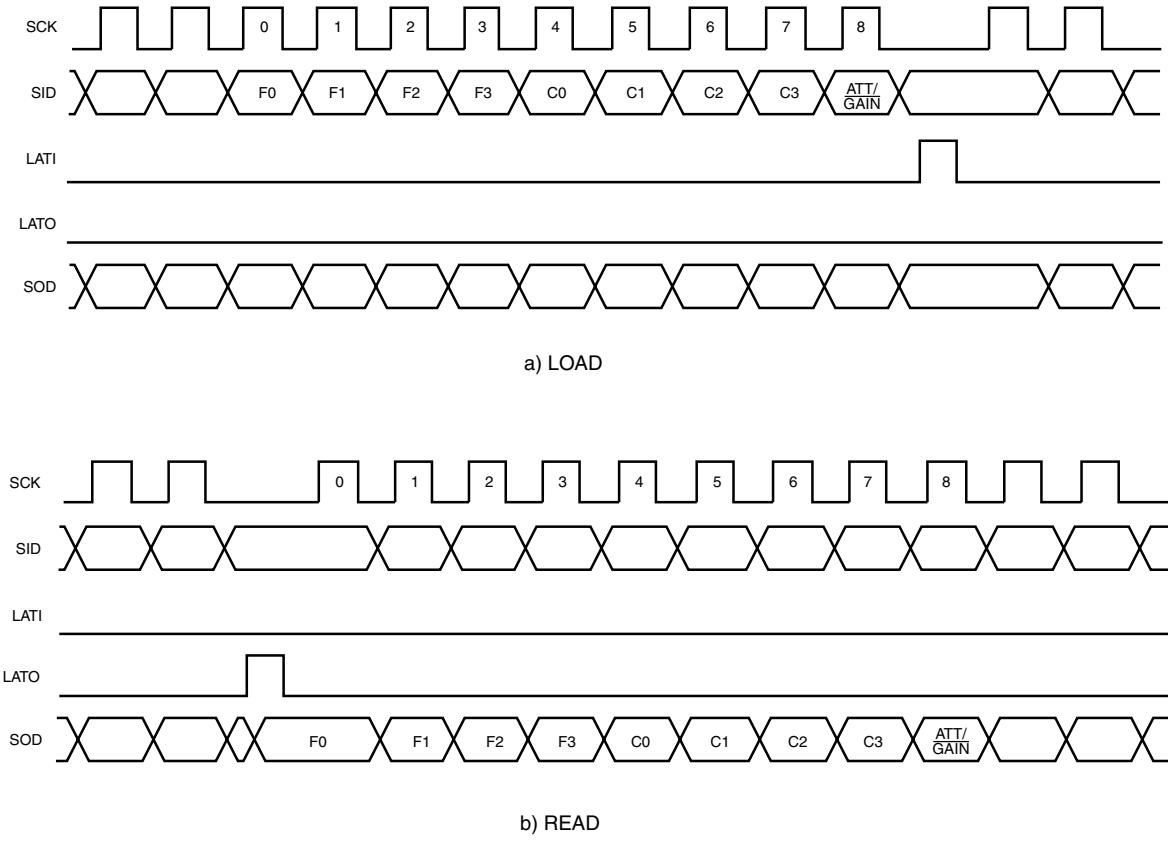


Figure 10. Serial Mode Timing

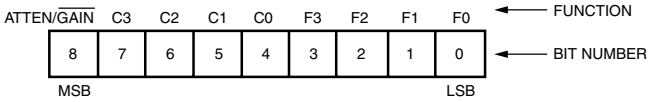


Figure 11. 9-Bit Latch

Applications

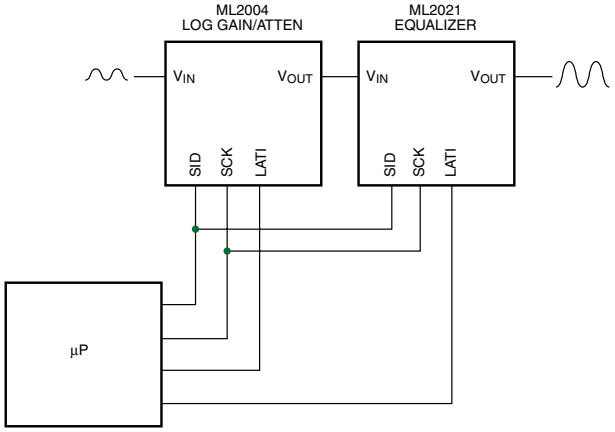


Figure 12. Typical Serial Interface

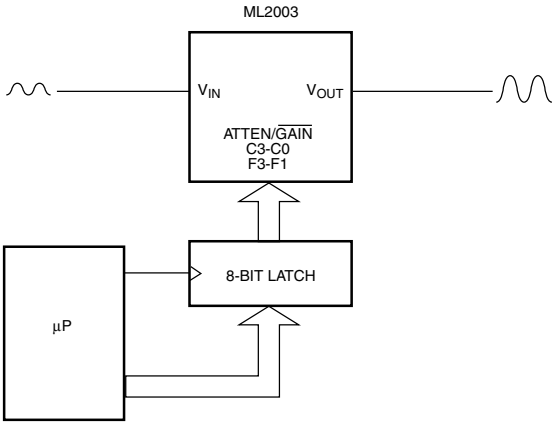


Figure 13. Typical µP Parallel Interface

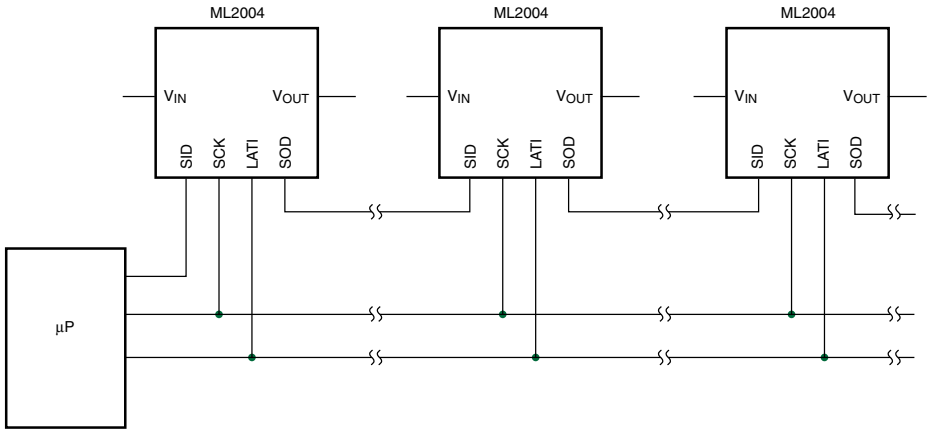


Figure 14. Controlling Multiple ML2004 with Only 3 Digital Lines Using One Long Data Word

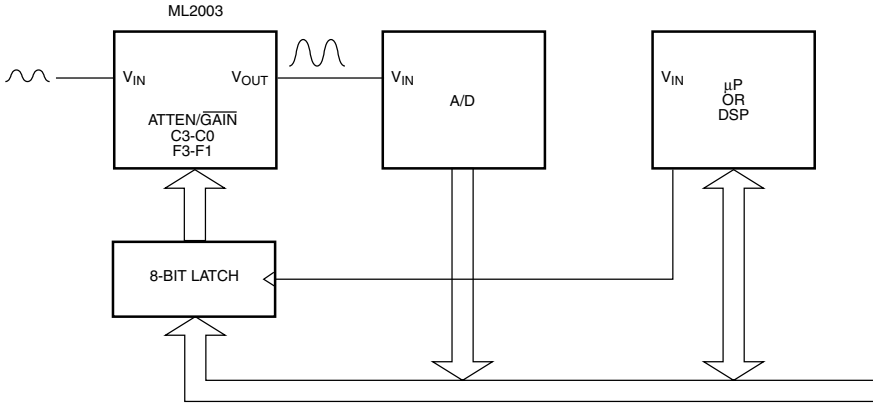


Figure 15. AGC for DSP or Modem Front End

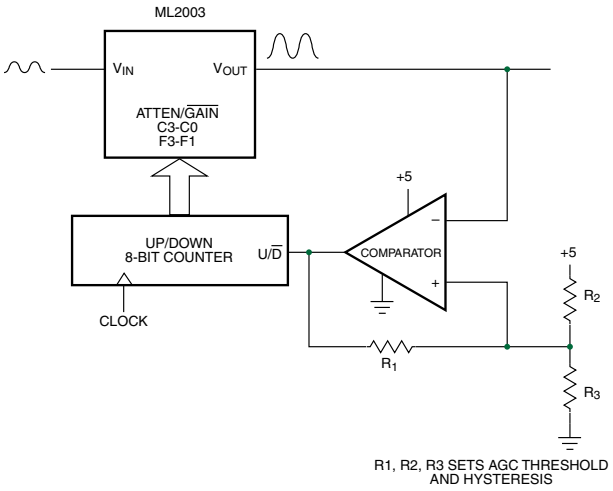


Figure 16. Analog AGC

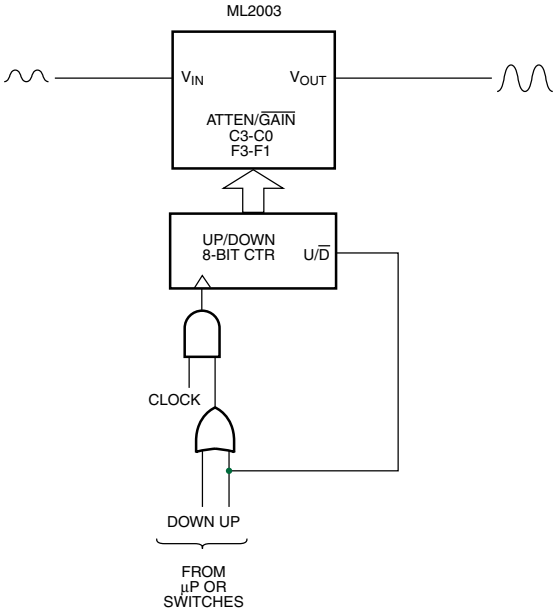


Figure 17. Digitally Controlled Volume Control

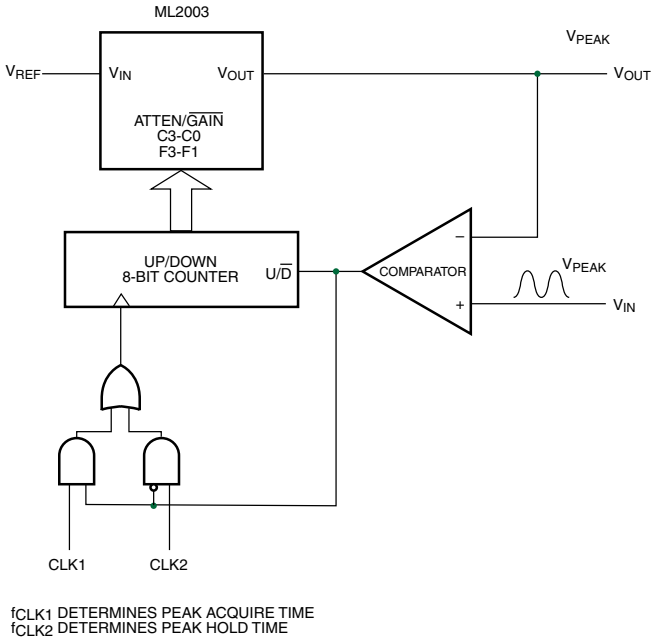


Figure 18. Precision Peak Detector (±1%) with Controllable Acquire and Hold Time

Ordering Information

Part Number	Temperature Range	Package
ML2003IQ	-40°C to 85°C	Molded PCC (Q20)
ML2003CP	0°C to 70°C	Molded DIP (P18)
ML2003CQ	0°C to 70°C	Molded PCC (Q20)
ML2004IP	-40°C to 85°C	Molded DIP (P14)
ML2004CP	0°C to 70°C	Molded DIP (P14)