SRDA3.3-6 and SRDA05-6
RailClamp®
Low Capacitance TVS Diode Array

PROTECTION PRODUCTS

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning.**

The unique design of the SRDA series devices incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect six high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges.

Features

- Transient protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 24A (8/20µs)
- Array of surge rated diodes with internal TVS diode
- Protects six I/O lines and power supply line
- Low capacitance (<15pF) for high-speed interfaces
- Low operating & clamping voltages
- Solid-state technology

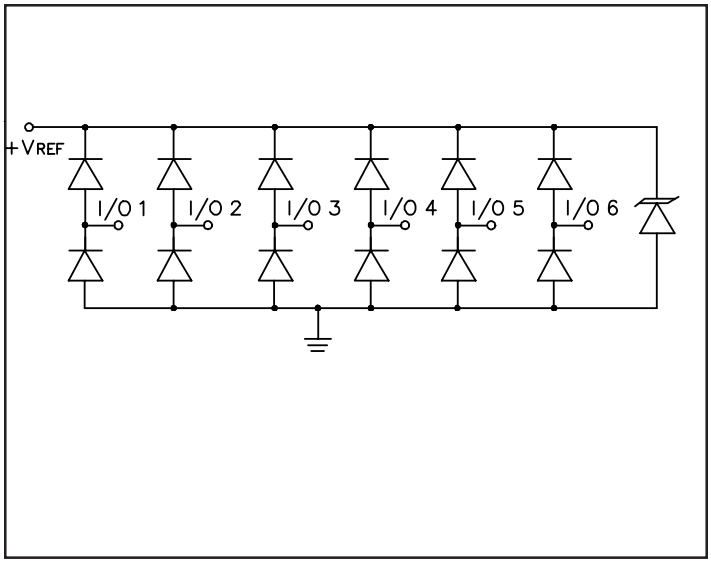
Mechanical Characteristics

- JEDEC SO-8 package
- UL 497B listed
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tube or Tape and Reel per EIA 481

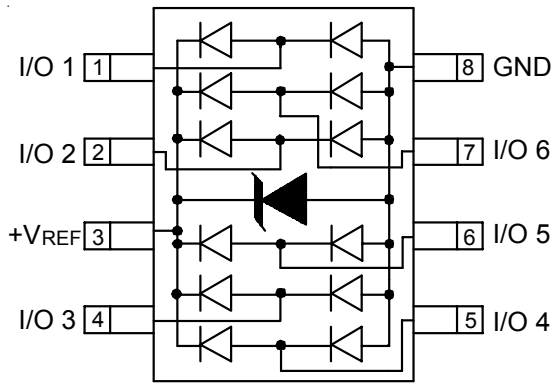
Applications

- USB Power & Data Line Protection
- T1/E1 secondary IC Side Protection
- Token Ring
- HDSL, SDSL secondary IC Side Protection
- Video Line Protection
- Microcontroller Input Protection
- Base stations
- I^2C Bus Protection

Circuit Diagram



Schematic and PIN Configuration



S0-8 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p = 8/20µs)	P_{pk}	500	Watts
Peak Forward Voltage (I_F = 1A, tp=8/20µs)	V_{FP}	1.5	V
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

SRDA3.3-6

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			5.3	V
Clamping Voltage	V_C	I_{PP} = 10A, tp = 8/20µs			10	V
Clamping Voltage	V_C	I_{PP} = 25A, tp = 8/20µs			15	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			25	A
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		8	15	pF
		Between I/O pins V_R = 0V, f = 1MHz		4		pF

Note:
(1) The SRDA3.3-6 is constructed using Semtech's proprietary EPD process technology. See applications section for more information.

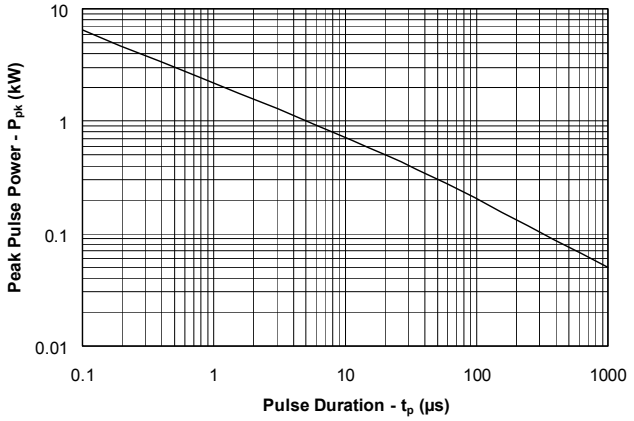
Electrical Characteristics *(continued)*

SRDA05-6

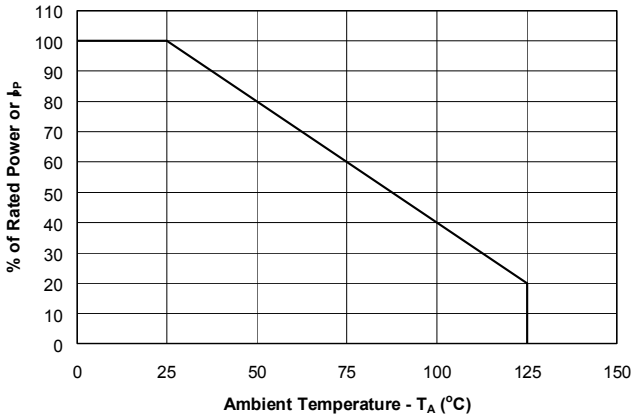
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			10	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			9.8	V
Clamping Voltage	V_C	I_{PP} = 10A, t_p = 8/20µs			12	V
Clamping Voltage	V_C	I_{PP} = 25A, t_p = 8/20µs			20	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			25	A
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		8	15	pF
		Between I/O pins V_R = 0V, f = 1MHz		4		pF

Typical Characteristics

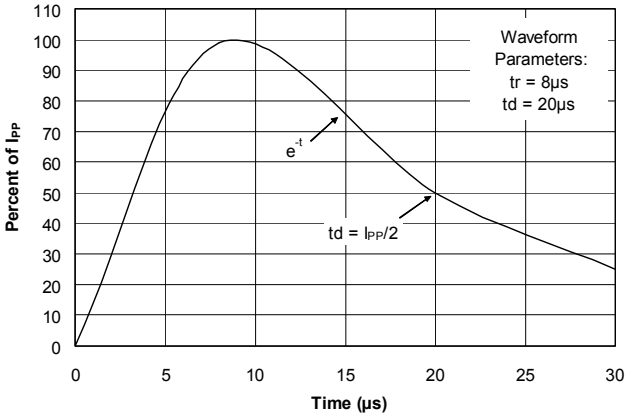
Non-Repetitive Peak Pulse Power vs. Pulse Time



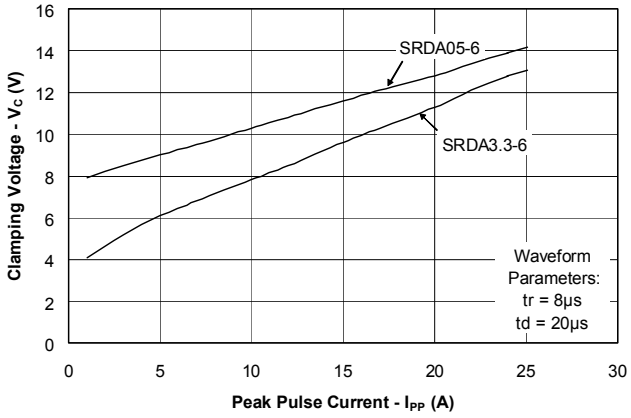
Power Derating Curve



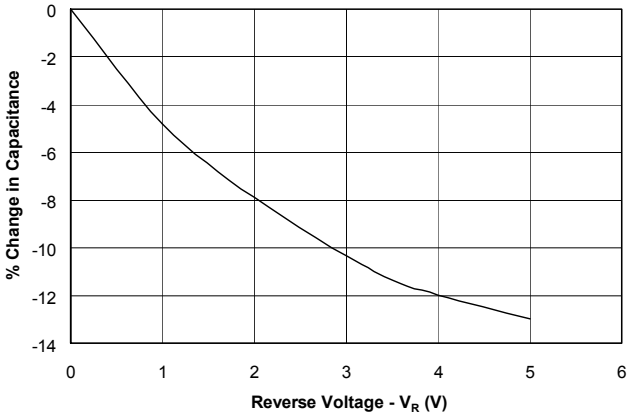
Pulse Waveform



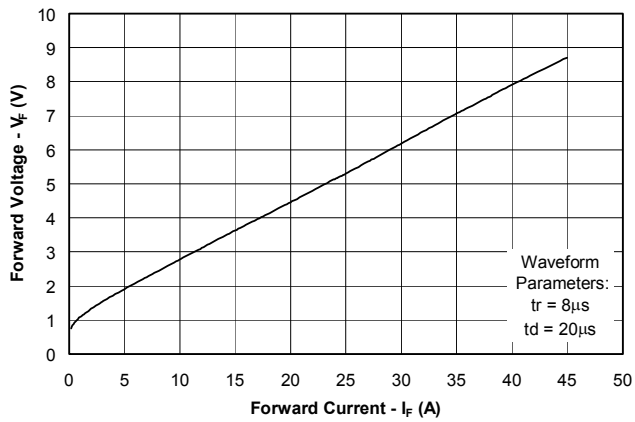
Clamping Voltage vs. Peak Pulse Current



Variation of Capacitance vs. Reverse Voltage



Forward Voltage vs. Forward Current



Applications Information

Device Connection Options for Protection of Six High-Speed Lines

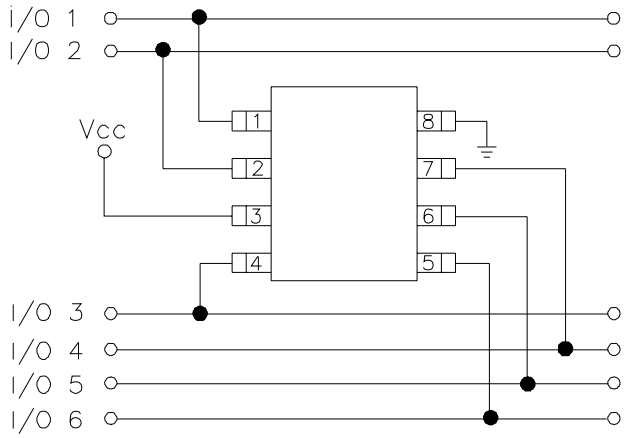
The SRDA TVS is designed to protect four data lines from transient overvoltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 2, 4, 5, 6 and 7. The negative reference is connected at pin 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pins 2 and 3. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SRDA can be isolated from the power supply by adding a series resistor between pin 3 and V_{CC}. A value of 10kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 3 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

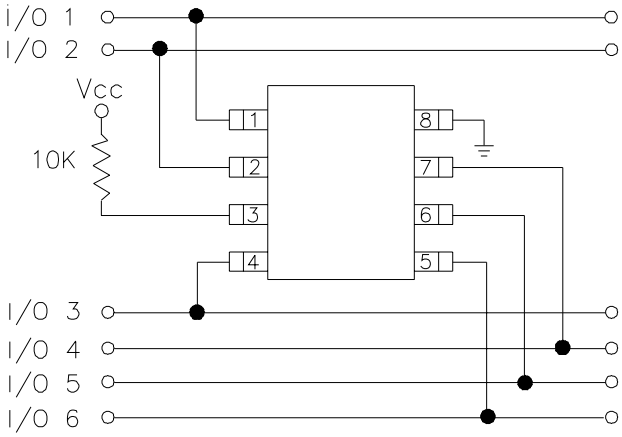
ESD Protection With RailClamps

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the V_F drop of the diode. For negative events, the bottom diode will be biased when the voltage exceeds the V_F of the diode. At first

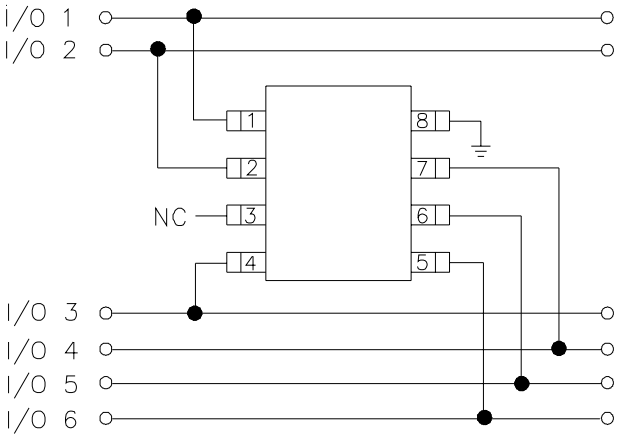
Data Line and Power Supply Protection Using Vcc as reference



Data Line Protection with Bias and Power Supply Isolation Resistor



Data Line Protection Using Internal TVS Diode as Reference



Applications Information *(continued)*

approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)

$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P \, di_{ESD}/dt$ (for positive duration pulses)

$V_C = -V_F - L_G \, di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 1000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P \, di_{ESD}/dt = 1X10^{-9} (30 / 1X10^{-9}) = 30V$

Example:
Consider a V_{CC} = 5V, a typical V_F of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note the high V_F of the discrete diode. It is not uncommon for the V_F of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event,

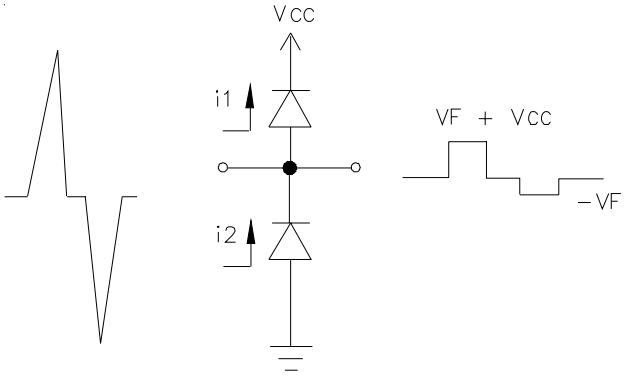


Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)

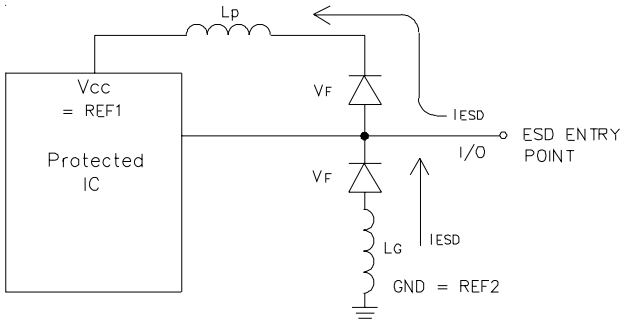


Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection

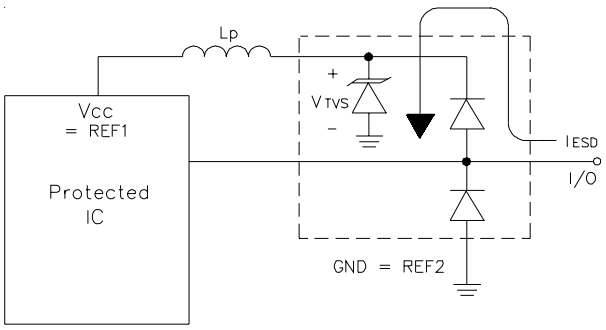


Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays

Applications Information *(continued)*

the current will be directed through the integrated TVS diode to ground. The total clamping voltage seen by the protected IC due to this path will be:

$$V_C = V_{F(RailClamp)} + V_{TVS}$$

This is given in the data sheet as the rated clamping voltage of the device. For an SRDA05-6 the typical clamping voltage is <16V at I_{PP}=30A. The diodes internal to the RailClamp are low capacitance, fast switching devices that are rated to handle high transient currents and maintain excellent forward voltage characteristics.

Using the RailClamp does not negate the need for good board layout. All other inductive paths must be considered. The connection between the positive supply and the SRDA and from the ground plane to the SRDA must be kept as short as possible. The path between the SRDA and the protected line must also be minimized. The protected lines should be routed directly to the SRDA. Placement of the SRDA on the PC board is also critical for effective ESD protection. The device should be placed as close as possible to the input connector. The reason for this is twofold. First, inductance resists change in current flow. If a significant inductance exists between the connector and the TVS, the ESD current will be directed elsewhere (lower resistance path) in the system. Second, the effects of radiated emissions and transient coupling can cause upset to other areas of the board even if there is no direct path to the connector. By placing the TVS close to the connector it will divert the ESD current immediately and absorb the ESD energy before it can be coupled into nearby traces.

(Reference Semtech application note SI99-01 for further information on board layout)

SRDA3.3-6 EPD TVS Characteristics

The internal TVS of the SRDA3.3-4 is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices that are internal to the SRDA05-6. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SRDA3.3-6 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

The IV characteristic curve of the EPD device is shown in Figure 4. The device represents a high impedance to the circuit up to the working voltage (V_{RWM}). During a transient event, the device will begin to conduct as it is biased in the reverse direction. When the punch-through voltage (V_{PT}) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current (approximately < 50mA) to allow it to travel back through the negative resistance region. If this is a concern, a 10kW current limiting resistor can be placed between the supply rail and the positive reference pin to prevent device latch-up.

RailClamp is a registered trademark of Semtech corporation

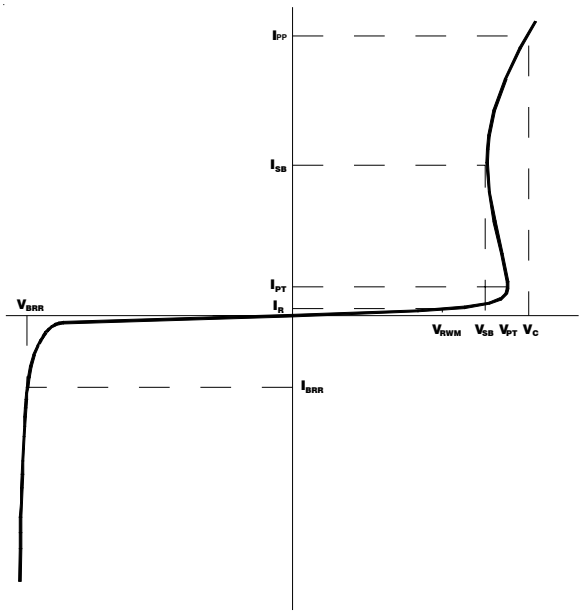
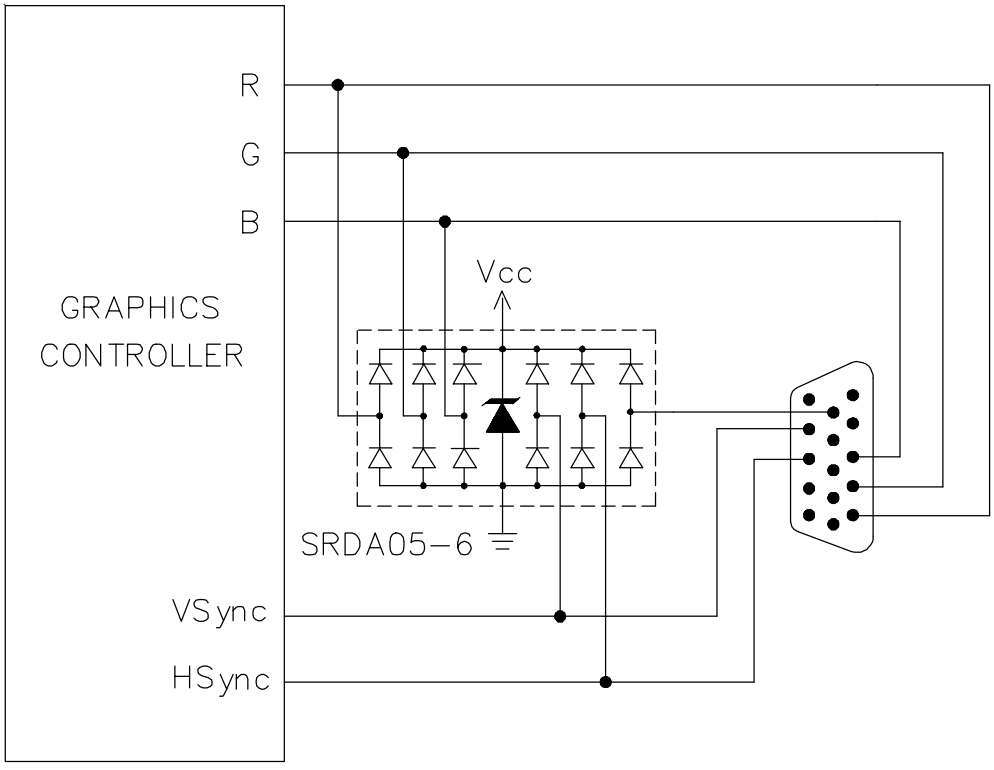


Figure 4 - EPD TVS IV Characteristic Curve

Typical Applications



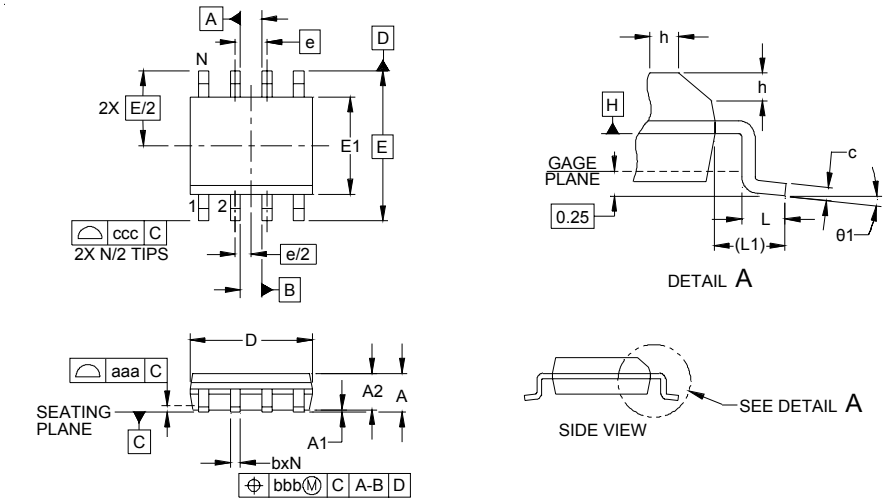
Video Line Protection

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

PROTECTION PRODUCTS

Outline Drawing - SO-8

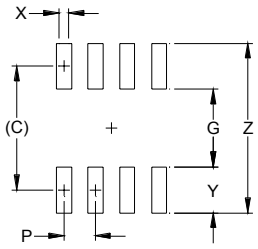


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Ordering Information

Part Number	Lead Finish	Qty/Pkg	Reel Size
SRDA3.3-6.TB	SnPb	500/Reel	7 Inch
SRDA05-6.TB	SnPb	500/Reel	7 Inch
SRDA3.3-6.TBT	Pb free	500/Reel	7 Inch
SRDA05-6.TBT	Pb free	500/Reel	7 Inch
SRDA3.3-6	SnPb	95/Tube	N/A
SRDA05-6	SnPb	95/Tube	N/A
SRDA3.3-6.T	Pb free	95/Tube	N/A
SRDA05-6.T	Pb free	95/Tube	N/A

Note: Lead-free devices are RoHS/WEEE Compliant

Contact Information

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