ComLink™ Series

CY2DP814

1:4 Clock Fanout Buffer

Features

- **Low voltage operation**
- **V_{DD} = 3.3V**
- **1:4 fanout**
- **Single-input configurable for LVDS, LVPECL, or LVTTL**
- **Four differential pairs of LVPECL outputs**
- **Drives 50-ohm load**
- **Low input capacitance**
- **Low output skew**
- **Low propagation delay**
  - **Typical (tpd < 4 ns)**
- **Industrial versions available**
- **Available packages include TSSOP, SOIC**

Description

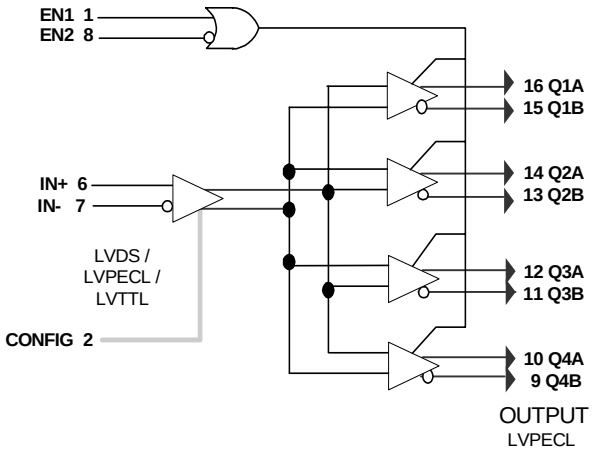
The Cypress CY2 series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic.

The Cypress CY2DP814 fanout buffer features a single LVDS- or a single LVPECL-compatible input and four LVPECL output pairs.

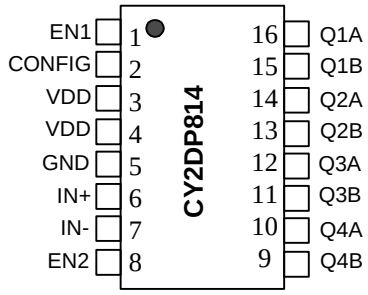
Designed for data communications clock management applications, the fanout from a single input reduces loading on the input clock.

The CY2DP814 is ideal for both level translations from single-ended to LVPECL and/or for the distribution of LVDS-based clock signals. The Cypress CY2DP814 has configurable input between logic families. The input can be selectable for an LVPECL/LVTTL or LVDS signal, while the output drivers support LVPECL capable of driving 50-ohm lines.

Block Diagram



Pin Configuration



16 pin TSSOP / SOIC

Pin Description

Pin Number	Pin Name	Pin Standard Interface	Description
6, 7	IN+, IN–	Configurable	**Differential input pair or single line**. LVPECL default. See CONFIG below.
2	CONFIG	LVTTL/LVCMOS	**Converts inputs** from the default LVPECL/LVDS (logic = 0) to LVTTL/LVCMOS (logic = 1). See *Figure 6* and *Figure 7* for additional information
1, 8	EN1, EN2	LVTTL/LVCMOS	**Enable/disable logic**. See Function Table below for details.
16, 15, 14, 13, 12, 11, 10, 9	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B	LVPECL	**Differential outputs**.
3, 4	V_{DD}	POWER	**Positive supply voltage**.
5	GND	POWER	**Ground**.

Maximum Ratings[1][2]

Storage Temperature: .....–65°C to +150°C
Ambient Temperature:.....–40°C to +85°C
Supply Voltage to Ground Potential
(Inputs and V_{CC} only)..... –0.3V to 4.6V
Supply Voltage to Ground Potential
(Outputs only)..... –0.3V to V_{DD} + 0.3V
DC Input Voltage ..... –0.3V to V_{DD} + 0.3V
DC Output Voltage..... –0.3V to V_{DD} + 0.9V
Power Dissipation..... 0.75W

Table 1. EN1 EN2 Function Table

Enable Logic		Input		Outputs	
EN1	EN2	IN+	IN–	QnA	QnB
H	H	H	L	H	L
H	L	H	L	H	L
L	L	H	L	H	L
L	H	X	X	Z	Z

Table 2. Input Receiver Configuration for Differential or LVTTL/LVCMOS

CONFIG Pin 2 Binary Value	Input Receiver Family	Input Receiver Type
1	LVTTL in LVCMOS	Single ended, non-inverting, inverting, void of bias resistors.
0	LVDS	Low voltage differential signaling
	LVPECL	Low voltage pseudo (positive) emitter coupled logic

Table 3. Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal

LVTTL/LVCMOS INPUT LOGIC			
Input Condition		Input Logic	Output Logic Q pins
Ground	IN- Pin 7		
	IN+ Pin 6	Input	True
V_{CC}	IN- Pin 7		
	IN+ Pin 6	Input	Invert
Ground	IN+ Pin 6		
	IN- Pin 7	Input	Invert
V_{CC}	IN+ Pin 6		
	IN- Pin 7	Input	True

Table 4. Power Supply Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Loaded		1.5	2.0	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Loaded, fL= 100 MHz		90	100	mA

Table 5. D.C. Electrical Characteristics: 3.3V–LVDS Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{ID}	Magnitude of Differential Input Voltage			100		600	mV
V_{IC}	Common-Mode of Differential Input Voltage $\|V_{ID}\|$ (min. and max.)			$\|V_{ID}\|$ /2		2.4– ($\|V_{ID}\|$ /2)	V
I_{IH}	Input High Current	V_{DD} = Max.	$V_{IN} = V_{DD}$		±10	±20	uA
I_{IL}	Input Low Current	V_{DD} = Max.	$V_{IN} = V_{SS}$		±0	±20	uA
I_I	Input High Current	V_{DD} = Max., $V_{IN} = V_{DD}$(max.)				±20	uA

Notes:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Table 6. D.C. Electrical Characteristics: 3.3V–LVPECL Input

Parameter	Description	Condition		Min.	Typ.	Max.	Unit
I V_{ID} I	Differential Input Voltage p-p	Guaranteed Logic High Level		400		2600	mV
VCM	Common-mode Voltage			1650		2250	mV
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = V_{DD}		±10	±20	uA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = V_{SS}		±10	±20	uA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(max.)				±20	uA

Table 7. D.C Electrical Characteristics: 3.3V–LVTTL/LVCMOS Input

Parameter	Description	Condition		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	V_{IN} = 2.7V			1	uA
I_{IL}	Input Low Current	V_{DD} = Max.	V_{IN} = 0.5V			–1	uA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(max.)				20	uA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
V_H	Input Hysteresis				80		mV

Table 8. D.C Electrical Characteristics: 3.3V–LVPECL Output

Parameter	Description	Condition		Min.	Typ.	Max.	Unit
I V_{OD} I	Driver Differential Output Voltage p-p	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	RL = 50 ohm	1000		3600	mV
I V_{OC} I	Driver common-mode p-p	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	RL = 50 ohm			226	mV
Rise Time	Differential 20% to 80%	CL–10 pF RL and CL to GND	RL = 50 ohm	300		800	pS
Fall Time							
V_{OH}	Output High Voltage	V_{DD} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.1		3.0	V
V_{OL}	Output Low Voltage	User-defined (see *Figure 1*)					V
I_{OS}	Short Circuit Current	V_{DD} = Max., V_{OUT} = G_{ND}		–125		–150	mA

Table 9. AC Switching Characteristics @ 3.3V V_{DD} = 3.3V ±5%, Temperature = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
IN [+,-] to Q[A,B] Data & Clock Speed						
t_{PLH}	Propagation Delay–Low to High	V_{OD} = 100 mV	3	4	5	nS
t_{PHL}	Propagation Delay–High to Low		3	4	5	nS
t_{PD}	Propagation Delay		3	4	5	ns
EN [1,2] to Q[A,B] Control Speed						
t_{PE}	Enable (EN) to functional operation				6	nS
Tpd	Functional operation to Disable				5	nS
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)				0.2	nS
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}–t_{PLH})			0.2		nS
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	V_{ID} = 100 mV			1	nS

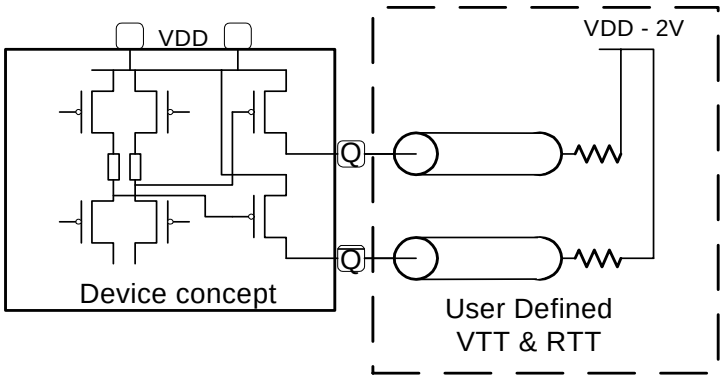
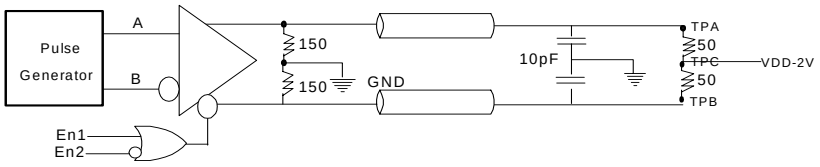


Figure 1. Differential PECL Output

Table 10. High-frequency Parametrics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum Frequency V_{DD} = 3.3V	50% Duty Cycle tW(50–50) Standard Load Circuit			450	MHz
Fmax(20)	Maximum Frequency V_{DD} = 3.3V	20% Duty Cycle tW(20–80) LVPECL Input Vin = V_{IH}(Max.)/V_{IL}(Min.) Vout = V_{OH}(Min.)/V_{OL} (Max.) (Limit)			175	MHz
TW	Minimum Pulse V_{DD} = 3.3V	LVPECL Input Vin = V_{IH}(Max.)/V_{IL}(Min.) F = 100 MHz Vout = V_{OH}(Min.)/V_{OL}(Max.).(Limit)	900			pS



Standard Termination

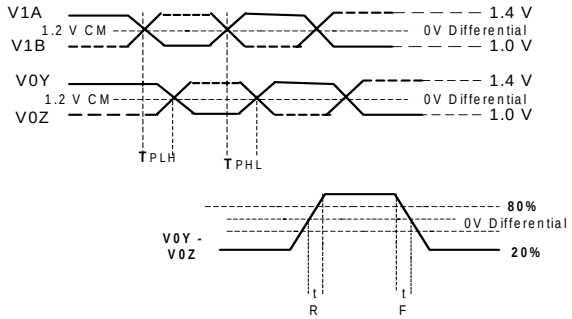


Figure 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time[3, 4, 5, 6, 7]

Notes:

3. RL = 50 ohm ± 1%; Zline = 50 ohm 6 = Ó.
4. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
5. TPA and B are used for prop delay and rise/fall measurements. T_{PC} is used for V_{OC} measurements only and otherwise connected to V_{DD} – 2.
6. When measuring Tr/Tf, tpd, V_{OD} point T_{PC} is held at V_{DD} – 2.0V.
7. LVCMOS/LVTTL single-ended input value. Ground either input: when on the B side, non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See *Table 3*.

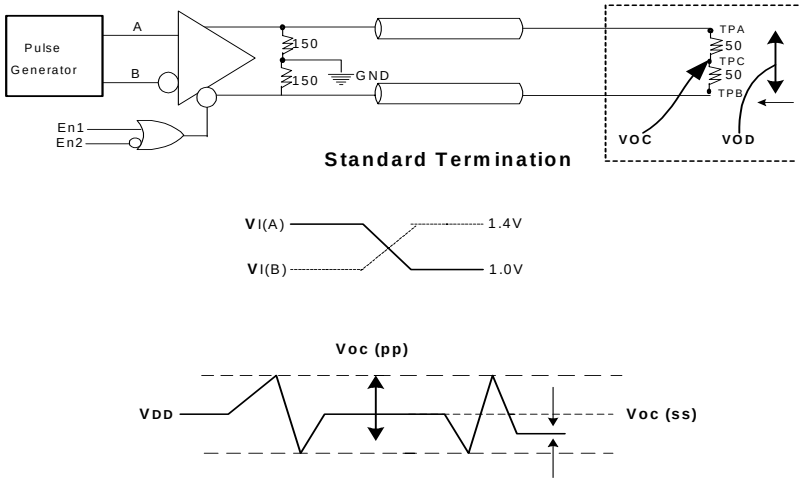
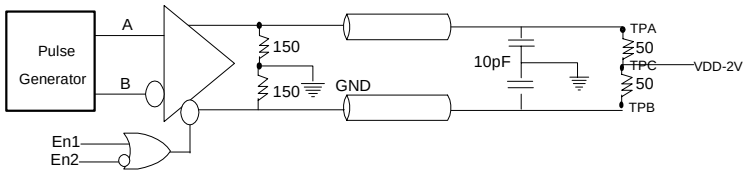


Figure 3. Test Circuit & Voltage Definitions for the Driver Common-mode Output Voltage[3, 4, 5, 7, 8]



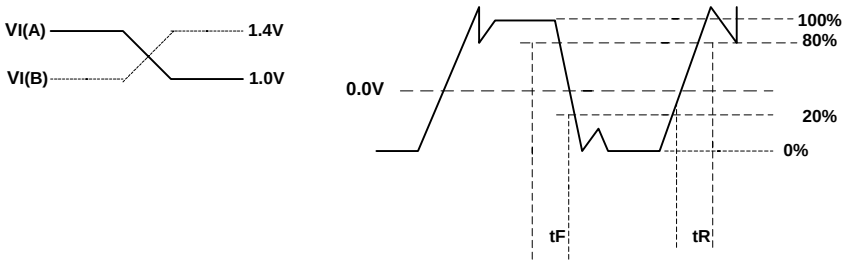


Figure 4. Test Circuit & Voltage Definitions for the Differential Output Signal [3, 4, 5, 6, 7]

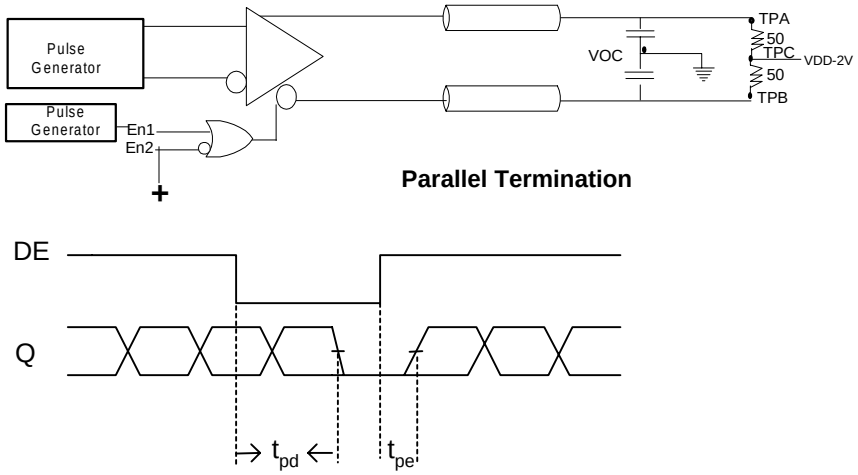
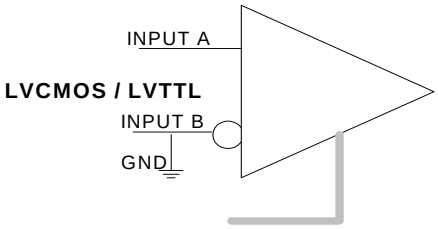


Figure 5. Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage[3, 4, 5, 8, 9]

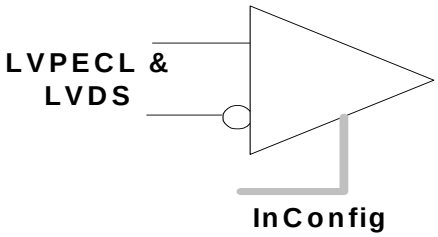
Notes:

8. V_{OC} measurement requires equipment with a 3-dB bandwidth of at least 300 MHz.
9. All input pulses are supplied by a frequency generator with the following characteristics: TR and tF ≤ 1 nS; pulse re-rate = 50 Mpps; pulse width = 10 ± 0.2 nS.



1	LVTTL/LVCMOS

Figure 6. [7]



0	LVDS/LVPECL

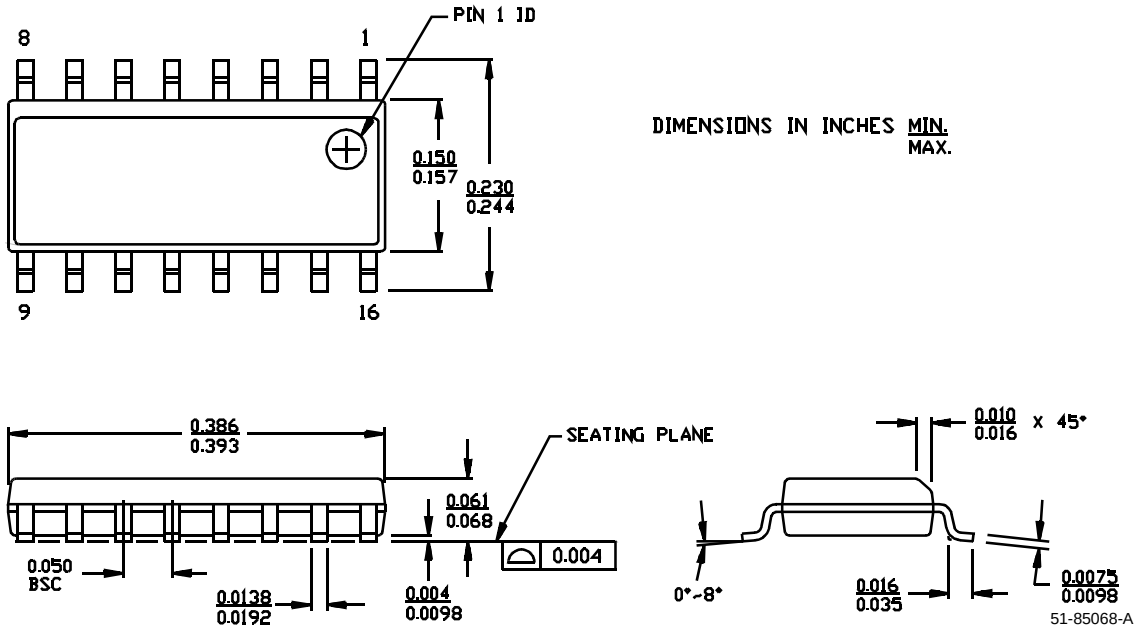
Figure 7. [10]

Ordering Information

Part Number	Package Type	Product Flow
CY2DP814ZI	16-pin TSSOP	Industrial, –40°C to 85°C
CY2DP814ZIT	16-pin TSSOP–Tape and Reel	Industrial, –40°C to 85°C
CY2DP814SI	16-pin SOIC	Industrial, –40°C to 85°C
CY2DP814SIT	16-pin SOIC–Tape and Reel	Industrial, –40°C to 85°C
CY2DP814ZC	16-pin TSSOP	Commercial, 0°C to 70 °C
CY2DP814ZCT	16-pin TSSOP–Tape and Reel	Commercial, 0°C to 70 °C
CY2DP814SC	16-pin SOIC	Commercial, 0°C to 70 °C
CY2DP814SCT	16-pin SOIC–Tape and Reel	Commercial, 0°C to 70 °C

Package Drawing and Dimensions

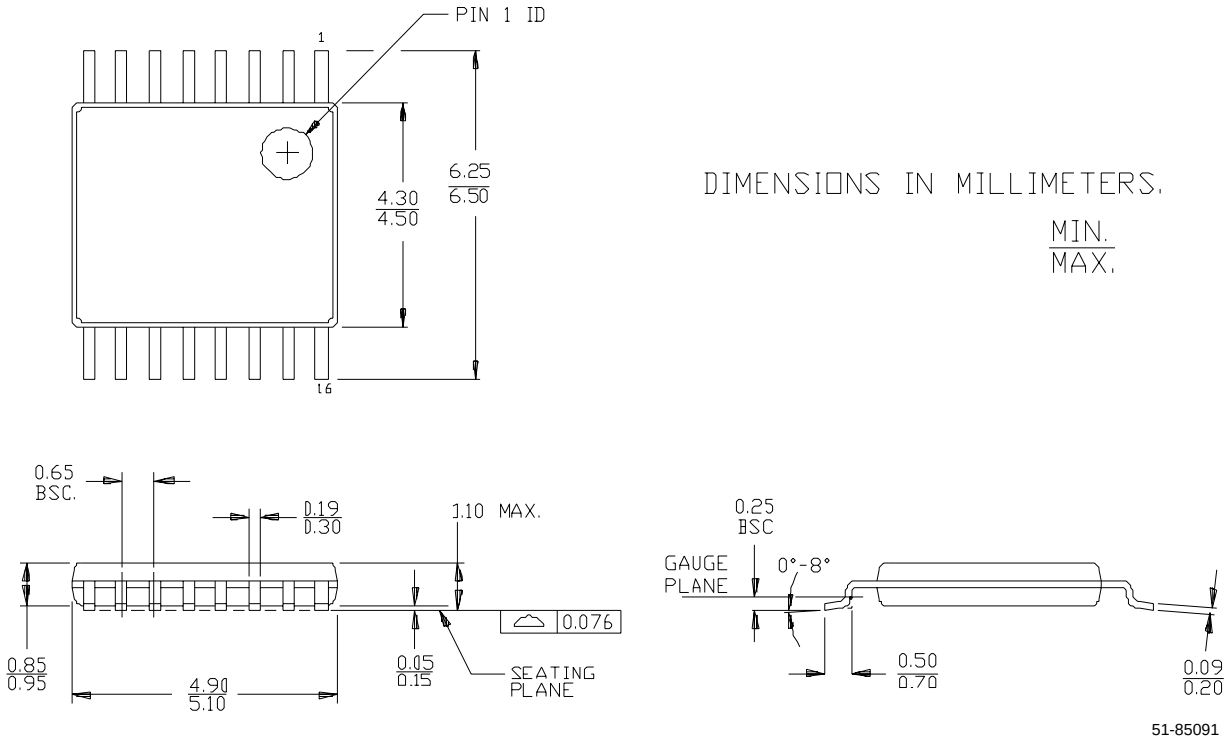
16-lead (150-mil) Molded SOIC S16



Note:
10. LVPECL or LVDS differential input value.

Package Drawings and Dimensions (continued)

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



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Document Title: ComLink™Series CY2DP814 1:4 Clock Fanout Buffer Document Number: 38-07060				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	10785	06/07/01	IKA	Convert from IMI to Cypress
*A	115610	07/02/02	CTK	Range of VCM
*B	122746	12/15/02	RBI	Added power-up requirements to maximum ratings information.