

16-Mbit (1M x 16) Static RAM

Features

- **Very high speed: 55 ns**
- **Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
 - Typical active current: 2 mA @ f = 1 MHz
 - Typical active current: 15 mA @ f = f_{max}
- **Ultra-low standby power**
- **Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball BGA and 48-pin TSOPI**

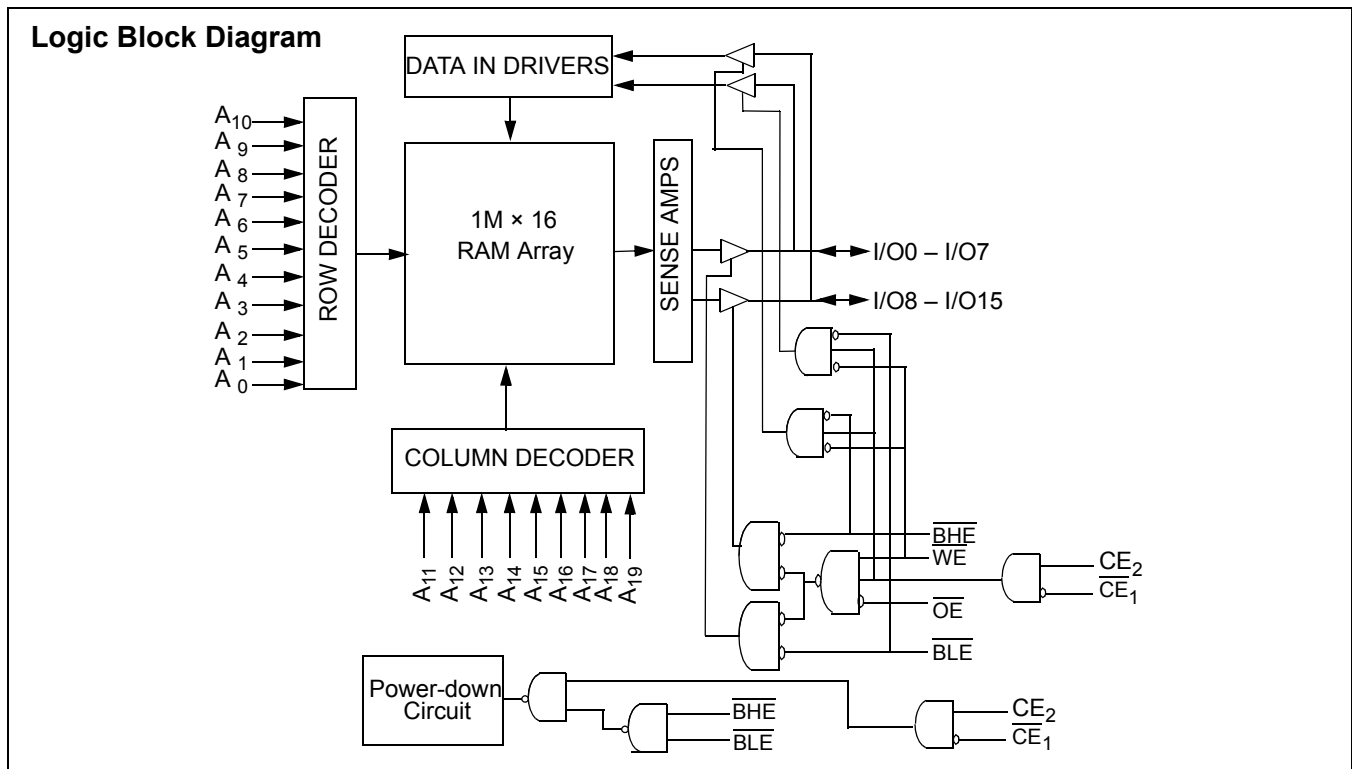
Functional Description^[1]

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly

reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both BHE and BLE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE}_1 HIGH or CE_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a Write operation (\overline{CE}_1 LOW, CE_2 HIGH and WE LOW).

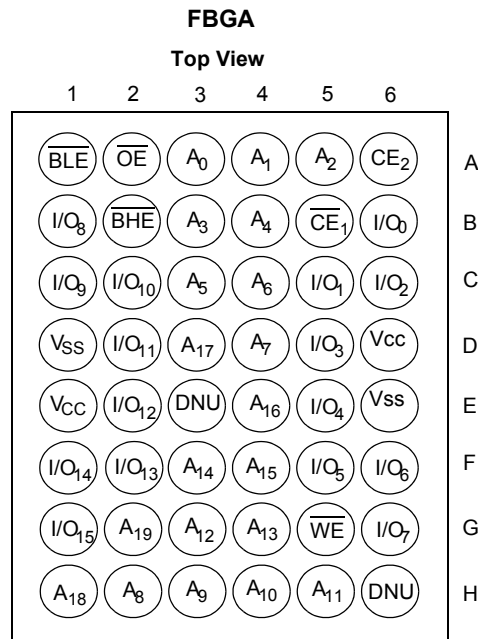
Writing to the device is accomplished by taking Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by taking Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

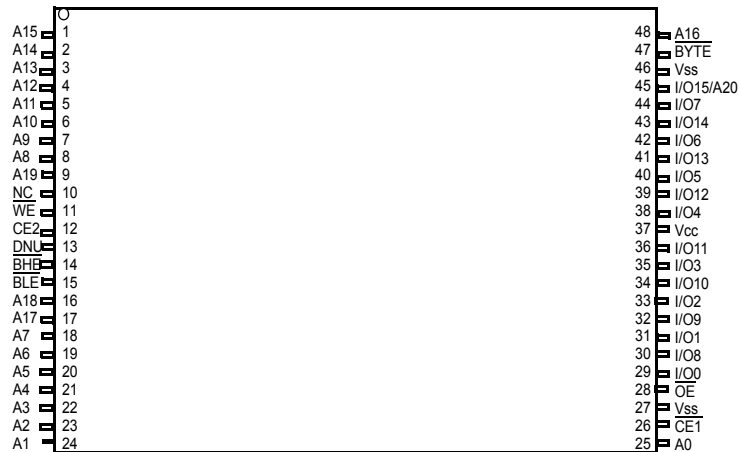


Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2, 3, 4, 5]


48TSOPI (Forward)
Top View


Notes:

2. NC pins are not connected on the die.
3. DNU pins have to be left floating.
4. The BYTE pin in the 48-TSOPI package has to be tied HIGH to use the device as a 1M × 16 SRAM. The 48-TSOPI package can also be used as a 2M × 8 SRAM by tying the BYTE signal LOW. For 2M × 8 Functionality, please refer to the CY62168DV30 datasheet. In the 2M × 8 configuration, Pin 45 is A20.
5. Ball H6 for the FBGA package can be used to upgrade to a 32M density.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C
 Ambient Temperature with Power Applied..... -55°C to + 125°C
 Supply Voltage to Ground Potential -0.2V to V_{CC} + 0.3V
 DC Voltage Applied to Outputs in High-Z State^[6, 7]..... -0.2V to V_{CC} + 0.3V
 DC Input Voltage^[6, 7] -0.2V to V_{CC} + 0.3V

Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[8]
CY62167DV30L	Industrial	-40°C to +85°C	2.20V to 3.60V
CY62167DV30LL			3.60V

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	Min.	Typ. ^[9]	Max.		f = 1MHz		f = f _{max}		Typ. ^[9]	Max.
CY62167DV30L	2.20	3.0	3.60	55	2	4	15	30	2.5	30
				70			12	25		
CY62167DV30LL				55	2	4	15	30	2.5	22
				70			12	25		

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62167DV30-55			CY62167DV30-70			Unit	
			Min.	Typ. ^[9]	Max.	Min.	Typ. ^[9]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA, V _{CC} = 2.20V	2.0			2.0			V	
		I _{OH} = -1.0 mA, V _{CC} = 2.70V	2.4			2.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA, V _{CC} = 2.20V			0.4			0.4	V	
		I _{OL} = 2.1mA, V _{CC} = 2.70V			0.4			0.4	V	
V _{IH}	Input HIGH Voltage	V _{CC} = 2.2V to 2.7V	1.8		V _{CC} + 0.3V	1.8		V _{CC} + 0.3V	V	
		V _{CC} = 2.7V to 3.6V	2.2		V _{CC} + 0.3V	2.2		V _{CC} + 0.3V	V	
V _{IL}	Input LOW Voltage	V _{CC} = 2.2V to 2.7V	-0.3		0.6	-0.3		0.6	V	
		V _{CC} = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} , V _{CC} = V _{CCmax} , I _{OUT} = 0 mA, CMOS levels		15	30		12	25	mA	
		f = 1 MHz		2	4		2	4	mA	
I _{SB1}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE, BLE), V _{CC} = 3.60V	L		2.5	30		2.5	25	μA
			LL		2.5	22		2.5	22	
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.60V	L		2.5	30		2.5	30	μA
			LL		2.5	22		2.5	22	

Notes:

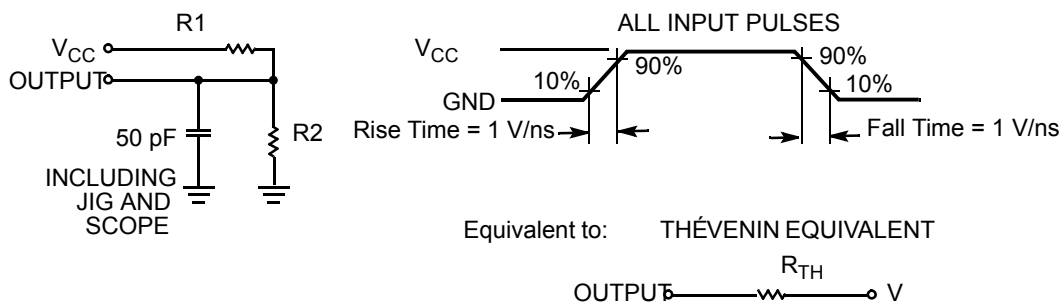
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- V_{IH(Max)} = V_{CC} + 0.75V for pulse durations less than 20 ns.
- Full Device AC operation requires linear V_{CC} ramp from 0 to V_{CC(min.)} >= 500 μs.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Capacitance^[10, 11]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$	8	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

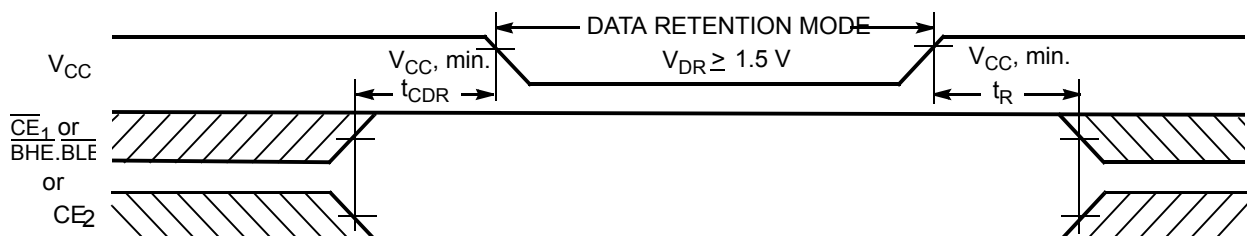
Parameter	Description	Test Conditions	BGA	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[10]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	60	$^\circ\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case) ^[10]		16	4.3	$^\circ\text{C/W}$

AC Test Loads and Waveforms


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[9]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5\text{V}$ $CE_1 \geq V_{CC} - 0.2\text{V}$, $CE_2 \leq 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	L		15	μA
			LL		10	
$t_{CDR}^{[10]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[12]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[13]

Notes:

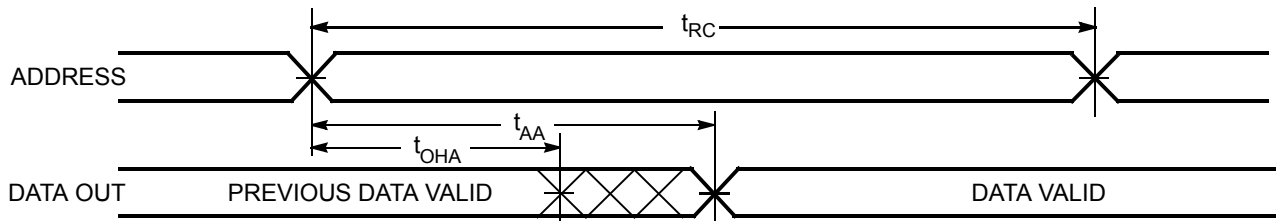
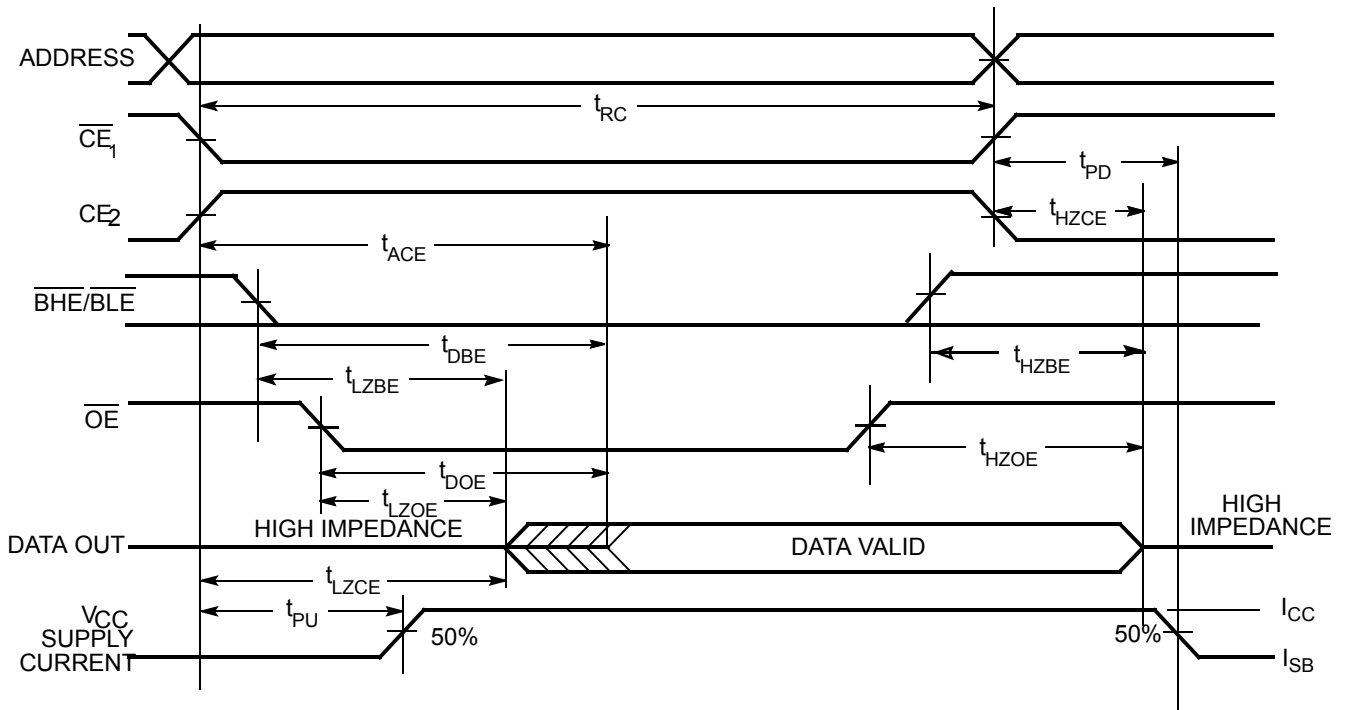
10. Tested initially and after any design or process changes that may affect these parameters.
11. This applies for all packages.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$ or stable at $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$.
13. $\overline{\text{BHE.BLE}}$ is the AND of both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$.

Switching Characteristics Over the Operating Range^[14]

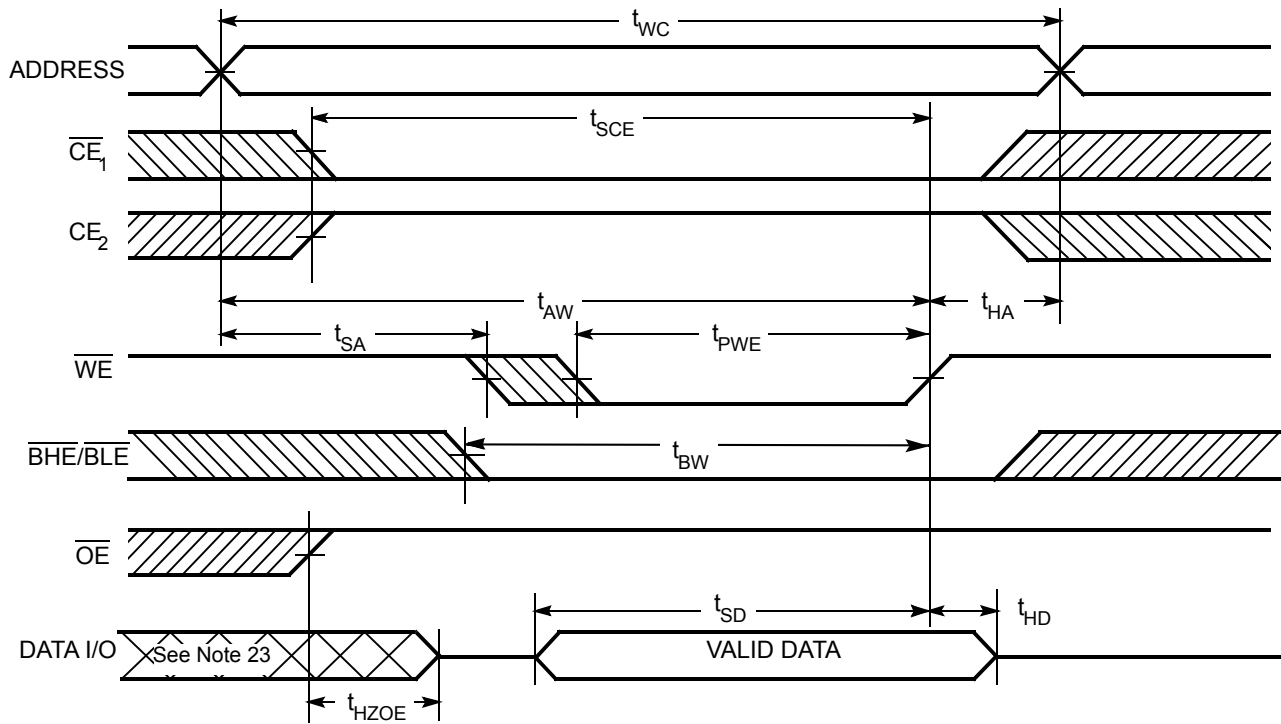
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[15]	5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[15, 16]		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[15]	10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to High Z ^[15, 16]		20		25	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-up	0		0		ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to Power-down		55		70	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[15]	10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z ^[15, 16]		20		25	ns
Write Cycle^[17]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	40		60		ns
t_{AW}	Address Set-Up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	40		45		ns
t_{BW}	$\overline{BLE} / \overline{BHE}$ LOW to Write End	40		60		ns
t_{SD}	Data Set-Up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[15, 16]		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[15]	10		10		ns

Notes:

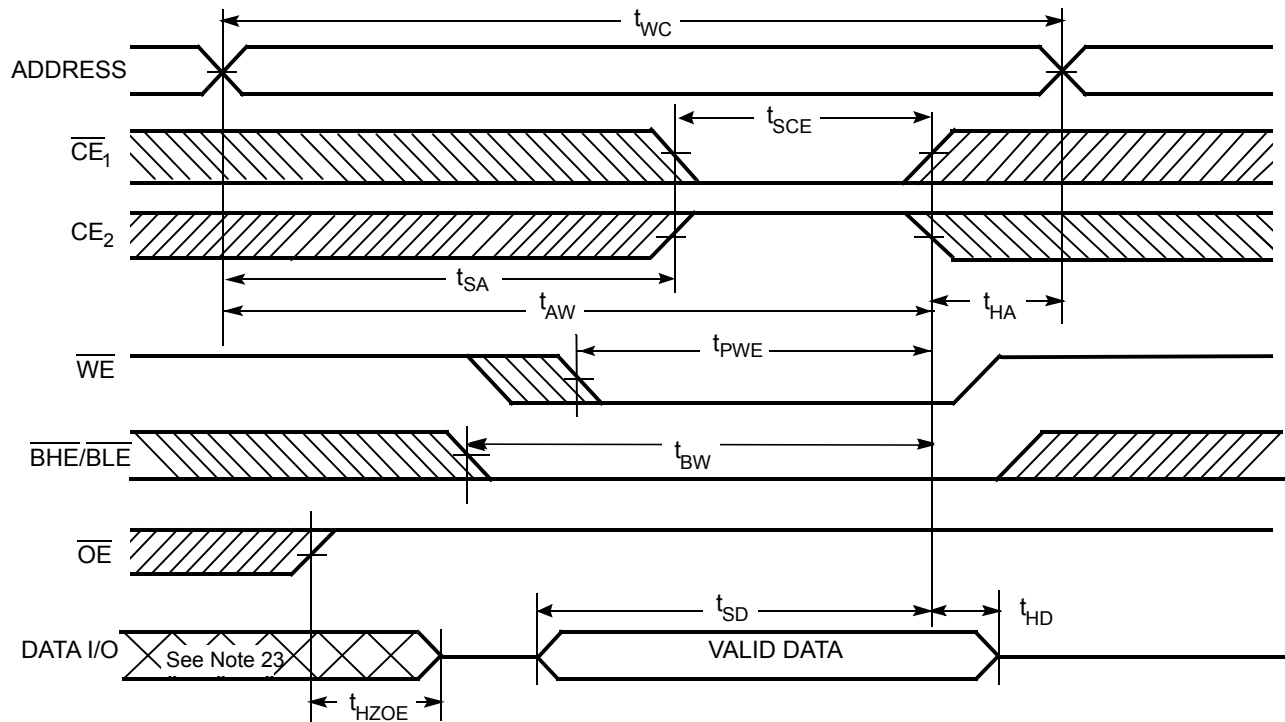
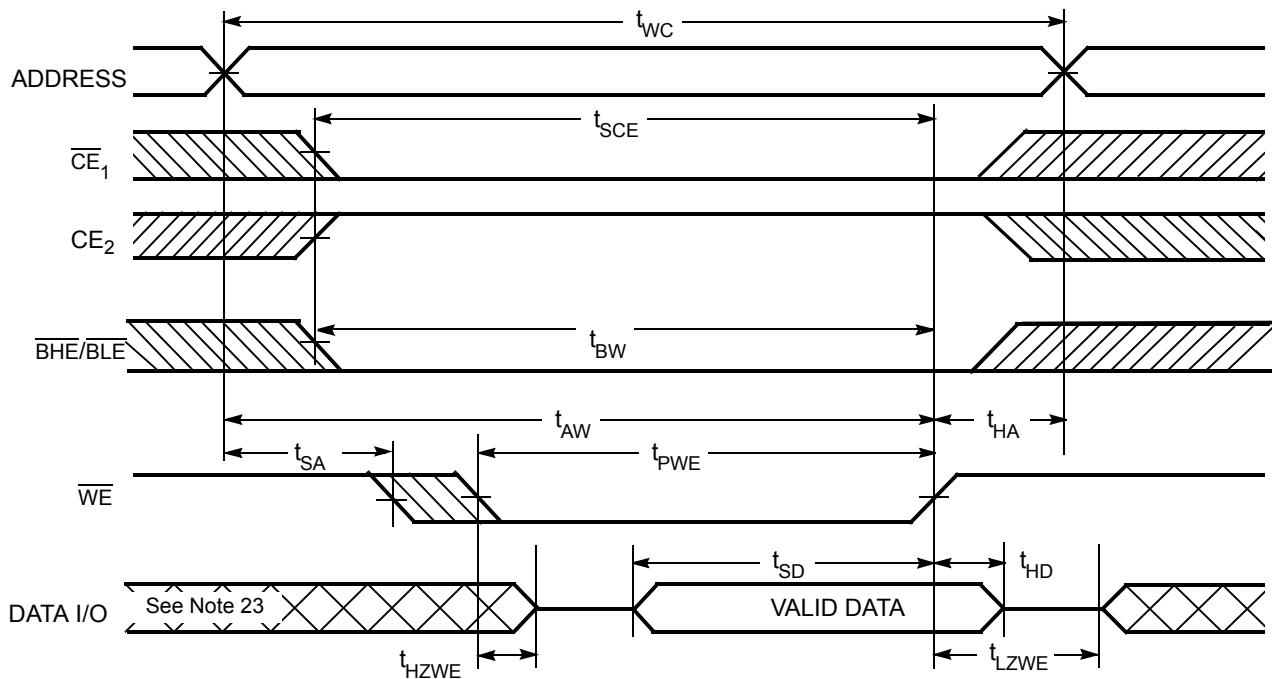
14. Test conditions for all parameters other than three-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

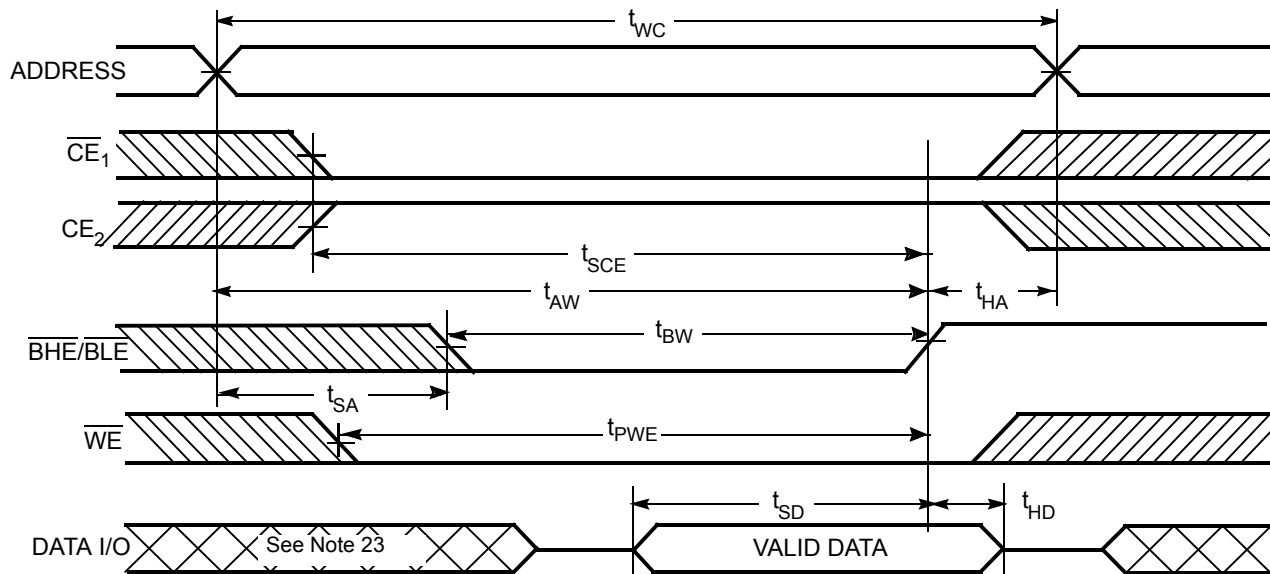
Switching Waveforms
Read Cycle 1 (Address Transition Controlled)^[18, 19]

Read Cycle 2 (\overline{OE} Controlled)^[19, 20]

Notes:

18. The device is continuously selected. OE, CE₁ = V_{IL}, BHE and/or BLE = V_{IL}, and CE₂ = V_{IH}.
 19. WE is HIGH for read cycle.

Switching Waveforms (continued)
Write Cycle 1 (WE Controlled)^[17, 21, 22, 23]

Notes:

20. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and \overline{CE}_2 transition HIGH.
21. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
22. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
23. During this period, the I/Os are in output state and input signals should not be applied.

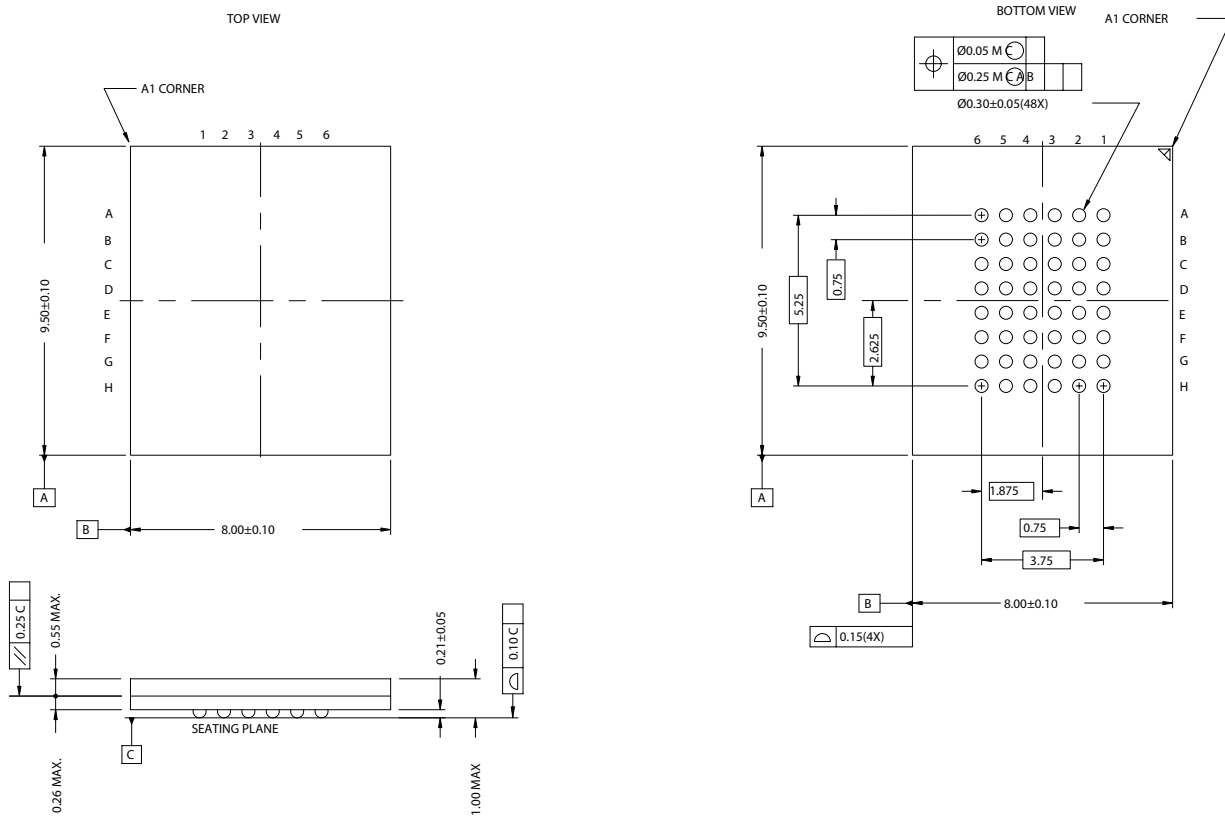
Switching Waveforms (continued)
Write Cycle 2 (\overline{CE}_1 or \overline{CE}_2 Controlled)^[17, 21, 22, 23]

Write Cycle 3 (WE Controlled, OE LOW)^[22, 23]


Switching Waveforms (continued)
Write Cycle 4 (BHE/BLE Controlled, OE LOW)^[22, 23]

Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62167DV30L-55BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-55BVI			
55	CY62167DV30L-55ZI	Z48A	48 Pin TSOP I	Industrial
	CY62167DV30LL-55ZI			
70	CY62167DV30L-70BVI	BV48B	48-ball Fine Pitch BGA (8 mm × 9.5mm × 1 mm)	Industrial
	CY62167DV30LL-70BVI			
70	CY62167DV30L-70ZI	Z48A	48-pin TSOP I	Industrial
	CY62167DV30LL-70ZI			

Package Diagrams
48-Lead VFBGA (8 x 9.5 x 1 mm) BV48B


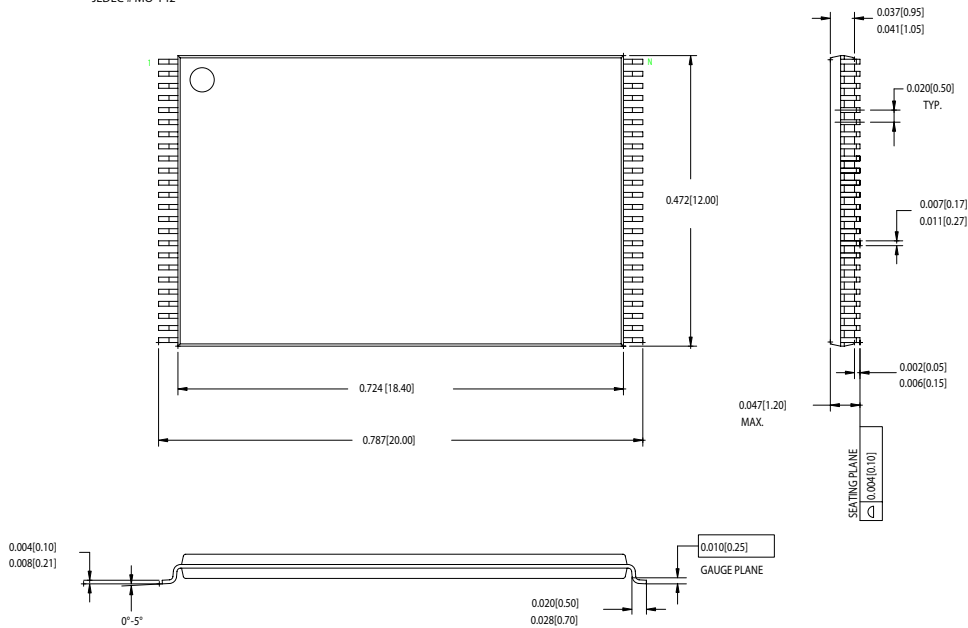
51-85178-**

Package Diagrams
48-Lead TSOP I (12 mm x 18.4 mm x 1.0 mm) Z48A

DIMENSIONS IN INCHES(MM) MIN.

MAX.

JEDEC # MO-142



51-85183-A

MoBL is a registered trademark and More Battery Life is a trademark of Cypress Semiconductor Corporation. All product and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title:CY62167DV30 MoBL [®] 16-Mbit (1M x 16) Static RAM Document Number: 38-05328				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	118408	09/30/02	GUG	New Data Sheet
*A	123692	02/11/03	DPM	Changed Advanced to Preliminary Added package diagram
*B	126555	04/25/03	DPM	Minor change: Changed Sunset Owner from DPM to HRT
*C	127841	09/10/03	XRJ	Added 48 TSOP I package
*D	205701		AJU	Changed BYTE pin usage description for 48 TSOP I package
*E	238050	See ECN	KKV/AJU	Replaced 48-lead VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B