CY7C43643
CY7C43663
CY7C43683

1K/4K/16K x36 Unidirectional Synchronous FIFO with Bus Matching

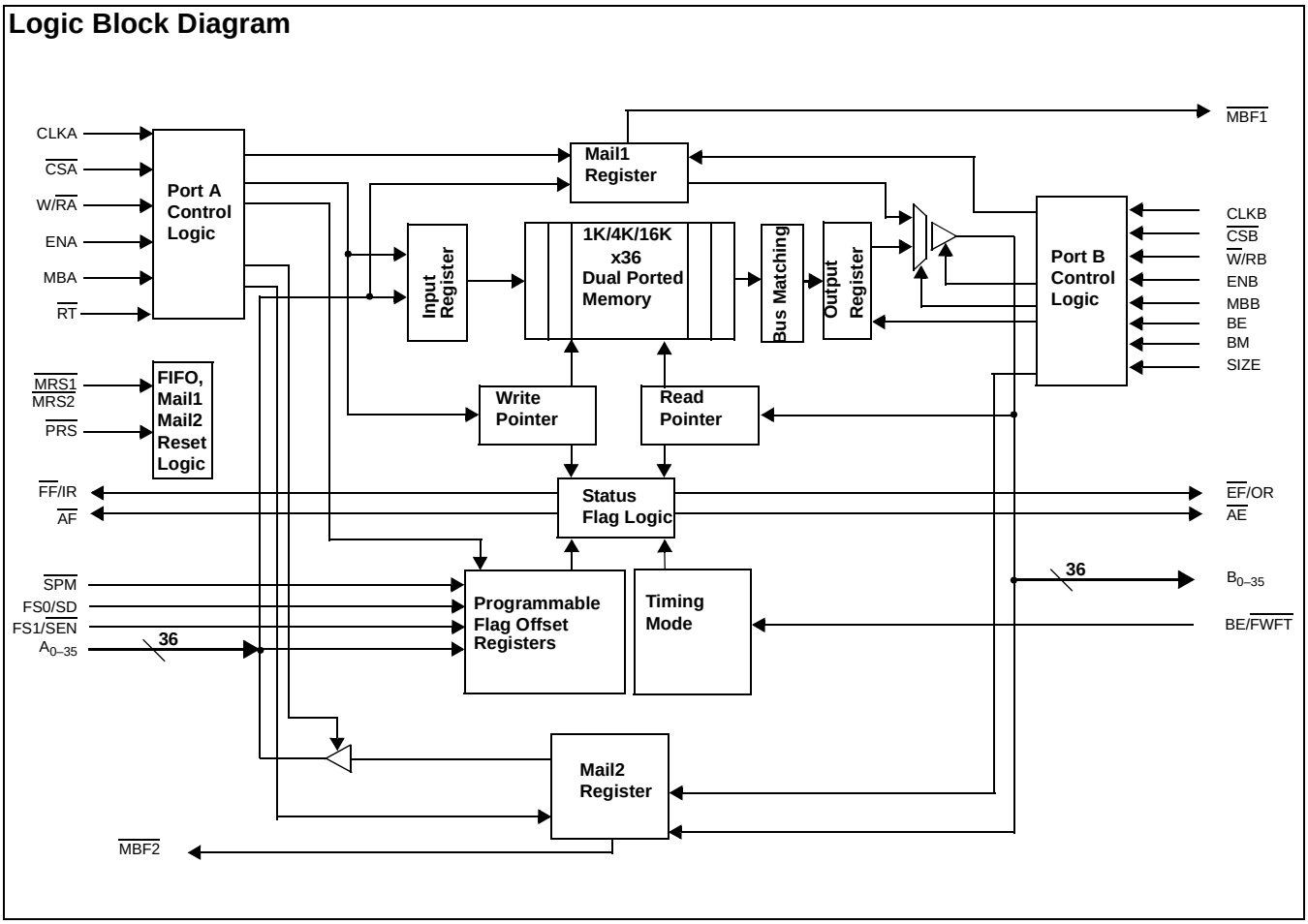
Features

- High-speed, low-power, Unidirectional, First-in, First-out (FIFO) memories w/bus matching capabilities
- 1Kx36 (CY7C43643)
- 4Kx36 (CY7C43663)
- 16Kx36 (CY7C43683)
- 0.35-micron CMOS for optimum speed/power
- High-speed 133-MHz operation (7.5 ns read/write cycle times)
- Low power
  - I_{CC} = 100 mA
  - I_{SB} = 10 mA

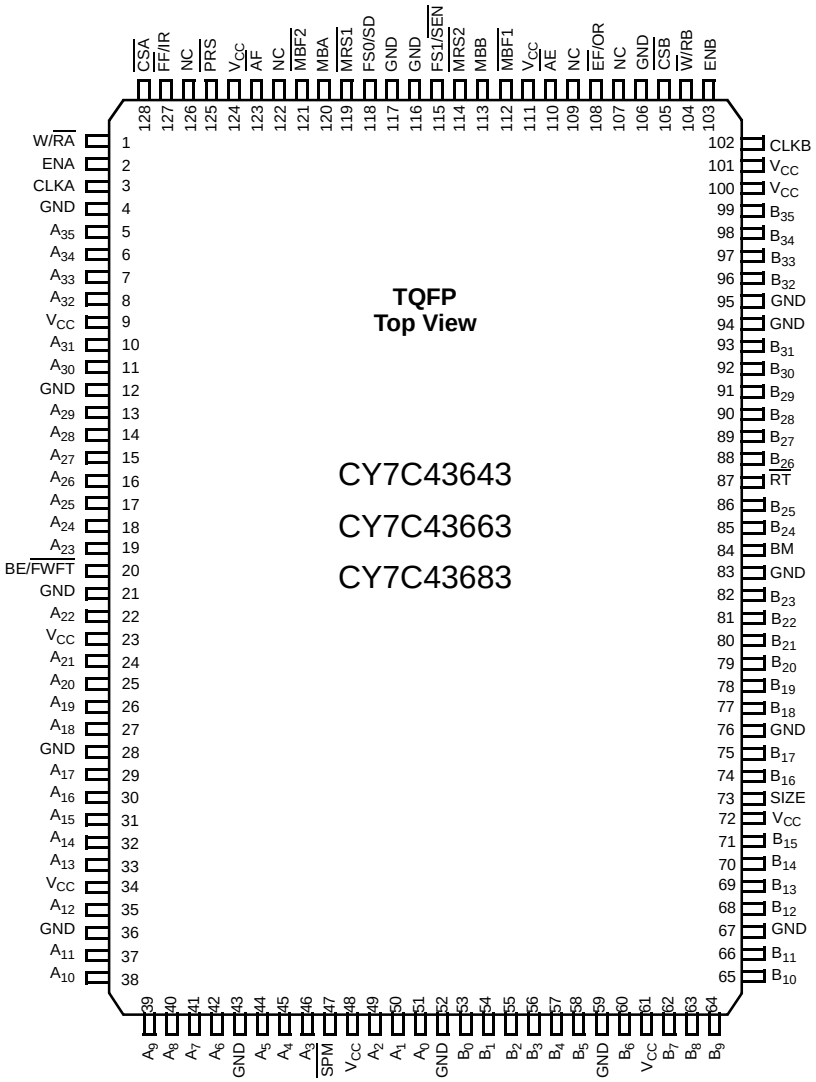
Table 1.

- Fully asynchronous and simultaneous read and write operation permitted
- Mailbox bypass register for each FIFO
- Parallel and Serial Programmable Almost Full and Almost Empty flags
- Retransmit function
- Standard or FWFT mode user selectable
- Partial Reset
- Big or Little Endian format for word or byte bus sizes
- 128-pin TQFP packaging
- Easily expandable in width and depth

Logic Block Diagram



Pin Configuration



Selection Guide

		CY7C43643/63/83 –7	CY7C43643/63/83 –10	CY7C43643/63/83 –15	Unit
Maximum Frequency		133	100	66.7	MHz
Maximum Access Time		6	8	10	ns
Minimum Cycle Time		7.5	10	15	ns
Minimum Data or Enable Set-up		3	4	5	ns
Minimum Data or Enable Hold		0	0	0	ns
Maximum Flag Delay		6	8	8	ns
Active Power Supply Current (I_{CC1})	Commercial	100	100	100	mA
	Industrial			100	

	CY7C43643	CY7C43663	CY7C43683
Density	1K x 36	4K x 36	16K x 36
Package	128 TQFP	128 TQFP	128 TQFP

Pin Definitions

Signal Name	Description	I/O	Function
$A_{0–35}$	Port A Data	I	**36-bit unidirectional data port for side A**.
$\overline{AE}$	Almost Empty Flag (Port B)	O	**Programmable Almost Empty flag synchronized to CLKA**. It is LOW when the number of words in the FIFO2 is less than or equal to the value in the Almost Empty A offset register, X.[1]
$\overline{AF}$	Almost Full Flag	O	**Programmable Almost Full flag synchronized to CLKA**. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Almost Full A offset register, Y.[1]
$B_{0–35}$	Port B Data	O	**36-bit unidirectional data port for side B**.
BE/$\overline{FWFT}$	Big Endian/First-Word Fall-Through Select	I	**This is a dual-purpose pin**. During Master Reset, a HIGH on BE will select Big Endian operation. In this case, depending on the bus size, the most significant byte or word on Port A is transferred to Port B first. A LOW on BE will select Little Endian operation. In this case, the least significant byte or word on Port A is transferred to Port B first. After Master Reset, this pin selects the timing mode. A HIGH on $\overline{FWFT}$ selects CY Standard Mode, a LOW selects First-Word Fall-Through Mode. Once the timing mode has been selected, the level on $\overline{FWFT}$ must be static throughout device operation.
BM	Bus Match Select (Port B)	I	**A HIGH on this pin enables either byte or word bus width on Port B**, depending on the state of SIZE. A LOW selects long-word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.
CLKA	Port A Clock	I	**CLKA is a continuous clock that synchronizes all data transfers through Port A** and can be asynchronous or coincident to CLKB. $\overline{FF}$/IR and $\overline{AF}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	**CLKB is a continuous clock that synchronizes all data transfers through Port B** and can be asynchronous or coincident to CLKA. $\overline{FB}$/IR, $\overline{EF}$/OR, $\overline{AF}$, and $\overline{AE}$ are all synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	**$\overline{CSA}$ must be LOW to enable a LOW-to HIGH transition of CLKA** to read or write on Port A. The $A_{0–35}$ outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	**$\overline{CSB}$ must be LOW to enable a LOW-to HIGH transition of CLKB** to read or write on Port B. The $B_{0–35}$ outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$/OR	Empty/Output Ready Flag (Port B)	O	**This is a dual-function pin**. In the CY Standard Mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In the FWFT mode, the OR function is selected. OR indicates the presence of valid data on $A_{0–35}$ outputs, available for reading. $\overline{EF}$/OR is synchronized to the LOW-to-HIGH transition of CLKB. [2]
ENA	Port A Enable	I	**ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA** to read or write data on Port A.
ENB	Port B Enable	I	**ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB** to read or write data on Port B.
$\overline{FF}$/IR	Port B Full/Input Ready Flag	O	**This is a dual-function pin**. In the CY Standard Mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the IR function is selected. IR indicates whether or not there is space available for writing to the FIFO memory. $\overline{FF}$/IR is synchronized to the LOW-to-HIGH transition of CLKA.

Notes:

1. When reading from the FIFO under FWFT, ORA/ORB signal should be included in the read logic to ensure proper operation. To read without gating the boundary flag (e.g., in bursts), use CY standard mode.
2. When FIFO is operated at the almost empty/full boundary, there may be an uncertainty of up to three clock cycles for flag assertion and deassertion. Refer to "Designing with CY7C436xx Synchronous FIFO" application notes for more details on flag uncertainties.

Pin Definitions (continued)

Signal Name	Description	I/O	Function
FS1/$\overline{SEN}$	Flag Offset Select 1/Serial Enable	I	**FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming**. During Master Reset, FS1/$\overline{SEN}$ and FS0/SD, together with SPM, select the flag offset programming method. Three offset register programming methods are available: automatically load one of three preset values (8, 16, or 64), parallel load from Port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA loads the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 20 for the CY7C43643, 24 for the CY7C43663, and 28 for the CY7C43683. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
FS0/SD	Flag Offset Select 0/Serial Data	I	
MBA	Port A Mailbox Select	I	**A HIGH level on MBA chooses a mailbox register for a Port A** read or write operation.
MBB	Port B Mailbox Select	I	**A HIGH level on MBB chooses a mailbox register** for a Port B read or write operation. When a read operation is performed on Port B, a HIGH level on MBB selects data from the Mail1 register for output and a LOW level selects FIFO output register data for output. Data can only be written into Mail 2 register through Port B (MBB HIGH) and not into the FIFO memory.
$\overline{MBF1}$	Mail1 Register Flag	O	**$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA** that writes data to the Mail1 register. Writes to the Mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Master or Partial Reset.
$\overline{MBF2}$	Mail2 Register Flag	O	**$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB** that writes data to the Mail2 register. Writes to the Mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Master or Partial Reset of FIFO2.
$\overline{MRS1}$	Master Reset	I	**A LOW on this pin initializes the FIFO read and write pointers** to the first location of memory and sets the Port B output register to all zeroes. A LOW pulse on $\overline{MRS1}$ selects the programming method (serial or parallel) and one of three programmable flag default offsets. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS1}$ is LOW.
$\overline{MRS2}$	Master Reset	I	**A LOW on this pin initializes the Mail2 register**.
$\overline{PRS}$	Partial Reset	I	**A LOW on this pin initializes the FIFO read and write pointers** to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{RT}$	Retransmit	I	**A LOW strobe on this pin will retransmit data on the FIFO**. This is achieved by bringing the read pointer back to location zero. The user will still need to perform read operation to retransmit the data. Retransmit function applies to CY standard mode only.
SIZE	Bus Size Select	I	**A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B**. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation.
$\overline{SPM}$	Serial Programming	I	**A LOW on this pin selects serial programming of partial flag offsets**. A HIGH on this pin selects parallel programming or default offsets (8, 16, or 64).
W/$\overline{RA}$	Port A Write/Read Select	I	**A HIGH selects a write operation and a LOW selects a read operation on Port A** for a LOW-to-HIGH transition of CLKA. The $A_{0–35}$ outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port B Write/Read Select	I	**A LOW selects a write operation and a HIGH selects a read operation on Port B** for a LOW-to-HIGH transition of CLKB. The $B_{0–35}$ outputs are in the high-impedance state when $\overline{W}$/RB is LOW.

Functional Description

The CY7C436x3 is a monolithic, high-speed, low-power, CMOS Unidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 133 MHz and has read access times as fast as 6 ns. Two independent 1K/4K/16K x 36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions. FIFO data on Port B can be output in 36-bit, 18-bit, or 9-bit formats with a choice of Big or Little Endian configurations.

The CY7C436x3 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple unidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFOs via two mailbox registers. The mailbox registers' width matches the selected Port B bus width. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on the CY7C436x3: Master Reset and Partial Reset. Master Reset initializes the read and write pointers to the first location of the memory array, configures the FIFO for Big or Little Endian byte arrangement and selects serial flag programming, parallel flag programming, or one of the three possible default flag offset settings, 8, 16, or 64. The FIFO also has two Master Reset pins, $\overline{MRS1}$ and $\overline{MRS2}$.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings. The FIFO has its own independent Partial Reset pin, $\overline{PRS}$.

The CY7C436x3 have two modes of operation: In the CY Standard Mode, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the First-Word Fall-Through Mode (FWFT), the first long-word (36-bit wide) written to an empty FIFO appears automatically on the outputs, no read operation required (nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/FWFT pin during FIFO operation determines the mode in use.

The FIFO has a combined Empty/Output Ready flag ($\overline{EF}$/OR) and a combined Full/Input Ready flag ($\overline{FF}$/IR). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the CY Standard Mode. $\overline{EF}$ indicates whether the memory is full or not. The IR and OR functions are selected in the First-Word Fall-Through Mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.[1]

The FIFO has a programmable Almost Empty flag ($\overline{AE}$) and a programmable Almost Full flag ($\overline{AF}$). $\overline{AE}$ indicates when a selected number of words written to FIFO memory achieve a predetermined "almost empty state." $\overline{AF}$ indicates when a selected number of words written to the memory achieve a predetermined "almost full state."[2]

IR and $\overline{AF}$ are synchronized to the port clock that writes data into its array. OR and $\overline{AE}$ are synchronized to the port clock that reads data from its array. Programmable offset for $\overline{AE}$ and $\overline{AF}$ can be loaded in parallel using Port A or in serial via the $\overline{SD}$ input. Three default offset settings are also provided. The $\overline{AE}$ threshold can be set at 8, 16, or 64 locations from the empty boundary and $\overline{AF}$ threshold can be set at 8, 16, or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

Two or more devices may be used in parallel to create wider data paths.

The CY7C436x3 are characterized for operation from 0°C to 70°C commercial, and from –40°C to 85°C industrial. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Signal Description

Master Reset ($\overline{MRS1}$, $\overline{MRS2}$)

The FIFO memory of the CY7C436x3 undergoes a complete reset by taking its associated Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Master Reset input can switch asynchronously to the clocks. A Master Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost Empty flag ($\overline{AE}$) LOW, and the Almost Full flag ($\overline{AF}$) HIGH. A Master Reset also forces the Mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation. A Master Reset must be performed on the FIFO after power up, before data is written to its memory.

A LOW-to-HIGH transition on a FIFO Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input latches the value of the Big Endian (BE) input or determining the order by which bytes are transferred through Port B.

A LOW-to-HIGH transition on a FIFO reset ($\overline{MRS1}$, $\overline{MRS2}$) input latches the values of the Flag select (FS0, FS1) and Serial Programming Mode ($\overline{SPM}$) inputs for choosing the Almost Full and Almost Empty offset programming method (see Almost Empty and Almost Full flag offset programming below).

Partial Reset ($\overline{PRS}$)

Each of the two FIFO memories of the CY7C436x3 undergoes a limited reset by taking its associated Partial Reset ($\overline{PRS}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Partial Reset inputs can switch asynchronously to the clocks. A Partial Rest initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost Empty flag ($\overline{AE}$) LOW, and the Almost Full flag ($\overline{AF}$) HIGH. A Partial Reset also forces the Mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or IDT Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where

reprogramming a FIFO following a Master Reset would be inconvenient.

Big Endian/First-Word Fall-Through (BE/$\overline{\text{FWFT}}$)

This is a dual-purpose pin. At the time of Master Reset, the BE select function is active, permitting a choice of Big or Little Endian byte arrangement for data written to or read from Port B. This selection determines the order by which bytes (or words) of data are transferred through this port. For the following illustrations, assume that a byte (or word) bus size has been selected for Port B. (Note that when Port B is configured for a long-word size, the Big Endian function has no application and the BE input is a “Don’t Care.”

A HIGH on the BE/$\overline{\text{FWFT}}$ input when the Master Reset ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) inputs go from LOW to HIGH will select a Big Endian arrangement. When data is moving in the direction from Port A to Port B, the most significant byte (word) of the long-word written to Port A will be transferred to Port B first; the least significant byte (word) of the long-word written to Port A will be transferred to Port B last.

A LOW on the BE/$\overline{\text{FWFT}}$ input when the Master Reset ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) inputs go from LOW to HIGH will select a Little Endian arrangement. When data is moving in the direction from Port A to Port B, the least significant byte (word) of the long-word written to Port A will be transferred to Port B first; the most significant byte (word) of the long-word written to Port A will be transferred to Port B last. After Master Reset, the FWFT select function is active, permitting a choice between two possible timing modes: CY Standard Mode or First-Word Fall-Through (FWFT) Mode. Once the Master Reset ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) input is HIGH, a HIGH on the BE/$\overline{\text{FWFT}}$ input at the second LOW-to-HIGH transition of CLKA will select CY Standard Mode. This mode uses the Empty Flag function ($\overline{\text{EF}}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{\text{FF}}$) to indicate whether or not the FIFO memory has any free space for writing. In CY Standard Mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Master Reset ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) input is HIGH, a LOW on the BE/$\overline{\text{FWFT}}$ input during the next LOW-to-HIGH transition of CLKA will select FWFT Mode. This mode uses the Output Ready function (OR) to indicate whether or not there is valid data at the data outputs ($B_{0–35}$). It also uses the Input Ready function (IR) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Master Reset, the level applied to the BE/$\overline{\text{FWFT}}$ input to choose the desired timing mode must remain static throughout the FIFO operation.

Programming the Almost Empty and Almost Full Flags

Two registers in the CY7C436x3 are used to hold the offset values for the Almost Empty and Almost Full flags. The Port B Almost Empty flag ($\overline{\text{AE}}$) offset register is labeled X. The Port A Almost Full flag ($\overline{\text{AF}}$) offset register is labeled Y. The index of each register name corresponds with preset values during the reset of a FIFO, programmed in parallel using the FIFO’s Port A data inputs, or programmed in serial using the Serial Data (SD) input (see *Table 2*).

To load a FIFO’s Almost Empty flag and Almost Full flag offset registers with one of the three preset values listed in *Table 2*, the Serial Program Mode ($\overline{\text{SPM}}$) and at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of its Master Reset input ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$). For example, to load the preset value of 64 into X and Y, $\overline{\text{SPM}}$, FS0 and FS1 must be HIGH when the FIFO reset ($\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) returns HIGH. When using one of the preset values for the flag offsets, the FIFO can be reset simultaneously or at different times.

To program the X and Y registers from Port A, perform a Master Reset on both FIFOs simultaneously with $\overline{\text{SPM}}$ HIGH and FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{\text{MRS1}}$/$\overline{\text{MRS2}}$. After this reset is complete, the first two writes to the FIFO do not store data in RAM but load the offset registers in the order Y and X. The Port A data inputs used by the offset registers are ($A_{0–9}$), ($A_{0–11}$), or ($A_{0–13}$),for the CY7C436x3, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 0 to 1023 for the CY7C43643; 0to 4095 for the CY7C43663; 0 to 16383 for the CY7C43683. Before programming the offset register, $\overline{\text{FF}}$/IR is set HIGH. FIFOs begin normal operation after programming is done.

To program the X and Y registers serially, initiate a Master Reset with $\overline{\text{SPM}}$ LOW, FS0/$\overline{\text{SD}}$ LOW, and FS1/$\overline{\text{SEN}}$ HIGH during the LOW-to-HIGH transition of $\overline{\text{MRS1}}$/$\overline{\text{MRS2}}$. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/$\overline{\text{SD}}$ input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{\text{SEN}}$ input is LOW. Twenty, twenty four, or twenty eight bit writes are needed to complete the programming for the CY7C436x3, respectively. The two registers are written in the order Y then finally X. The first-bit write stores the most significant bit of the Y register and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 0 to 1023 for the CY7C43643; 0to 4095 for the CY7C43663; 0 to 16383 (Cy7c43683).

When the option to program the offset registers serially is chosen, the Port A Full/Input Ready ($\overline{\text{FF}}$/IR) flag remains LOW until all register bits are written. $\overline{\text{FF}}$/IR is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO operation.

$\overline{\text{SPM}}$, FS0/$\overline{\text{SD}}$, and FS1/$\overline{\text{SEN}}$ function the same way in both CY Standard and FWFT modes.

FIFO Write/Read Operation

The state of the Port A data ($A_{0–35}$) lines is controlled by Port A Chip Select ($\overline{\text{CSA}}$) and Port A Write/Read Select (W/$\overline{\text{RA}}$). The $A_{0–35}$ lines are in the high-impedance state when either $\overline{\text{CSA}}$ or W/$\overline{\text{RA}}$ is HIGH. The $A_{0–35}$ lines are active mail 2 register outputs when both $\overline{\text{CSA}}$ and W/$\overline{\text{RA}}$ are LOW.

Data is loaded into the FIFO from the $A_{0–35}$ inputs on a LOW-to-HIGH transition of CLKA when $\overline{\text{CSA}}$ is LOW, W/$\overline{\text{RA}}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{\text{FF}}$/IR is HIGH (see *Table 3*). FIFO writes on Port A are independent of any concurrent Port B operation.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read Select (W/$\overline{\text{RB}}$) is the inverse of the Port A Write/Read Select (W/$\overline{\text{RA}}$). The state of the Port B data ($B_{0–35}$) lines is controlled by the Port B Chip Select ($\overline{\text{CSB}}$) and Port B Write/Read Select (W/$\overline{\text{RB}}$). The $B_{0–35}$

lines are in the high-impedance state when either $\overline{CSB}$ is HIGH or W/RB is LOW. The $B_{0–35}$ lines are active outputs when $\overline{CSB}$ is LOW and W/RB is HIGH.

Data is read from the FIFO to the $B_{0–35}$ outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/RB is HIGH, ENB is HIGH, MBB is LOW, and $\overline{EF}$/OR is HIGH (see *Table 4*). FIFO reads and writes on Port B are independent of any concurrent Port A operation.

The Set-up and hold time constraints to the port clocks for the port Chip Selects and Write/Read Selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select and Write/Read Select may change states during the Set-up and hold time window of the cycle.

When operating the FIFO in FWFT Mode with the Output Ready flag LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read Select, Enable, and Mailbox Select.

When operating the FIFO in CY Standard Mode, regardless of whether the Empty Flag is LOW or HIGH, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read Select, Enable, and Mailbox Select.

Synchronized FIFO Flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of the metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{EF}$/OR and $\overline{AE}$ are synchronized to CLKA. FF/IR and AF are synchronized to CLKB. *Table 5* shows the relationship of each port flag to the FIFO.

Empty/Output Ready Flags ($\overline{EF}$/OR)

These are dual-purpose flags. In the FWFT Mode, the Output Ready (OR) function is selected. When the Output Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.[1]

In the CY Standard Mode, the Empty Flag ($\overline{EF}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's RAM memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. For both the FWFT and CY Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, or empty+1.

In FWFT Mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In the CY Standard Mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Full/Input Ready Flags ($\overline{FF}$/IR)

This is a dual-purpose flag. In FWFT Mode, the Input Ready (IR) function is selected. In CY Standard Mode, the Full Flag ($\overline{FF}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. For both FWFT and CY Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, or full–1. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Almost Empty Flags ($\overline{AE}$)

The Almost Empty flag of the FIFO is synchronized to port B clock. The state machine that controls an Almost Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, or almost empty+1. The Almost Empty state is defined by the contents of register X for $\overline{AE}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words[2].

Two LOW-to-HIGH transitions of the Almost Empty flag synchronizing clock are required after a FIFO write for its Almost Empty flag to reflect the new level of fill. Therefore, the Almost empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Almost Full Flags ($\overline{AFA}$, $\overline{AFB}$)

The Almost Full flag of the FIFO is synchronized to port A clock. The state machine that controls an Almost Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, or almost full–1. The Almost Full state is defined by the contents of register Y for AF. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Full flag is LOW when the number of words in its FIFO is greater than or equal to (1024–Y), (4096–Y), or (16384–Y) for the CY7C436x3 respectively. An Almost Full flag is HIGH when the number of words in its FIFO is less than or equal to [1024–(Y+1)], [4096–(Y+1)], or [16384–(Y+1)], for the CY7C436x3 respectively.[2]

Two LOW-to-HIGH transitions of the Almost Full flag synchronizing clock are required after a FIFO read for its Almost Full flag to reflect the new level of fill. Therefore, the Almost Full flag of a FIFO containing [1024/4096/16384–(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [1024/4096/16384–(Y+1)]. An Almost Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [1024/4096/16384–(Y+1)]. A LOW-to-HIGH transition of an Almost Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [1024/4096/16384–(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Mailbox Registers

Each FIFO has a 36-bit bypass register to pass command and control information between Port A and Port B without putting it in queue. The Mailbox Select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes $A_{0\text{-}35}$ data to the Mail1 Register when a Port A write is selected by CSA, W/$\overline{RA}$, and ENA with MBA HIGH. If the selected Port A bus size is also 36 bits, then the usable width of the Mail1 Register employs data lines $A_{0–35}$. If the selected Port A bus size is 18 bits, then the usable width of the Mail1 Register employs data lines $A_{0\text{-}17}$. (In this case, $A_{18–35}$ are “don’t care” inputs.) If the selected Port A bus size is 9 bits, then the usable width of the Mail1 Register employs data lines $A_{0–8}$. (In this case, $A_{9–35}$ are “don’t care” inputs.)

A LOW-to-HIGH transition on CLKB writes $B_{0\text{-}35}$ data to the Mail2 register when a Port B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. If the selected Port B bus size is also 36 bits, then the usable width of the Mail2 Register employs data lines $B_{0–35}$. If the selected Port B bus size is 18 bits, then the usable width of the Mail2 register employs data lines $B_{0–17}$. (In this case, $B_{18–35}$ are “don’t care” inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail2 Register employs data lines $B_{0\text{-}8}$. (In this case, $B_{9\text{-}35}$ are “don’t care” inputs.)

Writing data to a mail register sets its corresponding flag (MBF1 or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox Select input is LOW and from the mail register when the port Mailbox Select input is HIGH.

The Mail1 Register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on $B_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $B_{0–17}$. (In this case, $B_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $B_{0–8}$. (In this case, $B_{9–35}$ are indeterminate.)

The Mail2 Register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A read is selected by CSA, W/RA, and ENA with MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on $A_{0–35}$. For an 18-bit bus size, 18 bits of mailbox data are placed on $A_{0–17}$. (In this case, $A_{18–35}$ are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data are placed on $A_{0–8}$. (In this case, $A_{9–35}$ are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian Select feature has no effect on the mailbox data.

Bus Sizing

The Port B bus can be configured in a 36-bit long-word, 18-bit word, or 9-bit byte format for data read from FIFO. The levels applied to the Port B Bus Size Select (SIZE) and the Bus Match Select (BM) determine the Port B bus size. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH.

Two different methods for sequencing data transfer are available for Port B when the bus size selection is either byte-or word-size. They are referred to as Big Endian (most significant byte first) and Little Endian (least significant byte first). The level applied to the Big Endian Select (BE) input during the LOW-to-HIGH transition of $\overline{MRS1}$/$\overline{MRS2}$ selects the endian method that will be active during FIFO operation. BE is a don’t care input when the bus size selected for Port B is long-word. The endian method is implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH.

Only 36-bit long-word data is written to or read from the two FIFO memories on the CY7C436x3. Bus-matching operations are done after data is read from the FIFO. These bus-matching

operations are not available when transferring data via mailbox registers. Furthermore, both the word- and byte-size bus selections limit the width of the data bus that can be used for mail register operations. In this case, only those byte lanes belonging to the selected word- or byte-size bus can carry mailbox data. The remaining data outputs will be indeterminate. The remaining data inputs will be don't care inputs. For example, when a word-size bus is selected, then mailbox data can be transmitted only between $A_{0–17}$ and $B_{0–17}$. When a byte-size bus is selected, then mailbox data can be transmitted only between $A_{0–8}$ and $B_{0–8}$.

Bus-Matching FIFO Reads

Data is read from the FIFO RAM in 36-bit long-word increments. If a long-word bus size is implemented, the entire long-word immediately shifts to the FIFO output register. If byte or word size is implemented on Port B, only the first one or two bytes appear on the selected portion of the FIFO output register, with the rest of the long-word stored in auxiliary registers. In this case, subsequent FIFO reads output the rest of the long-word to the FIFO output register.

When reading data from the FIFO in the byte or word format, the unused $B_{0–35}$ outputs are indeterminate.

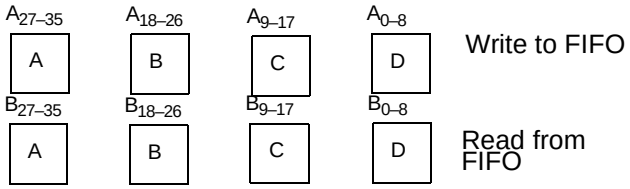
Retransmit ($\overline{RT}$)

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. Retransmit function applies to CY standard mode only.

The number of 36-/18-/9-bit words written into the FIFO should be less than full depth minus 2/4/8 words between the reset of the FIFO (master or partial) and Retransmit setup. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. CLKA and CLKB may be free-running but ENB must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also. The full depth of the FIFO can be repeatedly transmitted.

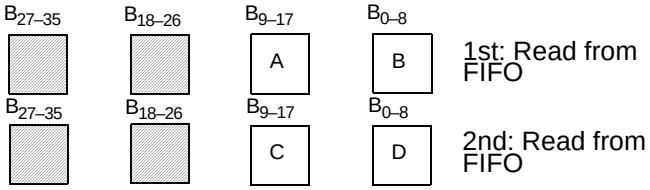
BYTE ORDER ON PORT A:

BE	BM	SIZE
X	L	X



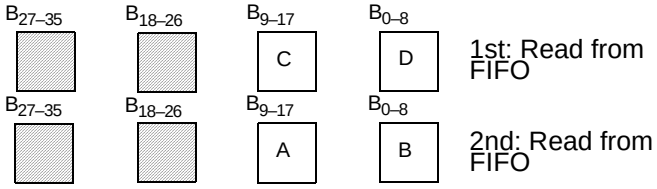
(a) LONG WORD SIZE

BE	BM	SIZE
H	H	L



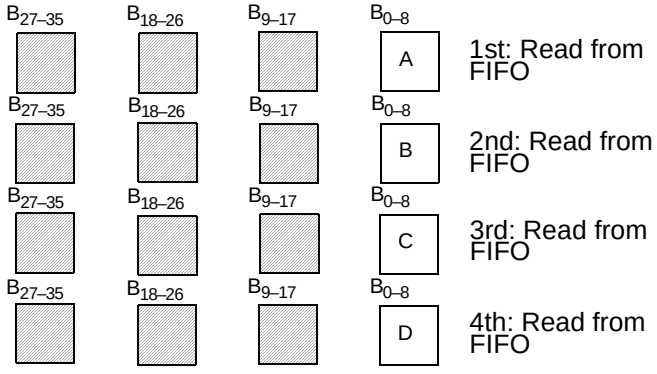
(b) WORD SIZE – BIG ENDIAN

BE	BM	SIZE
L	H	L



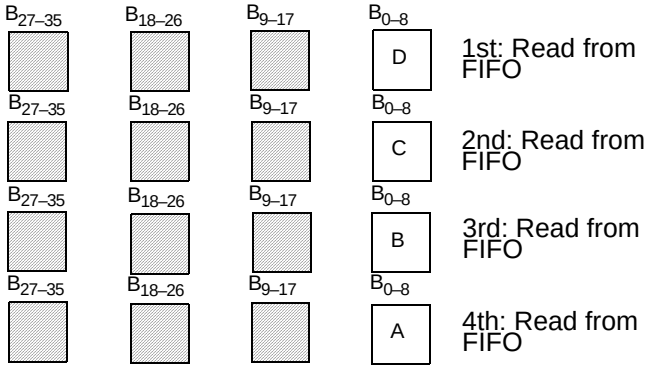
(c) WORD SIZE – LITTLE ENDIAN

BE	BM	SIZE
H	H	H



(d) BYTE SIZE – BIG ENDIAN

BE	BM	SIZE
L	H	H



(e) BYTE SIZE – LITTLE ENDIAN

Table 2. Flag Programming[2]

$\overline{SPM}$	FS1/$\overline{SEN}$	FS0/SD	$\overline{MRS1}$/$\overline{MRS2}$	X and Y Registers[3]
H	H	H	↑	64
H	H	L	↑	16
H	L	H	↑	8
H	L	L	↑	Parallel programming via Port A
L	H	L	↑	Serial programming via SD
L	H	H	↑	Reserved
L	L	H	↑	Reserved
L	L	L	↑	Reserved

Table 3. Port A Enable Function

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A_{0-35} Outputs	Port Function
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, Mail2 register	None
L	L	H	L	↑	Active, Mail2 register	None
L	L	L	H	X	Active, Mail2 register	None
L	L	H	H	↑	Active, Mail2 register	Mail2 read (set $\overline{MBF2}$ HIGH)

Table 4. Port B Enable Function

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B_{0-35} Outputs	Port Function
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	None
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO output register	None
L	H	H	L	↑	Active, FIFO output register	FIFO read
L	H	L	H	X	Active, Mail1 register	None
L	H	H	H	↑	Active, Mail1 register	Mail1 read (set $\overline{MBF1}$ HIGH)

Table 5. FIFO Flag Operation (CY Standard and FWFT Modes)[2]

Number of Words in FIFO Memory[4, 5, 6, 7]			Synchronized to CLKB		Synchronized to CLKA	
CY7C43643	CY7C43663	CY7C43683	$\overline{EF}$/OR	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$/IR
0	0	0	L	L	H	H
1 TO X1	1 TO X1	1 TO X1	H	L	H	H
(X1+1) to [1024–(Y1+1)]	(X1+1) to [4096–(Y1+1)]	(X1+1) to [16384–(Y1+1)]	H	H	H	H
(1024–Y1) to 1023	(4096–Y1) to 4095	(16384–Y1) to 16383	H	H	L	H
1024	4096	16384	H	H	L	L

Notes:
3. X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.
4. X is the Almost Empty offset for FIFO used by $\overline{AE}$. Y is the Almost Full offset for FIFO used by $\overline{AF}$. Both X and Y are selected during a FIFO reset or port A programming.
5. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
6. Data in the output register does not count as a "word in FIFO memory". Since in FWFT Mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
7. The OR and IR functions are active during FWFT mode; the $\overline{EF}$ and $\overline{FF}$ functions are active in CY Standard Mode.

Table 6. Data Size for FIFO Long-Word Reads

Size Mode[9]			Data Written to FIFO				Data Read From FIFO			
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$	$B_{27–35}$	$B_{18–26}$	$B_{9–17}$	$B_{0–8}$
L	X	X	A	B	C	D	A	B	C	D

Table 7. Data Size for Word Reads

Size Mode[9]			Data Written to FIFO				Read No.	Data Read From FIFO	
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$		$B_{9–17}$	$B_{0–8}$
H	L	H	A	B	C	D	1	A	B
							2	C	D
H	L	L	A	B	C	D	1	C	D
							2	A	B

Table 8. Data Size for Byte Reads from FIFO

Size Mode[9]			Data Written to FIFO				Read No.	Data Read From FIFO
BM	SIZE	BE	$A_{27–35}$	$A_{18–26}$	$A_{9–17}$	$A_{0–8}$		$B_{0–8}$
H	H	H	A	B	C	D	1	A
							2	B
							3	C
							4	D
H	H	L	A	B	C	D	1	D
							2	C
							3	B
							4	A

Notes:
8.
9. BE is selected at Master Reset; BM and SIZE must be static throughout device operation.

Maximum Ratings[10,12]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[11].....–0.5V to V_{CC}+0.5V

DC Input Voltage[11] .....–0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}[13]
Commercial	0°C to +70°C	5.0V ± 0.5V
Industrial	∠40°C to +85°C	5.0V ± 0.5V

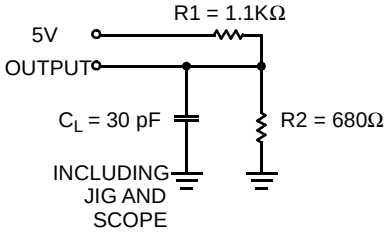
Electrical Characteristics Over the Operating Range

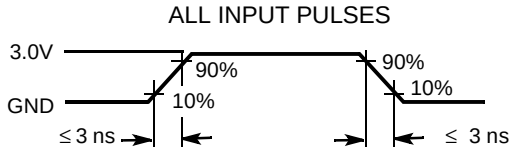
Parameter	Description	Test Conditions		CY7C43643/63/83 Min.	CY7C43643/63/83 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5V, I_{OH} = ∠4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5V, I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			∠0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		∠10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High-Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		∠10	+10	µA
I_{CC1}[14]	Active Power Supply Current		Com'l		100	mA
			Ind		100	mA
I_{SB}[15]	Average Standby Current		Com'l		10	mA
			Ind		10	mA

Capacitance[16]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	4	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms (-10 and -15)

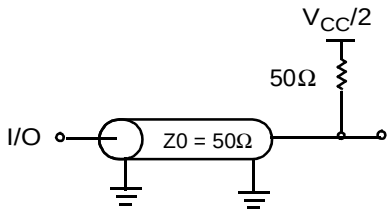


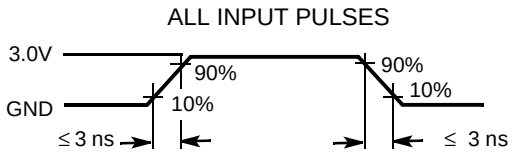


Notes:

10. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
11. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
12. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
13. Operating V_{CC} range for -7 speed is 5.0V ±0.25V.
14. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.
15. All inputs = V_{CC} – 0.2V, except RCLK and WCLK (which are at frequency = 0 MHz). All outputs are unloaded.
16. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms (-7)





Switching Characteristics Over the Operating Range

Parameter	Description	CY7C43643/63/83 –7		CY7C43643/63/83 –10		CY7C43643/63/83 –15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB		133		100		67	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	7.5		10		15		ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	3.5		4		6		ns
t_{CLKL}	Pulse Duration, CLKA or CLKB LOW	3.5		4		6		ns
t_{DS}	Set-up Time, $A_{0–35}$ before CLKA↑ and $B_{0–35}$ before CLKB↑	3		4		5		ns
t_{ENS}	Set-up Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB before CLKB↑	3		4		5		ns
t_{RSTS}	Set-up Time, $\overline{MRS1}$/$\overline{MRS2}$, $\overline{PRS}$ or $\overline{RT1}$ LOW before CLKA↑ or CLKB↑[17]	2.5		4		5		ns
t_{FSS}	Set-up Time, FS0 and FS1 before $\overline{MRS1}$/$\overline{MRS2}$ HIGH	6		7		7.5		ns
t_{BES}	Set-up Time, BE/FWFT before $\overline{MRS1}$/$\overline{MRS2}$ HIGH	5		7		7.5		ns
t_{SPMS}	Set-up Time, $\overline{SPM}$ before $\overline{MRS1}$/$\overline{MRS2}$ HIGH	5		7		7.5		ns
t_{SDS}	Set-up Time, FS0/SD before CLKA↑	3		4		5		ns
t_{SENS}	Set-up Time, FS1/$\overline{SEN}$ before CLKA↑	3		4		5		ns
t_{FWS}	Set-up Time, FWFT before CLKA↑	0		0		0		ns
t_{DH}	Hold Time, $A_{0–35}$ after CLKA↑ and $B_{0–35}$ after CLKB↑	0		0		0		ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB after CLKB↑	0		0		0		ns
t_{RSTH}	Hold Time, $\overline{MRS1}$/$\overline{MRS2}$, $\overline{PRS}$ or $\overline{RT1}$ LOW after CLKA↑ or CLKB↑[17]	1		2		4		ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{MRS1}$/$\overline{MRS2}$ HIGH	1		1		2		ns
t_{BEH}	Hold Time, BE/FWFT after $\overline{MRS1}$/$\overline{MRS2}$ HIGH	1		1		2		ns
t_{SPMH}	Hold Time, $\overline{SPM}$ after $\overline{MRS1}$/$\overline{MRS2}$ HIGH	1		1		2		ns
t_{SDH}	Hold Time, FS0/SD after CLKA↑	0		0		0		ns
t_{SENH}	Hold Time, FS1/$\overline{SEN}$ after CLKA↑	0		0		0		ns
t_{SPH}	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{MRS1}$/$\overline{MRS2}$ HIGH	0		1		2		ns

Note:
17. Requirement to count the clock edge as one of at least four needed to reset a FIFO.

Switching Characteristics Over the Operating Range (continued)

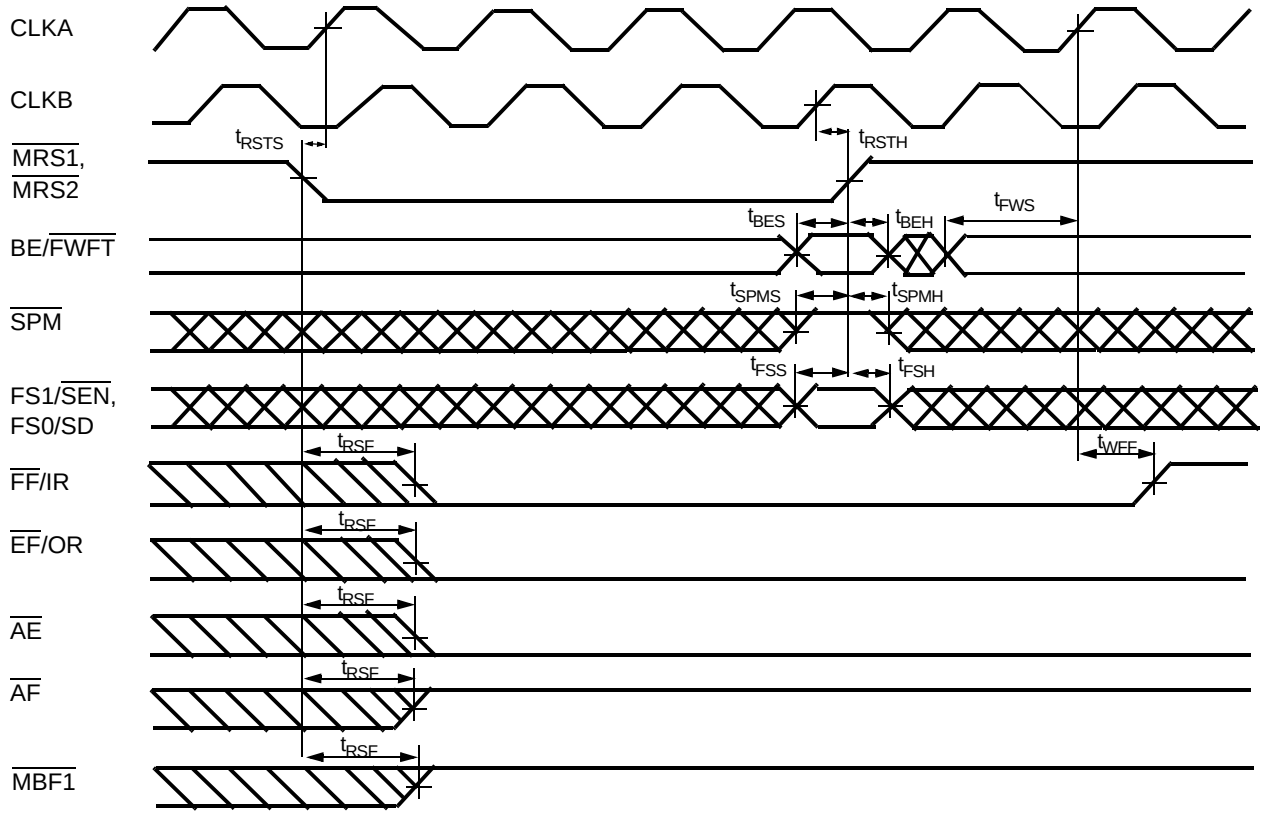
Parameter	Description	CY7C43643/63/83 –7		CY7C43643/63/83 –10		CY7C43643/63/83 –15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SKEW1}[18]	Skew Time between CLKA↑ and CLKB↑ for $\overline{EF}$/OR and $\overline{FF}$/IR	5		5		7.5		ns
t_{SKEW2}[18]	Skew Time between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	7		8		12		ns
t_A	Access Time, CLKA↑ to $A_{0–35}$ and CLKB↑ to $B_{0–35}$	1	6	1	8	3	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FF}$/IR	1	6	1	8	2	8	ns
t_{REF}	Propagation Delay Time, CLKB↑ to $\overline{EF}$/OR	1	6	1	8	1	8	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	1	6	1	8	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	1	6	1	8	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	6	0	8	0	12	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to $B_{0–35}$[19] and CLKB↑ to $A_{0–35}$[20]	1	7	2	11	3	12	ns
t_{MDV}	Propagation Delay Time, MBA to $A_{0–35}$ Valid and MBB to $B_{0–35}$ Valid	1	6	2	9	3	11	ns
t_{RSF}	Propagation Delay Time, $\overline{MRS1}$/$\overline{MRS2}$ or $\overline{PRS}$ LOW to $\overline{AE}$ LOW, $\overline{AF}$ HIGH, $\overline{FF}$/IR LOW, $\overline{EF}$/OR LOW and $\overline{MBF1}$/$\overline{MBF2}$ HIGH	1	6	1	10	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ or W/$\overline{RA}$ LOW to $A_{0–35}$ Active and $\overline{CSB}$ LOW and W/$\overline{RB}$ HIGH to $B_{0–35}$ Active	1	6	2	8	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to $A_{0–35}$ at High Impedance and $\overline{CSB}$ HIGH or W/$\overline{RB}$ LOW to $B_{0–35}$ at High Impedance	1	5	1	6	1	8	ns
t_{RTR}	Retransmit Recovery Time	90		90		90		ns

Notes:

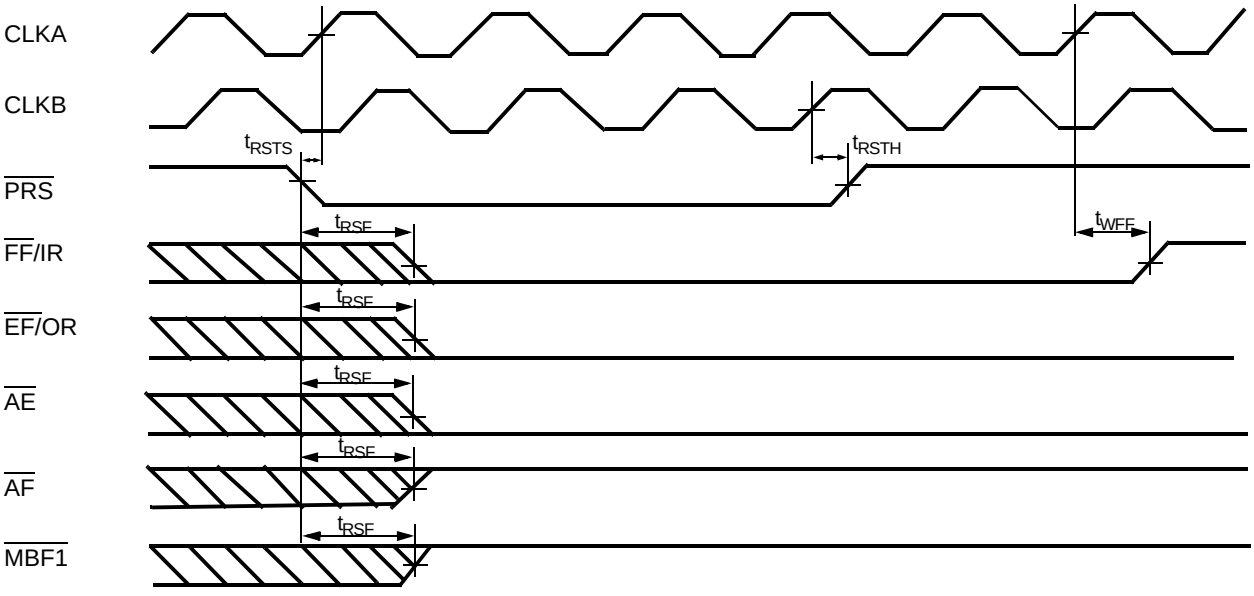
18. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between the CLKA cycle and the CLKB cycle.
19. Writing data to the Mail1 register when the $B_{0–35}$ outputs are active and MBB is HIGH.
20. Writing data to the Mail2 register when the $A_{0–35}$ outputs are active and MBA is HIGH.

Switching Waveforms

Master Reset Loading X and Y with a Preset Value of Eight [21]



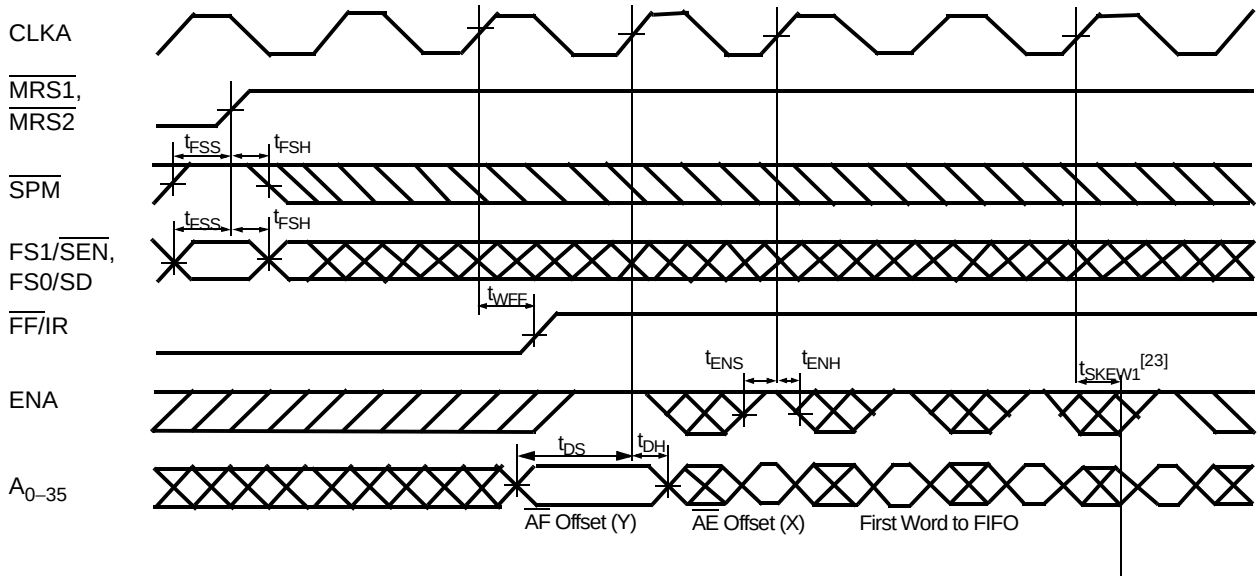
Partial Reset (CY Standard and FWFT Modes)[21]



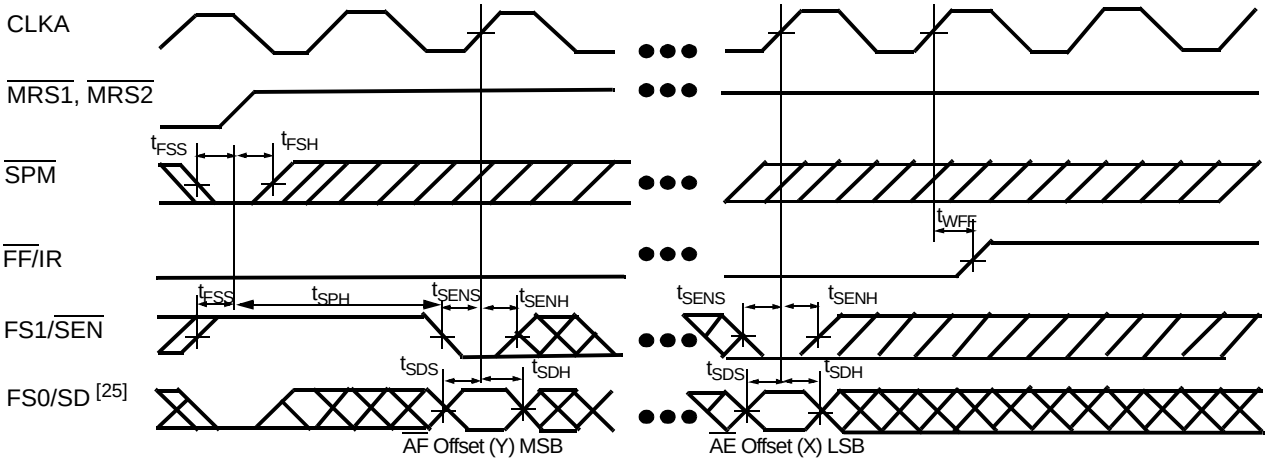
Note:
21. MRS1/MRS2 must be HIGH during Partial Reset.

Switching Waveforms (continued)

Parallel Programming of the Almost Full Flag and Almost Empty Flag Offset Values after Reset (CY Standard and FWFT Modes)[22]



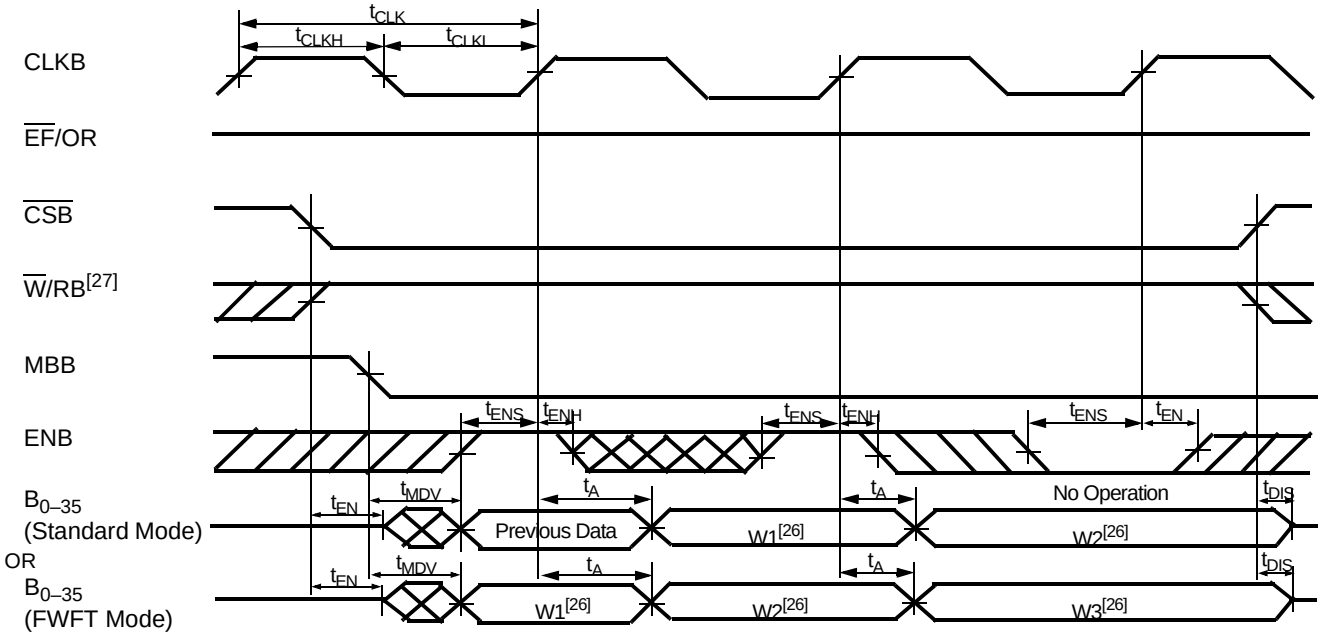
Serial Programming of the Almost Full Flag and Almost Empty Flag Offset Values (CY Standard and FWFT Modes)[24]



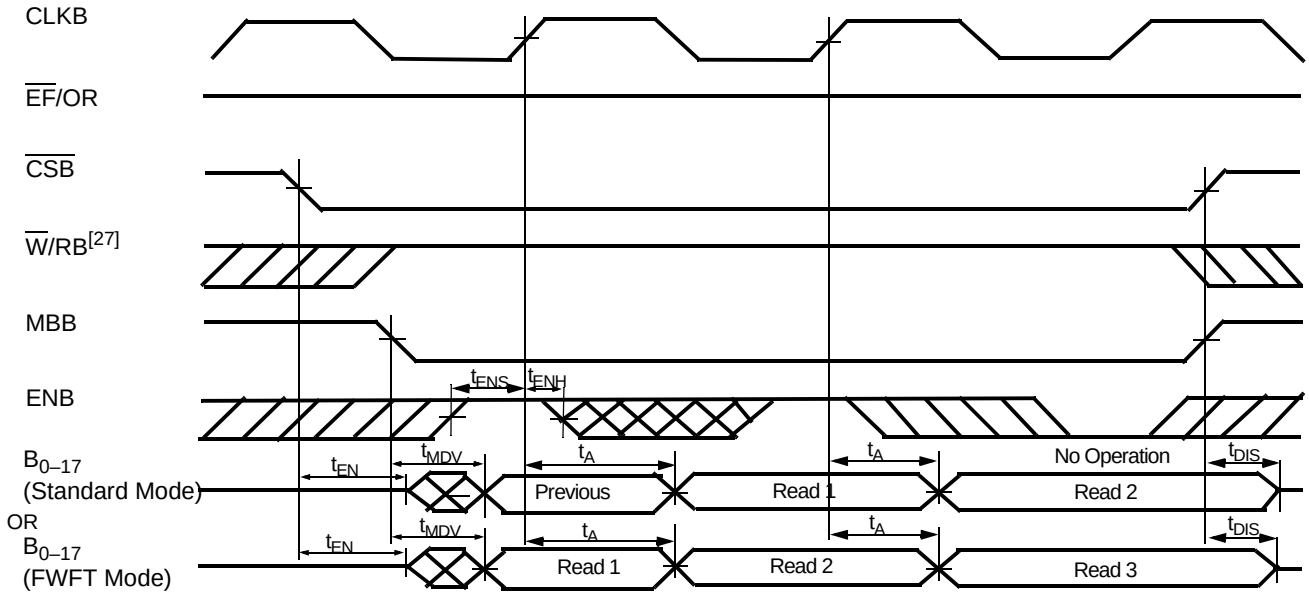
Notes:
22. CSA = LOW, W/RA = HIGH, MBA = LOW. It is not necessary to program offset register on consecutive clock cycles.
23. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKB for FF/IR to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{SKEW1}, then FF/IR may transition HIGH one cycle later than shown.
24. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set HIGH.
25. Programmable offsets are written serially to the SD input in the order AF offset (Y) then AE offset (X).

Switching Waveforms (continued)

Port B Long-Word Read Cycle Timing for FIFO (CY Standard and FWFT Modes)[1]



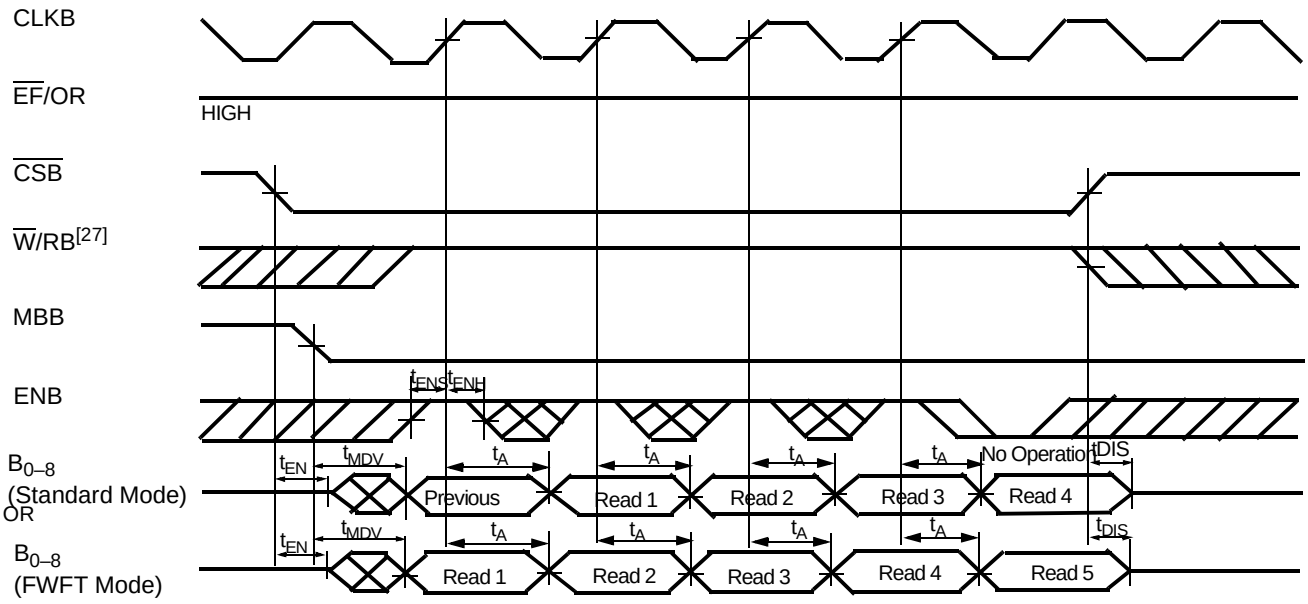
Port B Word Read Cycle Timing for FIFO (CY Standard and FWFT Modes) [1, 28]



Notes:
26. Read from FIFO.
27. If W/RB switches from read to write before the assertion of $\overline{CSB}$, $t_{ENS} = t_{DIS}+t_{ENS}$.
28. Unused word $B_{18–35}$ contains all zeroes for word-size reads.

Switching Waveforms (continued)

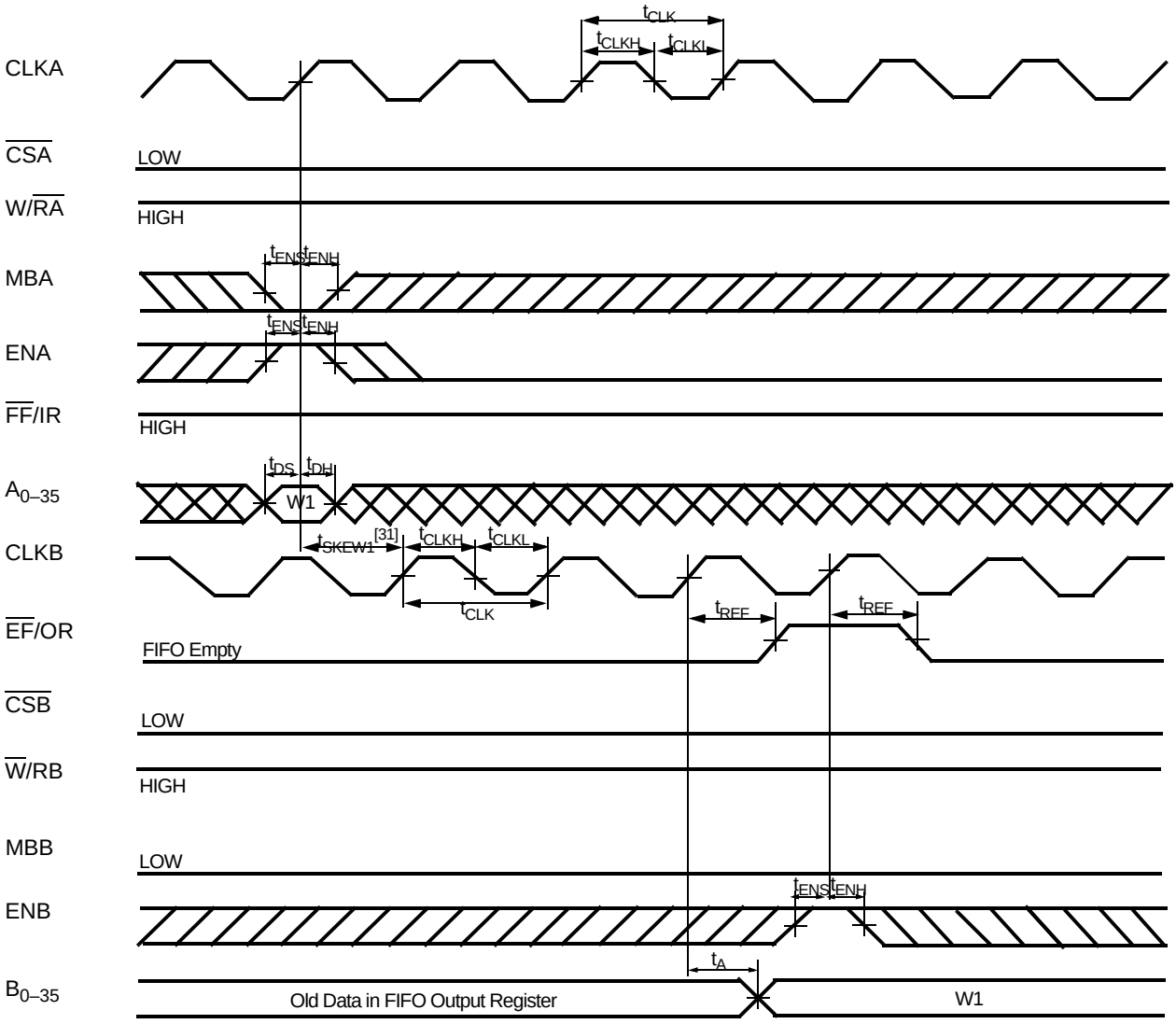
Port B Byte Read Cycle Timing for FIFO (CY Standard and FWFT Modes)[1, 29]



Notes:
29. Unused bytes $B_{9–17}$, $B_{18–26}$, and $B_{27–35}$ contain all zeroes for byte-size reads.

Switching Waveforms (continued)

OR Flag Timing and First Data Word Fall Through when FIFO is Empty (FWFT Mode)[1, 30]

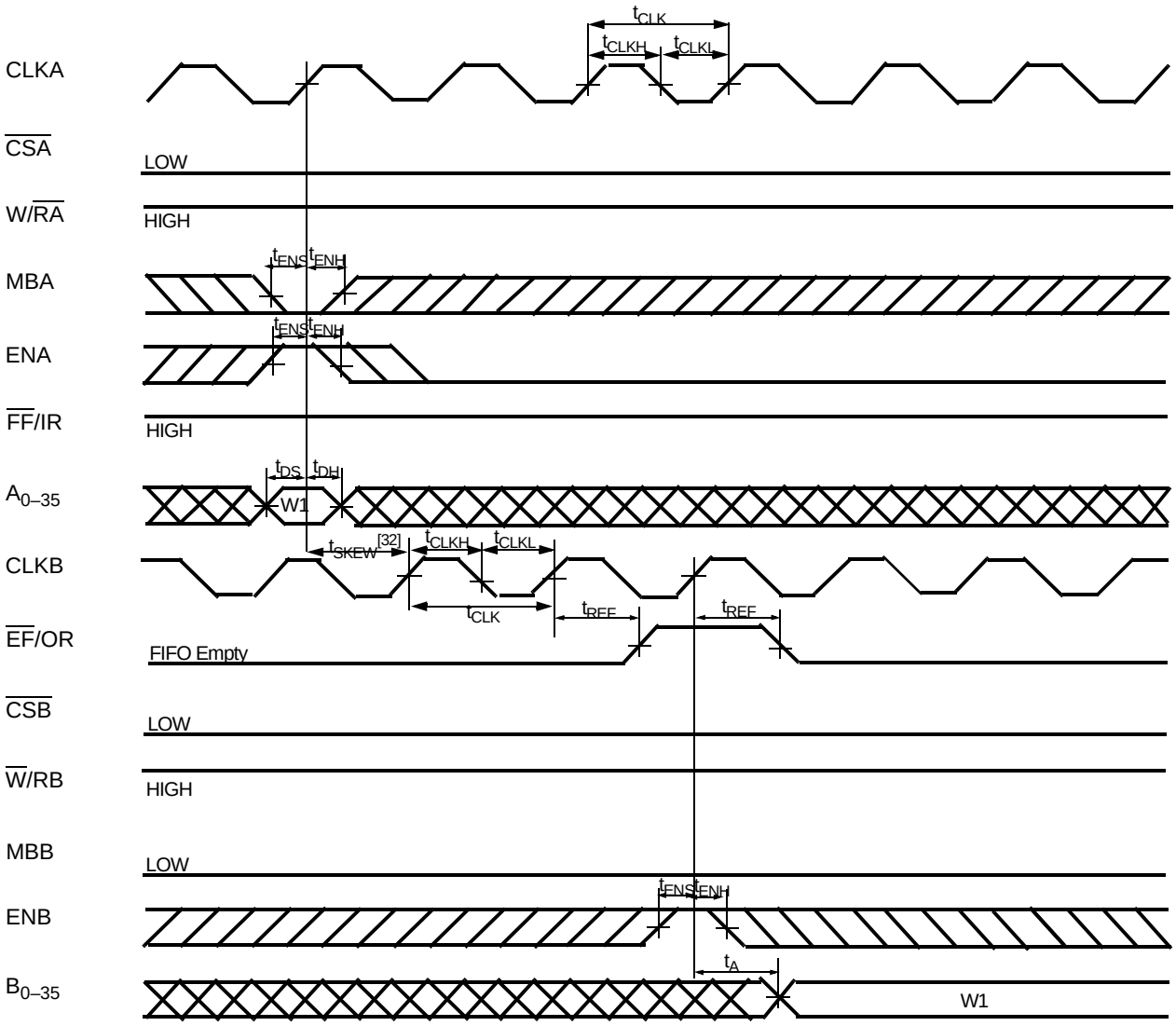


Notes:

30. If Port B size is word or byte, $\overline{EF}$ is set LOW by the last word or byte read from the FIFO, respectively.
31. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition HIGH and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of OR HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

$\overline{EF}$ Flag Timing and First Data Read Fall Through when FIFO is Empty (CY Standard Mode)[30]

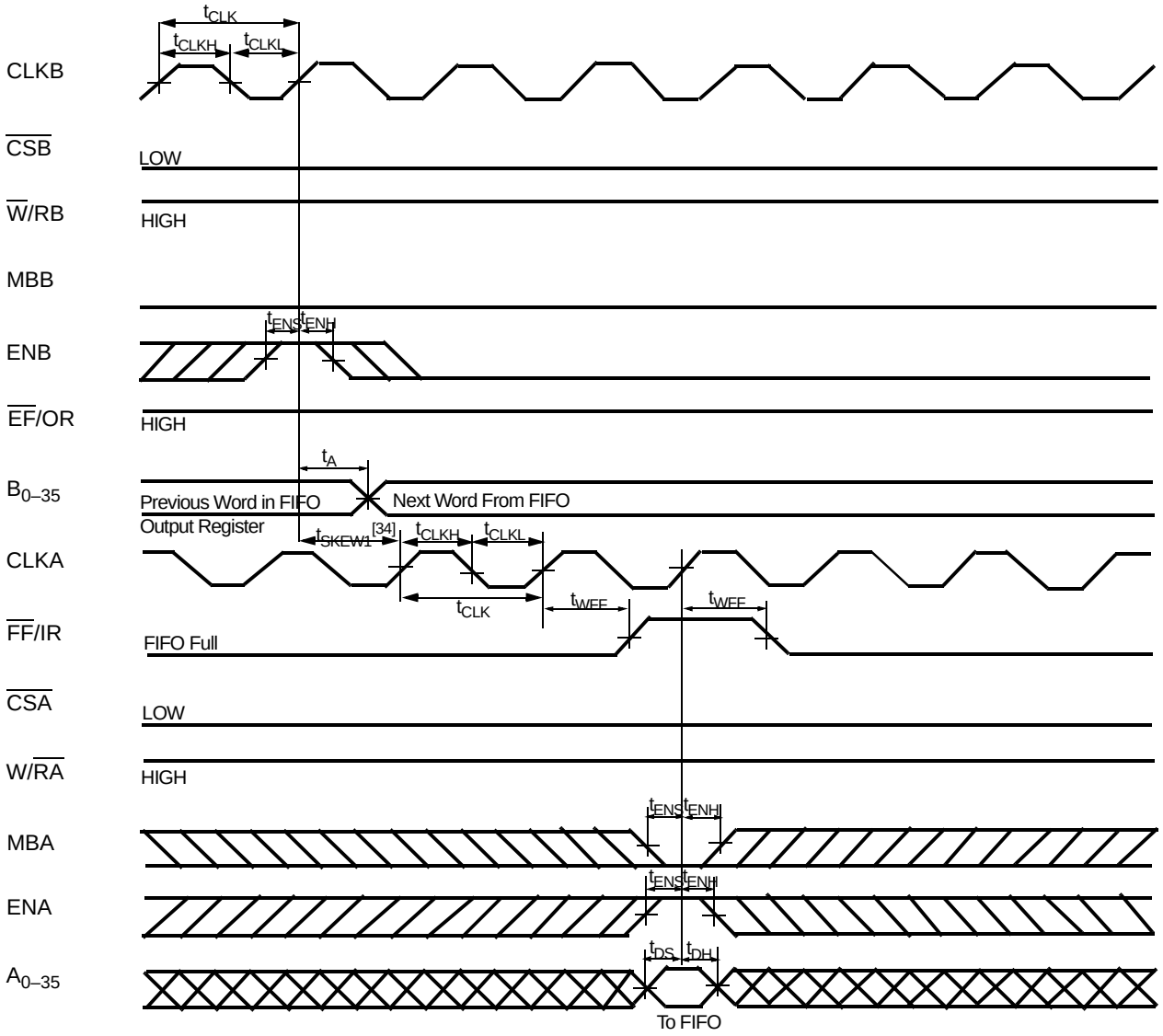


Notes:

32. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.

Switching Waveforms (continued)

IR Flag Timing and First Available Write when FIFO is Full (FWFT Mode)[33]

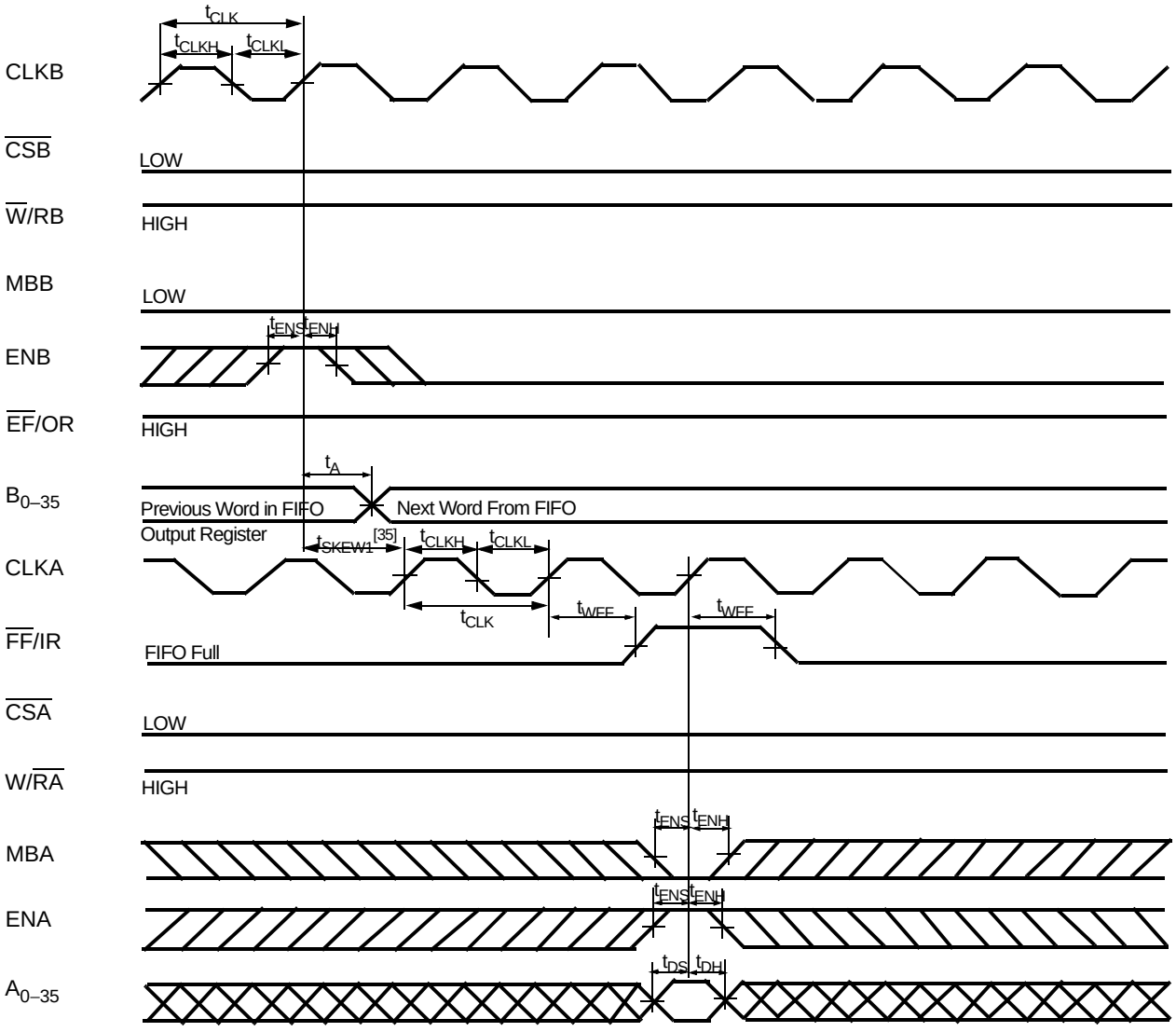


Notes:

33. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that reads the last word or byte write of the long word, respectively.
34. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IR may transition HIGH one CLKA cycle later than shown.

Switching Waveforms (continued)

$\overline{FF}$ Flag Timing and First Available Write when FIFO is Full (CY Standard Mode) [33]

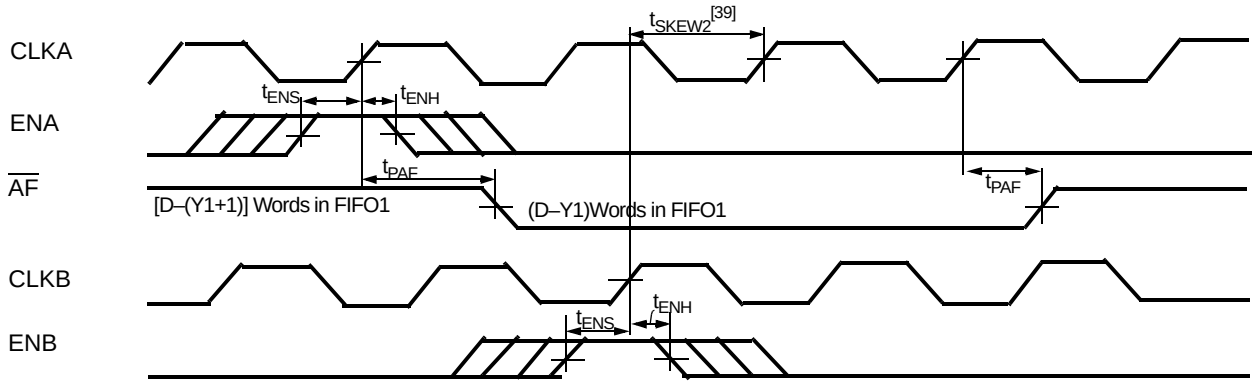


Note:

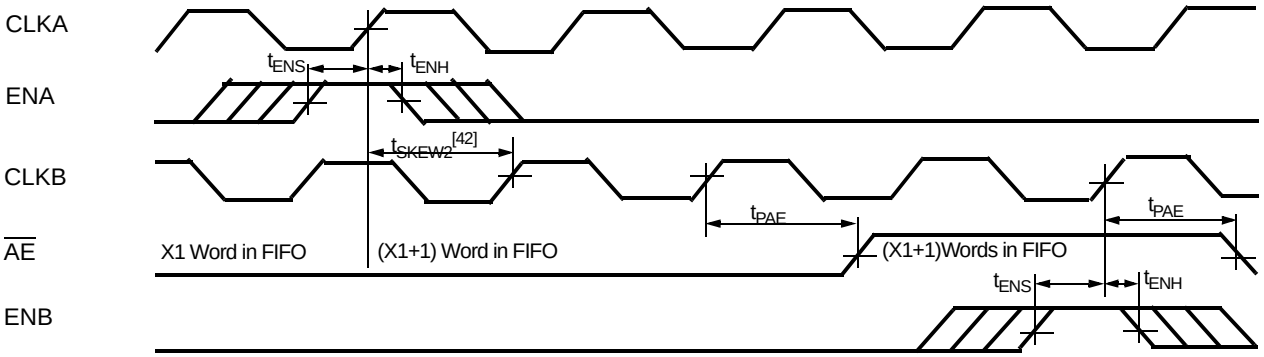
35. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{FF}$ HIGH may occur one CLKA cycle later than shown.

Switching Waveforms (continued)

Timing for $\overline{AF}$ when FIFO is Almost Full (CY Standard and FWFT Modes) [2, 36, 37, 38]



Timing for $\overline{AE}$ when FIFO is Almost Empty (CY Standard and FWFT Modes) [40, 41, 2]

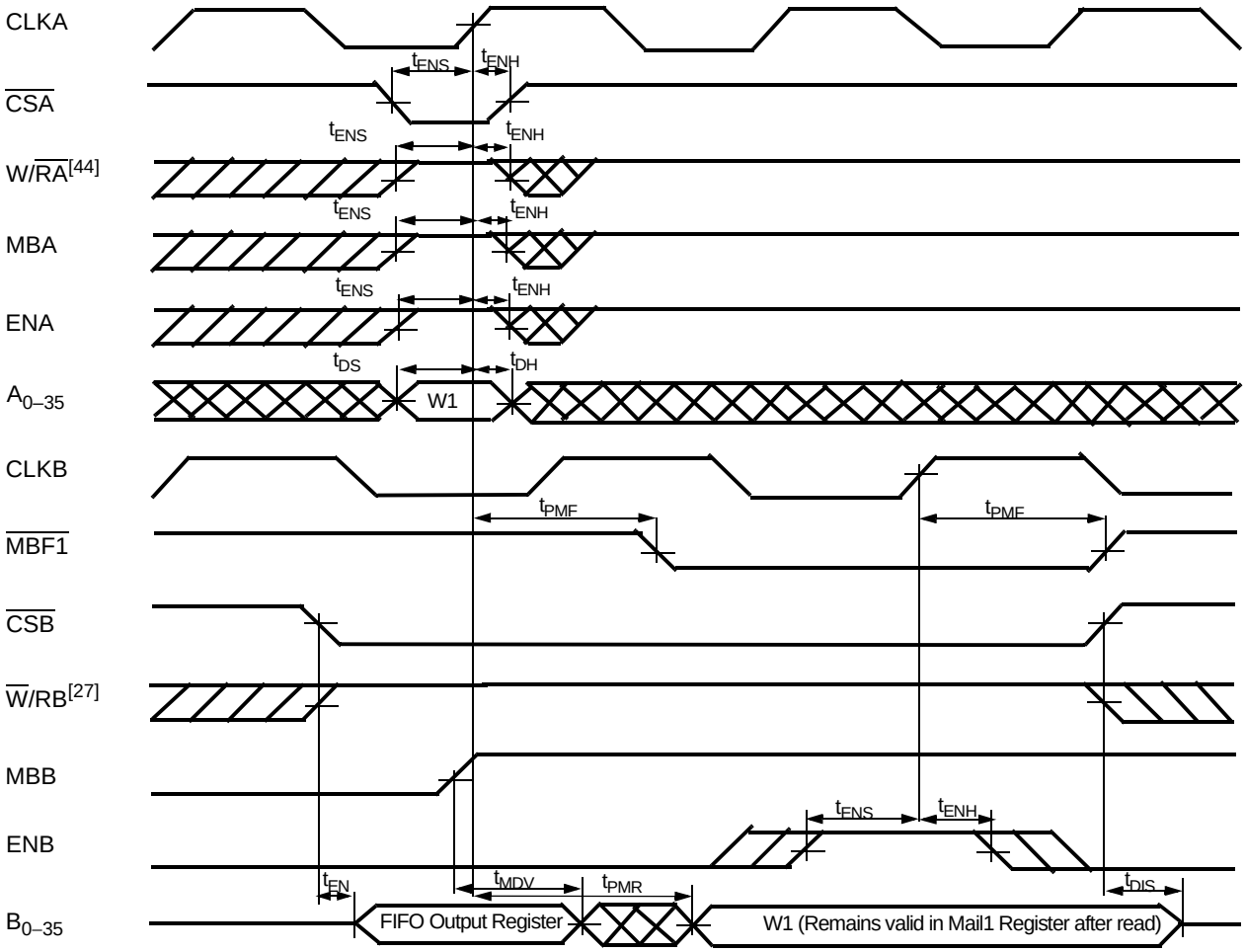


Notes:

36. FIFO Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO Read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
37. D = Maximum FIFO Depth 1K for the CY7C43643, 4K for the 43663, and 16K for the CY7C43683.
38. If Port B size is word or byte, t_{SKEW2} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.
39. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKB cycle later than shown.
40. FIFO Write (CSA = LOW, W/RA = LOW, MBA = LOW), FIFO Read (CSB = LOW, W/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
41. If Port B size is word or byte, $\overline{AE}$ is set LOW by the last word or byte read from FIFO, respectively.
42. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown.

Switching Waveforms (continued)

Timing for Mail1 Register and $\overline{MBF1}$ Flag (CY Standard and FWFT Modes) [43,45]

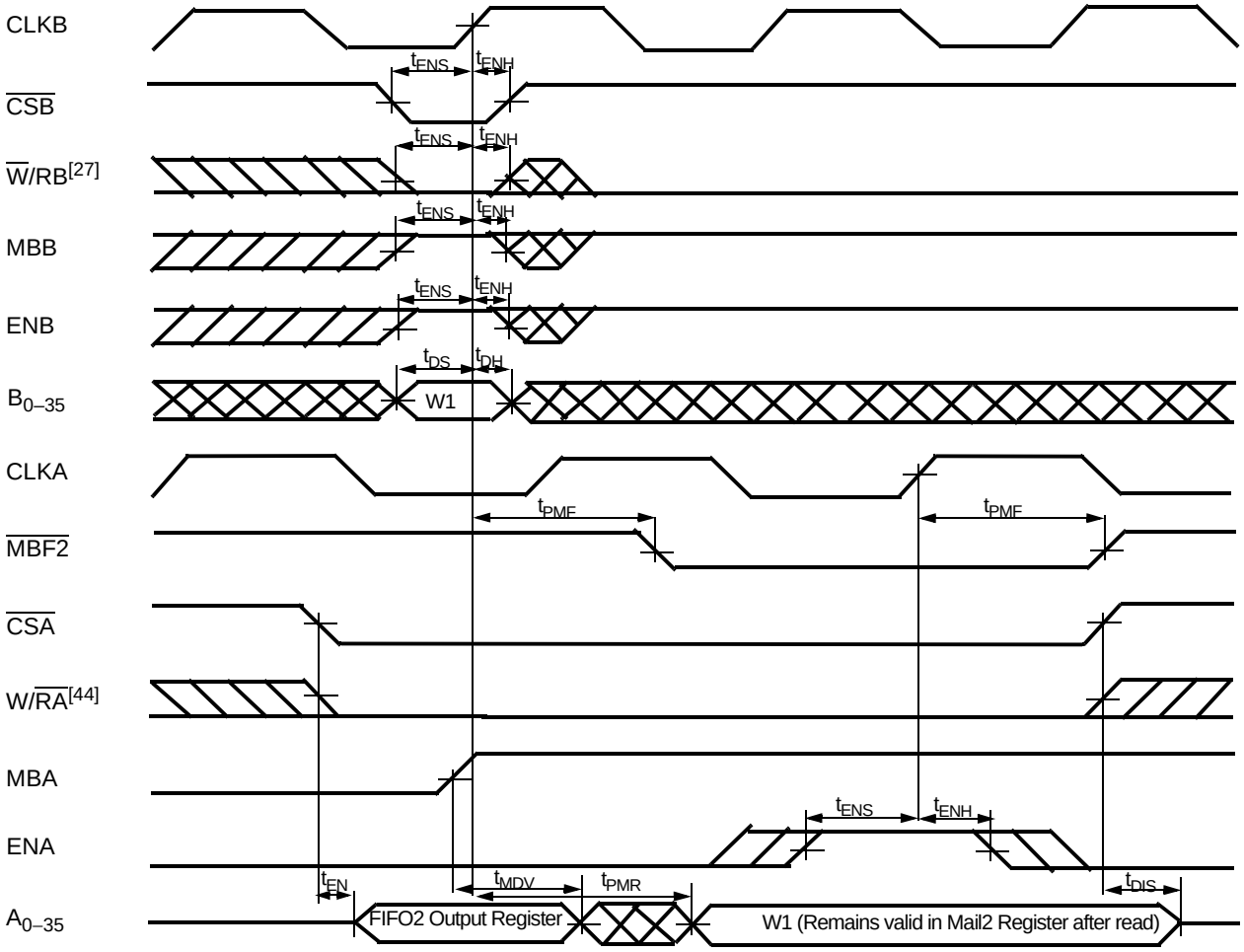


Note:

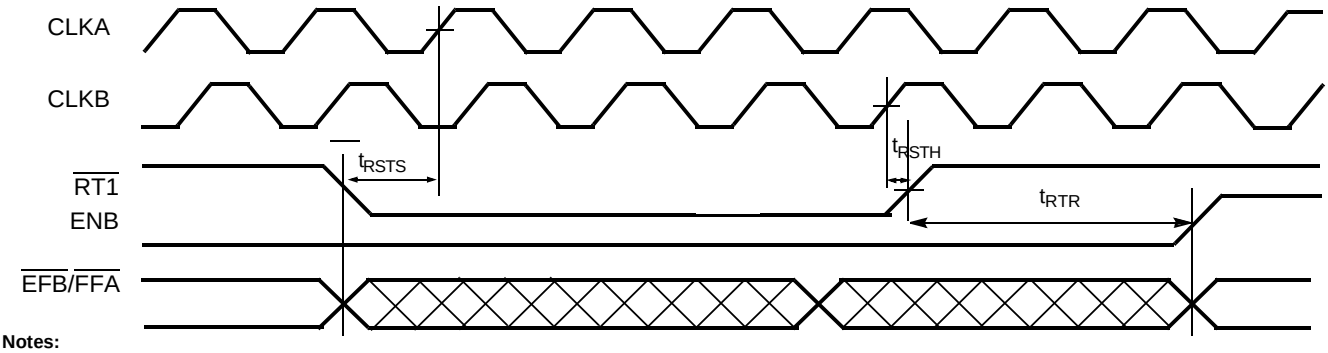
43. If Port B is configured for word size, data can be written to the Mail1 register using $A_{0–17}$ ($A_{18–35}$ are "don't care" inputs). In this first case $B_{0–17}$ will have valid data ($B_{18–35}$ will be indeterminate). If Port B is configured for byte size, data can be written to the Mail1 Register using $A_{0–8}$ ($A_{9–35}$ are "don't care" inputs). In this second case, $B_{0–8}$ will have valid data ($B_{9–35}$ will be indeterminate).
44. If W/$\overline{RA}$ switches from read to write before the assertion of $\overline{CSA}$, $t_{ENS} = t_{DIS}+t_{ENS}$.
45. Simultaneous writing to and reading from mailbox register is not allowed.

Switching Waveforms (continued)

Timing for Mail2 Register and MBF2 Flag (CY Standard and FWFT Modes)[46,45]



FIFO1 Retransmit Timing [47, 48, 49, 50, 51]



Notes:

46. If Port B is configured for word size, data can be written to the Mail2 register using $B_{0–17}$ ($B_{18–35}$ are "don't care" inputs). In this first case, $A_{0–17}$ will have valid data ($A_{18–35}$ will be indeterminate). If Port B is configured for byte size, data can be written to the Mail2 Register using $B_{0–8}$ ($B_{9–35}$ are "don't care" inputs). In this second case, $A_{0–8}$ will have valid data ($A_{9–35}$ will be indeterminate).
47. Retransmit is performed in the same manner for FIFO2.
48. Clocks are free-running in this case. CY standard mode only. Write operation should be prohibited one write clock cycle before the falling edge of $\overline{RT1}$, and during the retransmit operation, i.e. when RT1 is LOW and t_{RTR} after the RT1 rising edge.
49. The Empty and Full flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
50. For the AEA, AEB, AFA, and AFB flags, two clock cycle are necessary after t_{RTR} to update these flags.
51. The number of 36-/18-/9-bit words written into the FIFO should be less than full depth minus 2/4/8 words between the reset of the FIFO (master or partial) and the Retransmit setup.

Ordering Information

1K x36 Unidirectional Synchronous FIFO w/ Bus Matching

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43643–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43643–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43643–15AC	A128	128-lead Thin Quad Flat Package	Commercial

4K x36 Unidirectional Synchronous FIFO w/ Bus Matching

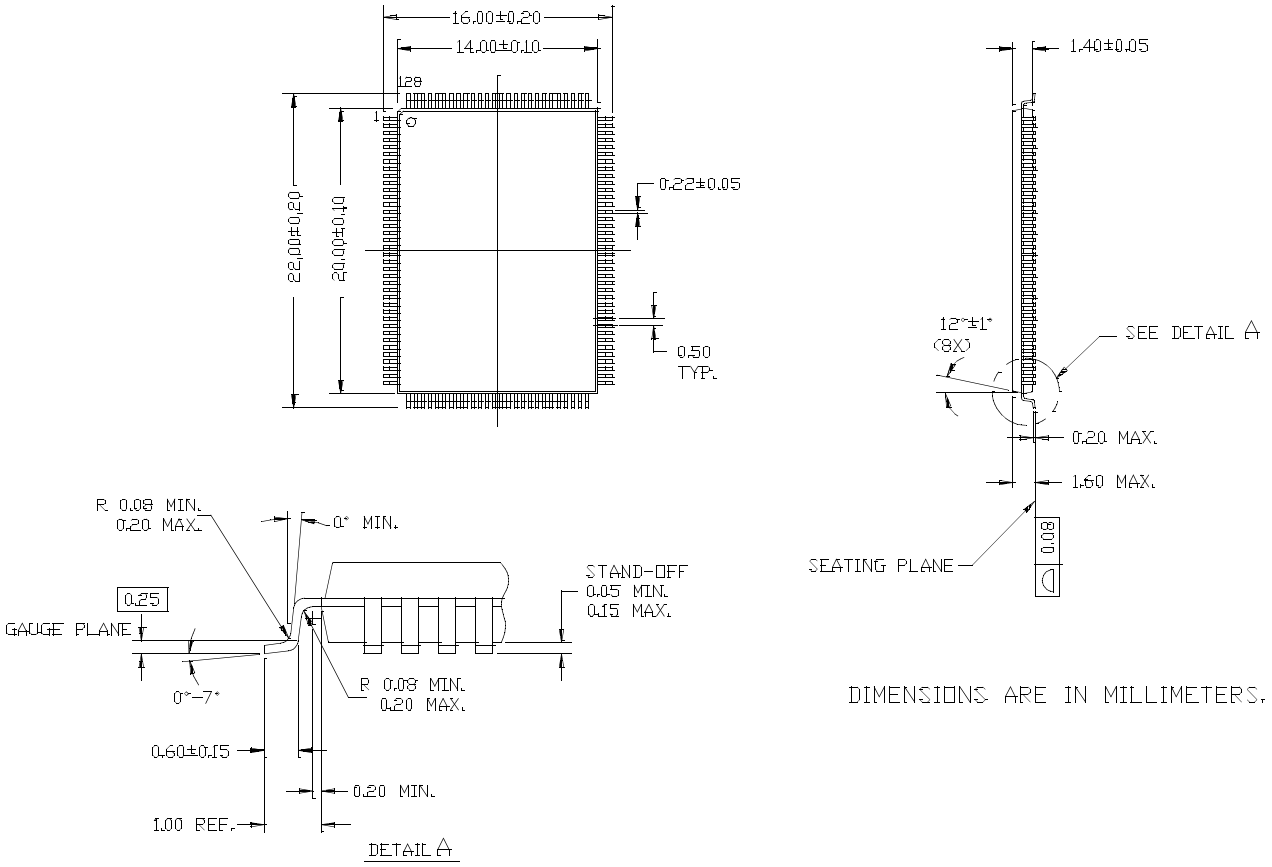
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43663–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43663–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43663–15AC	A128	128-lead Thin Quad Flat Package	Commercial

16K x36 Unidirectional Synchronous FIFO w/ Bus Matching

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7	CY7C43683–7AC	A128	128-lead Thin Quad Flat Package	Commercial
10	CY7C43683–10AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43683–15AC	A128	128-lead Thin Quad Flat Package	Commercial
15	CY7C43683–15AI	A128	128-lead Thin Quad Flat Package	Industrial

Package Diagram

128-Lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A128



51-85101-*B

Document Title: CY7C43643/ CY7C43663/ CY7C43683 1K/4K/16K x36 Unidirectional Synchronous FIFO with Bus Matching Document Number: 38-06021				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106563	05/17/01	SZV	Change from Spec #: 38-00699 to 39-06021
*A	117172	09/05/02	OOR	Added footnote to retransmit timing Added note to retransmit section
*B	122273	12/26/02	RBI	Power up requirements added to Maximum Ratings Information