256K x 16 Static RAM

Features

- **Pin equivalent to CY7C1041BV33**
- **High speed**
  - **t_{AA} = 10 ns**
- **Low active power**
  - **324 mW (max.)**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description[1]

The CY7C1041CV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$–I/O$_7$), is written into the location specified on the address pins (A$_0$–A$_{17}$). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$–I/O$_{15}$) is written into the location specified on the address pins (A$_0$–A$_{17}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ – I/O$_7$. If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O$_0$–I/O$_{15}$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1041CV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout, as well as a 48-ball fine-pitch ball grid array (FBGA) package.
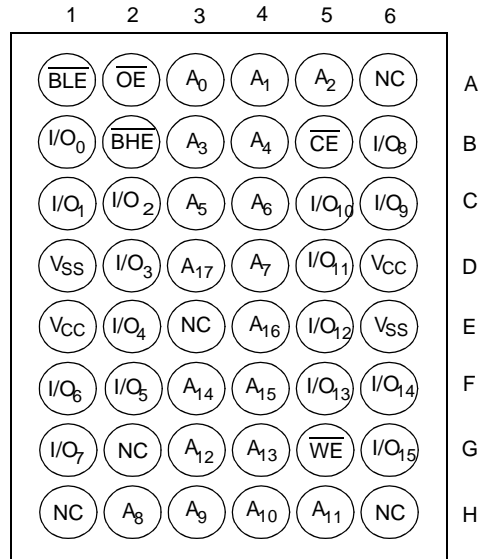
Logic Block Diagram

Pin Configuration

SOJ
TSOP II
Top View
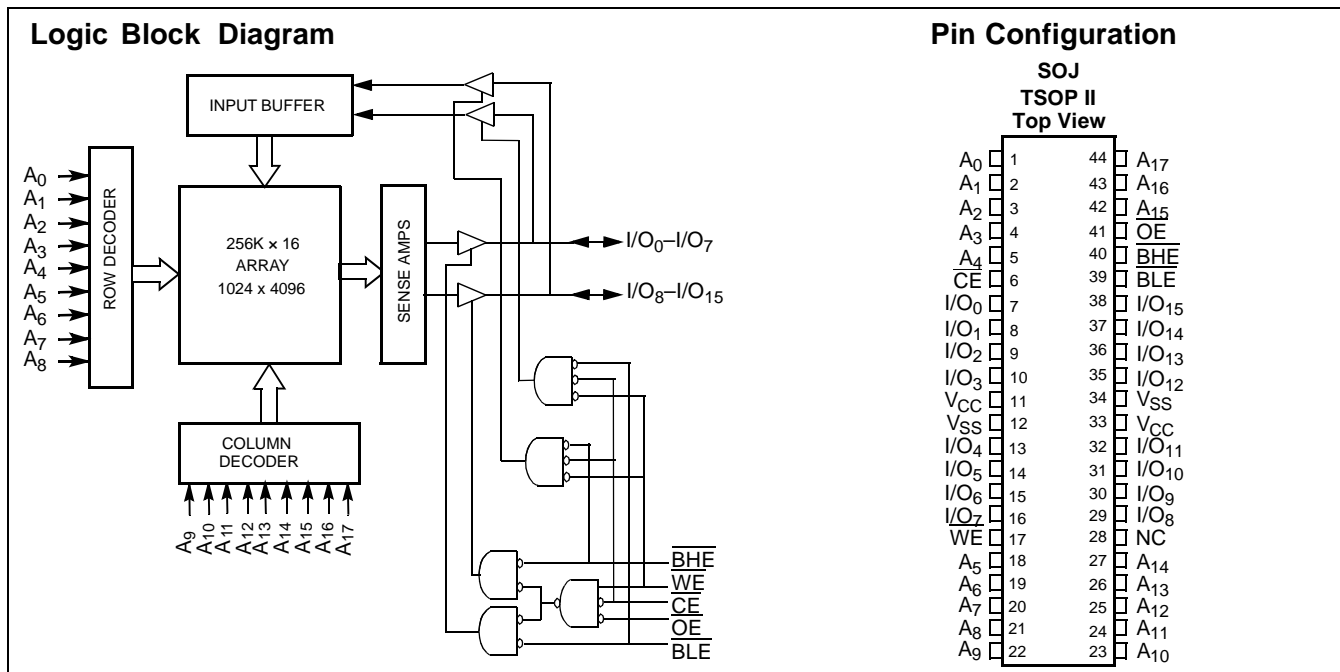
Selection Guide

		-8	-10	-12	-15	-20	Unit
Maximum Access Time		8	10	12	15	20	ns
Maximum Operating Current	Commercial	100	90	85	80	75	mA
	Industrial	110	100	95	90	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	10	10	10	10	10	mA

Shaded areas contain advance information.
Note:
1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com.

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Pin Configurations

48-ball Mini FBGA

(Top View)

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	I/O_0	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	I/O_8	B
C	I/O_1	I/O_2	A_5	A_6	I/O_{10}	I/O_9	C
D	V_{SS}	I/O_3	A_{17}	A_7	I/O_{11}	V_{CC}	D
E	V_{CC}	I/O_4	NC	A_{16}	I/O_{12}	V_{SS}	E
F	I/O_6	I/O_5	A_{14}	A_{15}	I/O_{13}	I/O_{14}	F
G	I/O_7	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_{15}	G
H	NC	A_8	A_9	A_{10}	A_{11}	NC	H

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied... −55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... −0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[2] .... −0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	−40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}[2]	Input LOW Voltage			−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	−1	+1	−1	+1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−1	+1	−1	+1	−1	+1	−1	+1	−1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Comm'l		100		90		85		80		75	mA
			Indus.		110		100		95		90		85	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40		40		40		40	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V, or V_{IN} ≤ 0.3V, f = 0	Comm'l Indus.		10		10		10		10		10	mA

Shaded areas contain advance information.

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Notes:
2. Minimum voltage is −2.0V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.
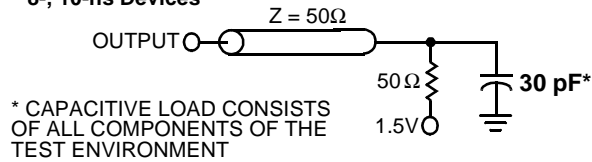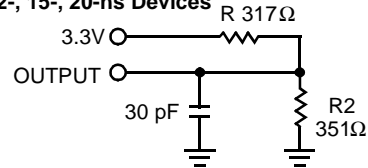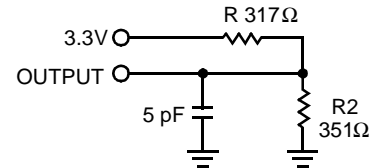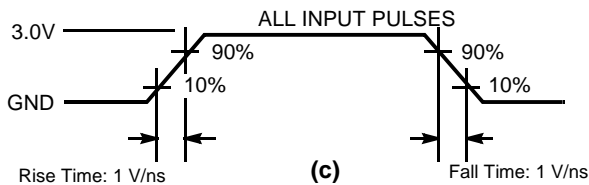
AC Switching Characteristics[4] Over the Operating Range

| Parameter	Description	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
Read Cycle												
t_{power}[5]	V_{CC}(typical) to the first access	1		1		1		1		1		µs
t_{RC}	Read Cycle Time	8		10		12		15		20		ns
t_{AA}	Address to Data Valid		8		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4		5		6		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		4		5		6		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		4		5		6		7		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		8		10		12		15		20	ns
t_{DBE}	Byte Enable to Data Valid		4		5		6		7		8	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		6		6		6		7		8	ns
Write Cycle[8, 9]												
t_{WC}	Write Cycle Time	8		10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	6		7		8		10		10		ns
t_{AW}	Address Set-Up to Write End	6		7		8		10		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		10		10		ns
t_{SD}	Data Set-Up to Write End	4		5		6		7		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		4		5		6		7		8	ns
t_{BW}	Byte Enable to End of Write	6		7		8		10		10		ns

Shaded areas contain advance information.

Notes:
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. CE and WE must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
9. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

AC Test Loads and Waveforms[10]

8-, 10-ns Devices

OUTPUT — Z = 50Ω

50Ω

1.5V

30 pF*

* CAPACITIVE LOAD CONSISTS
OF ALL COMPONENTS OF THE
TEST ENVIRONMENT

(a)

12-, 15-, 20-ns Devices R 317Ω

3.3V

OUTPUT

30 pF

R2
351Ω

(b)

3.0V — ALL INPUT PULSES

90%   90%

10%   10%

GND

Rise Time: 1 V/ns   Fall Time: 1 V/ns

(c)

High-Z Characteristics

R 317Ω

3.3V

OUTPUT

5 pF

R2
351Ω

(d)

Switching Waveforms

Read Cycle No. 1[11, 12]

t_{RC}

ADDRESS

t_{AA}

t_{OHA}

DATA OUT   PREVIOUS DATA VALID   DATA VALID
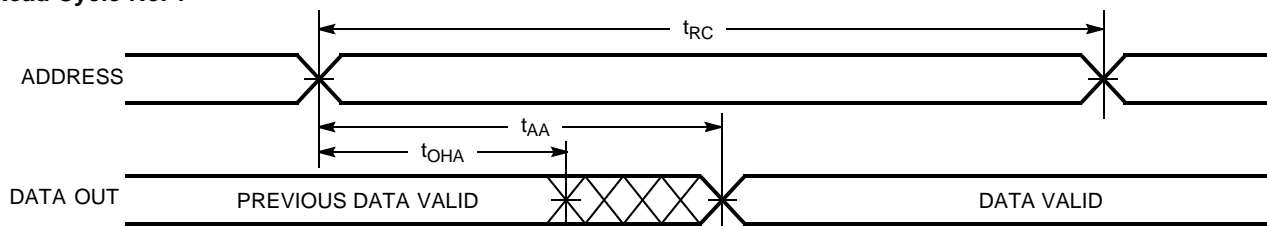
Read Cycle No. 2 ($\overline{OE}$ Controlled) [12, 13]

ADDRESS

t_{RC}

$\overline{CE}$

t_{ACE}

$\overline{OE}$

t_{HZOE}

$\overline{BHE}, \overline{BLE}$

t_{DOE}

t_{LZOE}

t_{DBE}

t_{LZBE}

t_{HZCE}

t_{HZBE}

HIGH
IMPEDANCE

DATA OUT   HIGH IMPEDANCE   DATA VALID

t_{LZCE}

t_{PU}

t_{PD}

V_{CC}
SUPPLY
CURRENT

50%   50%

I_{CC}

I_{SB}
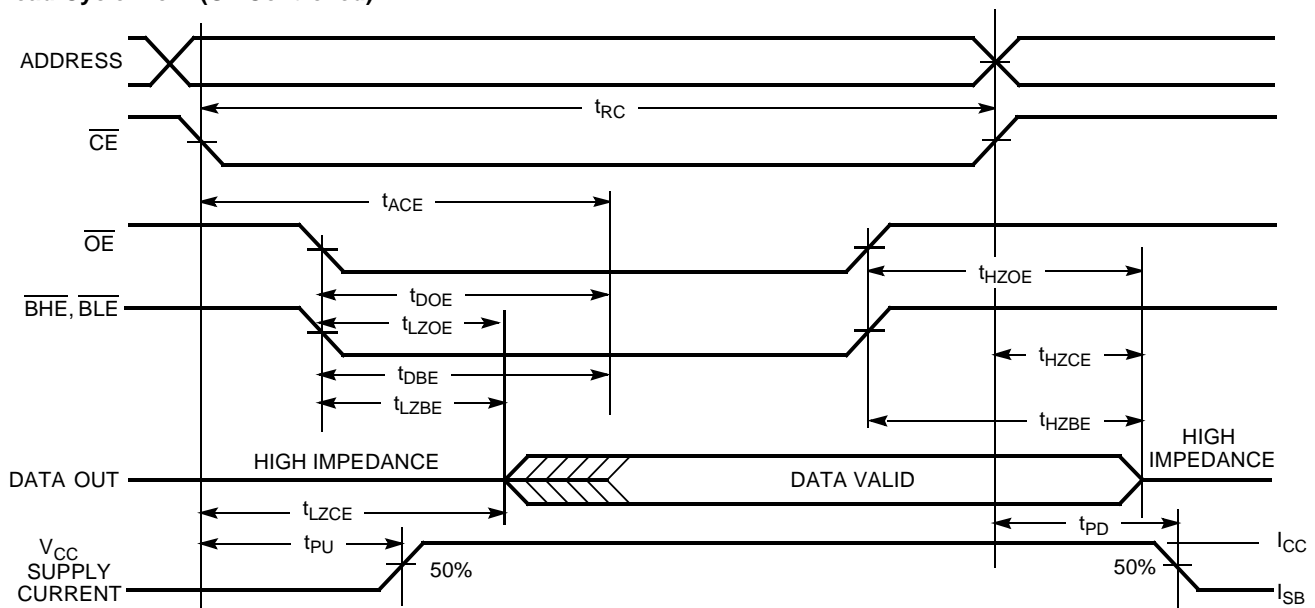
Notes:
10. AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
11. Device is continuously selected. OE, CE, BHE and/or BHE = V_{IL}.
12. $\overline{WE}$ is HIGH for Read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)[14, 15]
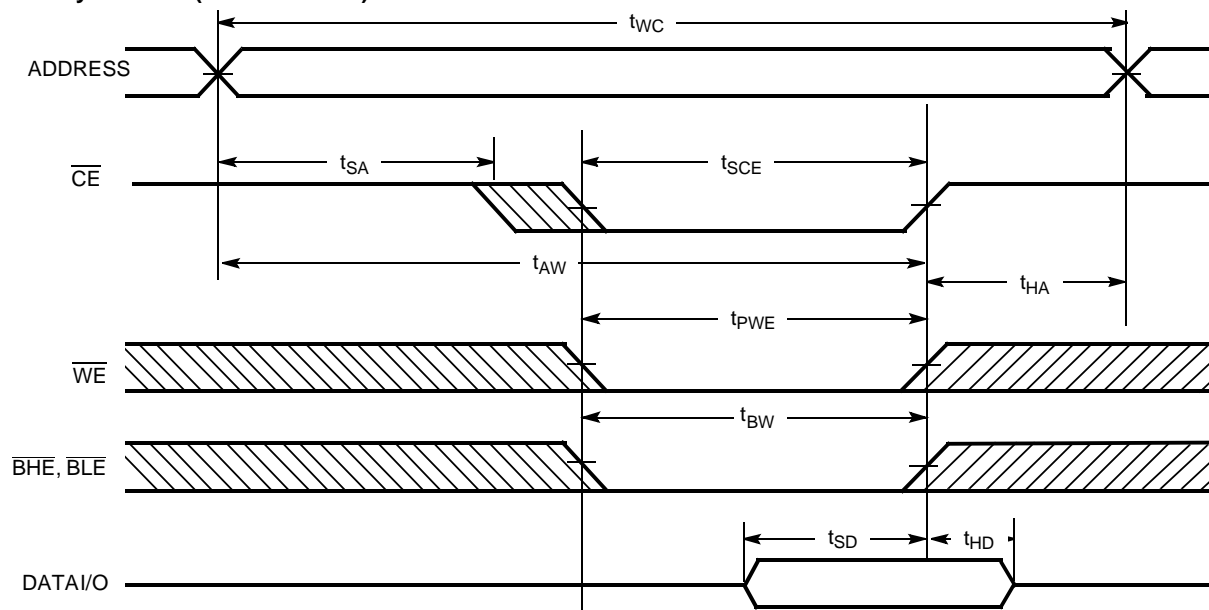
Write Cycle No. 2 (BLE or BHE Controlled)
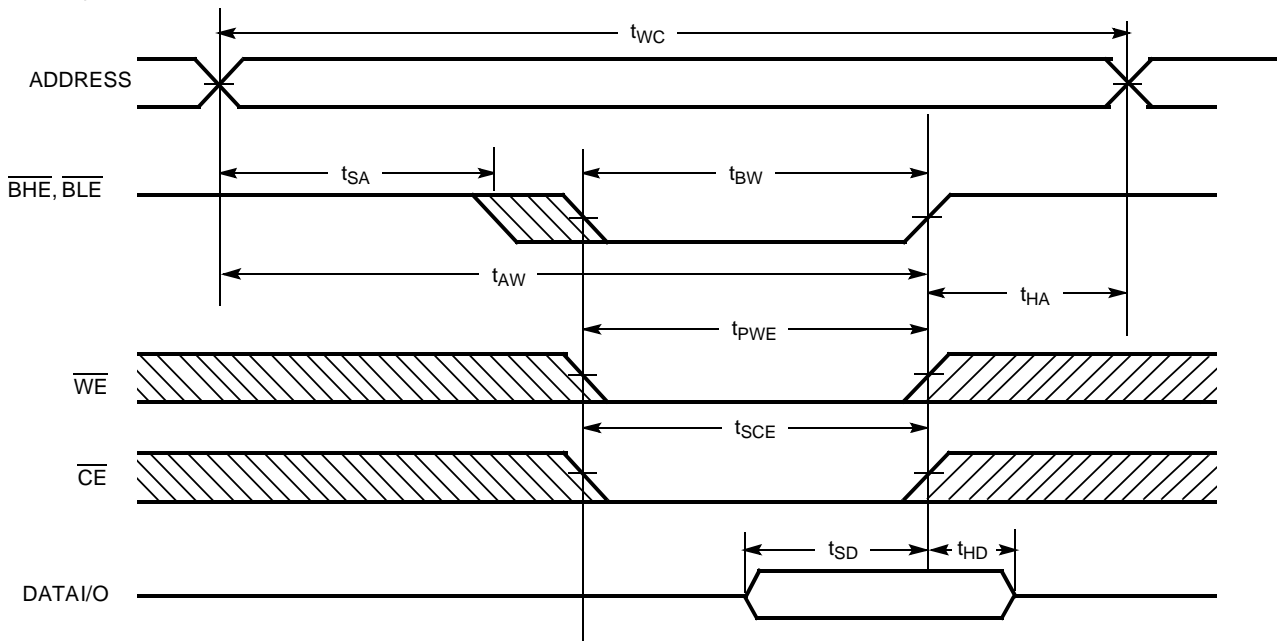
Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)
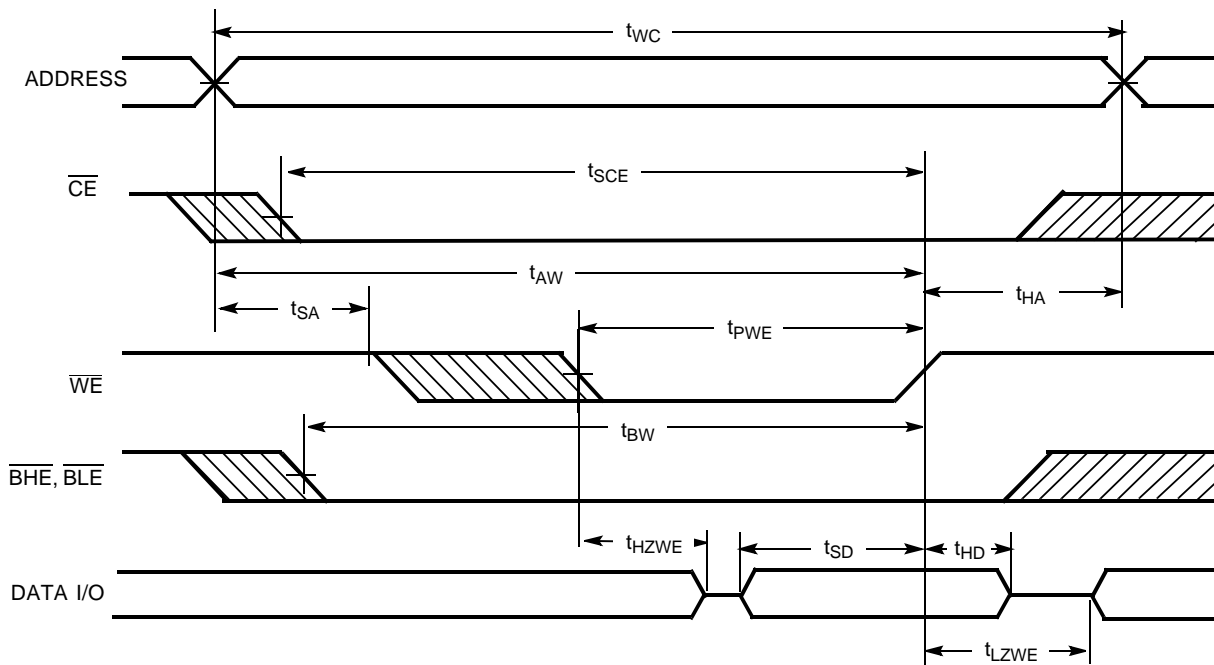
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

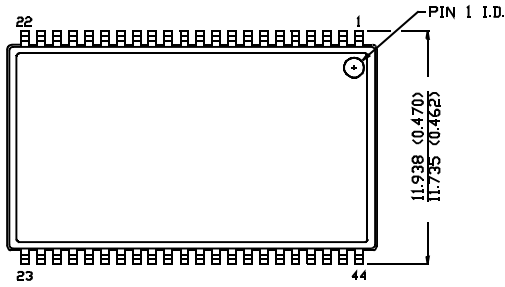| CY7C1041CV33				
Speed (ns)	**Ordering Code**	**Package Name**	**Package Type**	**Operating Range**
10	CY7C1041CV33-10BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-10VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-10ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-10BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-10VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-10ZI	Z44	44-pin TSOP II Z44	
12	CY7C1041CV33-12BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-12VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-12ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-12BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-12VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-12ZI	Z44	44-pin TSOP II Z44	
15	CY7C1041CV33-15BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-15VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-15ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-15BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-15VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-15ZI	Z44	44-pin TSOP II Z44	
20	CY7C1041CV33-20BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-20VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-20ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-20BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-20VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-20ZI	Z44	44-pin TSOP II Z44	

Package Diagrams

48-ball (7.00 mm x 8.5 mm x 1.2 mm) FBGA BA48B

51-85106-*D
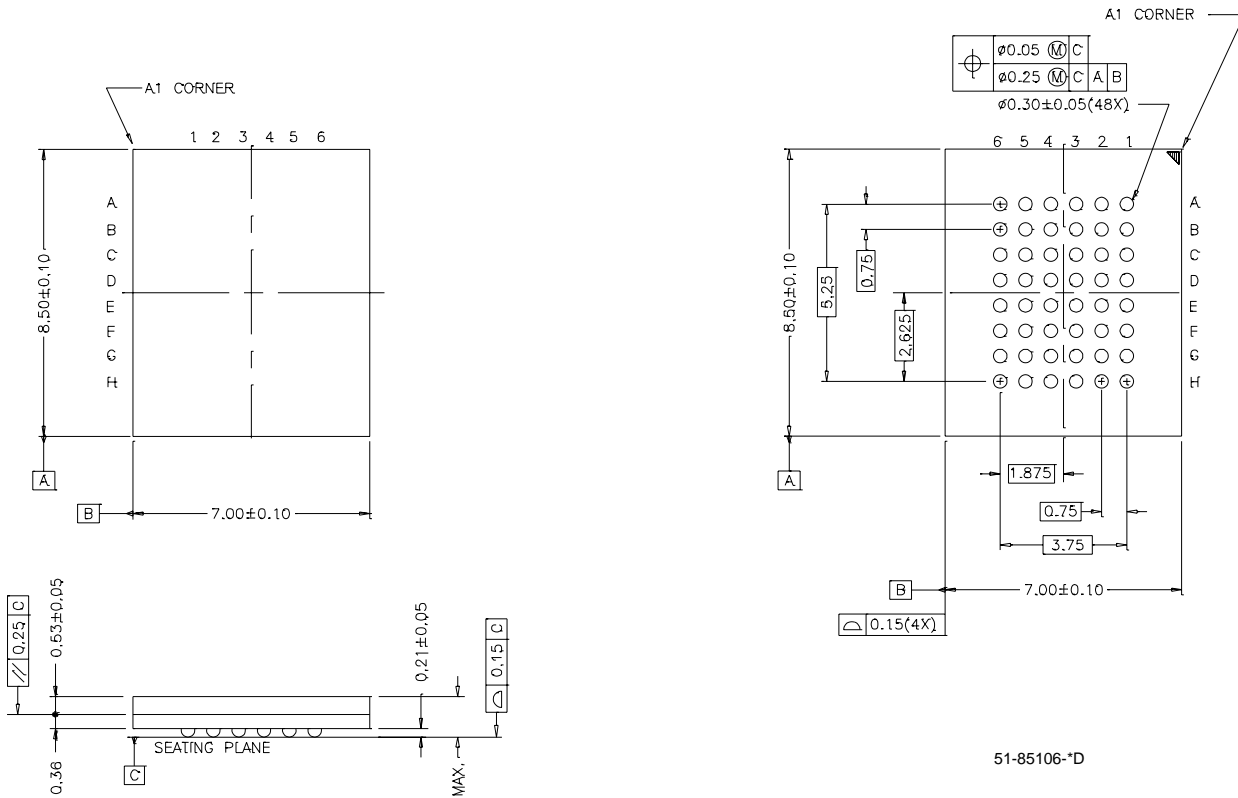
44-lead (400-mil) Molded SOJ V34
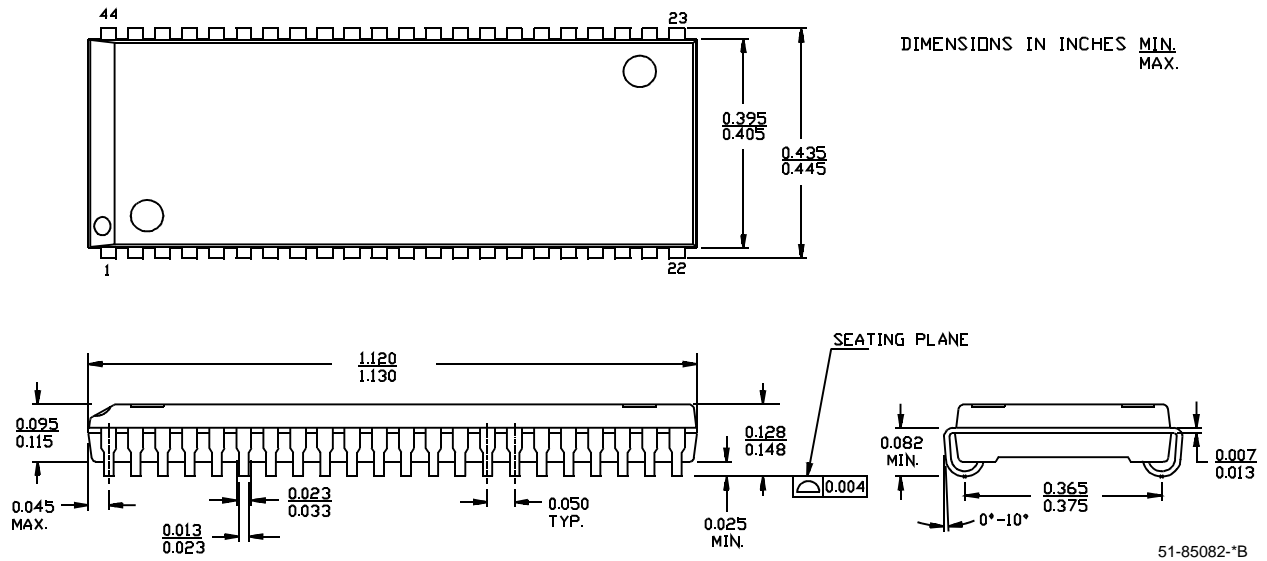
51-85082-*B

Package Diagrams (continued)

44-pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX
MIN.
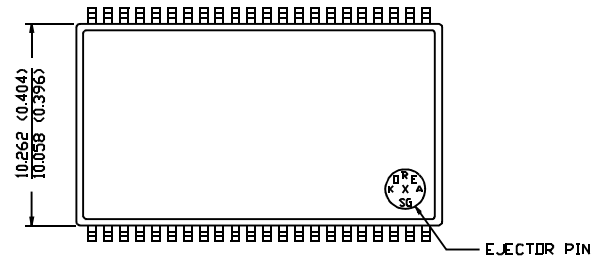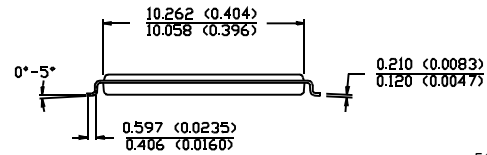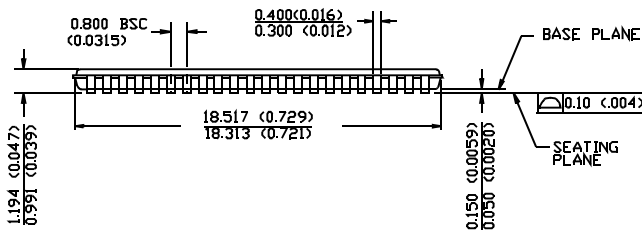
51-85087-*A

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Document History Page

Document Title: CY7C1041CV33 256K x 16 Static RAM Document Number: 38-05134				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109513	12/13/01	HGK	New Data Sheet
*A	112440	12/20/01	BSS	Updated 51-85106 from revision *A to *C
*B	112859	03/25/02	DFP	Added CY7C1042CV33 in BGA package Removed 1042 BGA option pin ACC Final Data Sheet
*C	116477	09/16/02	CEA	Add applications foot note to data sheet
*D	119797	10/21/02	DFP	Added 20-ns speed bin