



256K x 16 Static RAM

Features

- Pin equivalent to CY7C1041BV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 324 mW (max.)
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features

Functional Description<sup>[1]</sup>

The CY7C1041CV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

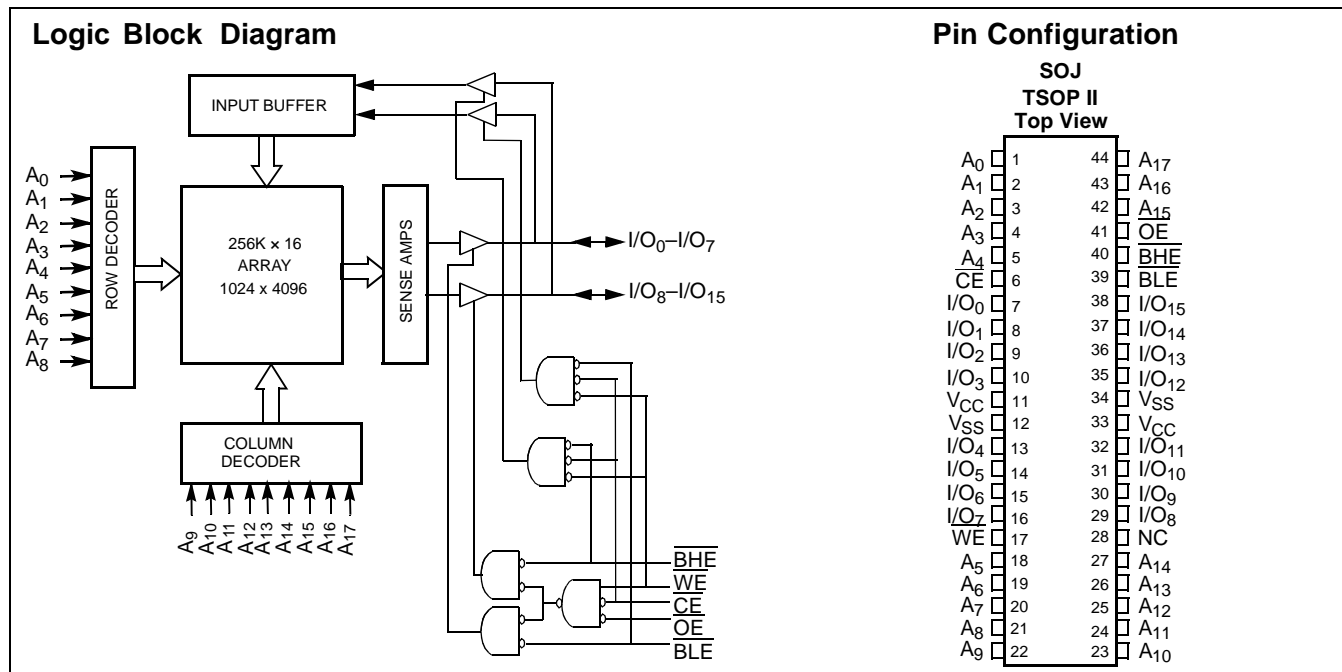
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte LOW Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub>–I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub>–A<sub>17</sub>). If Byte

HIGH Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub>–I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub>–A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte LOW Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> – I/O<sub>7</sub>. If Byte HIGH Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O<sub>0</sub>–I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled ( $\overline{BHE}$ , BLE HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1041CV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout, as well as a 48-ball fine-pitch ball grid array (FBGA) package.



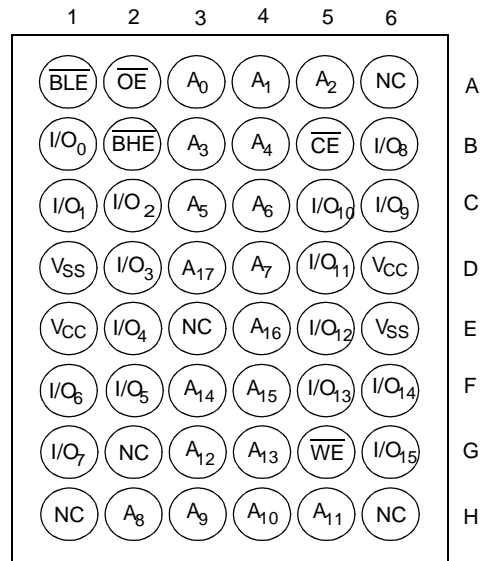
Selection Guide

		-8	-10	-12	-15	-20	Unit
Maximum Access Time		8	10	12	15	20	ns
Maximum Operating Current	Commercial	100	90	85	80	75	mA
	Industrial	110	100	95	90	85	mA
Maximum CMOS Standby Current	Commercial/ Industrial	10	10	10	10	10	mA

Shaded areas contain advance information.

Note:

1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configurations**
**48-ball Mini FBGA**
**(Top View)**


**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State<sup>[2]</sup>..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-8		-10		-12		-15		-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}^{[2]}$	Input LOW Voltage		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	-1	+1	-1	+1	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC},$ Output Disabled	-1	+1	-1	+1	-1	+1	-1	+1	-1	+1	µA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Comm'l	100		90		85		80		75	mA
			Indus.	110		100		95		90		85	mA
$I_{SB1}$	Automatic CE Power-down Current —TTL Inputs	Max. $V_{CC}, CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		40		40		40		40		40	mA
$I_{SB2}$	Automatic CE Power-down Current —CMOS Inputs	Max. $V_{CC}, CE \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V, f = 0$	Comm'l	10		10		10		10		10	mA
			Indus.										

Shaded areas contain advance information.

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	8	pF
$C_{OUT}$	I/O Capacitance		8	pF

**Notes:**

- Minimum voltage is -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

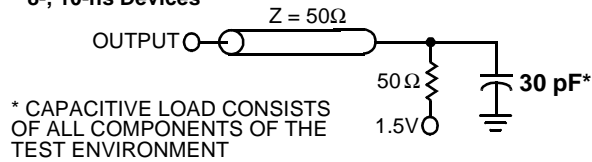
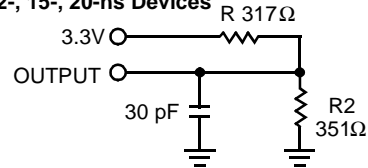
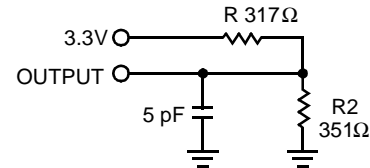
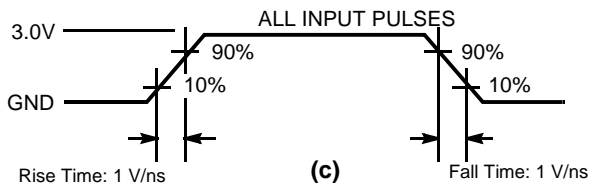
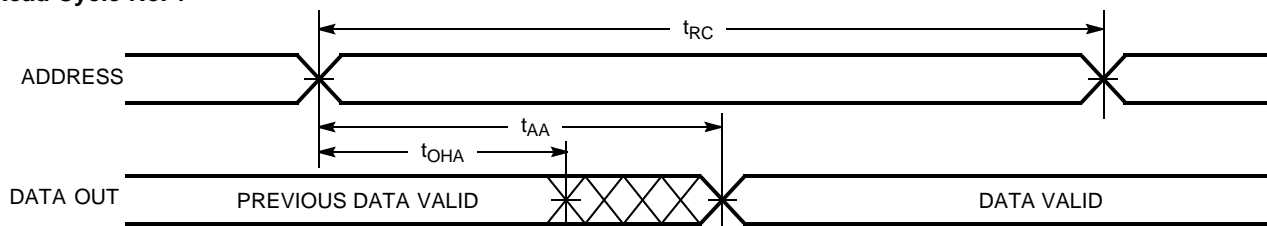
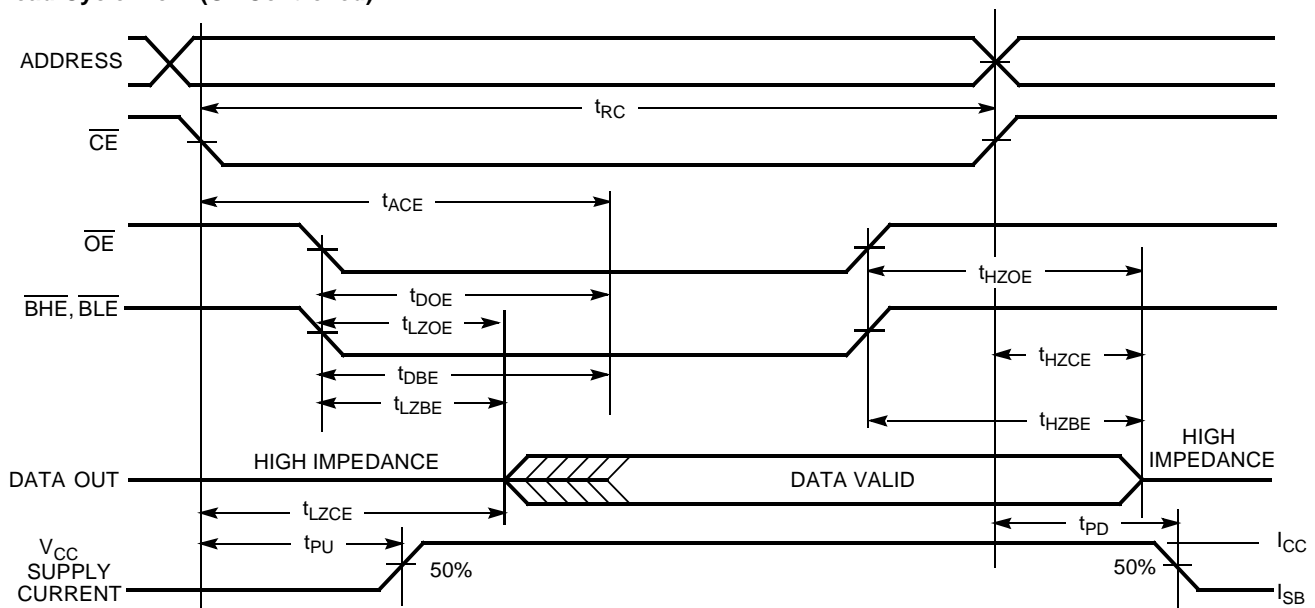
**AC Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	-8		-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>												
$t_{power}^{[5]}$	$V_{CC}$ (typical) to the first access	1		1		1		1		1		$\mu$ s
$t_{RC}$	Read Cycle Time	8		10		12		15		20		ns
$t_{AA}$	Address to Data Valid		8		10		12		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		8		10		12		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		4		5		6		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z	0		0		0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[6, 7]</sup>		4		5		6		7		8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[7]</sup>	3		3		3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[6, 7]</sup>		4		5		6		7		8	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		8		10		12		15		20	ns
$t_{DBE}$	Byte Enable to Data Valid		4		5		6		7		8	ns
$t_{LZBE}$	Byte Enable to Low-Z	0		0		0		0		0		ns
$t_{HZBE}$	Byte Disable to High-Z		6		6		6		7		8	ns
<b>Write Cycle<sup>[8, 9]</sup></b>												
$t_{WC}$	Write Cycle Time	8		10		12		15		20		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	6		7		8		10		10		ns
$t_{AW}$	Address Set-Up to Write End	6		7		8		10		10		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	6		7		8		10		10		ns
$t_{SD}$	Data Set-Up to Write End	4		5		6		7		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>	3		3		3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[6, 7]</sup>		4		5		6		7		8	ns
$t_{BW}$	Byte Enable to End of Write	6		7		8		10		10		ns

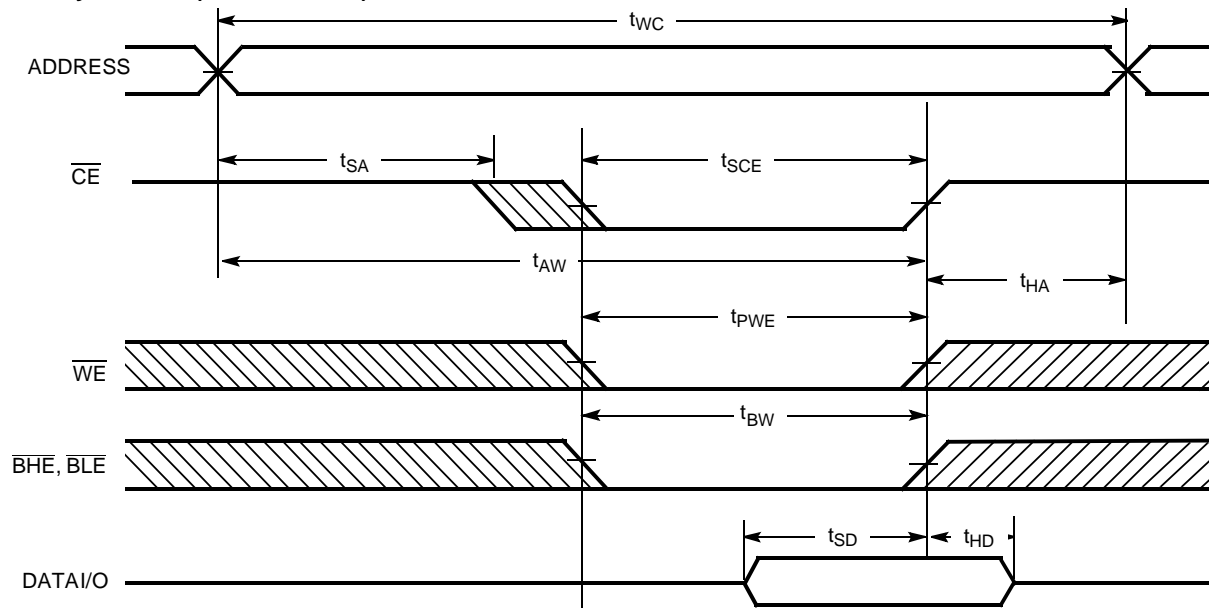
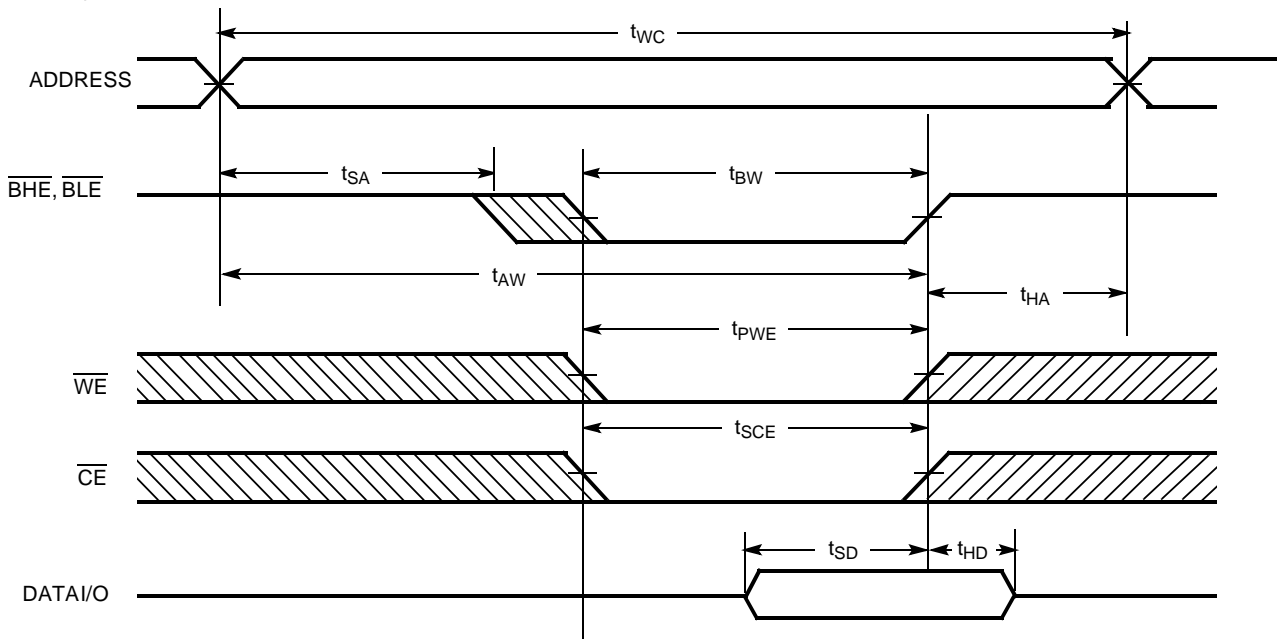
Shaded areas contain advance information.

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

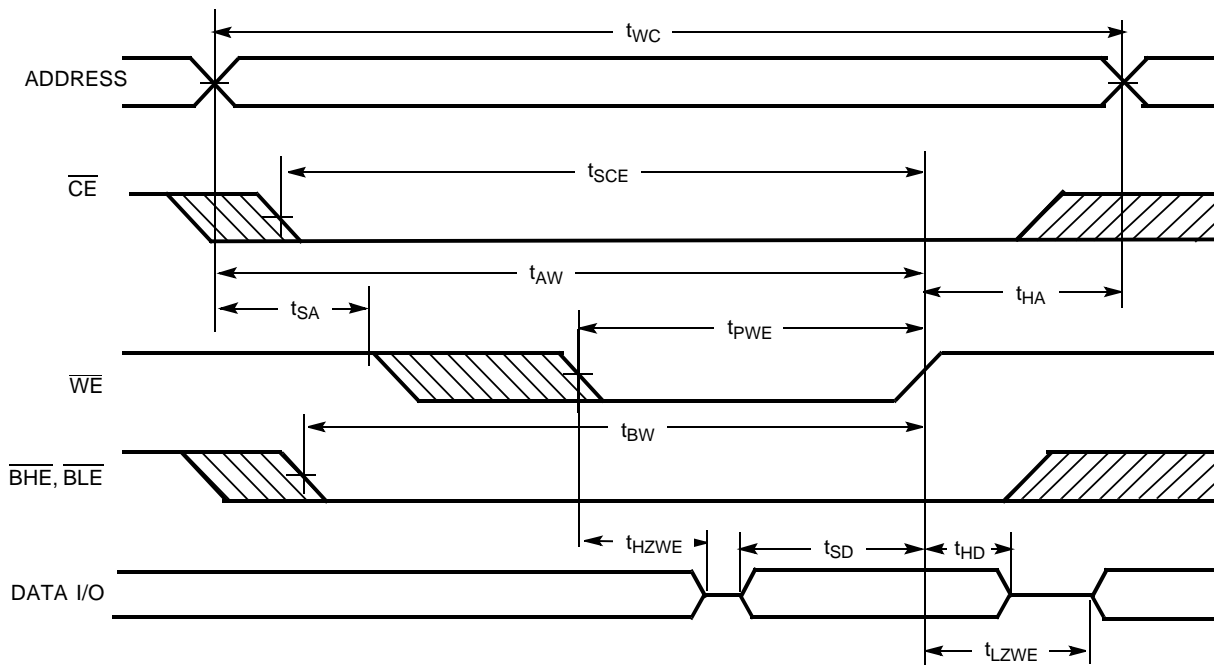
**AC Test Loads and Waveforms<sup>[10]</sup>**
**8-, 10-ns Devices**

**(a)**
**12-, 15-, 20-ns Devices**

**(b)**
**High-Z Characteristics**

**(d)**

**(c)**
**Switching Waveforms**
**Read Cycle No. 1<sup>[11, 12]</sup>**

**Read Cycle No. 2 (OE Controlled)<sup>[12, 13]</sup>**

**Notes:**

10. AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
11. Device is continuously selected. OE, CE, BHE and/or BLE =  $V_{IL}$ .
12. WE is HIGH for Read cycle.
13. Address valid prior to or coincident with CE transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

14. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active ( $I_{CC}$ )
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active ( $I_{CC}$ )
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write All Bits	Active ( $I_{CC}$ )
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active ( $I_{CC}$ )
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

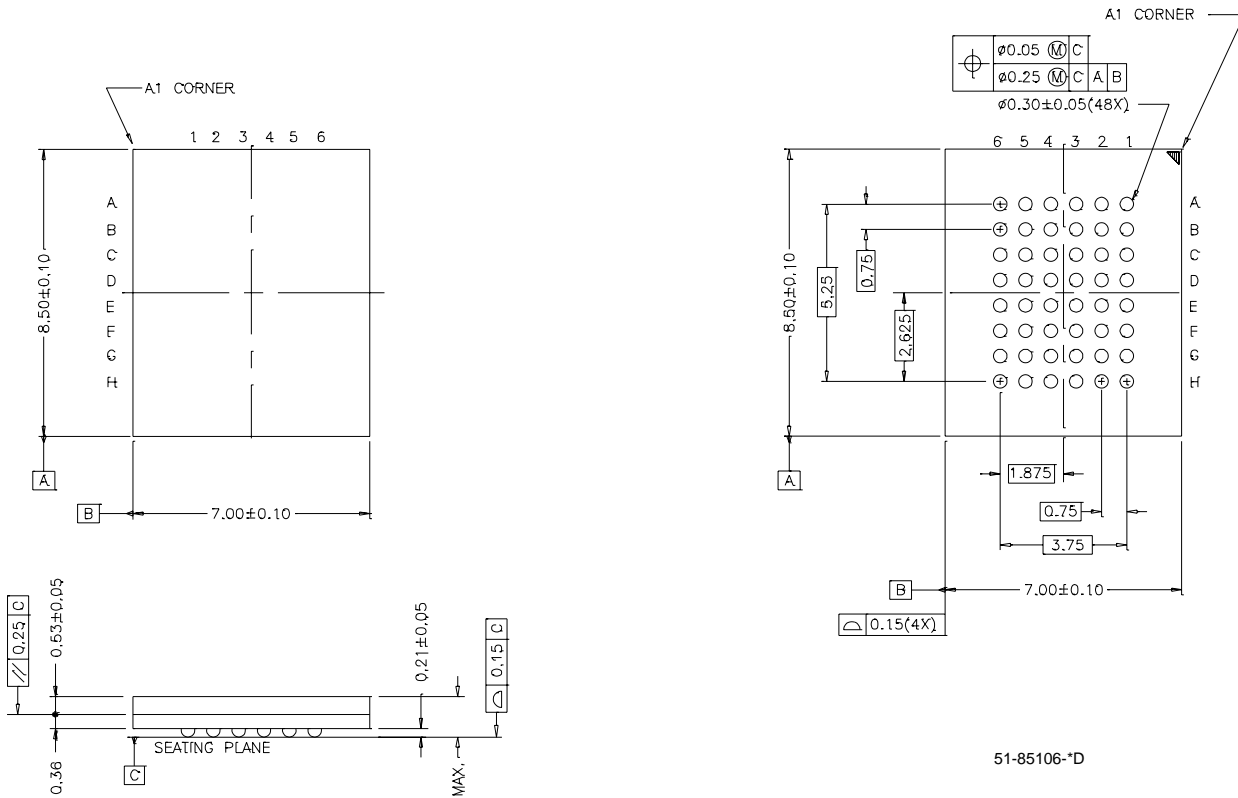
<b>CY7C1041CV33</b>				
<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
10	CY7C1041CV33-10BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-10VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-10ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-10BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-10VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-10ZI	Z44	44-pin TSOP II Z44	
12	CY7C1041CV33-12BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-12VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-12ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-12BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-12VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-12ZI	Z44	44-pin TSOP II Z44	
15	CY7C1041CV33-15BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-15VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-15ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-15BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-15VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-15ZI	Z44	44-pin TSOP II Z44	
20	CY7C1041CV33-20BAC	BA48B	48-ball Fine Pitch BGA	Commercial
	CY7C1041CV33-20VC	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-20ZC	Z44	44-pin TSOP II Z44	
	CY7C1041CV33-20BAI	BA48B	48-ball Fine Pitch BGA	Industrial
	CY7C1041CV33-20VI	V34	44-lead (400-mil) Molded SOJ	
	CY7C1041CV33-20ZI	Z44	44-pin TSOP II Z44	



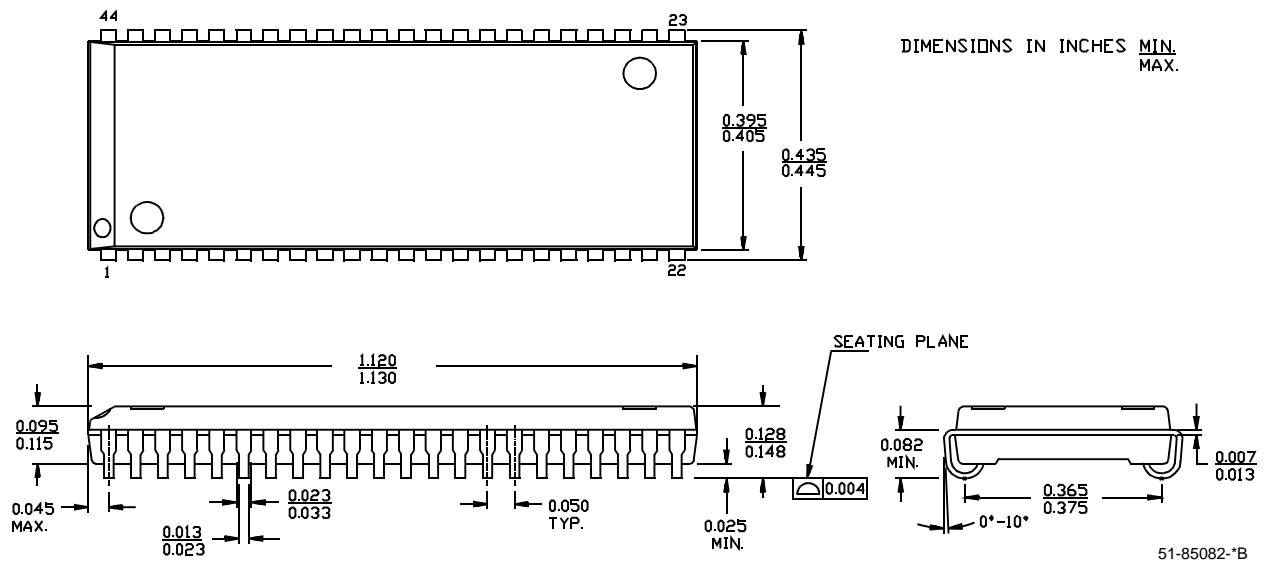
**Package Diagrams**
**48-ball (7.00 mm x 8.5 mm x 1.2 mm) FBGA BA48B**

TOP VIEW

BOTTOM VIEW

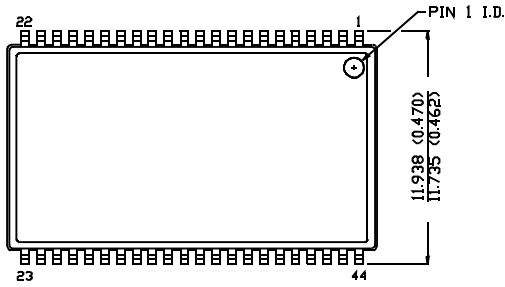
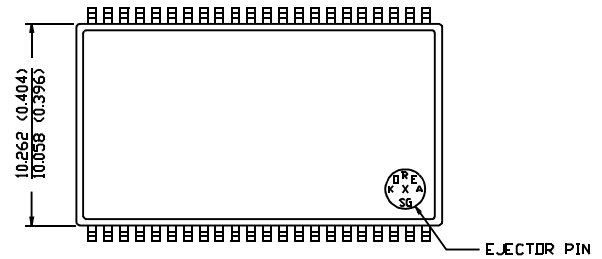
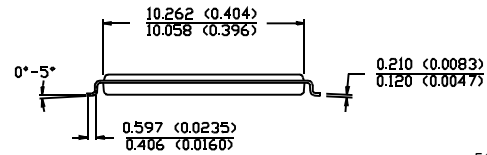
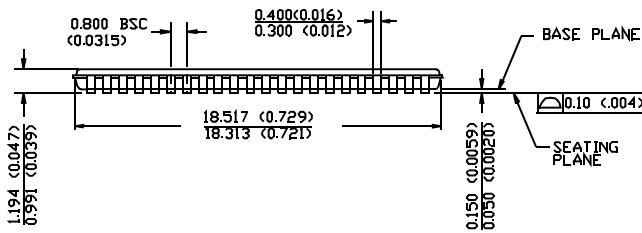


51-85106-\*D

**44-lead (400-mil) Molded SOJ V34**


51-85082-\*B

**Package Diagrams (continued)**
**44-pin TSOP II Z44**

 DIMENSION IN MM (INCH)  
 MAX  
 MIN.

**TOP VIEW**

**BOTTOM VIEW**


51-85087-A

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**Document History Page**

<b>Document Title: CY7C1041CV33 256K x 16 Static RAM</b>				
<b>Document Number: 38-05134</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109513	12/13/01	HGK	New Data Sheet
*A	112440	12/20/01	BSS	Updated 51-85106 from revision *A to *C
*B	112859	03/25/02	DFP	Added CY7C1042CV33 in BGA package Removed 1042 BGA option pin ACC Final Data Sheet
*C	116477	09/16/02	CEA	Add applications foot note to data sheet
*D	119797	10/21/02	DFP	Added 20-ns speed bin