CY7C1011CV33

128K x 16 Static RAM

Features

- **Pin equivalent to CY7C1011BV33**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— 360 mW (max.)**
- **Data Retention at 2.0**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Easy memory expansion with CE and OE features**
- **Available in 44-pin TSOP II, 44-pin TQFP, and 48-ball VFBGA**

Functional Description

The CY7C1011CV33 is a high-performance CMOS Static RAM organized as 131,072 words by 16 bits.

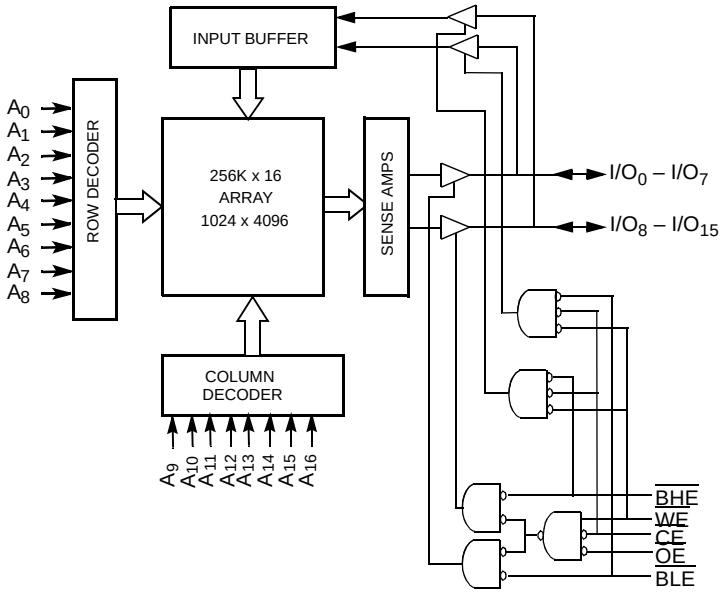
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

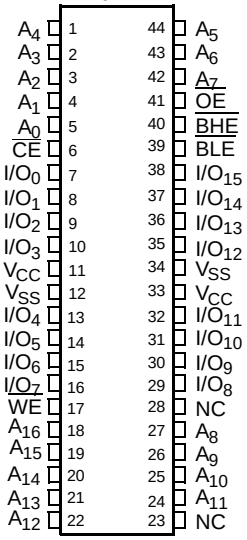
The CY7C1011CV33 is available in a standard 44-pin TSOP II package with center power and ground pinout, a 44-pin Thin Plastic Quad Flatpack (TQFP), as well as a 48-ball fine-pitch ball grid array (VFBGA) package.

Logic Block Diagram



Pin Configuration

TSOP II
Top View

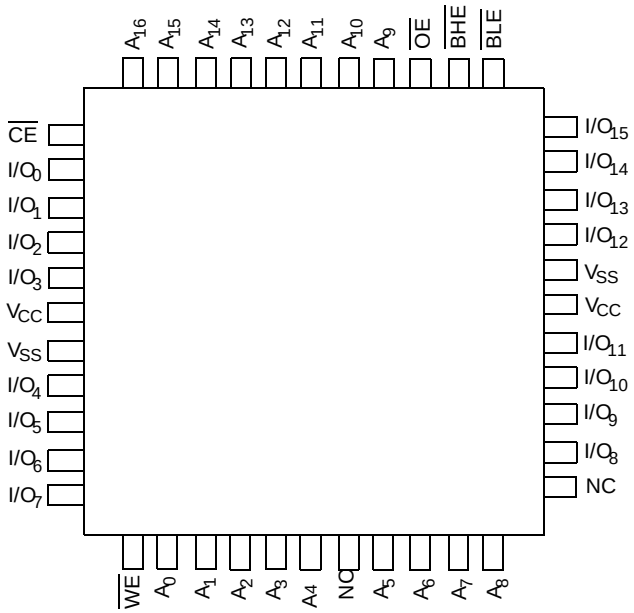


Selection Guide

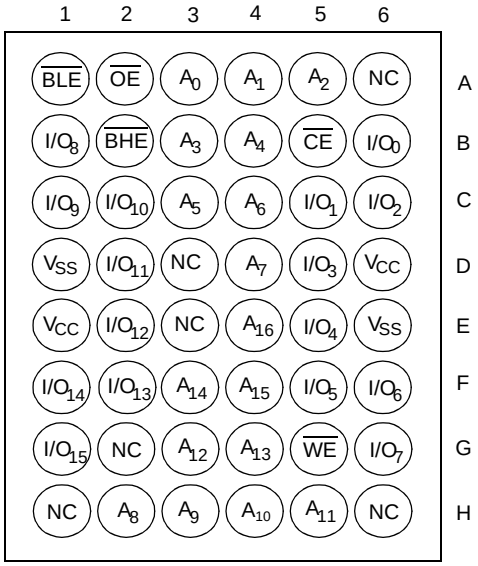
		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Comm'l	90	85	80	mA
	Ind'l	100	95	90	
Maximum CMOS Standby Current	Com'l/Ind'l	10	10	10	mA

Pin Configurations

44-pin TQFP
(Top View)



48-ball VFBGA
(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l		90		85		80	mA
			Ind'l		100		95		90	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40		40	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/ Ind'l		10		10		10	mA

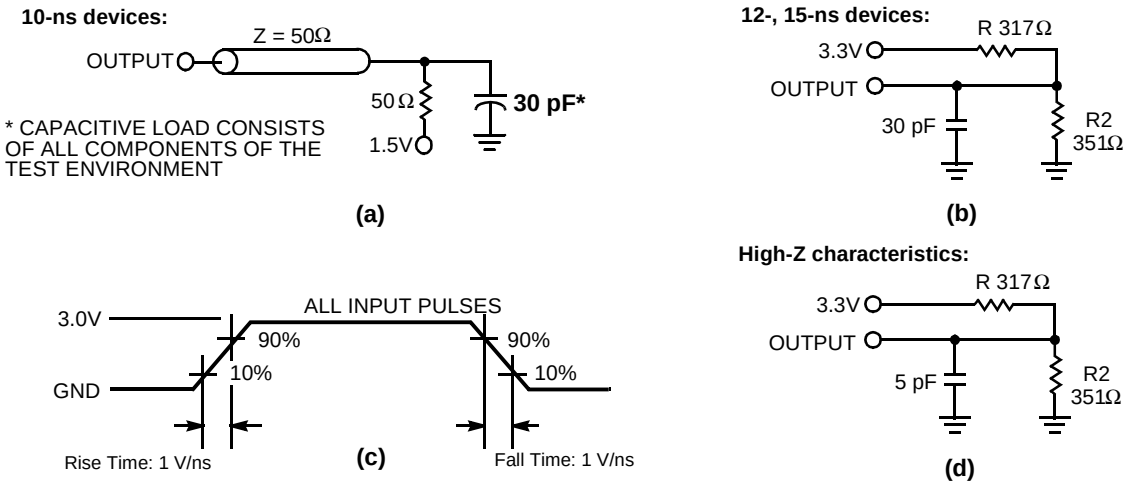
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]



AC Switching Characteristics Over the Operating Range [4]

Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}[5]	V_{CC}(typical) to the first access	1		1		1		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		6		6		7	ns
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	10		12		15		ns

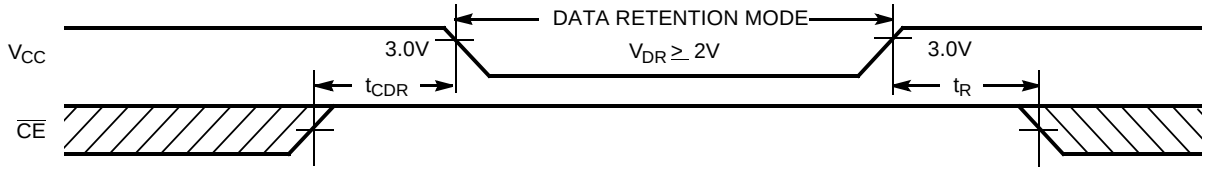
Notes:

3. AC characteristics (except High-Z) for all 10-ns parts are tested using the load conditions shown in (a). All other speeds are tested using the Thevenin load shown in (b). High-Z characteristics are tested for all speeds using the test load shown in (d).
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

AC Switching Characteristics Over the Operating Range (continued)[4]

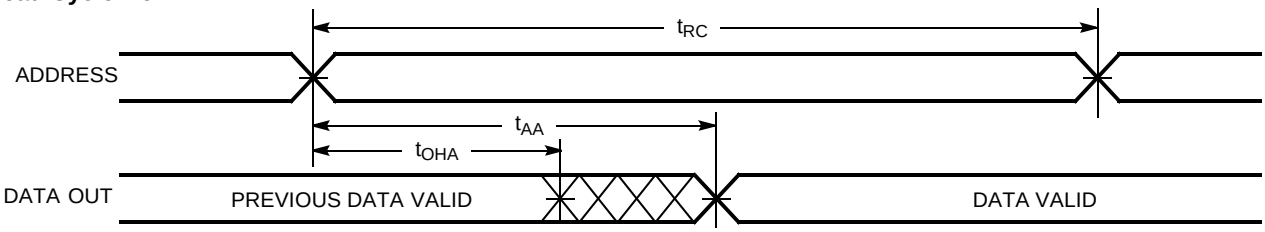
Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		10		ns
t_{AW}	Address Set-up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Set-up to Write End	5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		5		6		7	ns
t_{BW}	Byte Enable to End of Write	7		8		10		ns

Data Retention Waveform



Switching Waveforms

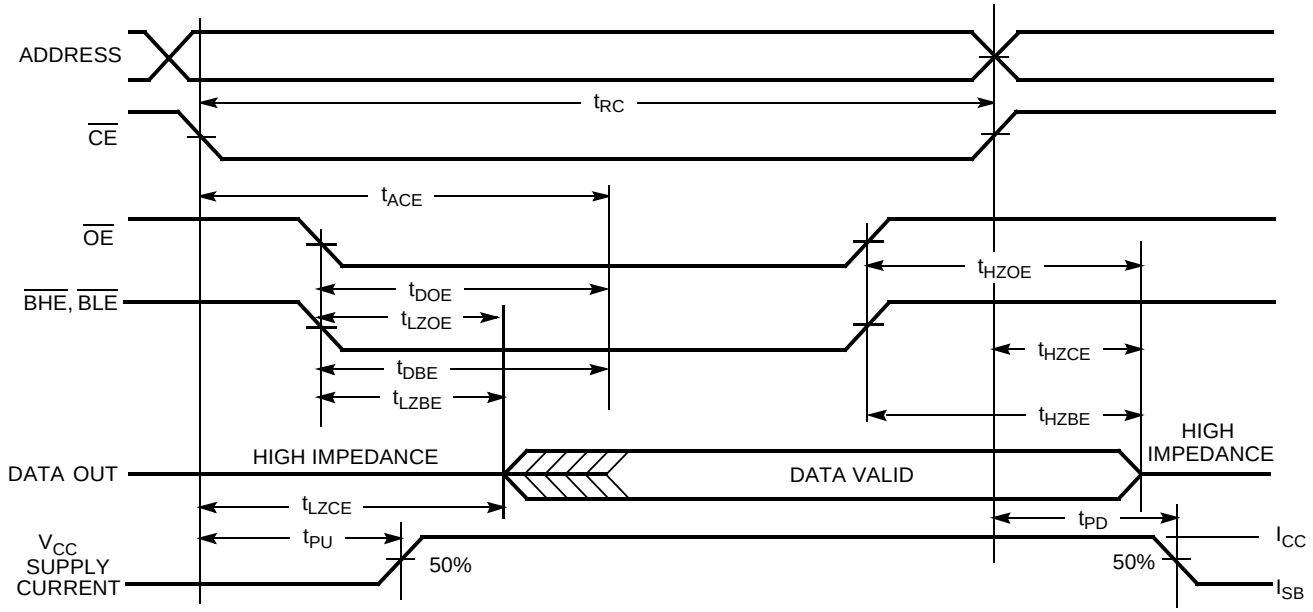
Read Cycle No. 1[10, 11]



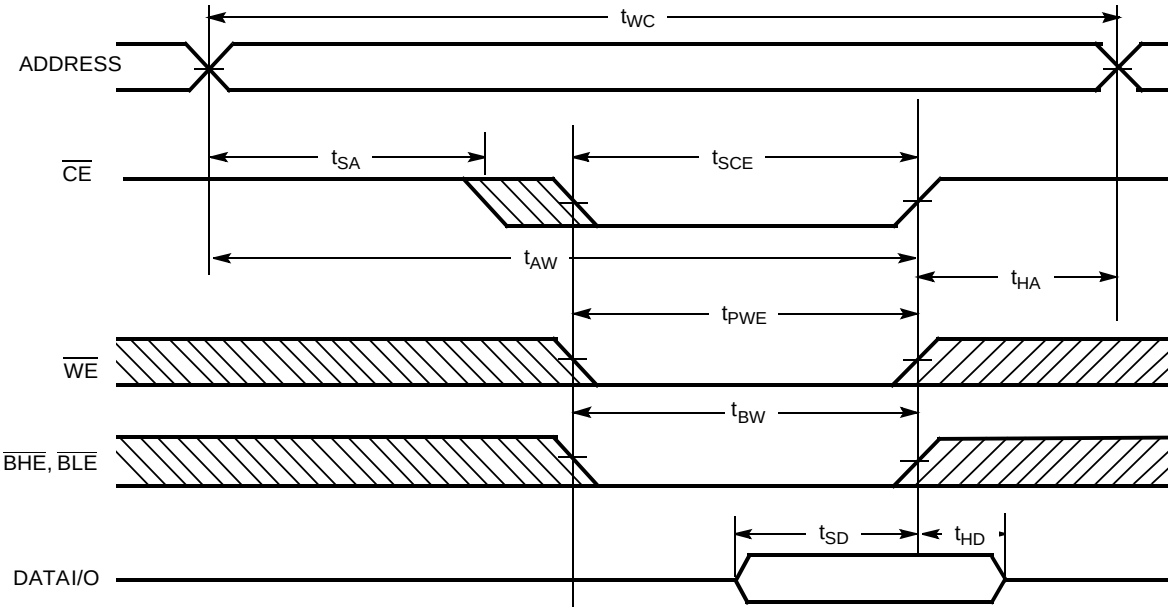
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled) [11, 12]



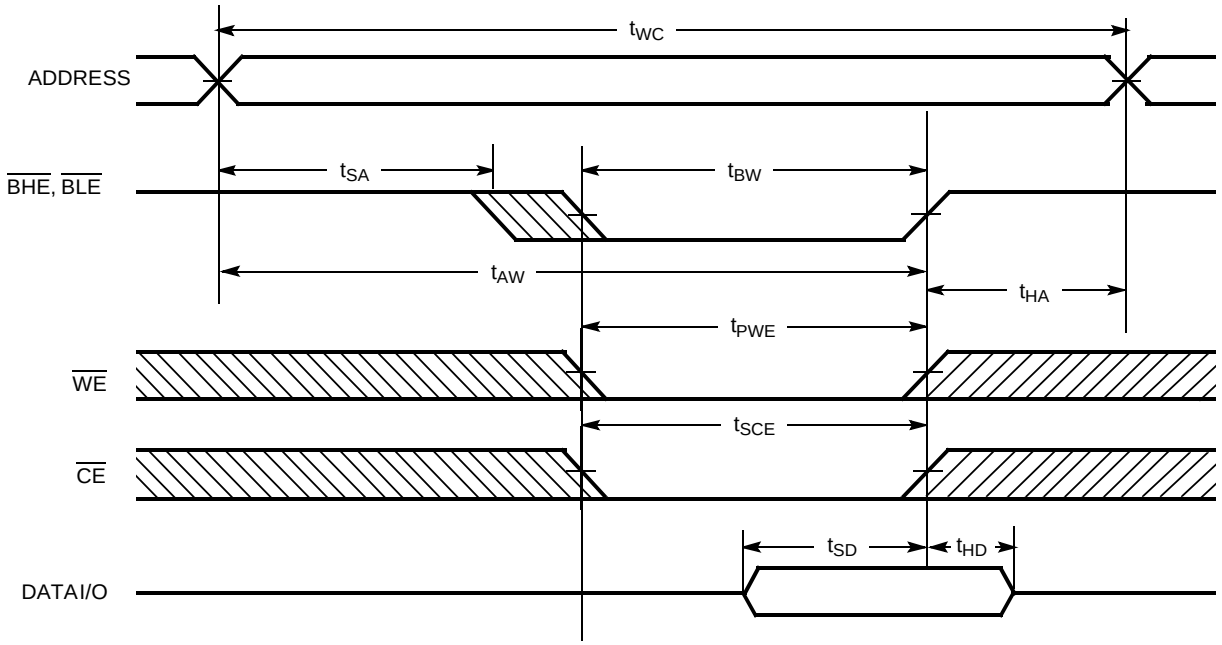
Write Cycle No. 1 ($\overline{CE}$ Controlled) [13, 14]



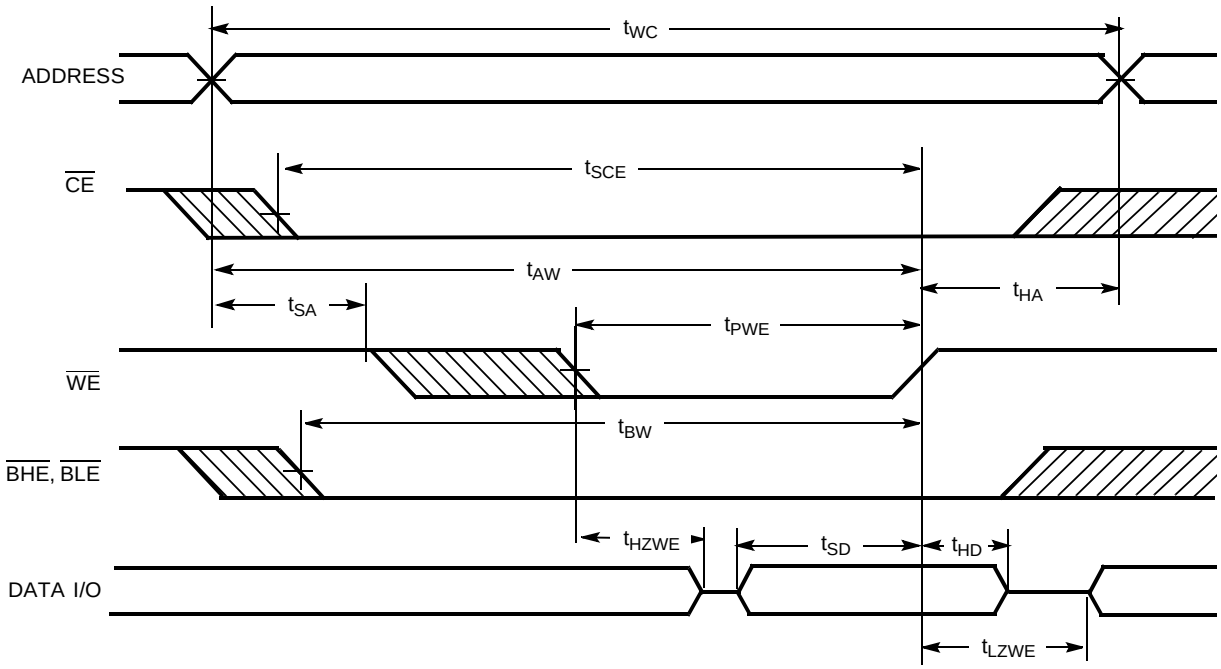
Notes:
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Write Cycle No. 3 ($\overline{WE}$ Controlled,



Truth Table

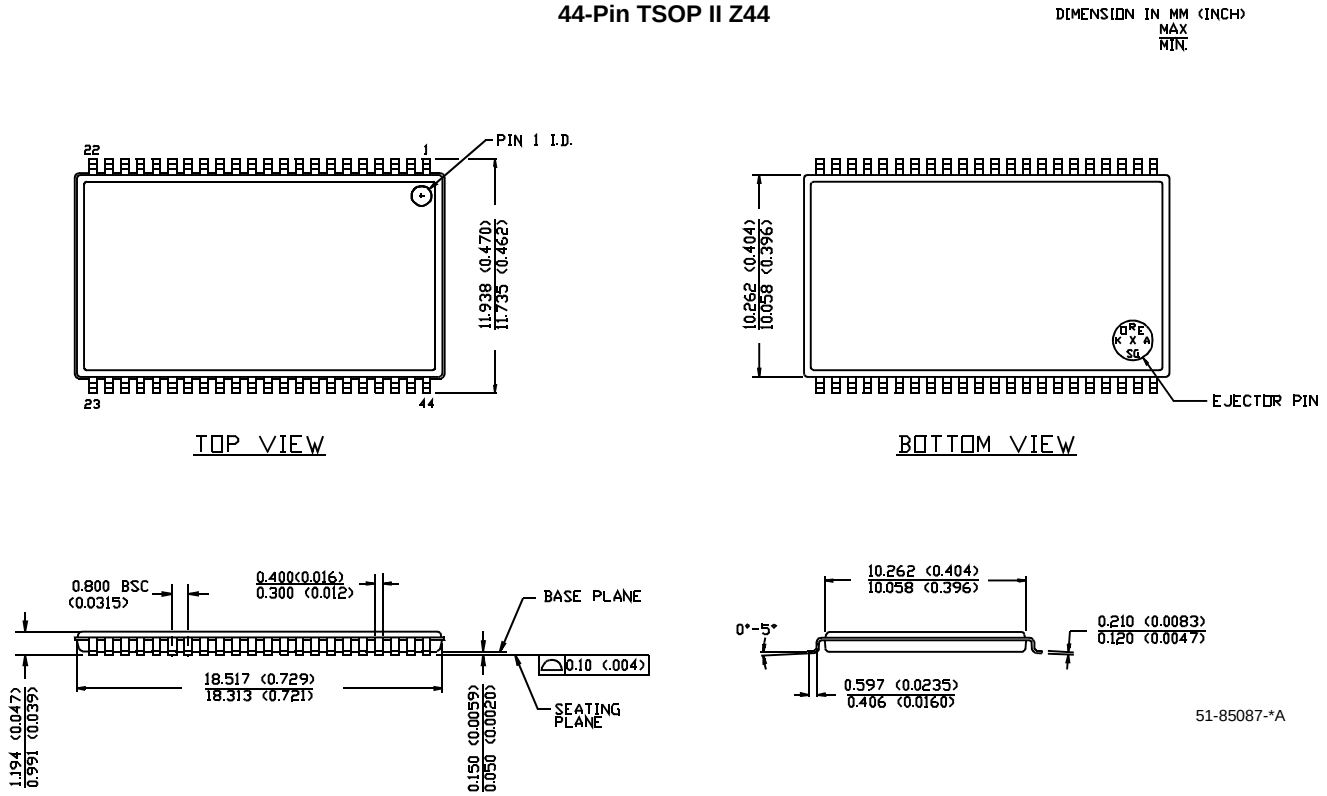
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

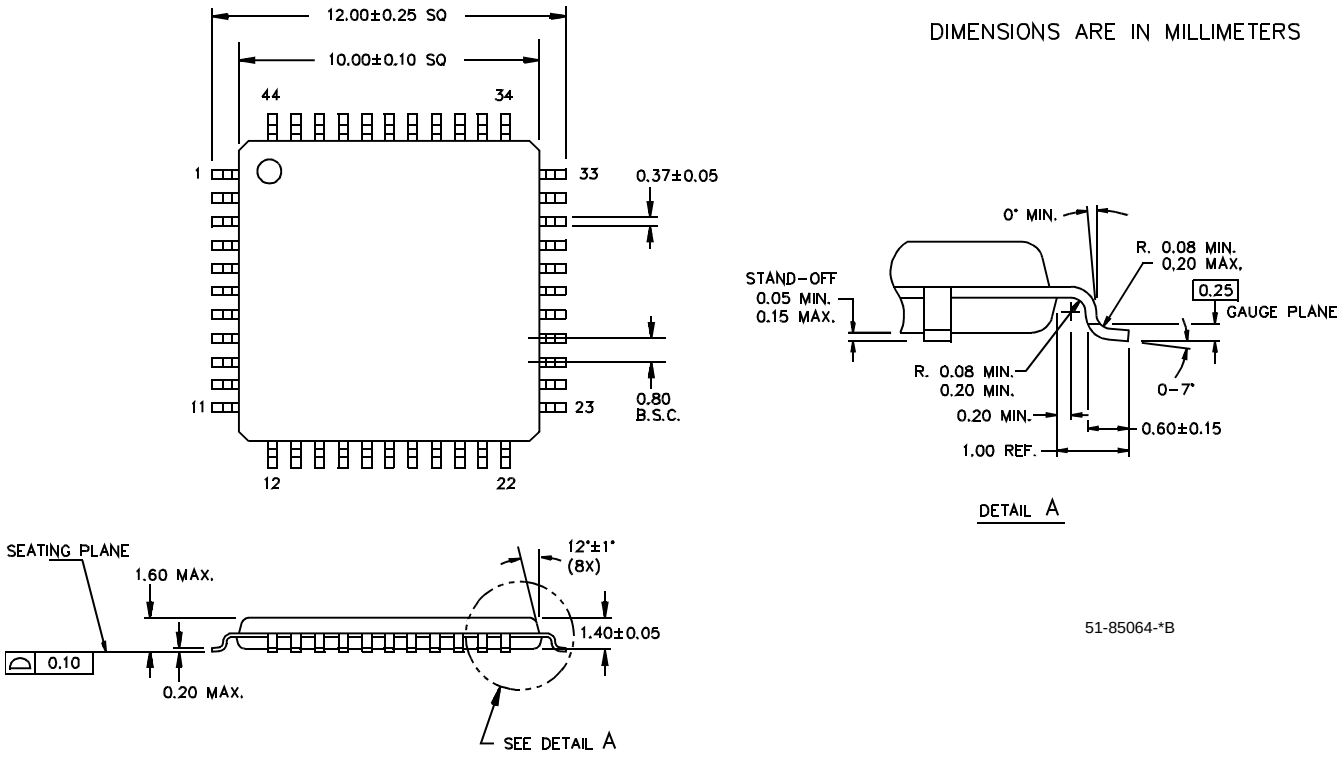
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1011CV33-10ZC	Z44	44-pin TSOP II	Commercial
	CY7C1011CV33-10BVC	BV48A	48-ball VFBGA	
	CY7C1011CV33-10ZI	Z44	44-pin TSOP II	Industrial
	CY7C1011CV33-10BVI	BV48A	48-ball VFBGA	
12	CY7C1011CV33-12ZC	Z44	44-pin TSOP II	Commercial
	CY7C1011CV33-12AC	A44	44-pin TQFP	
	CY7C1011CV33-12BVC	BV48A	48-ball VFBGA	
	CY7C1011CV33-12ZI	Z44	44-pin TSOP II	Industrial
	CY7C1011CV33-12AI	A44	44-pin TQFP	
	CY7C1011CV33-12BVI	BV48A	48-ball VFBGA	
15	CY7C1011CV33-15ZC	Z44	44-pin TSOP II	Commercial
	CY7C1011CV33-15AC	A44	44-pin TQFP	
	CY7C1011CV33-15BVC	BV48A	48-ball VFBGA	
	CY7C1011CV33-15ZI	Z44	44-pin TSOP II	Industrial
	CY7C1011CV33-15AI	A44	44-pin TQFP	
	CY7C1011CV33-15BVI	BV48A	48-ball VFBGA	

Package Diagrams

44-Pin TSOP II Z44

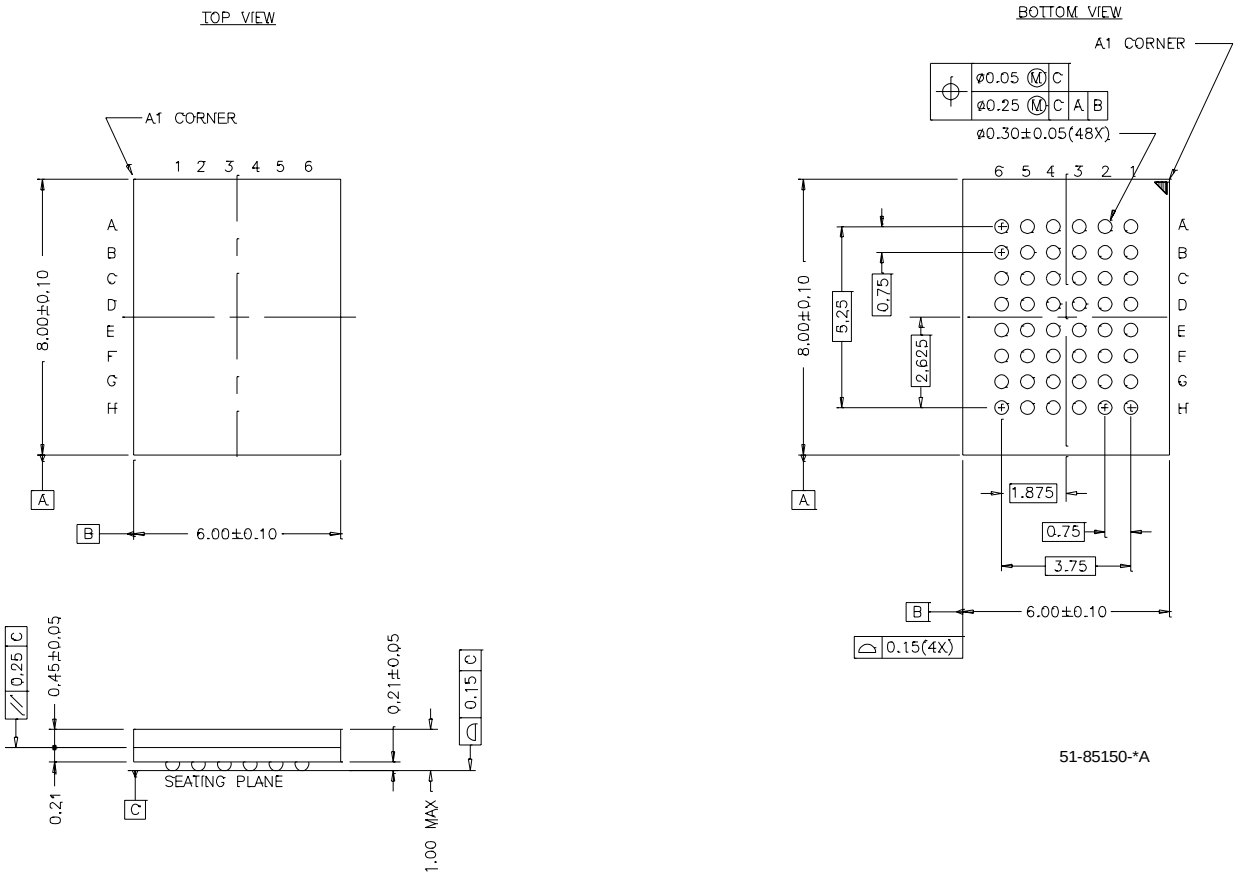


44-Lead Thin Plastic Quad Flat Pack A44



Package Diagrams (continued)

48-Lead VFBGA (6 x 8 x 1 mm) BV48A



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Document History Page

Document Title: CY7C1011CV33 128K x 16 Static RAM Document Number: 38-05232				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117132	07/31/02	HGK	New Data Sheet
*A	118057	08/19/02	HGK	Pin configuration for 48-ball FBGA correction
*B	119702	10/11/02	DFP	Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA.