FAIRCHILD SEMICONDUCTOR™

RC4200

Analog Multiplier

Features

- High accuracy
- Nonlinearity – 0.1%
  Temperature coefficient – 0.005%/°C
- Multiple functions
- Multiply, divide, square, square root, RMS-to-DC conversion, AGC and modulate/demodulate
- Wide bandwidth – 4 MHz
- Signal-to-noise ratio – 94 dB

Applications

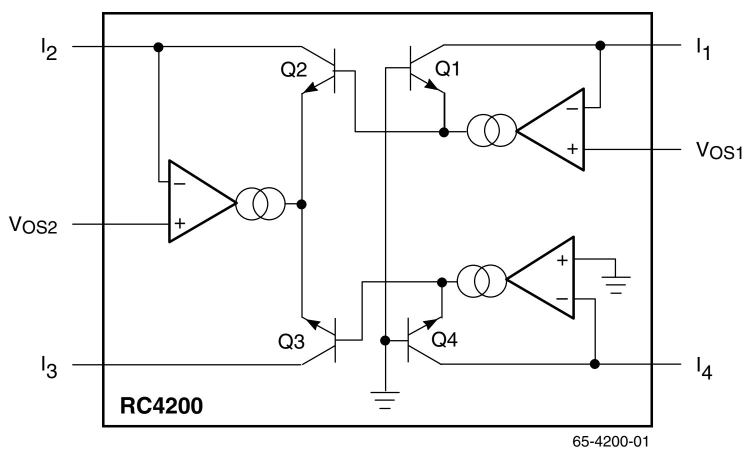
- Low distortion audio modulation circuits
- Voltage-controlled active filters
- Precision oscillators

Description

The RC4200 analog multiplier has complete compensation for nonlinearity, the primary source of error and distortion. This multiplier also has three onboard operational amplifiers designed specifically for use in multiplier logging circuits. These amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response.

The RC4200 can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very high accuracy and a low temperature coefficient.

Block Diagram



Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in the Block Diagram. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (1)$$

The three input currents must be positive and restricted to a range of 1 µA to 1 mA. These currents go into the multiplier chip at op amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capabilty of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2 and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship.

$$V_{BEN} = \frac{kT}{Q} \mathrm{In} \frac{I_{CN}}{I_{SN}} \quad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. The $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. Fairchild Semiconductor has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Fairchild Semiconductor developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{KT}{q}\left[\mathrm{In}\frac{I_1}{I_{S1}} = \mathrm{In}\frac{I_2}{I_{S2}} - \mathrm{In}\frac{I_3}{I_{S3}} - \mathrm{In}\frac{I_4}{I_{S4}}\right] = 0 \quad (3)$$

This equation reduces to:

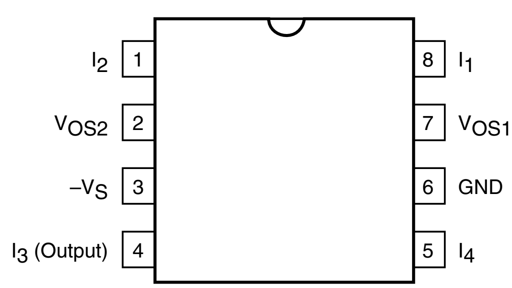
$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \quad (4)$$

The rate of reverse saturation current $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the rate is very close to unity, typically 1.0±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Pin Assignments



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Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
Supply Voltage[1]			-22	V
Input Current			-5	mA
Storage Temperature Range	RC4200/4200A	-55	+125	°C
Operating Temperature Range	RC4200/4200A	0	+70	°C

Notes:
1. For a supply voltage greater than -22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

(Still air, soldered into PC board)

	8-Lead Plastic DIP	8-Lead SOIC
Maximum Junction Temperature	+125°C	+125˚C
Maximum P_D T_A < 50°C	468mW	300mW
Thermal Resistance θ_{JC}	—	—
Thermal Resistance θ_{JA}	160°C/W	240˚C/W
For T_A > 50°C Derate at	6.25mW/°C	4.17mW/˚C

Electrical Characteristics

(Over operating temperature range, V_S = -15V unless otherwise noted)

		4200A			4200			
Parameters	**Test Conditlons**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Total Error as Multiplier	T_A = +25°C							
	Untrimmed[1]			±2.0			±3.0	%
	With External Trim		±0.2			±0.2		%
	Versus Temperature		±0.005			±0.005		%/°C
	Versus Supply (-9 to -18V)		±0.1			±0.1		%/V
Nonlinearity[2]	50µA ≤ $I_{1,2,4}$ ≤ 250 µA, T_A = +25°C			±0.1			±0.3	%
Input Current Range (I_1, I_2 and I_4)		1.0		1000	1.0		1000	µA
Input Offset Voltage	I_1 = I_2 = I_4 = 150 µA T_A = +25°C			±5.0			±10	mV
Input Bias Current	I_1 = I_2 = I_4 = 150 µA T_A = +25°C			300			500	nA
Average Input Offset Voltage Drift	I_1 = I_2 = I_4 = 150 µA			±50			±100	µV/°C
Output Current Range (I_3)[3]		1.0		1000	1.0		1000	µA

Electrical Characteristics (continued)

(Over operating temperature range, V_S = -15V unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Response, -3dB point			4.0			4.0		MHz
Supply Voltage		-18	-15	-9.0	-18	-15	-9.0	V
Supply Current	$I_1 = I_2 = I_4$ = 150 µA T_A = +25°C			4.0			4.0	mA

Notes:

1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at I_1, I_2, I_4 < 50 µA and linearity decreases when I_1, I_2, I_4 > 250 µA (eq. @ $I_1 = I_2$ = 500 µA, nonlinearity error ≈ 0.5%).
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Applications Discussion

Current Multiplier/ Divider

The basic design criteria for all circuit configurations using the RC4200 multiplier is contained in equation (1), that is,

$$I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

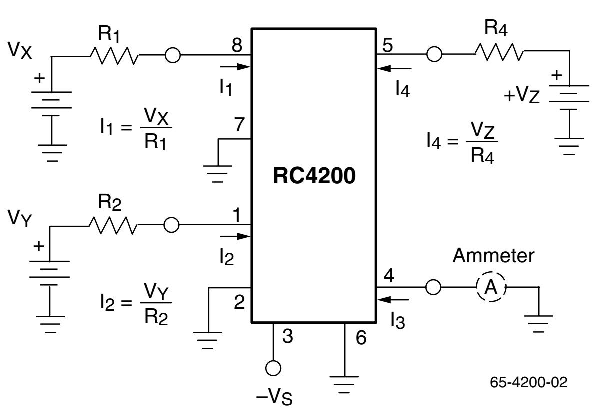


Figure 1. Current Multiplier/Divider

Dynamic Range and Stability

The precision dynamic range for the RC4200 is from +50 µA to +250 µA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50 µA, filter circuits ($R_S C_S$) are added to each input (see Figure 2).

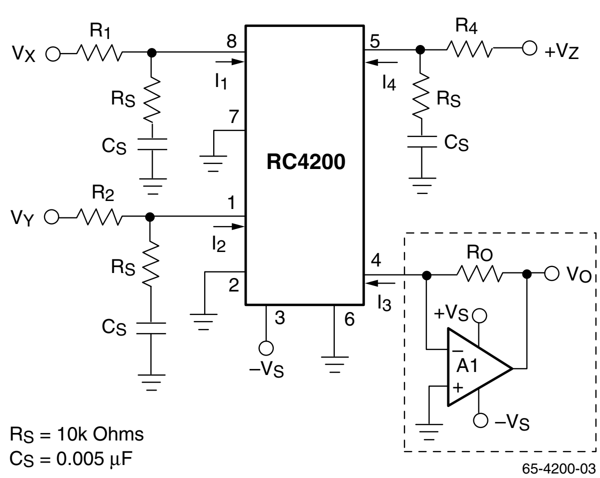


Figure 2. Current Multiplier/Divider with Filters

Amplifier A1 is used to convert the I_3 current to an output voltage.

Multiplier: Vz = constant ≠ 0
Divider: Vy = constant ≠ 0

Voltage Multiplier/Divider

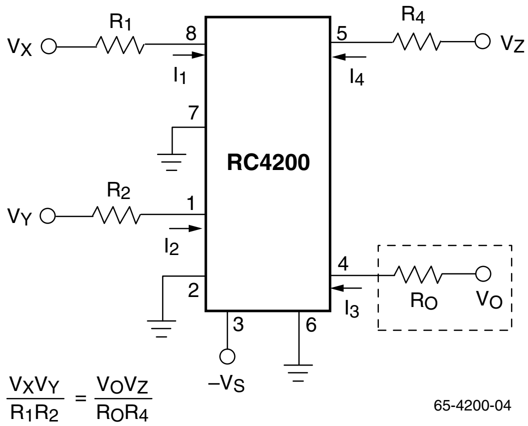


Figure 3. Voltage Multiplier/Divider

Solving for $V_0 = \frac{V_XV_Y}{V_Z}\frac{R_0R_4}{R_1R_2}$

For a multiplier circuit $V_Z = V_R = \text{constant}$

Therefore: $V_0 = V_XV_YK$ where $K = \frac{R_0R_4}{V_RR_1R_2}$

For a divider circuit $V_Y = V_R = \text{constant}$

Therefore: $V_0 = \frac{V_X}{V_Z}K$ where $K = \frac{V_RR_0R_4}{R_1R_2}$

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The R_SC_S filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50 µA min. and 250 µA max.

Extended Range Multiplier

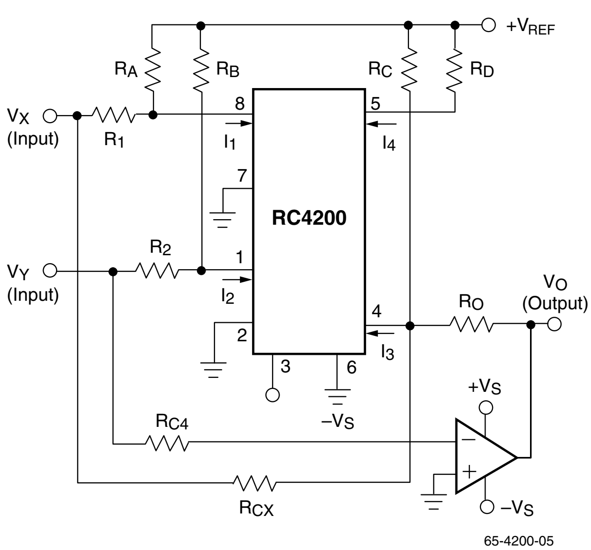


Figure 4. Extended Range Multiplier

Resistors R_a and R_b extend the range of the V_X and V_Y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_X(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\ \mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\ \mu A,$$

$$\text{also } I_2(\text{min.}) = \frac{V_Y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\ \mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_Y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\ \mu A.$$

Resistor R_C supplies bias current for I_3 which allows the output to go negative.

Resistors R_{CX} and R_{CY} permit equation (6) to balance, ie.:

$$\left(\frac{V_X}{R_1} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_Y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_C} + \frac{V_X}{R_{CX}} + \frac{V_Y}{R_{CY}}\right)\left(\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_YV_X}{R_1R_2} + \frac{V_XV_{REF}}{R_1R_b} + \frac{V_YV_{REF}}{R_2R_a} + \frac{V_{REF}}{R_aR_b} =$$

$$\frac{V_0V_{REF}}{R_0R_d} + \frac{V_XV_{REF}}{R_{cx}R_d} + \frac{V_YV_{REF}}{R_{CY}R_d} + \frac{V_{REF}}{R_cR_d}^2$$

Cross-Product Cancellation

Cross-products are a result of ths V_XV_R and V_YV_R terms. To the extend that $R_1R_b = R_{CX}R_D$, and $R_2R_a = R_{CY}R_d$ cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that $R_aR_b = R_0R_d$, and the result is:

$$\frac{V_YV_X}{R_1R_2} = \frac{V_0V_{REF}}{R_0R_d} \text{ or } V_0 = V_XV_YK$$

$$\text{where } K = \frac{R_0R_d}{V_{REF}R_1R_2}$$

Resistor Values

Inputs:

$$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$$

$$\Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$$

$$V_Y(\text{min.}) \le V_Y \le V_Y(\text{max.})$$

$$\Delta V_Y = V_Y(\text{max.}) = V_Y(\text{min.})$$

$$V_{REF} = \text{Constant } (+7V \text{ to } +18V)$$

$$K = \frac{V_0}{V_XV_Y}(\text{Design Requirements})$$

$$R_1 = \frac{\Delta V_X}{200\mu A}, R_2 = \frac{\Delta V_Y}{200\mu A}, R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(max.)}$$

$$R_b = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_Y - 200\mu A\ V_Y(max.)}$$

$$R_c = \frac{R_a R_b}{R_d}, R_{CX} = \frac{R_1 R_b}{R_d}, R_{cy} = \frac{R_2 R_a}{R_d}$$

$$R_0 = \frac{\Delta V_X \Delta V_Y K}{160\mu A}$$

Multiplying Circuit Offset Adjust

$10K \le R_5 = R_9 = R_{16} \le 50K$

$R_7 = R_{11} = R_{14}, = 100\Omega$

$R_6 = R_{10} = 100\Omega\ (V_S/0.05)$

$R_{15} = 100\Omega\ (V_S/0.10)$

$R_8 = R_1 \,||\, R_a$

$R_{12} = R_2 \,||\, R_b$

$R_{13} = R_0 \,||\, R_C \,||\, R_{CX} \,||\, R_{CY}$

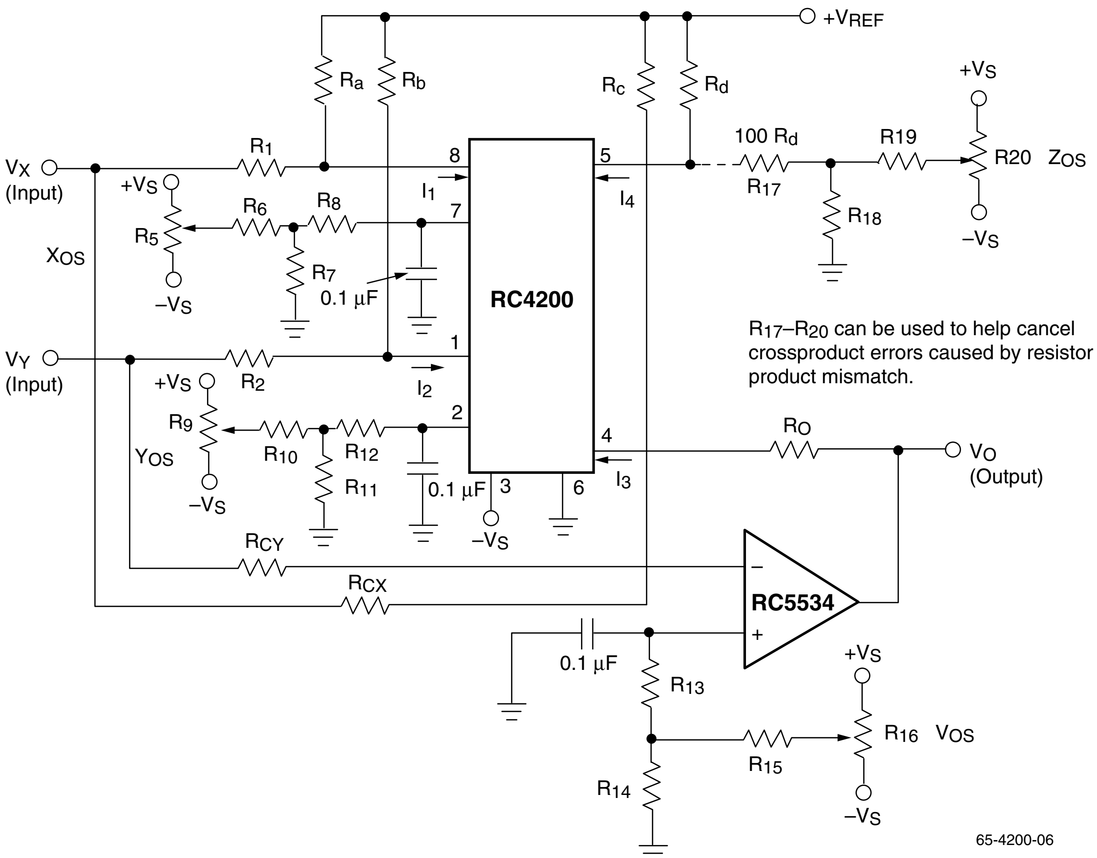


Figure 5. Multiplying Circuit Offset Adjust

Procedure

1. Set all trimmer pots to 0V on the wiper.
2. Connect V_X input to ground. Put in a full scale square wave on V_Y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).
3. Connect V_Y input to ground. Put in a full scale square wave on V_X input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).
4. Connect V_X and V_Y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Extended Range Divider

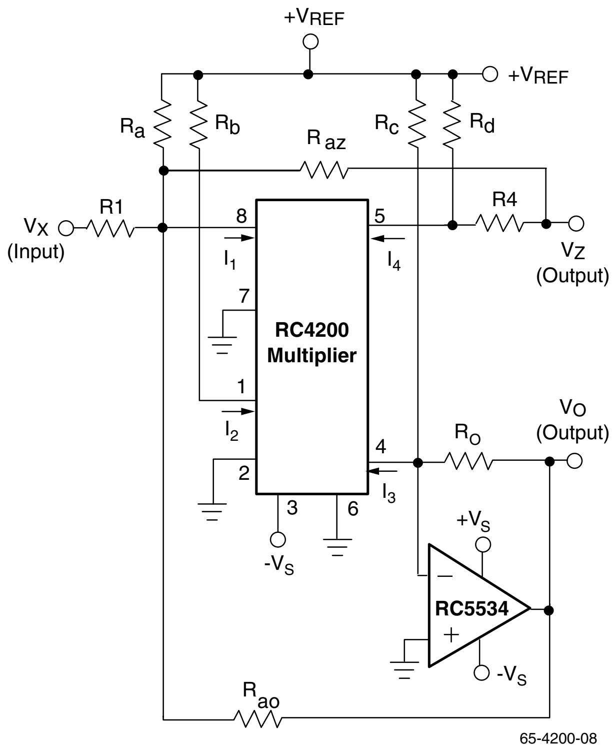


Figure 6. Extended Range Divider

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.

$$\left(\frac{V_X}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_Z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_C}\right)\left(\frac{V_Z}{R_4}+\frac{V_{REF}}{R_D}\right)$$

$$\frac{V_XV_{REF}}{R_1R_b}+\frac{V_0V_{REF}}{R_{ao}R_b}+\frac{V_ZV_{REF}}{R_{az}R_b}+\frac{V_{REF}^2}{R_aR_b}=$$

$$\frac{V_0V_Z}{R_0R_4}+\frac{V_0V_{REF}}{R_0R_d}+\frac{V_ZV_{REF}}{R_4R_c}+\frac{V_{REF}^2}{R_cR_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_XV_{REF}}{R_1R_b}=\frac{V_0V_Z}{R_0R_4} \quad \text{or} \quad V_0=\frac{V_X}{V_ZK}$$

where $K=\dfrac{V_{REF}R_0R_4}{R_1R_b}$

Notice that it is necessary to match the above resistor cross-products to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V. untrimmable output offset voltage.

Resistor Values

Inputs:

$V_X(\text{min.}) \le V_X \le V_X(\text{max.})$

$\Delta V_X = V_X(\text{max.}) = V_X(\text{min.})$

$V_Z(\text{min.}) \le V_Z \le V_Z(\text{max.})$

$\Delta V_Z = V_Z(\text{max.}) = V_Z(\text{min.})$

V_{REF} = Constant (+7V to +18V)

Outputs:

$V_0(\text{min.}) \le V_0 \le V_0(\text{max.})$

$\Delta V_0 = V_0(\text{max.}) = V_0(\text{min.})$

$$K = \frac{V_0V_Z}{V_X}\text{(Design Requirement)}$$

$$R_0 = \frac{\Delta V_0}{750\mu A},\ R_b = \frac{\Delta V_{REF}}{250\mu A},\ R_4 = \frac{\Delta V_Z}{200\mu A}$$

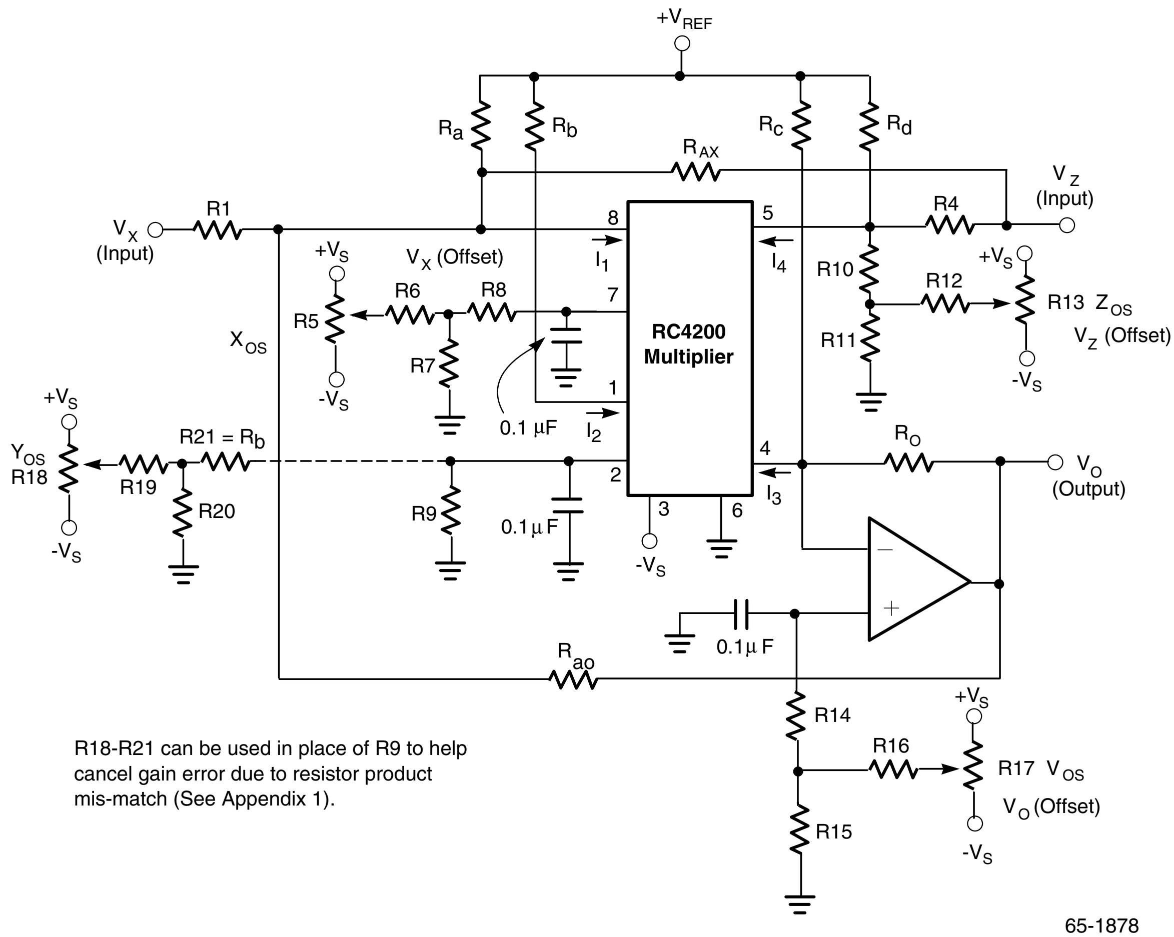
$$R_c = \frac{\Delta V_0V_{REF}}{750\mu A\Delta V_0 - 700\mu A\ V_0(\text{max.})}$$

$$R_d = \frac{\Delta V_XV_{REF}}{250\mu A\Delta V_Z - 200\mu A\ V_Z(\text{max.})}$$

$$R_a = \frac{R_cR_d}{R_b},\ R_{az} = \frac{R_cR_4}{R_b},\ R_{ao} = \frac{R_0R_d}{R_b}$$

$$R_1 = \frac{\Delta V_0\Delta V_Z}{600\mu AK}$$

Divider Circuit with Offset Adjustment



General

$10K \le R_5 = R_{13} = R_{17} \le 50K$

$R_7 + R_8 \approx R_1 \,||\, R_a \,||\, R_{az} \,||\, R_{ao}$

$R_6 \approx R_7 (V_S/0.05)$

$R_9 = R_b$

$R_{10} \approx 100 \times R_4$

$R_{11} = 20K$

$R_{12} = 100K$

$R_{14} + R_{15} \approx R_0 \,||\, R_c$

$R_{16} \approx R_{15} (V_S/0.10)$

Example: Two-Quad Divider

$V_0 = K(V_X/V_Z)$, $K = k$, $V_{REF} = +V_S = +15V$

$-10 \le V_X \le +10$, therefore $\Delta V_X = 20$

$0 \le V_Z \le +10$, therefore $\Delta V_Z = 20$

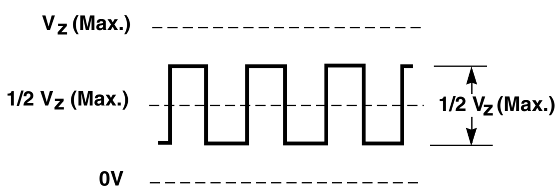
$-10 \le V_0 \le +10$, therefore $\Delta V_0 = 20$

$R_0 = 26.7K$	$R_1 = 333K$
$R_b = 60K$	$R_5, R_{13}, R_{17} = 10K$
$R_4 = 50K$	$R_7, R_{15} = 1K$
$R_c = 37.5K$	$R_8, R_{11} = 20K$
$R_d = 300K$	$R_6, R_9, R_{16} = 300K$
$R_a = 187.5K$	$R_{10} = 4.7M$
$R_{az} = 31.25$	$R_{12} = 100K$
$R_{ao} = 133K$	

Figure 7. Divider Circuit with Offset Adjustment

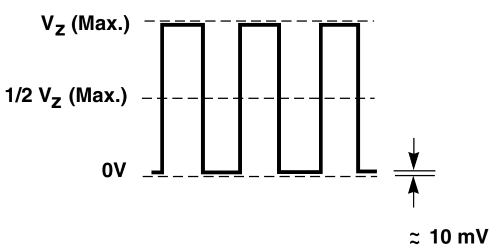
Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.
2. Connect V_X (input) to ground. Put a DC voltage of approximatey 1/2 V_Z (max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of 1/2 V_Z (max.) peak-to-peak superimposed on it. Adjust X_{OS} (R5) for zero feedthrough. (No AC at V_0)



3. Connect V_X (input) to V_Z (input) and put in the 1/2 V_Z(max.) DC with an AC of approximately 20 mV less than V_Z(max.).

   Adjust Z_{OS} (R_{13}) for zero feedthrough.



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4. Return V_X (Input) to ground and connect V_Z(max.) DC on V_Z(input). Adjust output V_{OS}(R_{17}) for V_O = $0V_O$
5. Connect V_X (input) to V_Z (input) and and in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_0 - K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue steps 4 and 5 until V_Z reduces to the lowest value desired.

Notice that as the input to VX and VZ gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit $V_0 = N\sqrt{V_X}$

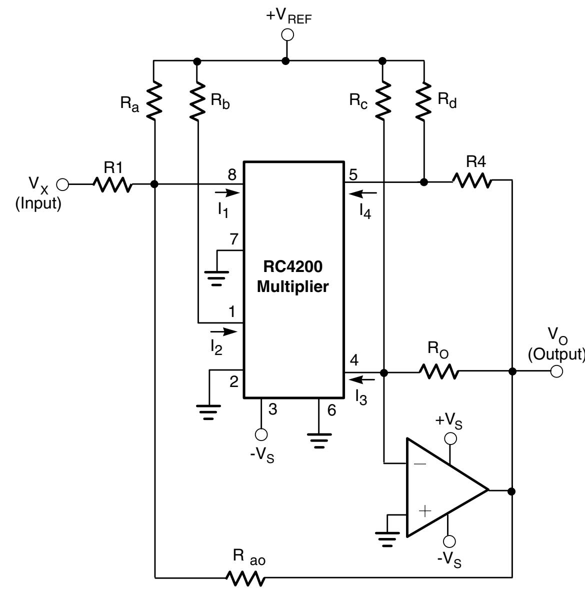

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Figure 8.

$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_0 V_{REF}}{R_{ao} R_b} = \frac{V_0^2}{R_0 R_4} + \frac{V_0 V_{REF}}{R_c R_4} + \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_0 R_d + R_{ao} R_b R_c R_4 = R_c R_d R_0 R_4$

Then $\frac{V_0^2}{R_0 R_4} = \frac{V_X V_{REF}}{R_1 R_b}$ or $V_0^2 = V_X K$ where $K = \frac{V_{REF} R_0 R_4}{R_1 R_b}$

and $V_0 = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X(\text{max.})$ and $V_0(\text{max.}) = N\sqrt{V_X(\text{max.})}$

$$N = \frac{V_0}{\sqrt{V_X}} \text{(Design Requirements)}$$

$$R_1 = \frac{V_0(\text{max.})^2}{74\mu A\ N^2}$$

$$R_a = R_d = \frac{V_{REF}}{50\mu A}$$

$$R_b = R_c = \frac{V_{REF}}{150\mu A}$$

$$R_4 = \frac{V_0(\text{max.})}{50\mu A}$$

$$R_{ao} = \frac{V_0(\text{max.})}{125\mu A}$$

$$R_0 = \frac{V_0(\text{max.})}{225\mu A}$$

Square Root Circuit Offset Adjust

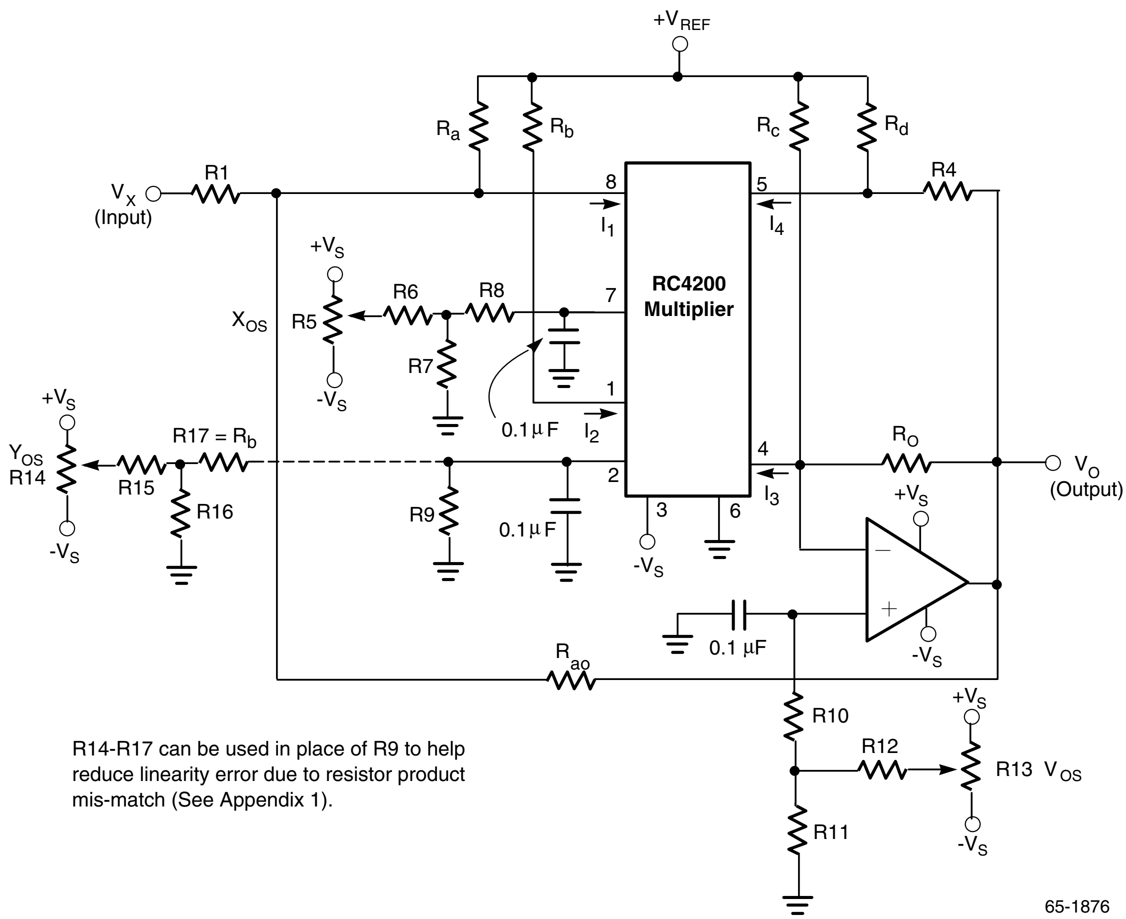


Figure 9. Square Root Circuit Offset Adjust

$10K \le R_5 = R_{13} \le 50K$

$R_7 = 100\Omega$

$$R_6 = R_7 \frac{V_S}{0.05}$$

$R_8 = R_1 \parallel R_a \parallel R_{ao}$

$R_9 = R_b$

$R_{10} = R_0 \parallel R_C$

$R_{11} = 100\Omega$

$$R_{12} = R_{11} \frac{V_S}{0.1}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_X(max.) squarewave on V_X input. Adjust X_{OS}(R5) for proper peak-to-peak amplitude on V_0 output. (Scaling adjust)
3. Connect V_X input to ground. Adjust V_{OS}(R13) for 0V on V_0 output.

Squaring Circuits $V_0 = K V_X^2$

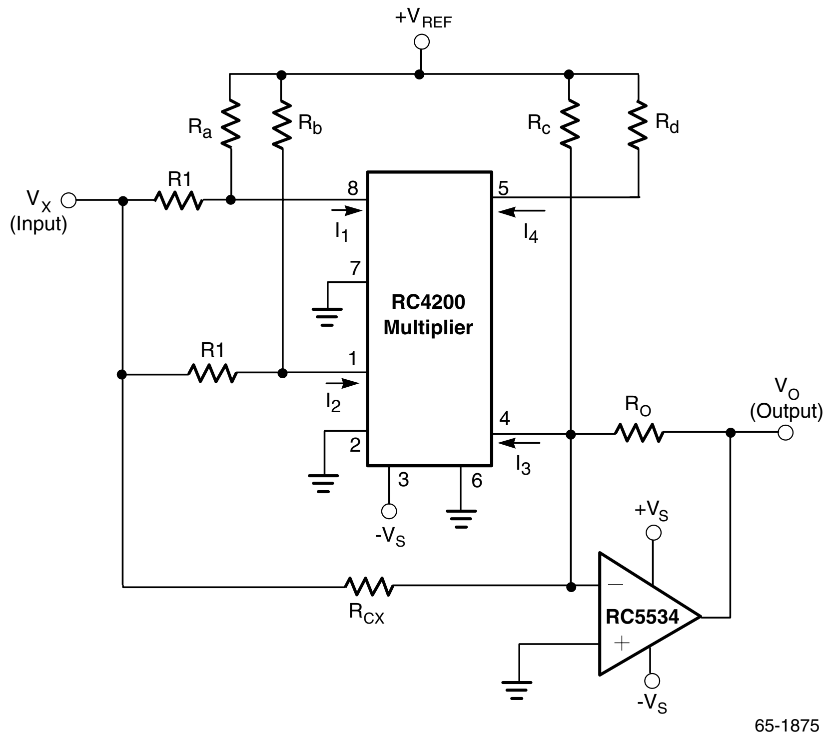


Figure 10. Squaring Circuit

$$\frac{V_X^2}{R_1^2} + \frac{2V_X V_{REF}}{R_1 R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0 V_{REF}}{R_0 R_d} + \frac{V_{REF}^2}{R_c R_d} + \frac{V_X V_{REF}}{R_c R_d}$$

if $R_a^2 = R_c R_d$ and $R_1 R_a = 2R_{CX} R_D$

then $\frac{V_0 V_{REF}}{R_0 R_d} = \frac{V_X^2}{R_1^2}$ or $V_0 = KV_X^2$ where $K = \frac{R_0 R_d}{V_{REF} R_1^2}$

$V_X(\text{min.}) \le V_X \le V_X(\text{max.}) \quad \Delta V_X = V_X(\text{max.}) - V_X(\text{min.})$

$K = \frac{V_0}{V_X^2}$ (Design Requirement)

$$R_1 = \frac{\Delta V_X}{200\mu A}$$

$$R_a = \frac{\Delta V_X V_{REF}}{250\mu A \Delta V_X - 200\mu A\ V_X(\text{max.})}$$

$$R_d = \frac{V_{REF}}{250\mu A}$$

$$R_c = \frac{R_a^2}{R_d}$$

$$R_{cx} = \frac{R_1 R_a}{2R_d}$$

$$R_0 = \frac{\Delta V_X^2 K}{160\mu A}$$

Squaring Circuits Offset Adjust

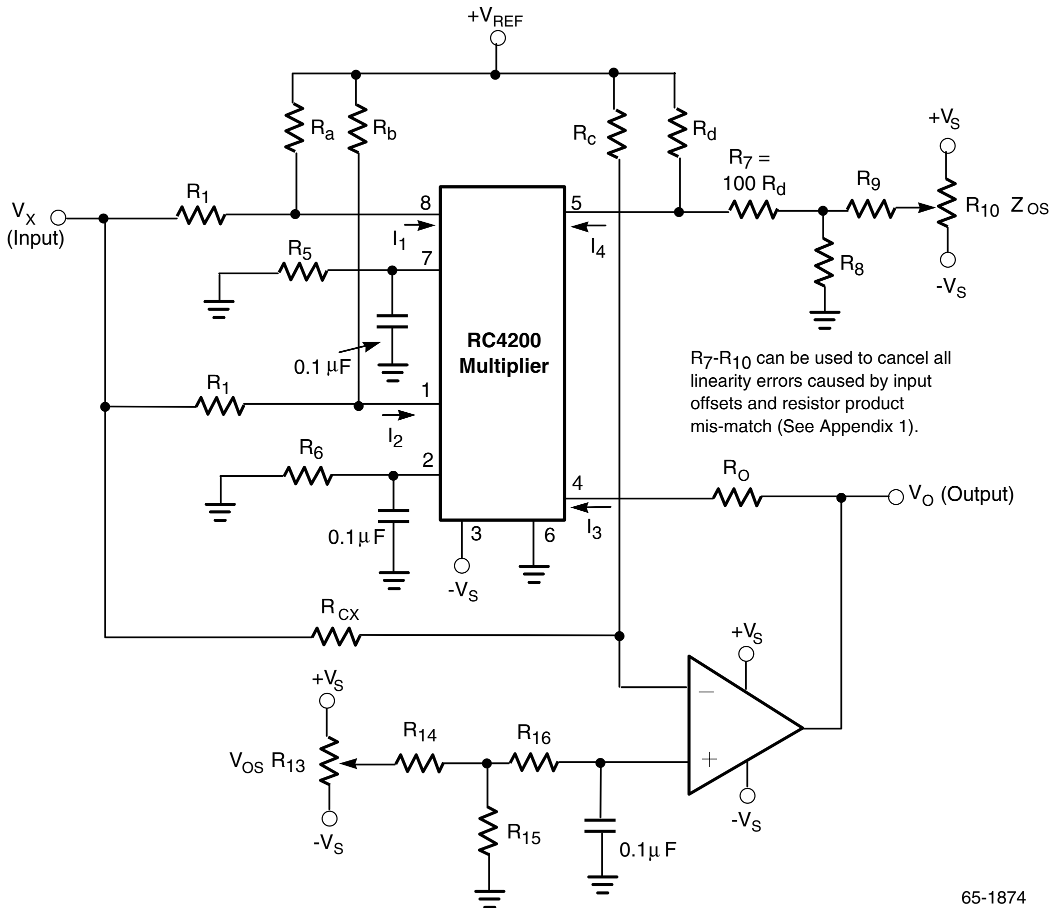


Figure 11. Squaring Circuit Offset Adjust

$$10K \le R_{10} = R_{11} \le 50K$$

$$R_8,\ R_{15} = 100\Omega$$

$$R_9,\ R_{14} = 100\Omega\frac{V_S}{0.1}$$

$$R_5,\ R_6 = R_1 \parallel R_a$$

$$R_{16} = R_0 \parallel R_c \parallel R_a$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale ($\pm V_X$) squarewave on V_X input. Adjust Z_{OS}(R10) for uniform output.
3. Connect V_X input to ground. Adjust $V_{OS}(R_{11})$ for 0V on V_0 outputs.

Appendix 1—System Errors

There are four types of accuracy errors which affect overall system performance. They are:

- Nonimearity—Incremental deviation from absolute accuracy. See Note 1.
- Scaling Error—Linear deviation from absolute accuracy.
- Output Offset—Constant deviation from absolute accuracy.
- Feedthrough.—Cross-product errors caused by input offsets and external circuit limitations. See Note 2.

This nonlinearity error in the transfer function of the RC4200 is ±0.1% maximum (±0.03 maximum for the RC4200A). That is,

$$I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\%\ \text{F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the RC4200 and can be as high as ±3.0% (±2.0% for RC4200A).

$$V_0 = \frac{V_X V_Y}{V_Z}\,\frac{R_0 R_4}{R_1 R_2} \pm 3.0\%\ \text{F.S.}^{(3)(4)}$$

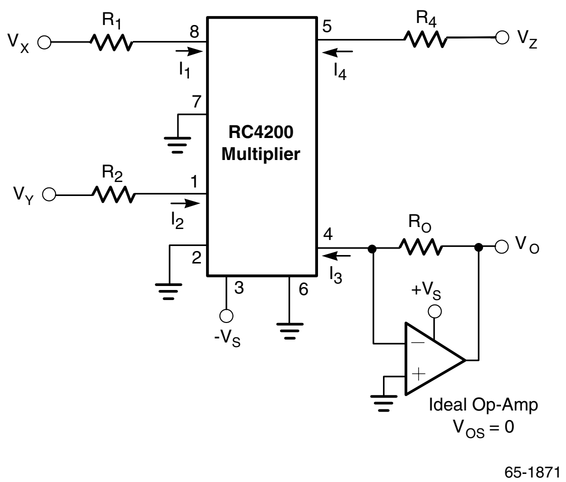


Figure 12.

Notes:

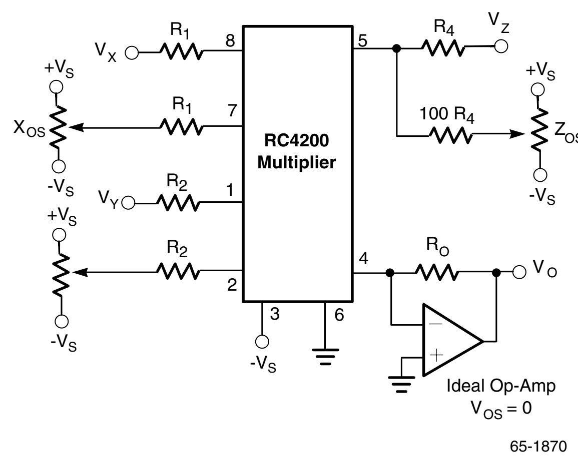
1. The input circuits tend to become unstable at I_1, I_2, I_4 < 50 µA and linearity decreases when I_1, I_2, I_4 > 250 µA (e.g., @ $I_1 = I_2 =$ 500µA nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (refer to Figure 12.)
3. Not including resistor tolerance or output offset on the operational amplifier.
4. For 50 µA ≤ I_1, I_2, I_4 ≤ 250 µA.

Errors Caused by Input Offsets

$$V_0 = \frac{R_0 R_4}{R_0 R_4}\left[\frac{V_X V_Y}{V_Z} \pm \frac{1}{V_Z}\; V_Y V_{OSX} \pm V_X V_{OSY} \pm V_0 V_{OSZ} \pm V_{OSX} V_{OSY}\right]$$

V_Y Feedthrough ($V_Y V_{OSX}$)
V_X Feedthrough ($V_X V_{OSY}$)
Scaling Error ($V_0 V_{OSZ}$)
Output Offset Error ($V_{OSX} V_{OSY}$)

System errors can be greatly reduced by externally trimming the input offset voltages of the RC4200. (±3.0% F.S. for RC4200 and ±0.1% for RC4200A.)



If $X_{OS} = X_{OSX}$, $Y_{OS} = Y_{OSY}$, $Z_{OS} = -V_{OSZ}$,

$$\text{then } V_O \frac{V_X V_Y}{V_Z}\,\frac{R_0 R_4}{R_1 R_2} \pm 0.3\%\ \text{F.S.}^{(3)}$$

Figure 13. RC4200 with Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

Multiplier

An error in resistor product matching will cause an equivalent feedthrough or output offset error. See Figure 6.

$R_1 R_b = R_{CX} R_d \pm\alpha$, V_X feedthrough ($V_Y = 0$) = $I\alpha V_X$

$R_2 R_a = R_{CY} R_d \pm\beta$, V_Y feedthrough ($V_X = 0$) = $\pm\beta V_Y$

$R_a R_b = R_C R_d \pm\gamma$, V_0 offset ($V_X = V_Y = 0$) = $\pm\gamma V_{REF}$*

Note:

* Output offset errors can always be trimmed out with the output op amp offset adjust, VOS (R16).

Reducing Mismatch Errors

You need not use 0.01% resistors to reduce resistor product mismatch errors. Here are a couple of ways to obtain maximum accuracy out of the extended range multiplier (see Figure 4) using 1% resistors.

Method 1

V_X feedthrough, for example, occurs when $V_Y = 0$ and $V_{OSY} \neq 0$. This V_X feedthrough will equal $\pm V_X V_{OSY}$. Also, if $V_{OSZ} \neq 0$, there is a V_X feedthrough equal to $V_X V_{OSZ}$. A resistor-product error of α will cause a V_X feedthrough of $\pm\alpha V_X$. Likewise, V_Y feedthrough errors are: $\pm V_Y V_{OSX}$, $\pm V_Y V_{OSZ}$ and $\pm\beta V_Y$

Total feedthrough:
$\pm V_X V_{OSY} \pm V_Y V_{OSX} \pm\alpha V_X \pm\beta V_Y \pm(V_X + V_Y)\, V_{OSZ}$

By carefully abusing $X_{OS}(R_5)$, $Y_{OS}(R_9)$ and $Z_{OS}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual of set will probably remain which can be trimmed outwith $V_{OS}(R_{16})$ at the output of amp.

Method 2

Notice that the ratios of R_1R_b:$R_{CX}R_d$ and R_2R_a:$R_{CY}R_d$ are both dependent of R_d also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_X and V_Y then $R_1 = R_2$, $R_{CX} = R_{CY}$ and $R_a = R_b$. (Note: it is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{OS}(R_{20})$ on pin 5.

This technique causes: a slight gain error which can be compensated with the R_0 value, and an output of offset error that can be trimmed with $V_{OS}(R_{16})$ on the output op amp.

Extended Range Divider

The only cross-product error of interest is the V_Z feedthrough ($V_X = 0$ and $V_{OSX} \neq 0$) which is easily adjusted with $X_{OS}(R_5)$. See Figure 6.

Resistor product mismatch will cause scaling errors (gain) that could be a problem for very low values of V_Z. Adjustments to $Y_{OS}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Cross product errors will effect incremental accuracy that can be corrected $Y_{OS}(R_{14})$ or $Z_{OS}(R_{10})$. See Figure 9 and Figure 11.

Appendix 2—Applications

Design Considerations for RMS-to-DC Circuits

Average Value

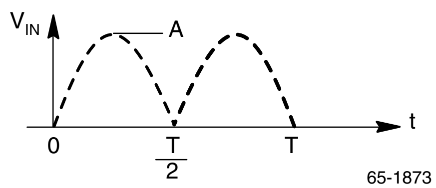
Consider $V_{in} = A\sin\omega\tau$. By definition,

$$V_{AG} = \int_0^{\frac{T}{2}} V_{IN} dt$$

Where T = Period

$$\omega = 2\pi f$$

$$= \frac{2\pi}{T}$$



$$V_{AG} = \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\ dt$$

$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\ \omega t\ \right]_0^{\frac{T}{2}}$$

$$= \frac{2A}{2\pi}[-\cos(\pi) + \cos(0)]$$

Average Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again, consider $V_{IN} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{IN}]^2 dt}$$

V_{rms} for $A\sin\omega t dt$:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T A^2 \sin^2 \omega t\ dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{T}\int_0^T \left[\frac{1}{2} - \frac{1}{2}\cos 2\cos 2\ \omega t\right] dt}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2} - \frac{1}{4\omega}\sin 2\ \omega t\right]_0^T}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}\left[\frac{T}{2}\right]}$$

$$V_{rms} = \sqrt{\frac{A^2}{2}}$$

Therefore, the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Waves

Consider $V_{in} = |A \sin \omega t|$, a rectified wave. To solve, integrate of each half cycle.

$$\text{i.e. } \frac{1}{T}\int_0^T V_{in}^2\ dt =$$

$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2 \sin^2 \omega t\ dt + \int_{\frac{T}{2}}^{T} (-A\sin\omega t)^2 dt\right]$$

This is the same as $\frac{1}{1}\int_0^T A^2 \sin^2 \omega t\ dt$

so, $|A\sin\omega t|_{rms} = A\sin\omega t_{rms}$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonics; $A\sin\omega t$ does not. Therefore, non-ideal integrators may cause different errors for two approaches.

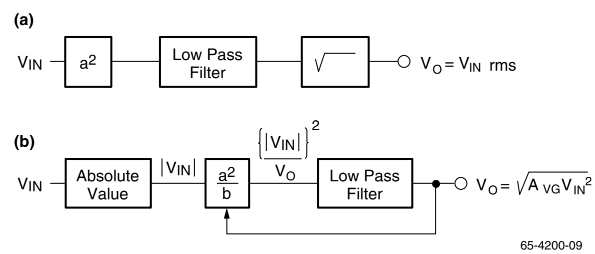


Figure 14.

$$Avg\left[\frac{V_{IN}^2}{V_0}\right] = V_0$$

$$\text{implies } V_0 = \sqrt{Avg(|V_{IN}^2|)}$$

$$V_0 = \sqrt{Avg\ \ V_{IN}^2}$$

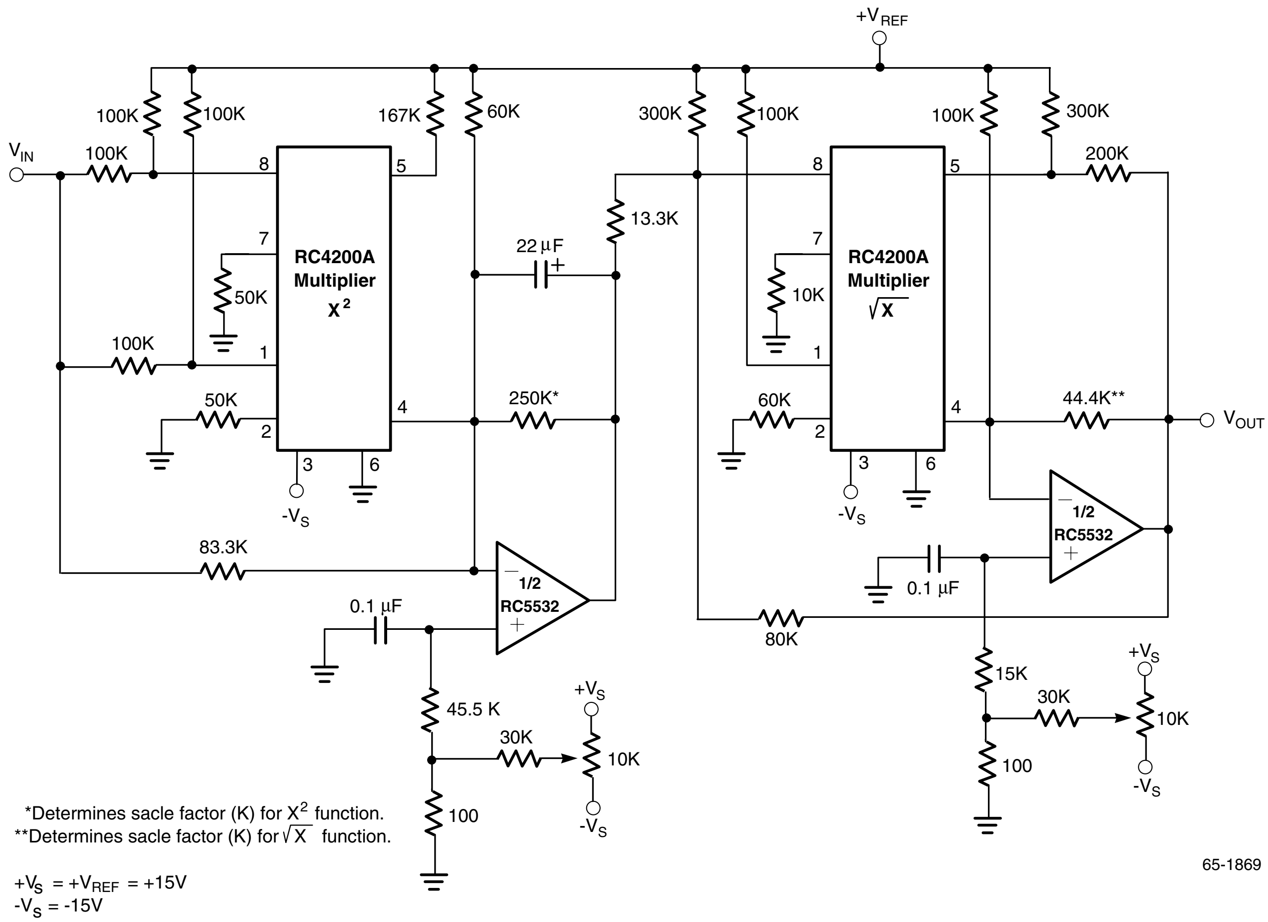


Figure 15. RMS to DC Converter $V_{OUT}=\sqrt{V_{IN}^2}$

Amplitude Modulator with A.G.C.

In many AC modulator applications, unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilizes to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 4) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_X V_Y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_Y (where V_Y is the carrier input) such that:

$$V_{REF} = V_H = \int(|V_Y|)$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_X) modulates the carrier (V_Y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of Asinωt (i.e., 2A/π) and scaled by a value of π/2 then:

V_H=A

and if: V_X = Modulating input (V_M)

and: V_Y Carrier input (Asinωt)

Then: $V_0 = K\, V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:

- Modulation voltage (V_M): $0 \le V_M \le V_X$(max.)
- Carrier (V_Y): V_Y = Asinωt
- Carrier amplitude fluctuation (ΔA):
  - A(min.) sint ≤ V_Y ≤ A(max.) sinΩωt
- Dynamic Range (N): A(max.)/A(min.),
- A(max.) = V_H(max.) and A(min.) = V_H(min.)

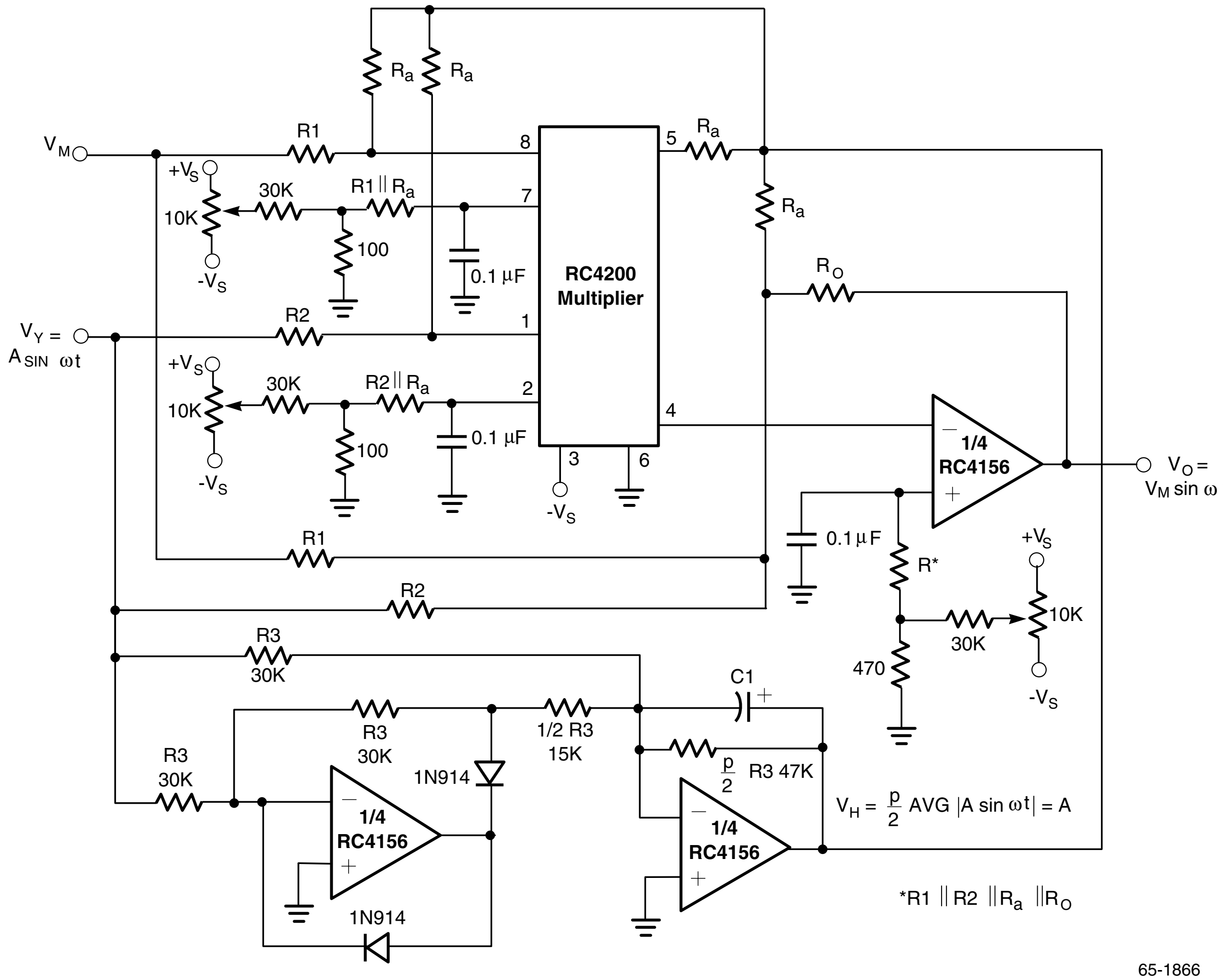


Figure 16. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(\text{max.}) = \frac{V_X(\text{max.})}{R_1} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_1(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A \; V_M(\text{min.}) = 0$$

$$I_2(\text{max.}) = \frac{A(\text{max.})}{R_2} + \frac{V_H(\text{max.})}{R_a} = 250\mu A$$

$$I_2(\text{min.}) = \frac{V_H(\text{min.})}{R_a} = 50\mu A$$

For a dynamic range of N, where

$$N = \frac{A(\text{max.})}{A(\text{min.})} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_X(\text{max.})}{(5-N)50\mu A}, \; R2\frac{A(\text{max.})}{(5-N)50\mu A},$$

$$R_a = \frac{A(\text{min.})}{50\mu A} \text{ and } R_O = K\frac{R_1R_2}{R_a},$$

Example 1

$V_Y = A\sin\omega t$ $2.5V \le A \le 10V$, therefore N = 4
$0V \le V_M \le 10V$, therefore $V_X(\text{max.}) = 10V$
K = 1, therefore $V_0 = V_M \sin\omega t$

$$R_1 = \frac{V_X(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

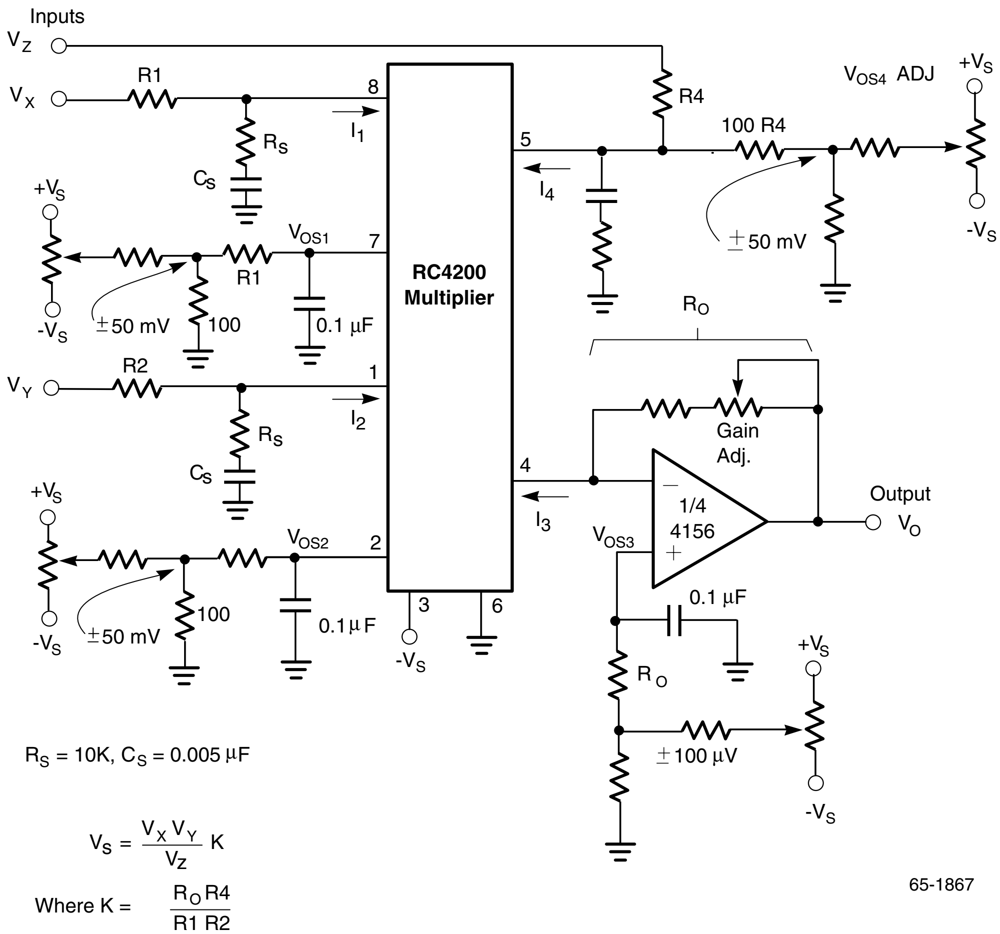
$$R_1 = \frac{A(\text{max.})}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(\text{min.})}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_O = K\frac{R_1R_2}{R_a} = 1\frac{200K \times 200K}{50K} = 800K$$

Example 2

$V_Y = A\sin\omega t$ $3 \le A \le 6$, therefore N = 2
$0V \le V_M \le 8V$, therefore $V_X(\text{max.}) = 8V$
K = 0.2, therefore $V_0 = 0.2\, V_M \sin wt$
so:
$R_1 = 53.3K$, $R_2 = 40K$
$R_a = 60K$ and $R_0 = 7.11K$



Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is sightly error is slightly less for lower input currents.

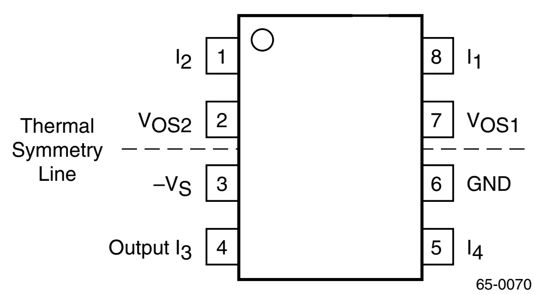
The circuit also has no standby current to add to the noise content, although the signal-to-noise ratio worsens at very low input currents (1-5 µA) due to the noise current of the input stages.

The $R_S C_S$ filter circuits are added to each input to improve the stability for input currents below 50 µA.

Caution!

The bandpass drops off significantly for lower currents (<50 µA) and non-symmetrical rise and fall times can cause second harmonic distortion.

Thermal Symmetry



The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that forces generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

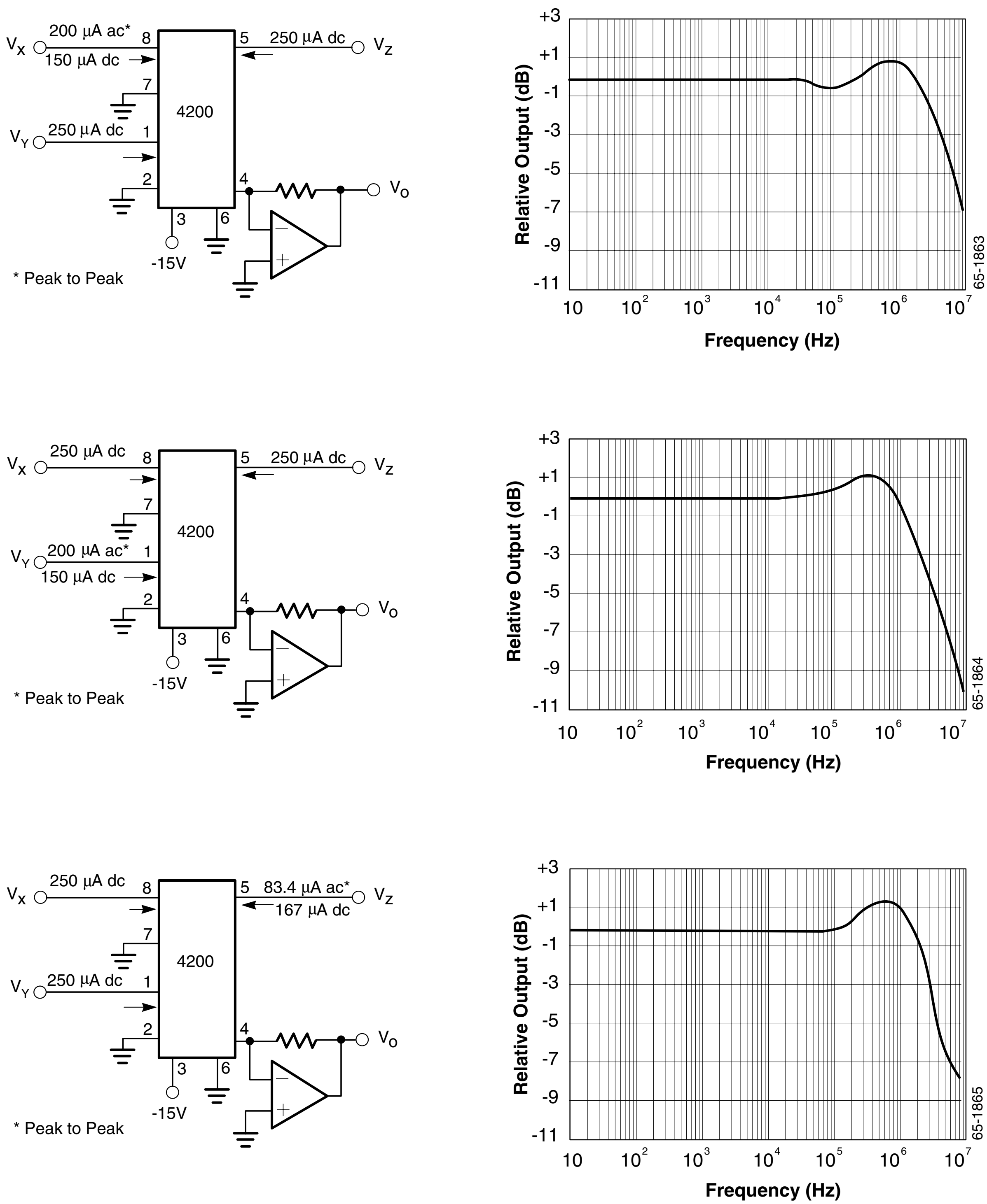


Figure 18. Outputs

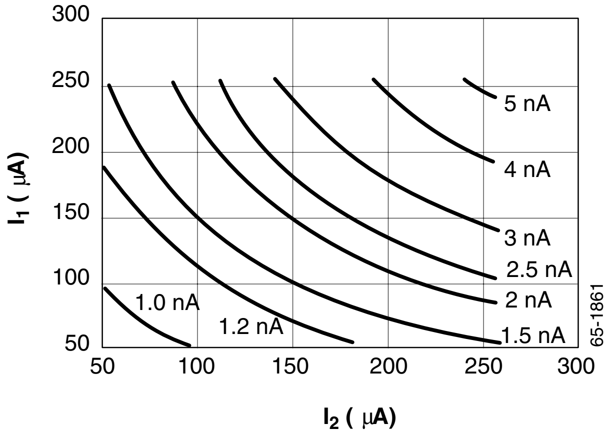


Figure 19a. Output Noise Current (I_3) vs. Input Currents (I_1, I_2) for I_4 = 250μA

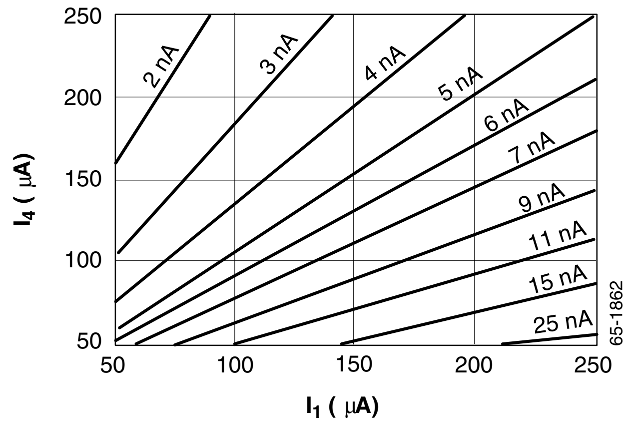


Figure 19b. Output Noise Current (I_3) vs. Input Currents (I_4, I_1) for I_2 = 250μA

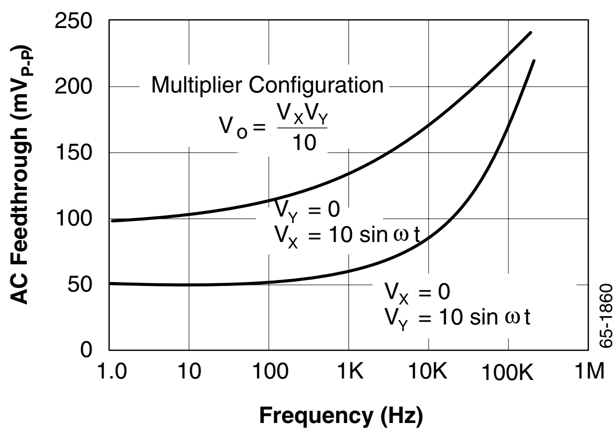


Figure 20. AC Feedthrough vs. Frequency

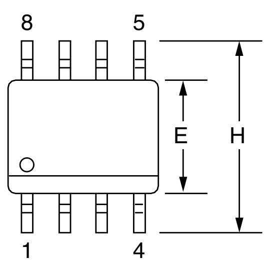
Mechanical Dimensions

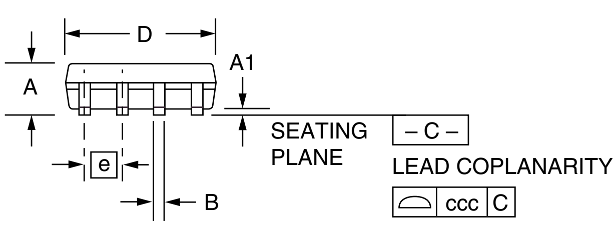
8-Lead SOIC Package

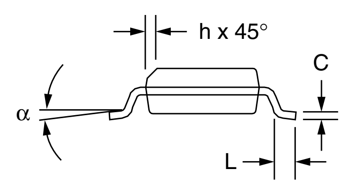
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







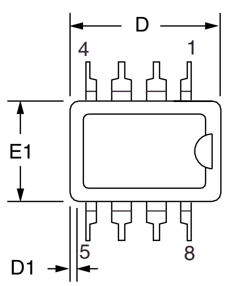
Mechanical Dimensions (continued)

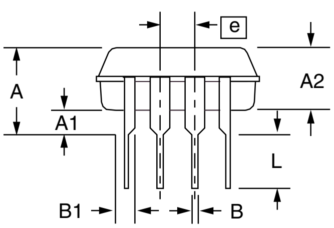
8-Lead Plastic DIP Package

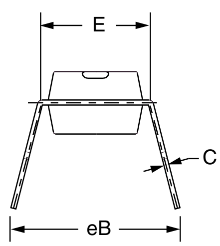
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	8-Lead Plastic DIP	0°C to +70°C
RC4200AN	8-Lead Plastic DIP	0°C to +70°C
RC4200M	8-Lead SOIC	0°C to +70°C
RC4200AM	8-Lead SOIC	0°C to +70°C

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Stock#DS30004841