FAIRCHILD

SEMICONDUCTOR™

April 1988
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74F521
8-Bit Identity Comparator

General Description

The 74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

■ Compares two 8-bit words in 6.5 ns typ
■ Expandable to any word length
■ 20-pin package

Ordering Code:

Order Number	Package Number	Package Description
74F521SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F521SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F521MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F521PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

IEEE/IEC

Connection Diagram
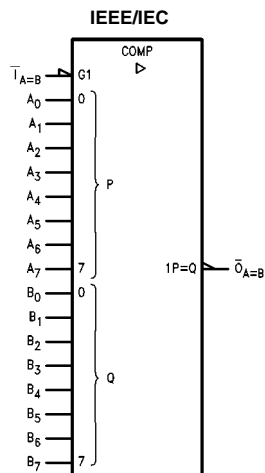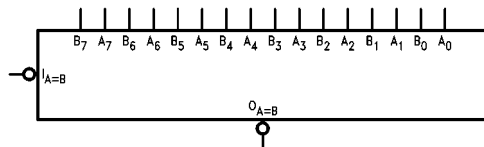
DS009545   www.fairchildsemi.com
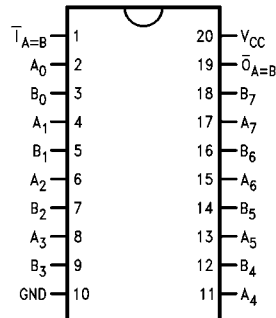
Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	Word A Inputs	1.0/1.0	20 μA/–0.6 mA
B_0–B_7	Word B Inputs	1.0/1.0	20 μA/–0.6 mA
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA
$\overline{O}_{A=B}$	Identity Output (Active LOW)	50/33.3	–1 mA/20 mA

Truth Table

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B (Note 1)	L
L	A ≠ B	H
H	A = B (Note 1)	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level

Note 1: $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram
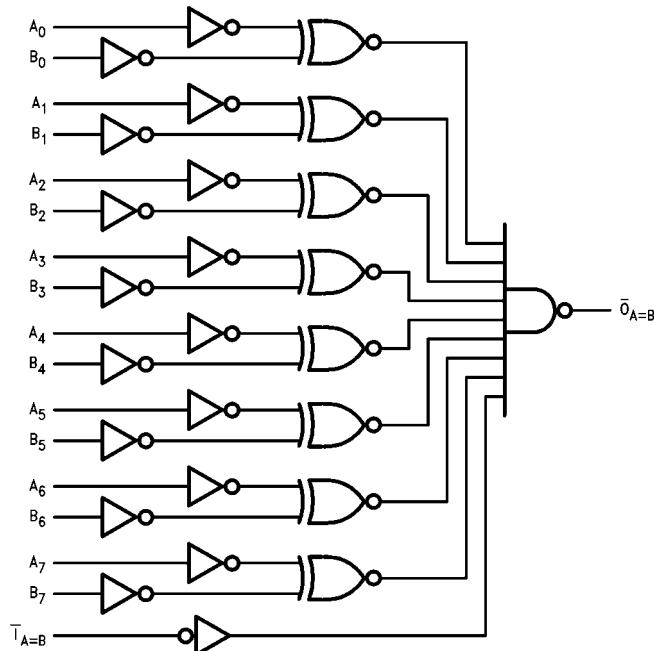
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V$_{CC}$ Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V$_{CC}$ = 0V)	
Standard Output	−0.5V to V$_{CC}$
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I$_{OL}$ (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V$_{CC}$	Conditions
V$_{IH}$	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V$_{IL}$	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V$_{CD}$	Input Clamp Diode Voltage				−1.2	V	Min	I$_{IN}$ = −18 mA
V$_{OH}$	Output HIGH	10% V$_{CC}$	2.5			V	Min	I$_{OH}$ = −1 mA
	Voltage	5% V$_{CC}$	2.7					I$_{OH}$ = −1 mA
V$_{OL}$	Output LOW	10% V$_{CC}$			0.5	V	Min	I$_{OL}$ = 20 mA
	Voltage							
I$_{IH}$	Input HIGH Current				5.0	µA	Max	V$_{IN}$ = 2.7V
I$_{BVI}$	Input HIGH Current Breakdown Test				7.0	µA	Max	V$_{IN}$ = 7.0V
I$_{CEX}$	Output HIGH Leakage Current				50	µA	Max	V$_{OUT}$ = V$_{CC}$
V$_{ID}$	Input Leakage Test		4.75			V	0.0	I$_{ID}$ = 1.9 µA All Other Pins Grounded
I$_{OD}$	Output Leakage Circuit Current				3.75	µA	0.0	V$_{IOD}$ = 150 mV All Other Pins Grounded
I$_{IL}$	Input LOW Current				−0.6	mA	Max	V$_{IN}$ = 0.5V
I$_{OS}$	Output Short-Circuit Current		−60		−150	mA	Max	V$_{OUT}$ = 0V
I$_{CCH}$	Power Supply Current			21	32	mA	Max	V$_O$ = HIGH

AC Electrical Characteristics

| Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = -55°C \text{ to } +125°C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0°C \text{ to } +70°C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	3.0	7.0	10.0	3.0	14.0	3.0	11.0	ns
t_{PHL}	A_n or B_n to $\overline{O}_{A=B}$	4.5	7.0	10.0	4.0	15.0	4.0	11.0	
t_{PLH}	Propagation Delay	3.0	5.0	6.5	3.0	8.5	3.0	7.5	ns
t_{PHL}	$\bar{I}_{A=B}$ to $\overline{O}_{A=B}$	3.5	6.5	9.0	3.5	13.5	3.5	10.0	

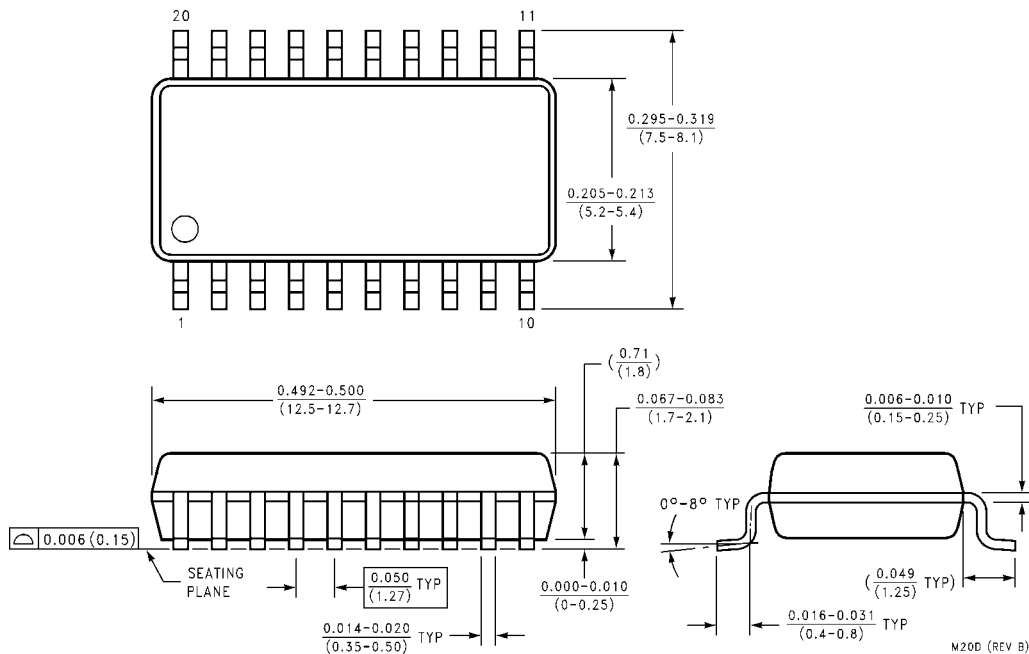## Applications

Ripple Expansion
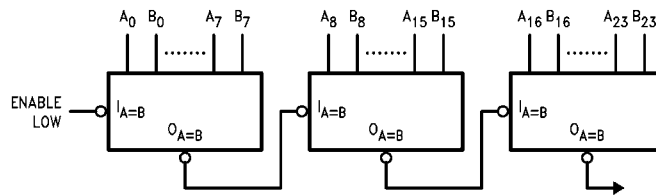
Parallel Expansion
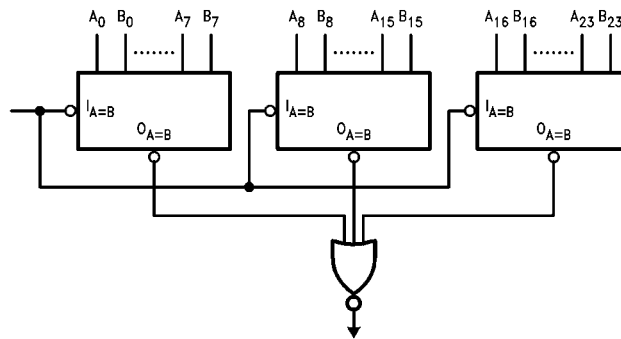
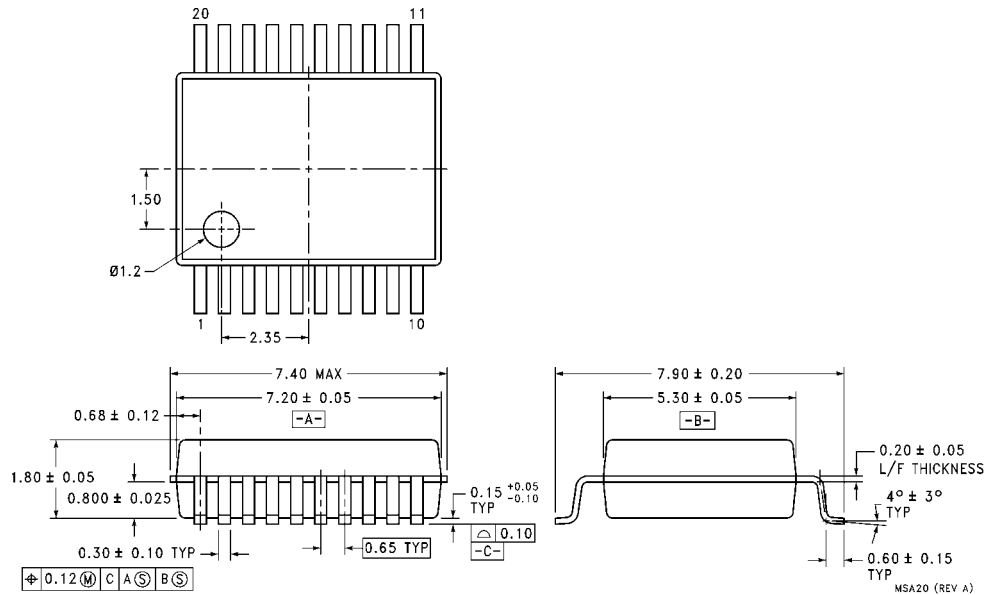# Physical Dimensions inches (millimeters) unless otherwise noted
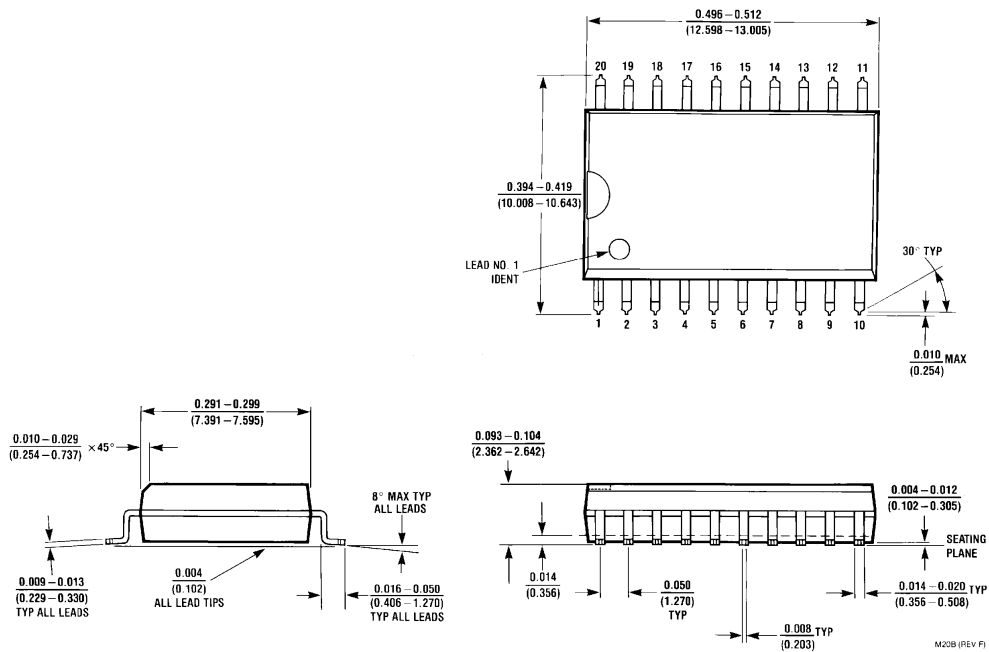
**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
Package Number M20B

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

20   11

1.50

Ø1.2

1   10

2.35

7.40 MAX

7.20 ± 0.05

-A-

0.68 ± 0.12

1.80 ± 0.05

0.800 ± 0.025

0.30 ± 0.10 TYP

0.15 +0.05 -0.10 TYP

0.65 TYP

-C-

△ 0.10

⊕ 0.12 Ⓜ C A Ⓢ B Ⓢ

7.90 ± 0.20

5.30 ± 0.05

-B-

0.20 ± 0.05 L/F THICKNESS

4° ± 3° TYP

0.60 ± 0.15 TYP

MSA20 (REV A)

20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
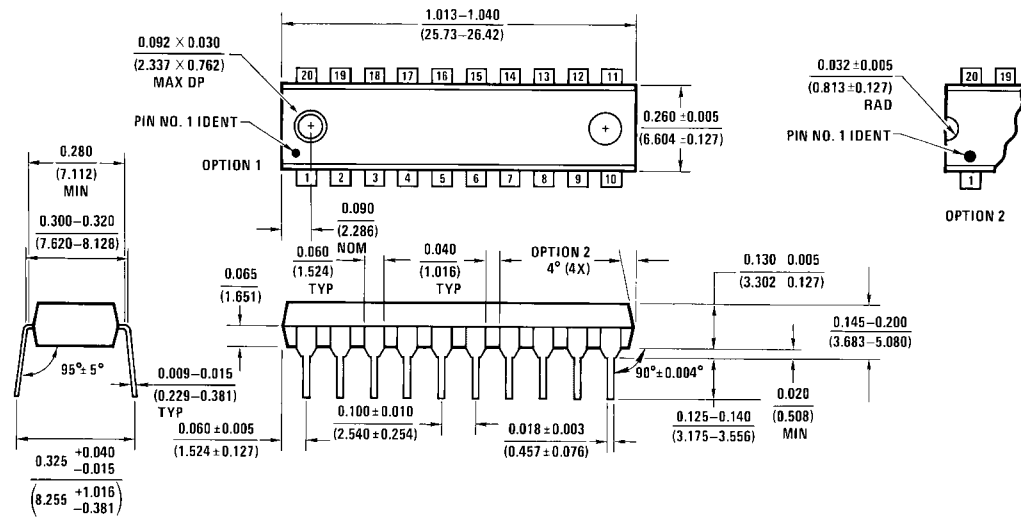
20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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