

128K x 8 Static RAM

Features

- **High speed**
— $t_{AA} = 12 \text{ ns}$
- **Low active power**
— 495 mW (max. 12 ns)
- **Low CMOS standby power**
— 55 mW (max.) 4 mW
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} options**

Functional Description

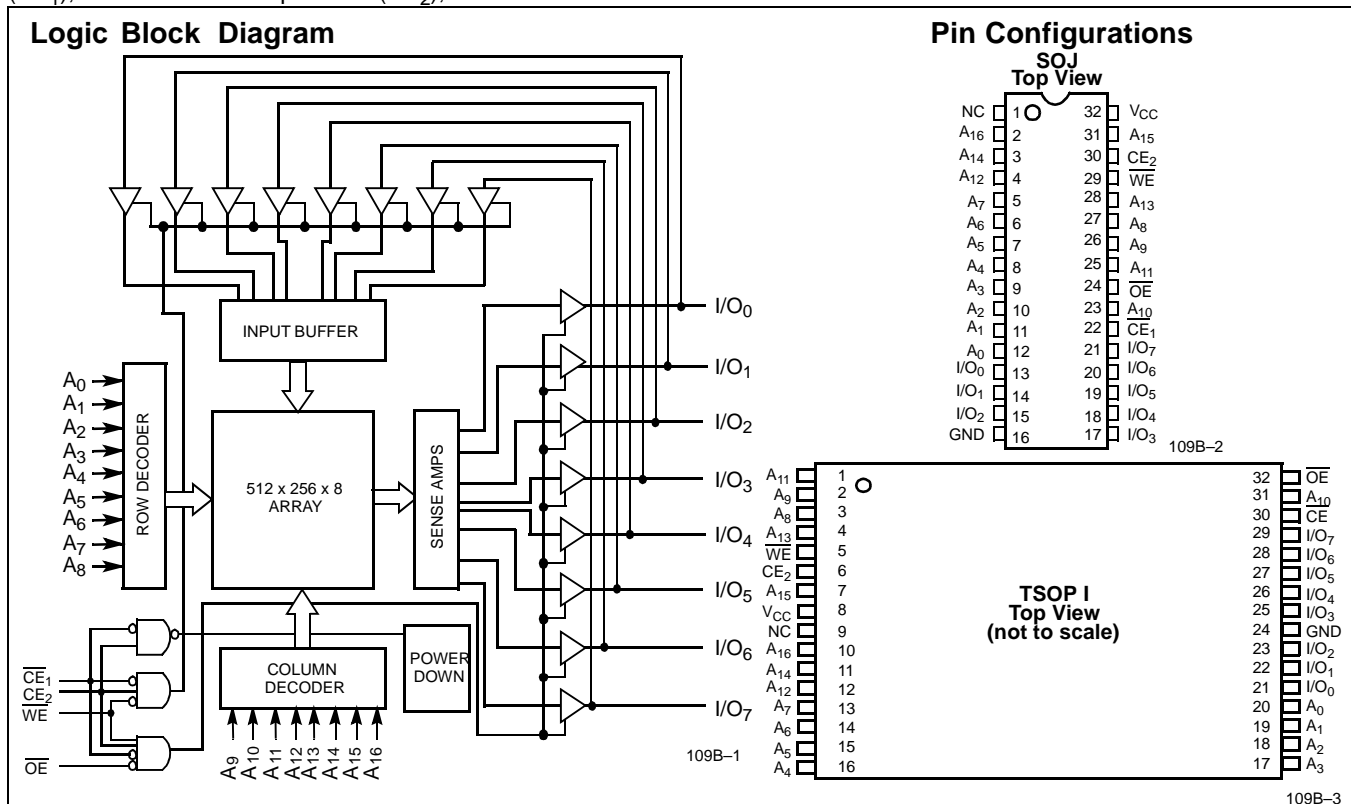
The CY7C109B / CY7C1009B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1), an active HIGH Chip Enable (\overline{CE}_2), an active LOW Out-

put Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable Two (\overline{CE}_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable Two (\overline{CE}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW).

The CY7C109B is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009B is available in a 300-mil-wide SOJ package. The CY7C1009B and CY7C109B are functionally equivalent in all other respects.



Selection Guide

| | 7C109B-12 7C1009B-12 | 7C109B-15 7C1009B-15 | 7C109B-20 7C1009B-20 | 7C109B-25 7C1009B-25 | 7C109B-35 7C1009B-35 |
|--|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Maximum Access Time (ns) | 12 | 15 | 20 | 25 | 35 |
| Maximum Operating Current (mA) | 90 | 80 | 75 | 70 | 60 |
| Maximum CMOS Standby Current (mA) | 10 | 10 | 10 | 10 | 10 |
| Maximum CMOS Standby Current (mA) Low Power Version | 2 | 2 | 2 | - | - |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V
 DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

| Range | Ambient Temperature ^[2] | V _{CC} |
|------------|------------------------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C109B-12 7C1009B-12 | | 7C109B-15 7C1009B-15 | | Unit |
|------------------|--|--|-------------------------|-----------------------|-------------------------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{Ix} | Input Load Current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output Short Circuit Current ^[3] | V _{CC} = Max., V _{OUT} = GND | | -300 | | -300 | mA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 90 | | 80 | mA |
| I _{SB1} | Automatic CE Power-Down Current —TTL Inputs | Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$ or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 45 | | 40 | mA |
| I _{SB2} | Automatic CE Power-Down Current —CMOS Inputs | Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | | 10 | | 10 | mA |
| | | | L | 2 | | 2 | mA |

Notes:

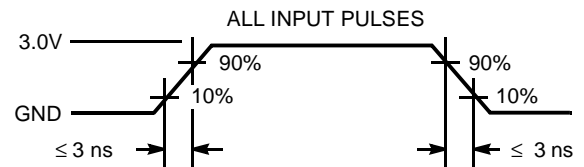
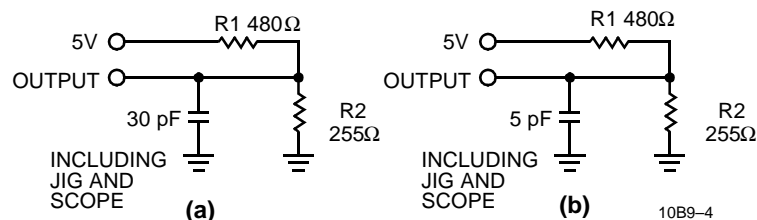
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | Test Conditions | 7C109B-20 7C1009B-20 | | 7C109B-25 7C1009B-25 | | 7C109B-35 7C1009B-35 | | Unit |
|-----------|---|---|-------------------------|----------------|-------------------------|----------------|-------------------------|----------------|---------------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$, $I_{OH} = -4.0 \text{ mA}$ | 2.4 | | 2.4 | | 2.4 | | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$, $I_{OL} = 8.0 \text{ mA}$ | | 0.4 | | 0.4 | | 0.4 | V |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | 2.2 | $V_{CC} + 0.3$ | V |
| V_{IL} | Input LOW Voltage ^[1] | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I_{IX} | Input Load Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{CC}$, Output Disabled | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I_{OS} | Output Short Circuit Current ^[3] | $V_{CC} = \text{Max.}$, $V_{OUT} = GND$ | | -300 | | -300 | | -300 | mA |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$ | | 75 | | 70 | | 60 | mA |
| I_{SB1} | Automatic CE Power-Down Current — TTL Inputs | Max. V_{CC} , $CE_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | | 30 | | 30 | | 25 | mA |
| I_{SB2} | Automatic CE Power-Down Current — CMOS Inputs | Max. V_{CC} , $CE_1 \geq V_{CC} - 0.3\text{V}$, or $CE_2 \leq 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$, or $V_{IN} \leq 0.3\text{V}$, $f = 0$ | | 10 | | 10 | | 10 | mA |
| | | | L | | 2 | | — | | — |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|-----------|--------------------|--|------|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0\text{V}$ | 9 | pF |
| C_{OUT} | Output Capacitance | | 8 | pF |

AC Test Loads and Waveforms


109B-5

Equivalent to: THÉVENIN EQUIVALENT

OUTPUT $\text{---} \frac{167\Omega}{\text{---}} \text{---} 1.73\text{V}$

Note:

4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

| Parameter | Description | 7C109B-12 7C1009B-12 | | 7C109B-15 7C1009B-15 | | Unit |
|----------------------------------|--|-------------------------|------|-------------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | |
| t_{RC} | Read Cycle Time | 12 | | 15 | | ns |
| t_{AA} | Address to Data Valid | | 12 | | 15 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | 3 | | ns |
| t_{ACE} | \overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid | | 12 | | 15 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 6 | | 7 | ns |
| t_{LZCE} | \overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[7] | 3 | | 3 | | ns |
| t_{HZCE} | \overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[6, 7] | | 6 | | 7 | ns |
| t_{PU} | \overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up | 0 | | 0 | | ns |
| t_{PD} | \overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down | | 12 | | 15 | ns |
| WRITE CYCLE^[8] | | | | | | |
| t_{WC} | Write Cycle Time ^[9] | 12 | | 15 | | ns |
| t_{SCE} | \overline{CE}_1 LOW to Write End, CE_2 HIGH to Write End | 10 | | 12 | | ns |
| t_{AW} | Address Set-Up to Write End | 10 | | 12 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 10 | | 12 | | ns |
| t_{SD} | Data Set-Up to Write End | 7 | | 8 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 3 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[6, 7] | | 6 | | 7 | ns |

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

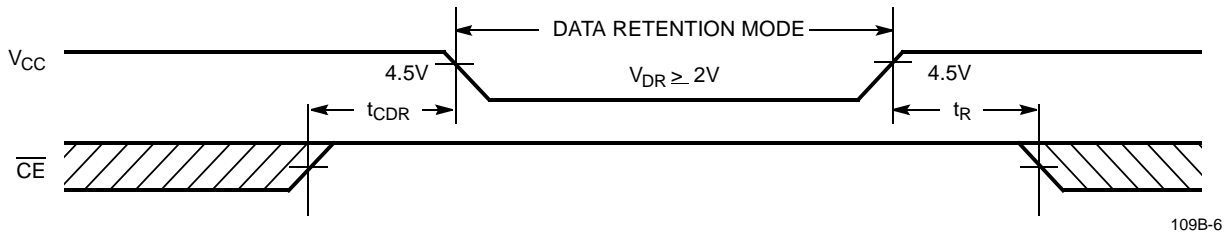
Switching Characteristics^[5] Over the Operating Range (continued)

| Parameter | Description | 7C109B-20 7C1009B-20 | | 7C109B-25 7C1009B-25 | | 7C109B-35 7C1009B-35 | | Unit |
|----------------------------------|---|-------------------------|------|-------------------------|------|-------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 20 | | 25 | | 35 | | ns |
| t _{AA} | Address to Data Valid | | 20 | | 25 | | 35 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 5 | | 5 | | ns |
| t _{ACE} | \overline{CE}_1 LOW to Data Valid, CE ₂ HIGH to Data Valid | | 20 | | 25 | | 35 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 8 | | 10 | | 15 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 8 | | 10 | | 15 | ns |
| t _{LZCE} | \overline{CE}_1 LOW to Low Z, CE ₂ HIGH to Low Z ^[7] | 3 | | 5 | | 5 | | ns |
| t _{HZCE} | \overline{CE}_1 HIGH to High Z, CE ₂ LOW to High Z ^[6, 7] | | 8 | | 10 | | 15 | ns |
| t _{PU} | \overline{CE}_1 LOW to Power-Up, CE ₂ HIGH to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE}_1 HIGH to Power-Down, CE ₂ LOW to Power-Down | | 20 | | 25 | | 35 | ns |
| WRITE CYCLE^[8] | | | | | | | | |
| t _{WC} | Write Cycle Time ^[9] | 20 | | 25 | | 35 | | ns |
| t _{SCE} | \overline{CE}_1 LOW to Write End, CE ₂ HIGH to Write End | 15 | | 20 | | 25 | | ns |
| t _{AW} | Address Set-Up to Write End | 15 | | 20 | | 25 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 12 | | 15 | | 20 | | ns |
| t _{SD} | Data Set-Up to Write End | 10 | | 15 | | 20 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 5 | | 5 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[6, 7] | | 8 | | 10 | | 15 | ns |

Data Retention Characteristics Over the Operating Range (Low Power version only)

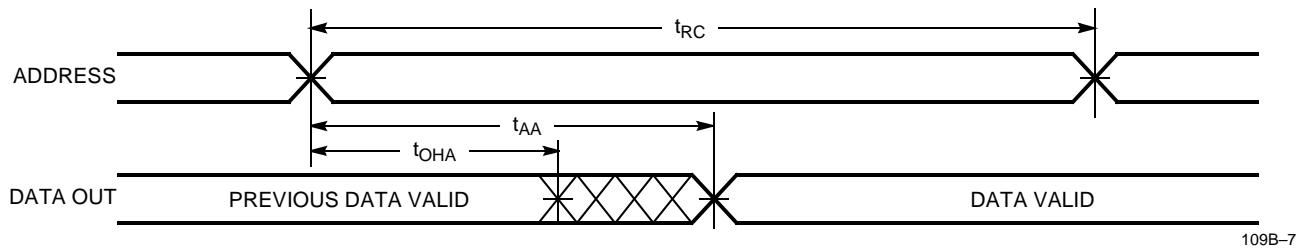
| Parameter | Description | Conditions | Min. | Max | Unit | |
|-------------------|--------------------------------------|--|------|-----|------|----|
| V _{DR} | V _{CC} for Data Retention | No input may exceed V _{CC} + 0.5V V _{CC} = V _{DR} = 2.0V, CE ₁ ≥ V _{CC} - 0.3V or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | 2.0 | | V | |
| I _{CCDR} | Data Retention Current | | | 150 | μA | |
| t _{CDR} | Chip Deselect to Data Retention Time | | | 0 | | ns |
| t _R | Operation Recovery Time | | | 200 | | μs |

Data Retention Waveform

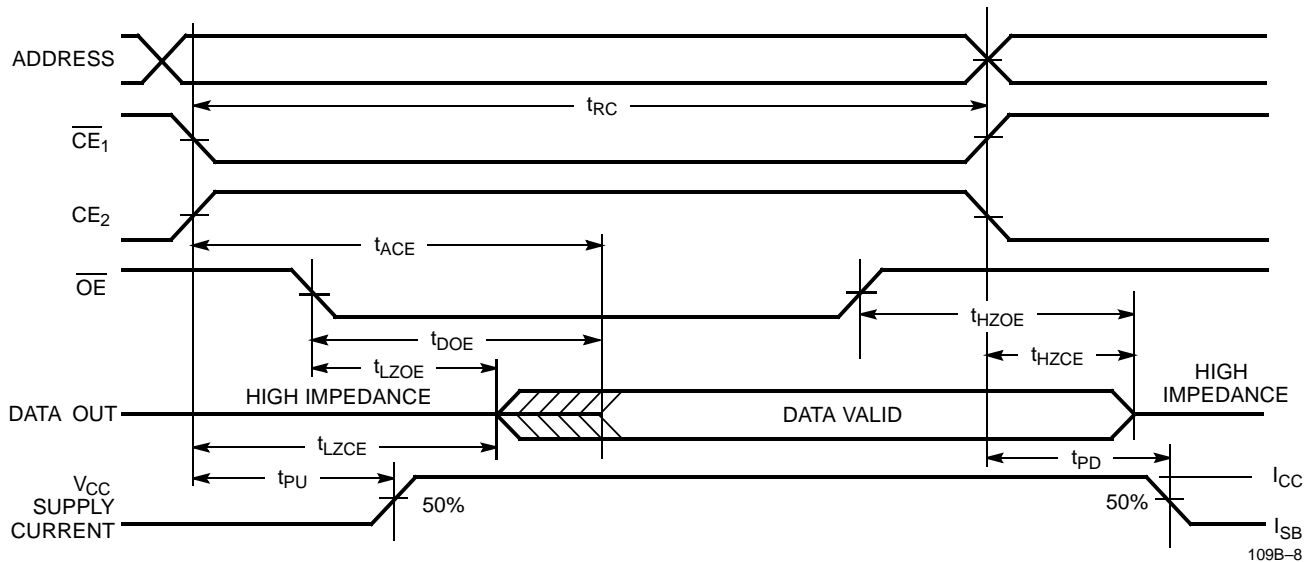


Switching Waveforms

Read Cycle No. 1^[10, 11]

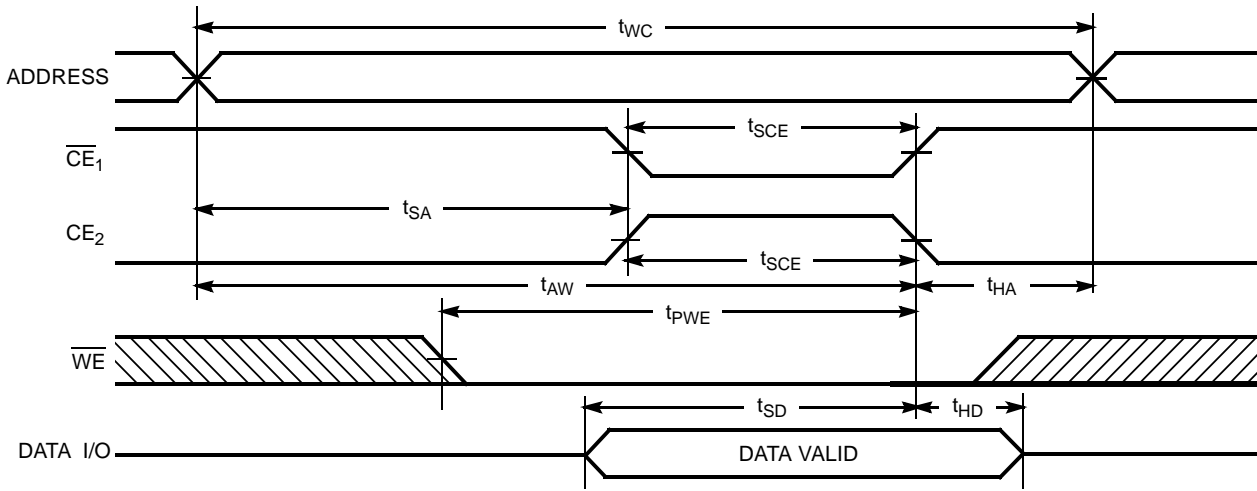


Read Cycle No. 2 (OE Controlled)^[11, 12]

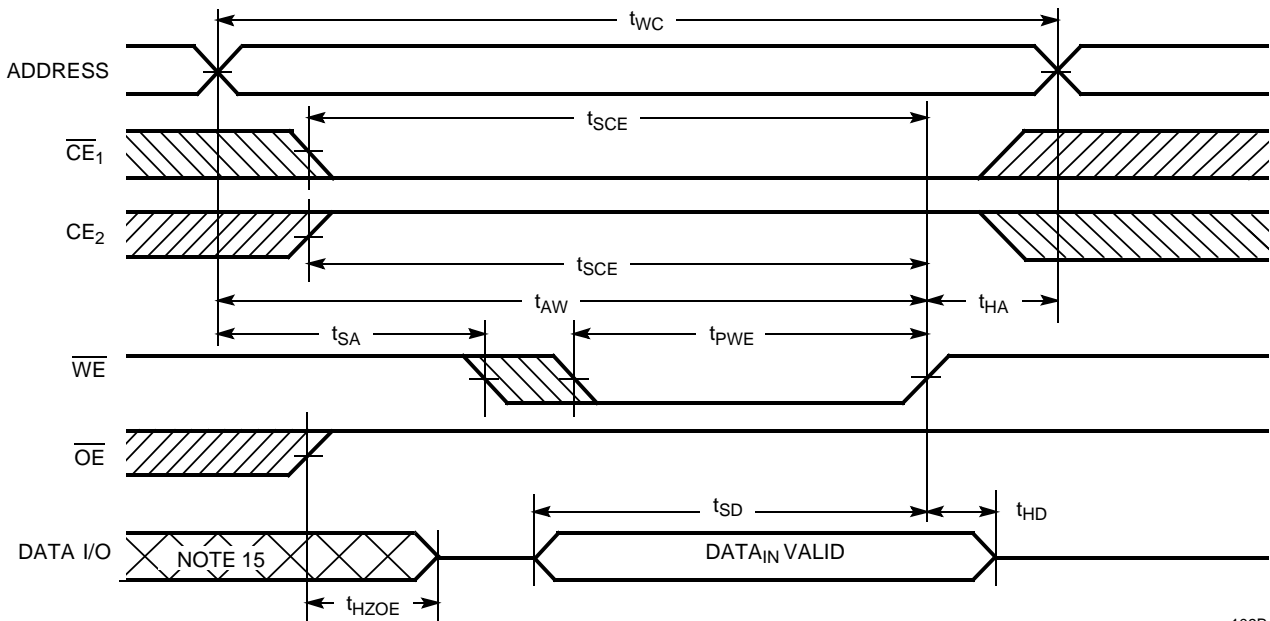


Notes:

10. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled)^[13, 14]


109B-9

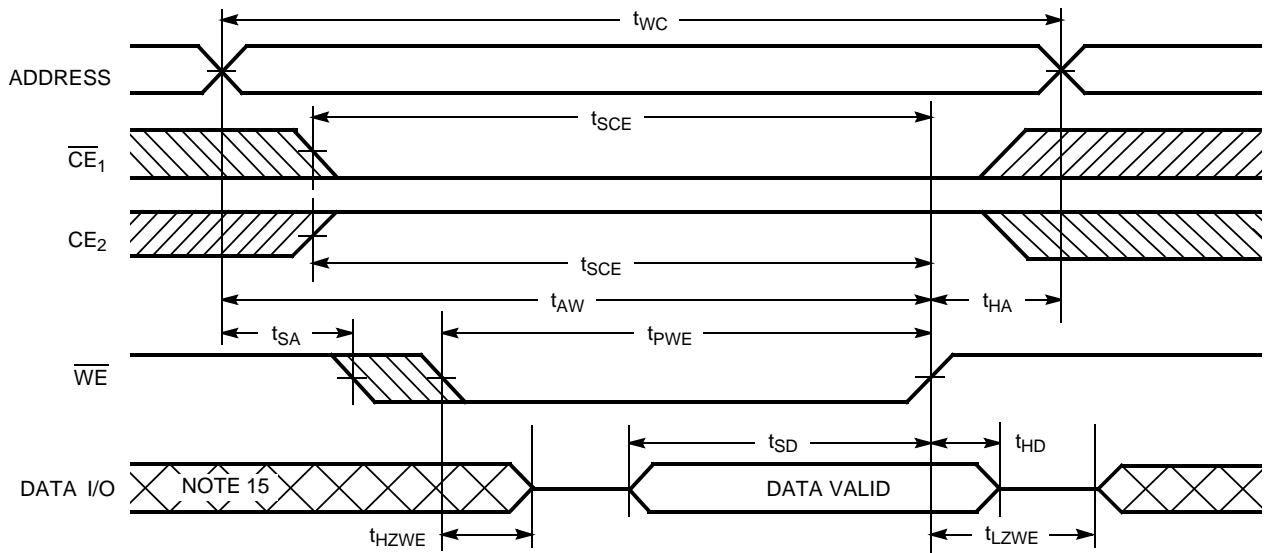
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]


109B-10

Notes:

13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[14]


10B9-11

Truth Table

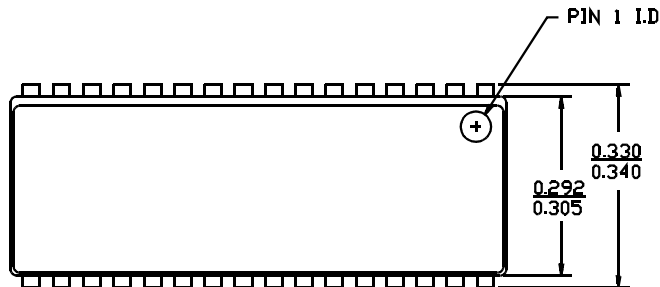
| \overline{CE}_1 | \overline{CE}_2 | \overline{OE} | \overline{WE} | $I/O_0 - I/O_7$ | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|-----------------|----------------------------|----------------------|
| H | X | X | X | High Z | Power-Down | Standby (I_{SB}) |
| X | L | X | X | High Z | Power-Down | Standby (I_{SB}) |
| L | H | L | H | Data Out | Read | Active (I_{CC}) |
| L | H | X | L | Data In | Write | Active (I_{CC}) |
| L | H | H | H | High Z | Selected, Outputs Disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|----------------|--------------|------------------------------|-----------------|
| 12 | CY7C109B-12VC | V33 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009B-12VC | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-12ZC | Z32 | 32-Lead TSOP Type I | |
| 15 | CY7C109B-15VC | V33 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C109BL-15VC | V33 | 32-Lead (400-Mil) Molded SOJ | |
| | CY7C1009B-15VC | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-15ZC | Z32 | 32-Lead TSOP Type I | |
| | CY7C109BL-15ZC | Z32 | 32-Lead TSOP Type I | |
| | CY7C109B-15VI | V33 | 32-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C109BL-15VI | V33 | 32-Lead (400-Mil) Molded SOJ | |
| | CY7C1009B-15VI | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-15ZI | Z32 | 32-Lead TSOP Type I | |
| 20 | CY7C109B-20VC | V33 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009B-20VC | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-20VI | V33 | 32-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C109B-20ZC | Z32 | 32-Lead TSOP Type I | Commercial |
| | CY7C109B-20ZI | Z32 | 32-Lead TSOP Type I | Industrial |
| 25 | CY7C109B-25VC | V33 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009B-25VC | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-25VI | V33 | 32-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C109B-25ZC | Z32 | 32-Lead TSOP Type I | Commercial |
| | CY7C109B-25ZI | Z32 | 32-Lead TSOP Type I | Industrial |
| 35 | CY7C109B-35VC | V33 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009B-35VC | V32 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109B-35VI | V33 | 32-Lead (400-Mil) Molded SOJ | Industrial |

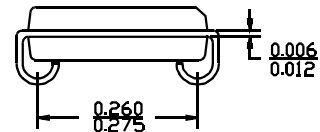
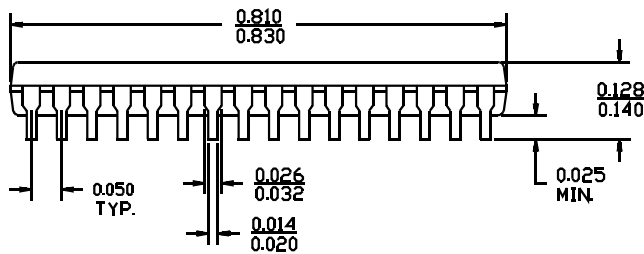
Package Diagrams

32-Lead (300-Mil) Molded SOJ V32



DIMENSIONS IN INCHES MIN. MAX.

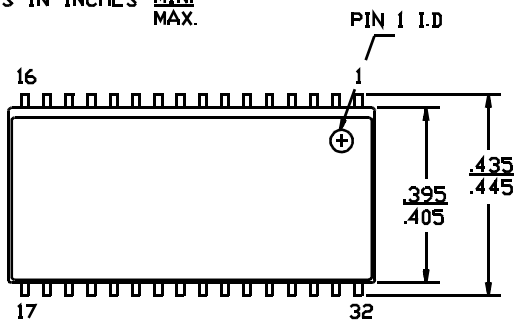
LEAD COPLANARITY 0.004 MAX.



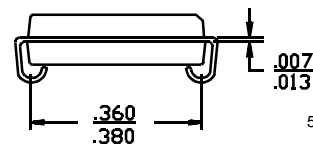
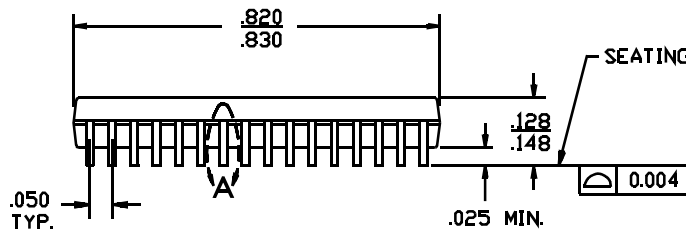
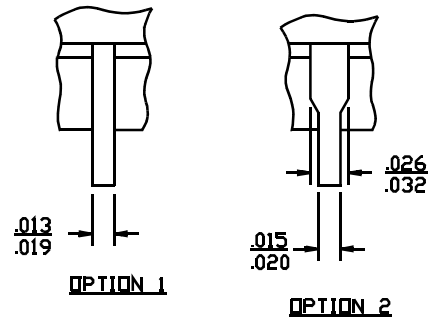
51-85041-A

32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES MIN. MAX.



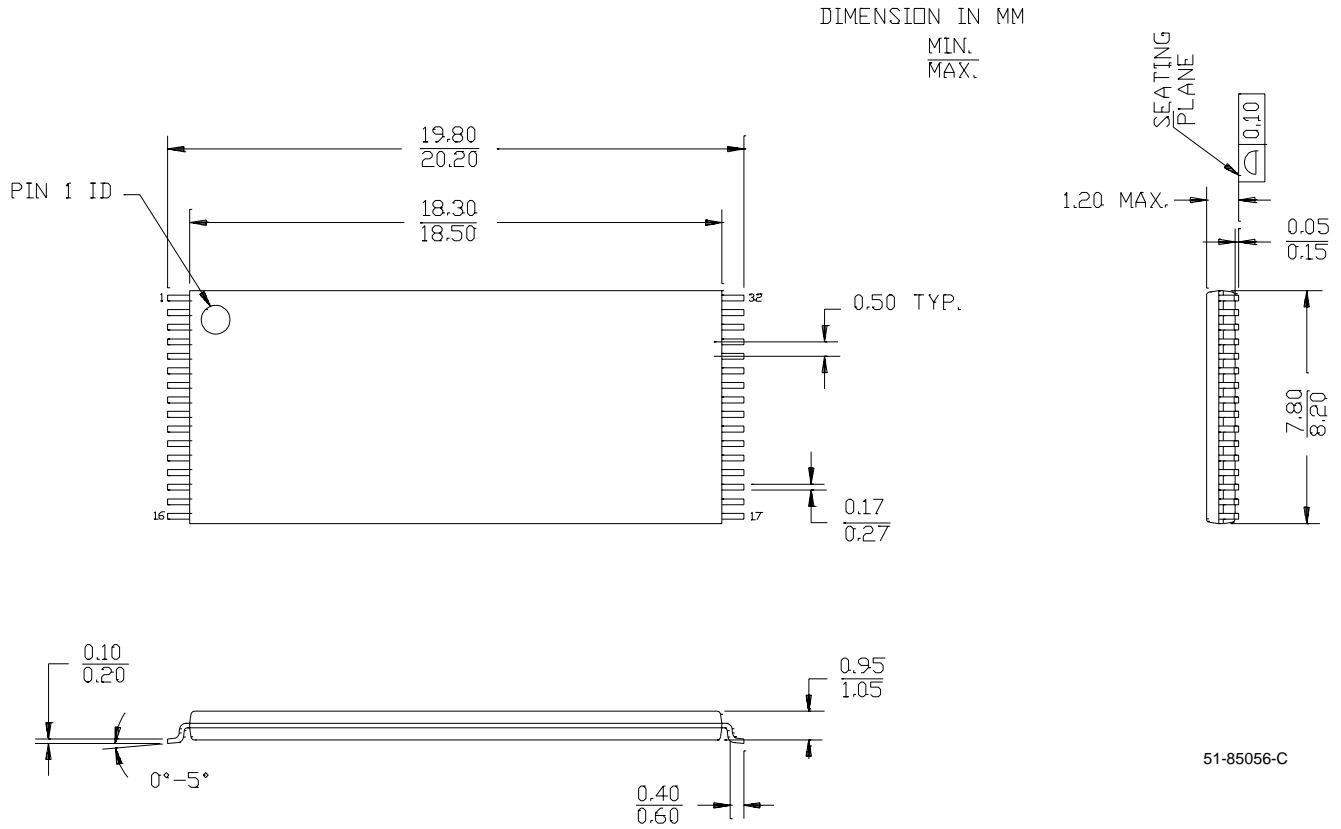
DETAIL A
EXTERNAL LEAD DESIGN



51-85033-A

Package Diagrams (continued)

32-Lead Thin Small Outline Package Z32



51-85056-C

| Document Title: CY7C109B, CY7C1009 128K x 8 SRAM Document Number: 38-05038 | | | | |
|---|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106832 | 09/22/01 | SZV | Change from Spec number: 38-00971 to 38-05038 |