

September 1983 Revised February 1999

MM74HC174 Hex D-Type Flip-Flops with Clear

General Description

The MM74HC174 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC174 is functionally as well as pin compatible to the 74LS174. All inputs are protected from damage due to static discharge by diodes to $\rm V_{CC}$ and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2-6V
- Low input current: 1 µA maximum
- \blacksquare Low quiescent current: 80 μA (74HC Series)
- Output drive: 10 LSTTL loads

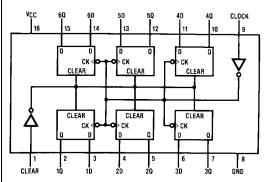
Ordering Code:

Order Number	Package Number	Package Description
MM74HC174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Truth Table

(Each Flip-Flop)

	Outputs		
Clear	Clock	D	Q
L	Х	Х	L
Н	1	Н	Н
Н	1	L	L
Н	L	Х	Q_0

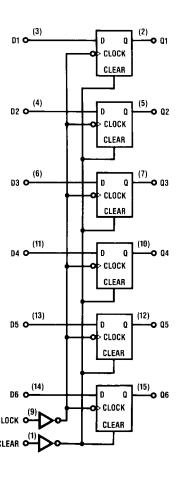
- H = HIGH Level (steady state)
- L = LOW Level (steady state)
- X = Don't Care
- \uparrow = Transition from LOW-to-HIGH level
- Q₀ = The level of Q before the indicated steady state input conditions were established

© 1999 Fairchild Semiconductor Corporation

DS005318.prf

www.fairchildsemi.com

Logic Diagram



www.fairchildsemi.com

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to V_{CC} +1.5V
DC Output Voltage (V _{OUT})	-0.5 to V_{CC} +0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –
12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

(Soldering 10 seconds)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
Зушьог		Conditions	VCC	Тур		Guaranteed L	imits	Units
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μΑ
	Current							
I _{CC}	Maximum Quiescent	V _{IN} = V _{CC} or GND	6.0V		8.0	80	160	μΑ
	Supply Current	$I_{OUT} = 0 \mu A$						

260°C

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15pF$, $t_r = t_f = 6$ ns

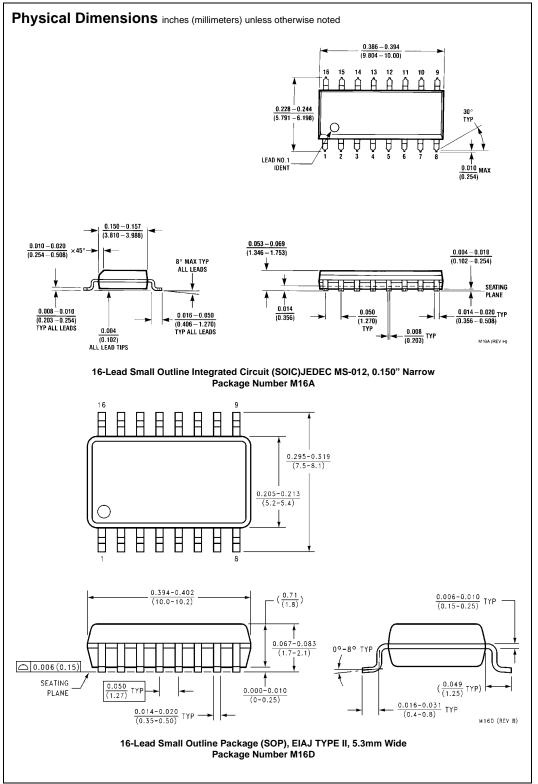
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating		50	30	MHz
	Frequency				
t _{PHL} , t _{PLH}	Maximum Propagation		16	30	ns
	Delay, Clock or Clear to Output				
t _{REM}	Minimum Removal Time,		-2	5	ns
	Clear to Clock				
t _S	Minimum Setup Time		10	20	ns
	Data to Clock				
t _H	Minimum Hold Time		0	5	ns
	Clock to Data				
t _W	Minimum Pulse Width		10	16	ns
	Clock or Clear				

AC Electrical Characteristics

 $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

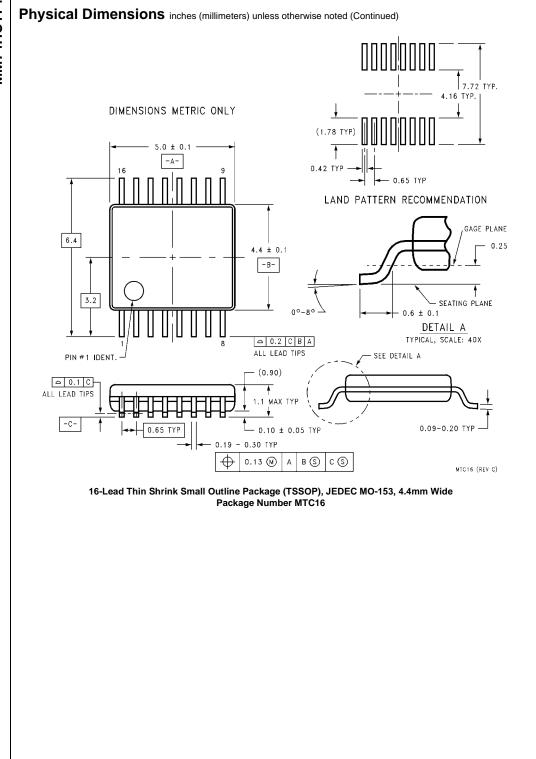
Symbol	Parameter	Conditions	V _{CC}	$T_A = 25^{\circ}C$		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	T _A = -55 to 125°C	Units
			• 66	Тур	Guaranteed Limits			Oille
f _{MAX}	Maximum Operating		2.0V		5	4	3	MHz
	Frequency		4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	55	165	206	248	ns
	Delay Clock or Clear to Output		4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t _{REM}	Minimum Removal Time		2.0V	1	5	5	5	ns
	Clear to Clock		4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t _S	Minimum Setup Time		2.0V	42	100	125	150	ns
	Data to Clock		4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t _H	Minimum Hold Time		2.0V	1	5	5	5	ns
	Clock to Data		4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t _W	Minimum Pulse Width		2.0V	35	80	106	120	ns
	Clock or Clear		4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t _{TLH} , t _{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t _r , t _f	Maximum Input Rise and		2.0V		1000	1000	1000	ns
	Fall Time		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C _{PD}	Power Dissipation	(per package)		136				pF
	Capacitance (Note 5)							
C _{IN}	Maximum Input			5	10	10	10	pF
	Capacitance							

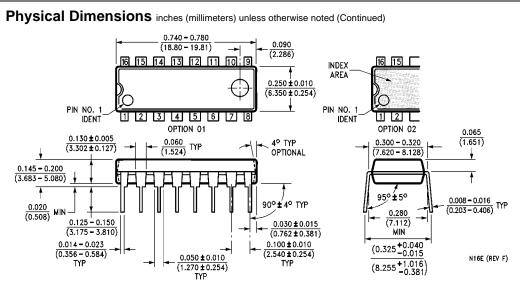
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.



5

www.fairchildsemi.com





16-Lead Plastic Dual-In Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.