FAIRCHILD SEMICONDUCTOR™

April 1988
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74F161A • 74F163A
Synchronous Presettable Binary Counter

General Description

The 74F161A and 74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 74F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 74F161A and 74F163A are high-speed versions of the 74F161 and 74F163.

Features

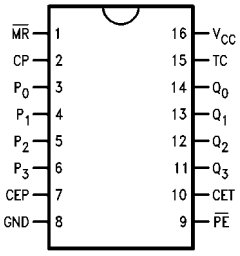
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120 MHz

Ordering Code:

Order Number	Package Number	Package Description
74F161ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F161ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F161APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F163ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F163ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F163APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



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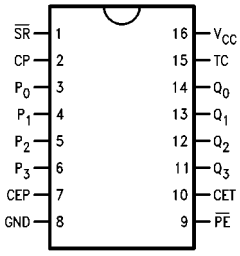

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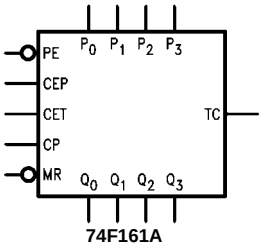
Logic Symbols



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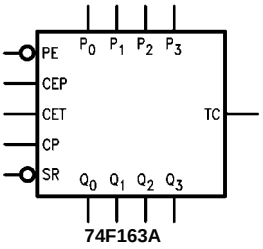
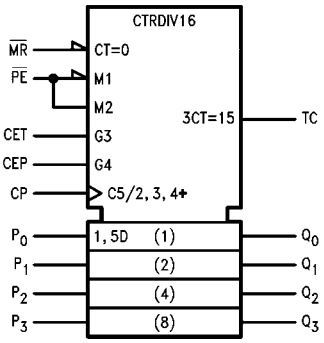


74F163A

IEEE/IEC



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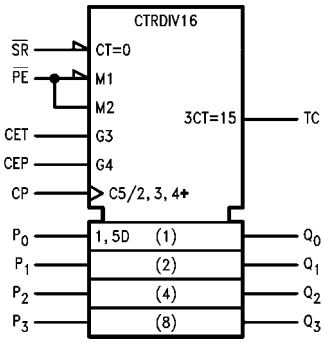
IEEE/IEC



74F163A

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 µA/–0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 µA/–1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{MR}$ (74F161A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{SR}$ (74F163A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
TC	Terminal Count Output	50/33.3	–1 mA/20 mA

Functional Description

The 74F161A and 74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (74F161A), synchronous reset (74F163A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 74F161A), Synchronous Reset ($\overline{SR}$, 74F163A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F161A) or $\overline{SR}$ (74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 74F161A and 74F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

$$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$$

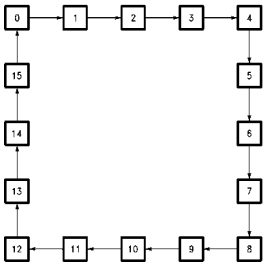
Mode Select Table

$\overline{SR}$ (Note 1)	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

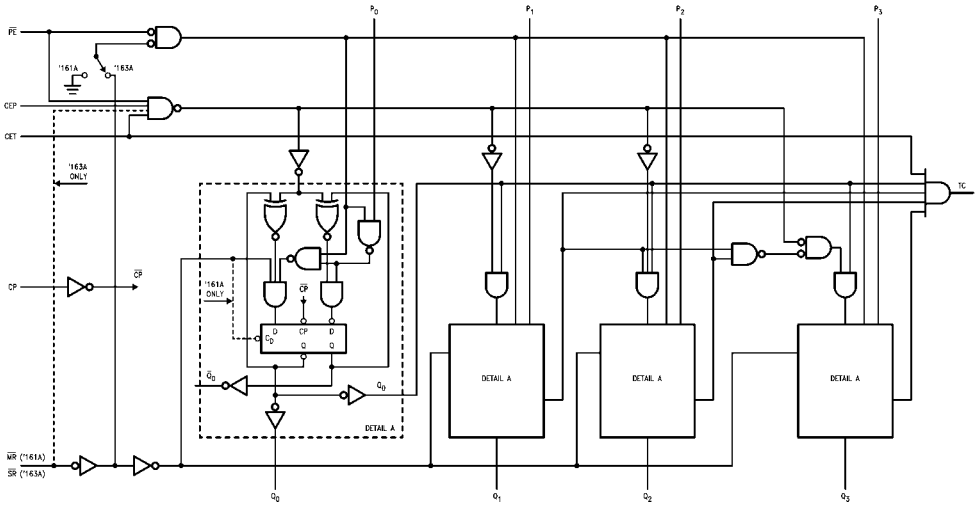
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: For 74F163A only

State Diagram



Block Diagram



Absolute Maximum Ratings (Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	
		5% V_{CC}	2.7					
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CEP, CP, $\overline{MR}$, P_0–P_3)
					−1.2	mA	Max	V_{IN} = 0.5V (CET, $\overline{PE}$, $\overline{SR}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			37	55	mA	Max	

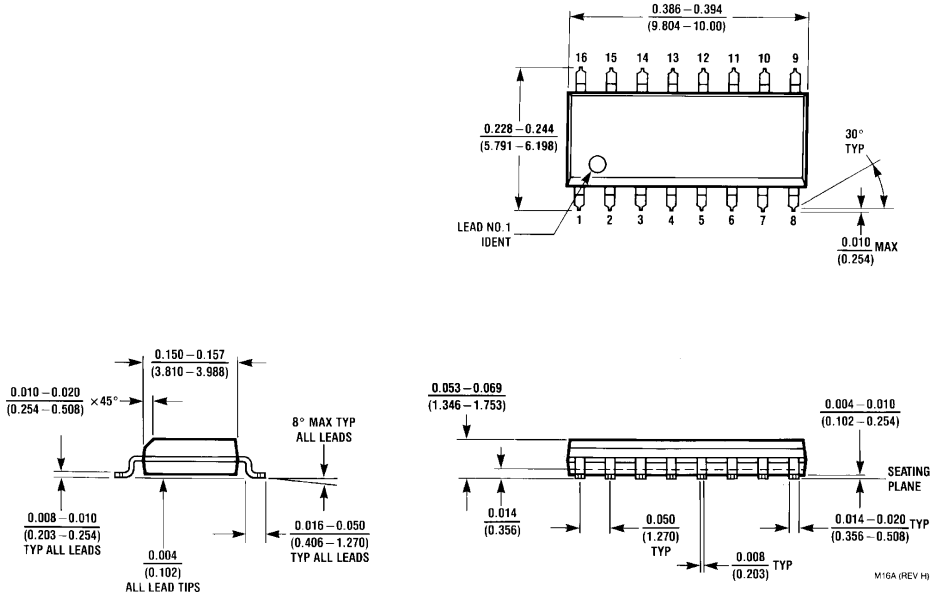
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Count Frequency	100	120		75		90		MHz
t_{PLH}	Propagation Delay	3.5	5.5	7.5	3.5	9.0	3.5	8.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ Input HIGH)	3.5	7.5	10.0	3.5	11.5	3.5	11.0	
t_{PLH}	Propagation Delay	4.0	6.0	8.5	4.0	10.0	4.0	9.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ Input LOW)	4.0	6.0	8.5	4.0	10.0	4.0	9.5	
t_{PLH}	Propagation Delay	5.0	10.0	14.0	5.0	16.5	5.0	15.0	ns
t_{PHL}	CP to TC	5.0	10.0	14.0	5.0	15.5	5.0	15.0	
t_{PLH}	Propagation Delay	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns
t_{PHL}	CET to TC	2.5	4.5	7.5	2.5	9.0	2.5	8.5	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (74F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC (74F161A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns

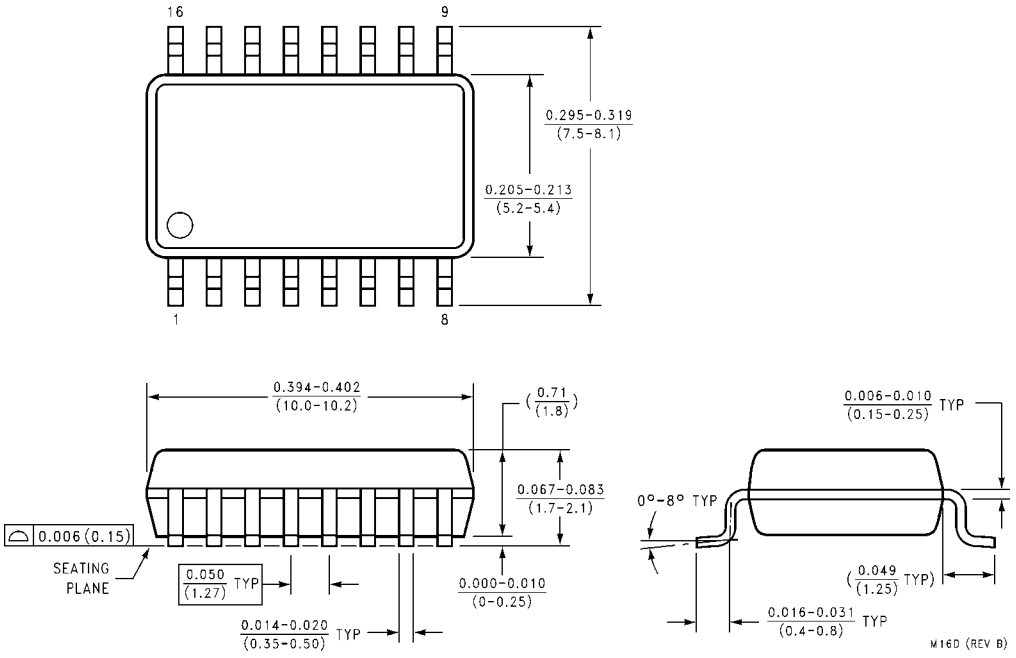
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	5.0		5.5		5.0		ns
$t_S(L)$	P_n to CP	5.0		5.5		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.5		2.0		
$t_H(L)$	P_n to CP	2.0		2.5		2.0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		13.5		11.5		ns
$t_S(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	8.5		10.5		9.5		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		3.6		2.0		
$t_H(L)$	$\overline{PE}$ or $\overline{SR}$ to CP	0		0		0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		13.0		11.5		ns
$t_S(L)$	CEP or CET to CP	5.0		6.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_H(L)$	CEP or CET to CP	0		0		0		
$t_W(H)$	Clock Pulse Width (Load)	5.0		5.0		5.0		ns
$t_W(L)$	HIGH or LOW	5.0		5.0		5.0		
$t_W(H)$	Clock Pulse Width (Count)	4.0		5.0		4.0		ns
$t_W(L)$	HIGH or LOW	6.0		8.0		7.0		
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW (74F161A)	5.0		5.0		5.0		ns
t_{REC}	Recovery Time $\overline{MR}$ to CP (74F161A)	6.0		6.0		6.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted

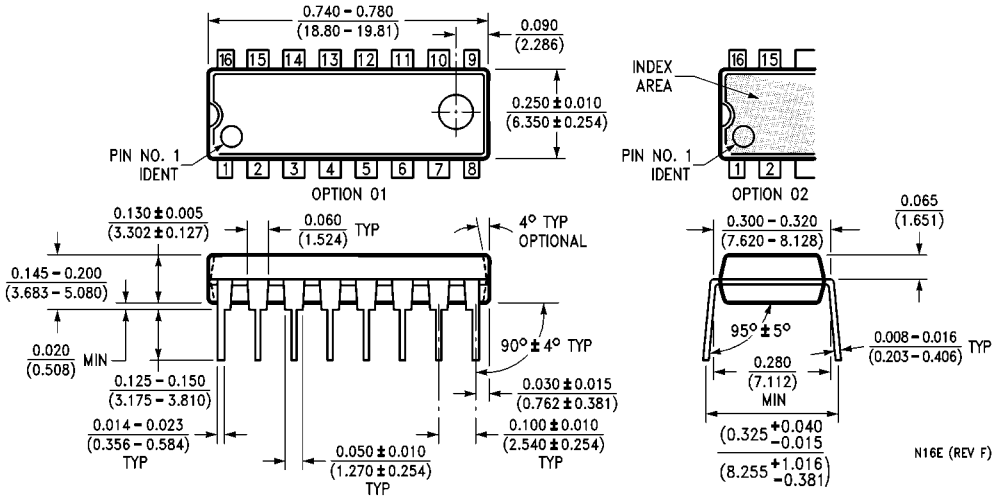


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E