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MT90220

Octal IMA/UNI PHY Device

DS5036 ISSUE 4 December 1999

Ordering Information

MT90220AL 208 Pin MQFP

-40°C to +85°C

Features

- Cost effective, single chip, 8-port ATM IMA and UNI processor
- Up to 4 IMA groups over 8 T1/E1 links can be implemented
- Supports MIXED mode; links not assigned to an IMA group can be used in UNI mode
- Versatile PCM Interface to most popular T1 or E1 framers, reducing development time
- Supports Symmetrical and Asymmetrical Operation
- Supports both Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) clocking modes
- Supports T1 ISDN lines
- Provides UTOPIA Level 2 MPHY Interface (MT90220 device slaved to ATM device)
- Complies with ITU G.804 recommendations for performing cell mapping into T1 and E1 transmission systems
- Provides ATM framing using cell delineation according to the ITU I.432 cell delineation process
- Provides Header Error Control (HEC) verification and generation, error detection, Filler cell filtering (IMA mode) and Idle/ Unassigned cell filtering (UNI mode)
- Provides statistics to support MIB
- Connects to popular asychronous SRAM
- Provides statistics on the number of HEC errors
- 8 bit Microprocessor Interface, compatible with Intel and Motorola
- 3.3V operation / 5V tolerant inputs
- MQFP-208 pin
- JTAG Test support

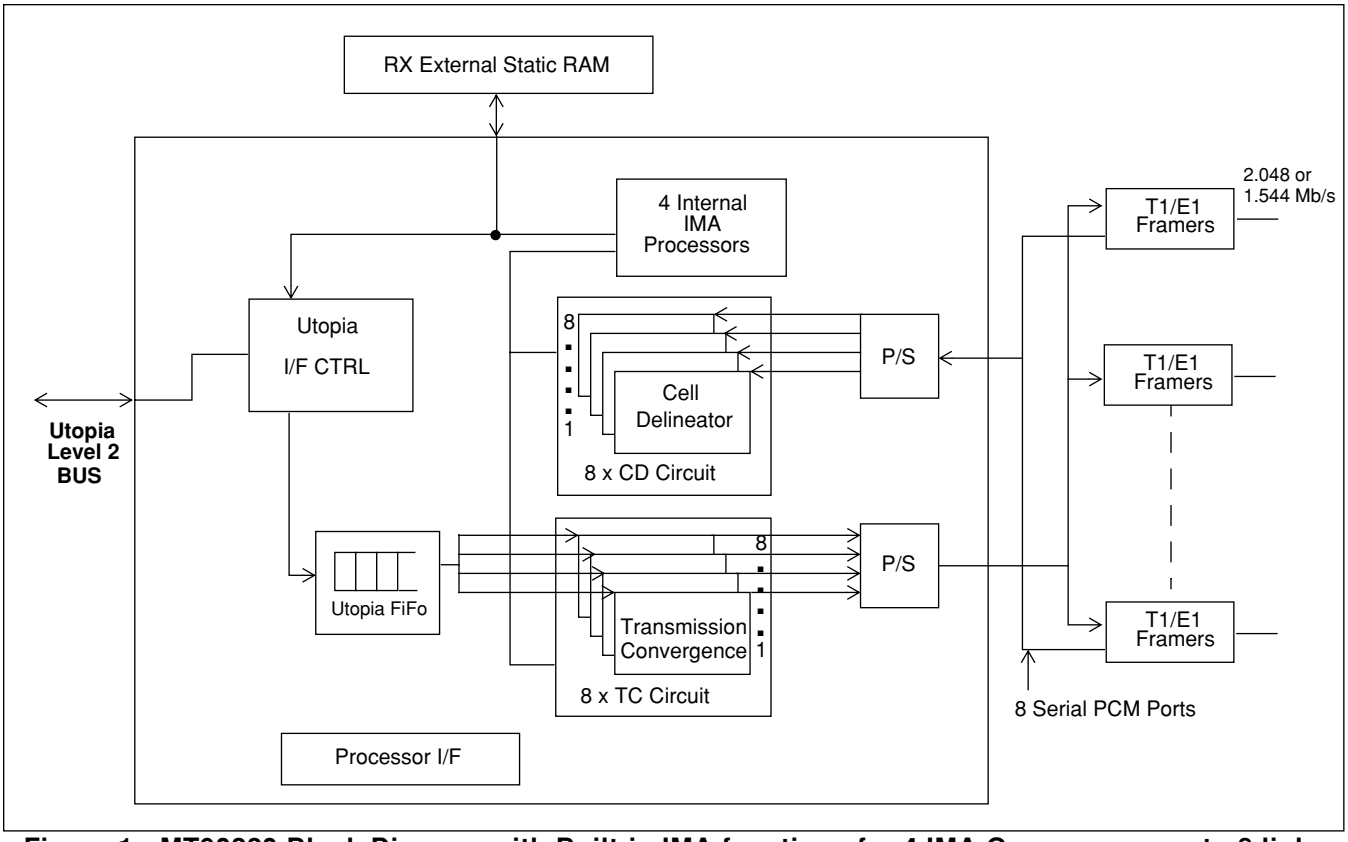

Figure 1 - MT90220 Block Diagram with Built-in IMA functions for 4 IMA Groups over up to 8 links

Applications

- Cost effective single chip solution to implement IMA and UNI links over T1 or E1 in all public or private UNI, NNI and B-ICI applications
- ATM Edge switch IMA and UNI Line Card Design
- Can be used for cost reduction in current applications based on FPGA implementation

Description

The MT90220 device is targeted to systems implementing the ATM FORUM UNI specifications for T1/E1 rates or Inverse Multiplexing for ATM (IMA). In the MT90220 architecture, up to 8 physical and independent T1/E1 streams can be terminated through the utilization of off-the-shelf, traditional T1/E1 framers and LIUs. This allows ATM designers to leverage previous T1/E1 design experience, hardware and software implementation, and to select the best T1/E1 framer for the required application.

The MT90220 device provides ATM system designers with a flexible architecture when implementing ATM access over existing and deployed trunk interfaces, allowing a migration towards ATM service technology. In addition to allowing for the design of ATM UNI specifications for T1/E1 rates, the MT90220 device is compliant with the ATM FORUM IMA specifications for controlling IMA groups of up to 8 trunks in a single chip. The MT90220 can be configured to operate in different modes to facilitate the implementation of the IMA function at both CPE and Central Office sites. For systems targeting ATM over T1/E1 with IMA and UNI operating simultaneously, the MT90220 device provides the ideal architecture and capabilities.

The device provides up to 4 internal IMA circuits and allows for bandwidth scaleability through the use of the UTOPIA MPHY, Level 2 specification at 25Mhz.

The implementation of the IMA as per AF-PHY-0086.001 Inverse Multiplexing for ATM (IMA) Specification Version 1.1 is divided into hardware and software functions. Hardware functions are implemented in the MT90220 device and software functions are implemented by the user. Additional hardware functions are included to assist in the collection of statistical information to support MIB implementation.

Hardware functions that are implemented in the MT90220 device are:

- Utopia Level 2 PHY Interface
- Incoming HEC verification and correction (optional),
- Generation of a new HEC byte
- Format outgoing bytes into multi-vendor PCM formats
- Retrieve ATM Cells from the incoming multi-vendor PCM format
- Perform cell delineation
- Provide various counters to assist in performance monitoring

Hardware functions that are implemented by the IMA processor in the MT90220 device are:

- Transmit scheduler (one per IMA group)
- Generation of the TX IMA Data Cell Rate
- Generation and insertion of ICP cells, Filler Cells and Stuff Cells in IMA mode and Idle Cells in UNI (non-IMA) mode; the ICP cells are programmed by the user and the Filler and Idle cells are pre-defined
- Retrieve and process ICP cells in IMA Mode
- Perform IMA Frame synchronization
- Management of RX links to be part of the internal re-sequencer when active
- Extraction of RX IMA Data Cell Rate
- Verification of delays between links
- Perform re-sequencing of ATM cells using external asynchronous Static RAM
- Can accommodate more than 400 msec of link differential delay depending on the amount of external memory
- Provide structured Interrupt scheme to report various events.

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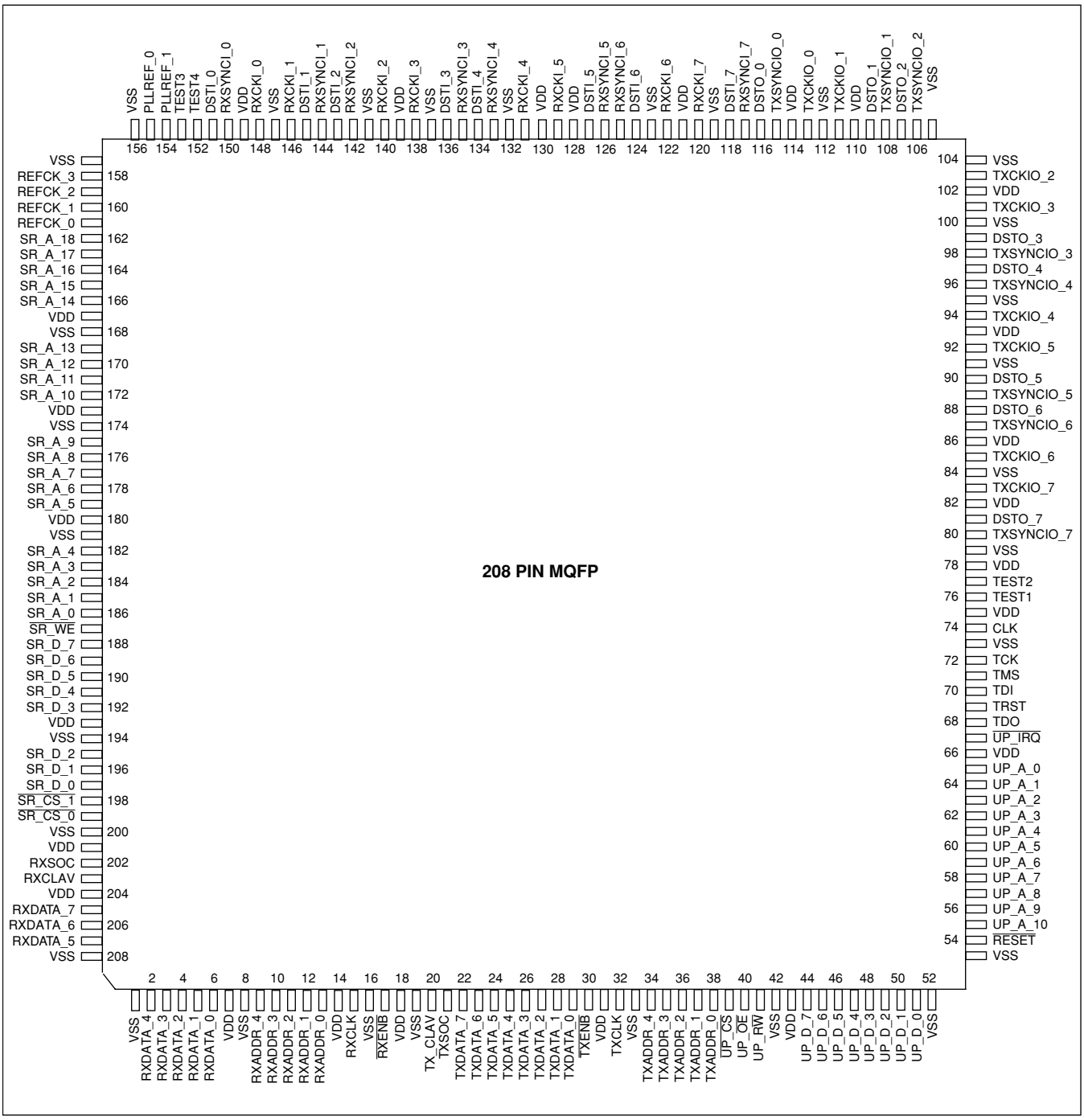


Figure 2 - Pin Connections

Pin Description

Pin #	Name	I/O	Description
ATM Input Port Signals (UTOPIA Transmit Interface)			
22, 23, 24, 25, 26, 27, 28, 29	TxData [7:0]	I	**UTOPIA Transmit Data Bus.** Byte-wide data driven from ATM LAYER device to MT90220. Bit 7 is the MSB. All arriving data between the last byte of the previous cell and the first byte of the following cell (indicated by the SOC signal) is ignored.
21	TxSOC	I	**UTOPIA Transmit Start of Cell Signal.** Active HIGH signal asserted by the ATM LAYER device when TxData[7:0] contains the first valid byte of the cell. After this signal is high, the following 52 bytes should contain valid data. The MT90220 waits for another TxSOC signal after reading a complete cell.
32	TxClk	I	**UTOPIA Transmit Clock.** Transfer clock from the ATM Layer device to the MT90220 which synchronizes data transfers on TxData[7:0]. This signal is the clock of the incoming data. Data is sampled on the rising edge of this signal.
30	$\overline{\text{TxEnb}}$	I	**UTOPIA Transmit Data Enable.** Active LOW signal asserted by the ATM LAYER device during cycles when TxData contains valid cell data.
20	TxClav	O	**UTOPIA Transmit Cell Available Indication Signal.** For cell-level flow control in a MPHY environment, TxClav is an active high tri-stateable signal from the MT90220 to the ATM LAYER device. A polled MT90220 drives TxClav only during each cycle following one with its address on the TxAddr lines. The polled MT90220 asserts TxClav high to indicate it can accept the transfer of a complete cell, otherwise it de-asserts the signal.
34, 35, 36, 37, 38	TxAddr [4:0]	I	**Transmit Address**.Five bit wide true data driven from the ATM to the PHY layer to poll and select the appropriate MT90220. TxAddr[4] is the MSB. Each MT90220 keeps its addresses. The value for the Tx and Rx portions of the MT90220 can be different
ATM Output Port Signals (UTOPIA Receive Interface) (see Note 1)			
205, 206, 207, 2, 3, 4, 5, 6	RxData [7:0]	O	**UTOPIA Receive Data Bus.** Byte-wide data driven from MT90220 to ATM layer device. RxData[7] is the MSB. To support multiple PHY configurations, RxData is tri-stateable, enabled only in cycles following those with $\overline{\text{RxEnb}}$ asserted.
202	RxSOC	O	**UTOPIA Receive Start of Cell Signal.** Active high asserted by the MT90220 when RxData contains the first valid byte of a cell. To support multiple PHY configurations, RxSOC is tri-stateable, enabled only in cycles following those with $\overline{\text{RxEnb}}$ asserted.
15	RxClk	I	UTOPIA Receive Byte Clock. This signal is the clock of the outgoing data. Data changes after the rising edge of this signal. The RxClk needs to be synchronized with the system clock.
17	$\overline{\text{RxEnb}}$	I	**UTOPIA Receive Data Enable.** Active LOW signal asserted by the ATM layer device to indicate that RxData[7:0] and RxSOC will be sampled at the end of the next cycle. In multiple PHY configurations, $\overline{\text{RxEnb}}$* is used to tri-state RxData and RxSOC MT90220 outputs. In that case, RxData and RxSOC would be enabled only in cycles following those with $\overline{\text{RxEnb}}$ asserted.
203	RxClav	O	**UTOPIA Receive Cell Available Indication Signal.** For cell-level flow control in a MPHY environment, RxClav is an active high tri-stateable signal from the MT90220 to ATM LAYER device. A polled MT90220 drives RxClav only during each cycle following one with its address on the TxAddr lines. The polled MT90220 asserts RxClav high to indicate it has a complete cell available for transfer to the ATM Layer device, otherwise it de-asserts the signal.

Pin Description (continued)

Pin #	Name	I/O	Description
9, 10, 11, 12, 13	RxAddr [4:0]	I	**Receive Address**. Five bit wide true data driven from the ATM to PHY layer to select the appropriate MT90220. RxAddr[4] is the MSB. Each MT90220 keeps its address. The value for the Tx and Rx portions of the MT90220 can be different.
Receiver Static Memory Interface Signals (see Note 1)			
188, 189, 190, 191, 192, 195, 196,197	sr_d [7:0]	I/O	**Static Memory Data Bus**. Data Bus to exchange data between the MT90220 and the external static memory.
162, 163, 164, 165, 166, 169, 170, 171, 172, 175, 176, 177, 178, 179, 182, 183, 184, 185, 186	sr_a [18:0]	O	**Static Memory Address Bus**. The signal is used to select an entry in the external static memory.
187	$\overline{\text{sr\_we}}$	O	**Static Memory Read/Not Write**. If low, data is written from the MT90220 to the memory. If high, data is read from the memory to the MT90220.
198, 199	$\overline{\text{sr\_cs\_1, 0}}$	O	**Static Memory Chip Control Signal**.
Processor Interface Signals (see Note 2)			
44, 45, 46, 47, 48, 49, 50, 51	up_d [7:0]	I/O	**Processor Data Bus**. Data Bus to exchange data between the MT90220 and a local processor.
55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65	up_a [10:0]	I	**Processor Address Bus**. They are used to select the internal registers and memory positions of the MT90220.
41	up_r/$\overline{\text{w}}$ or $\overline{\text{up\_wr}}$	I	**Processor Read/Not Write. Motorola Mode.** This is an input signal. If low, data is written from the processor to the MT90220. If high, data is read from the MT90220 to the processor. **Processor Not Write (Intel Mode).** This is an input signal. If low, data is written from the processor to the MT90220. De-asserting this signal to high will terminate a write access cycle.
40	up_$\overline{\text{oe}}$ or $\overline{\text{up\_rd}}$	I	**Output enable Motorola Mode.** This is an input signal. This signal should be tied to GND for Motorola timing mode. **Processor Not Read (Intel Mode).** This is an input signal. If low, data is read from the MT90220.
39	$\overline{\text{up\_cs}}$	I	**Processor Chip Select**. This is an active low input signal. If this signal is high, the MT90220 ignores all other signals on its processor bus. If this signal is low, the MT90220 accepts the signals on its processor bus. De-asserting this signal to high will terminate an access cycle.
67	$\overline{\text{up\_irq}}$	O	**Processor Interrupt Request**. If this signal is low, the MT90220 signals to the processor that an interrupt condition is pending inside the MT90220. Otherwise no interrupt is pending inside the MT90220. Open drain signal.
PCM Interface Signals			

Pin Description (continued)

Pin #	Name	I/O	Description
81,88, 90, 97,99,107, 109,116	DSTo [7:0]	O	**Serial PCM Data Output 7-0**. A 1.544 Mbit/s or 2.048 Mbps serial stream which contain 24 (T1) or 32 (E1) PCM or data channels received on T1 or E1 line. The output is set to high impedance for unused channels and if the link is not used.
118, 124, 127, 134, 136, 143, 145, 151	DSTi [7:0]	I	**Serial PCM Data Input 7-0**. A 1.544 Mbit/s or 2.048 Mbps serial stream which contains the 24 (T1) or 32 (E1) PCM or data channels on T1 or E1 line.
83, 85, 92, 94, 101, 103, 111, 113	TXCKi/o [7:0]	I/O	**PCM Interface Transmit Clock 7-0.** This pin is an input for PCM Modes 2, 4, 5 and 7. It is an output for Interface Modes 1, 3, 6 and 8 (see Section 4.2, PCM System Interface Modes). It is the clock for serial PCM data transmission of the T1 and E1 framers. The TXCK source is software selectable and can be either one of the eight RXCK or one of the four REFCK signals. It is used for internal transmit timing and should be connected to the Transmit Clock of the framer. 1. The TXCK is 4.096 MHz for ST-BUS applications. 2. For generic PCM Interfaces (non ST-BUS or asynchronous line termination), these outputs can be programmed to provide either a 1.544 MHz (T1) or 2.048 MHz (T1 or E1) clock.
80, 87, 89, 96, 98, 106, 108, 115	TXSYNCio [7:0]	I/O	**Transmit Line 8KHz Frame Pulse 7-0**. This pin is an input for Interface Modes 2, 4, 5 and 7. It is an output for Interface Modes 1, 3, 6 and 8 (see PCM Section 4.2, PCM System Interface Modes). It is the 8 kHz reference used as transmit synchronization for the PCM system interface. When an output, the TXSYNC is generated from the TXCK signal and is independent from other TXSYNC signals. Two output modes can be programmed: 1. For ST-BUS applications, it is a low going pulse (F0), that delimits the 32 channel frame of the ST-BUS interface at DSTi and DSTo lines (see Figure 25 - ST-BUS Timing Diagram for this sync pulse). The frame pulse is typically received through the RXSYNC[0] pin. 2. For generic PCM Interfaces, it can be programmed to generate either a positive or negative pulse polarity that lines up with the first bit of the PCM system interface.
117, 125, 126, 133, 135, 142, 144, 150	RXSYNCi [7:0]	I	**Receive line 8KHz Frame Pulse 7-0**. This signal represents the 8 KHz reference received from the incoming T1 or E1 line. The MT90220 can be programmed to accept different 8 KHz pulse formats at this input. 1. For ST-BUS applications, it is a low going pulse (F0), which delimits the 32 channel frame of ST-BUS interface at DSTi and DSTo lines. See STBUS timing diagram for this sync pulse. 2. For generic PCM Interfaces, it can be programmed to accept either positive or negative pulse polarities.
120, 122, 129, 131, 138, 140, 146, 148	RXCKi [7:0]	I	**PCM Interface Receive Clock 7-0.** This input line represents the clock for the receive serial PCM data of the T1 and E1 framers. The T1 or E1 frequency value to be received at this input clock is defined by the user through an internal register. 1. For ST-BUS applications, input pin RXCKi receives the 4.096 MHz signal. 2. For generic PCM Interfaces, these inputs can be programmed to accept either a 1.544 MHz (T1) or 2.048 MHz (T1 or E1) clock.
154, 155	PLLREF [1:0]	O	**Output reference to an external PLL**. See 4.3 Description of the PCM Interface for details.
158, 159, 160, 161	REFCK [3:0]	I	**Input reference clock inputs 3 to 0.** Receive the de-jittered transmit clock reference to be internally routed to the T1/E1 framer transmit clocks (output pins TXCK[7:0]. See “Description of the PCM Interface” on page 23. for more details.
System Signals			

Pin Description (continued)

Pin #	Name	I/O	Description
74	Clk	I	**System Clock (25 MHz nominal)**. In the MT90220, this clock is used for all internal operations of the device.
76	Test1	I	**Test1.** This signal should be high for normal operation. The signal should be pulled up for normal operation.
54	$\overline{\text{Reset}}$	I	**System Reset.** This is an active low input signal. It causes the device to enter the initial state. The Clk signal must be active to reset the internal registers.
72	TCK	I	**JTAG Test Clock.** It should be pulled down if not used
71	TMS	I	**JTAG Test Mode Select**. TMS is sampled on the rising edge of TCK. TMS has an internal pull- up resistor.
70	TDI	I	**JTAG Test Data Input**.
68	TDO	O	**JTAG Test Data Output**. **Note:** TDO is tristated by TMS pin.
69	TRST	I	**TAG Test Reset** (active low). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. **Note:** This pin has an internal **pull-down**.
77	Test2	I	**Test2**. It should be pulled down for normal operation.
153	Test3	I	**Test3**. It should be pulled down for normal operation.
152	Test4	I	**Test4**. It should be pulled up for normal operation. **NOT 5V TOLERANT**

Notes:
1. Static memory stores the received cells. RAM is used for reordering the cells
2. These signals are used to transfer data between the MT90220 and the local processor

Pinout Summary

Type	Input	Output	I/O	Power	Ground
TX UTOPIA	16	1			
RX UTOPIA	7	10			
Microprocessor Interface	14	1	8		
External Memory Interface		22	8		
TX PCM Interface		8	16		
RX PCM Interface	24				
PLL Interface	4	2			
Miscellaneous	10	1			
Power				25	
Ground					31
Total 208	75	45	32	25	31

1.0 Device Architecture

The MT90220, supported by software, implements the ATM Forum Inverse Multiplexing for Asynchronous Transfer Mode (IMA) Specification. This approach minimizes the impact of any changes that might occur in the specification. Actions are implemented by the MT90220 and decisions by the software.

The MT90220 supports following two major modes of operation:

- the IMA mode (as defined by the ATM Forum IMA Specification)
- the User Network Interface (UNI) mode

Up to four IMA Groups can be implemented. Any of the eight PCM Interfaces can be assigned dynamically to any of these IMA Groups. A different UTOPIA PHY address is assigned to each of the IMA Groups.

The UNI mode is used to transfer the cells from the UTOPIA Interface to a PCM port without any overhead. Up to 8 UTOPIA PHY addresses can be supported in UNI mode.

The MT90220 also supports a mixed mode where the PCM Interfaces not assigned to an IMA Group can be used in UNI mode.

The IMA implementation is divided into hardware and software functions. The MT90220 implements the hardware functions. The software functions are implemented by the user. The hardware and software functions are described below. Notice that a number of MT90220 functions are included to assist in the collection of statistical information. This information supports the MIB implementation.

1.1 Software Functions

For the MT90220 to comply with the IMA specification, the following functions must be implemented by software:

- the transmit and receive Link State Machines (LSM)
- the IMA Group State Machines (GSM)
- the IMA Group Traffic State Machines (GTSM)
- the Operations and Maintenance (OAM) functions

1.1.1 Link State Machines

The software implemented transmit and receive LSMs are independent (i.e., each link has its own LSM). LSMs rely on various events from the MT90220 interface, such as cell errors, excessive delay between-links, etc.; or, from the T1 or E1 framer, such as Loss Of Signal (LOS), Loss Of Frame (LOF), Remote Alarm Indication (RAI) etc.

On-chip registers are used to generate the ICP cells that communicate the LSM states to the Far End (FE).

1.1.2 IMA Group State Machines

The IMA GSMs and Group Traffic State Machines (GTSM) must be implemented in software. One of each state machine should be implemented for each IMA Group.

On-chip registers are used to generate the ICP cells that communicate the various states to the FE.

1.1.3 Link Addition, Removal or Restoration

The addition, removal or restoration of a link is controlled by software using the various control registers in the MT90220 and in the T1 or E1 framers. Decisions are based on the MT90220 and T1 or E1 framers status registers.

1.1.4 Interrupt

The MT90220 provides numerous registers and counters to implement a polling and/or interrupt mechanism for tracking link and IMA Group status. This traffic in and out information is used by the Management Information Base (MIB) for each IMA Group.

1.1.5 Signaling and Rate Adjustment

The microprocessor controls the operation of the T1 or E1 link by providing handshaking between the FE and Near Ends (NE) including such functions as signaling and loopback controls. Rate adjustment is controlled by:

- adding or removing one or more T1 or E1 links
- providing feedback to the ATM network for adjusting the ATM traffic.

1.1.6 Performance Monitoring

Software implements most of the performance monitoring. The MT90220 provides status information for:

- the Cell Delineation Block and IMA Frame State Machine
- the number of ICP violations
- the total number of cells
- the number of idle or discarded cells.

It also provides the content for received ICP cells that contain some changes. The external T1 or E1 framers provide the low level status of the link. The software integrates and responds to the various events.

1.2 Hardware Functions

The MT90220 circuitry implements the following functions:

- UTOPIA L2 Interface
- verification of the incoming HEC (optional)
- generation of a new HEC byte
- transmit scheduler
- generation of the TX IMA Data Cell Rate (IDCR)
- generation and insertion of ICP cells, Filler Cells and Stuff Cells in IMA mode
- generation of Idle Cells in UNI mode (from on-chip copies of the cells)
- flexible PCM formatting of the outgoing bytes
- retrieval of ATM Cells from the incoming PCM format
- cell delineation
- retrieval and processing of ICP cells
- synchronization of the IMA Frame
- management of the internal re-sequencer RX links (when active)
- extraction of the RX IDCR
- verification of the delays between-links
- re-sequencing of ATM cells using external Static RAM
- various performance monitoring counters
- 8-bit microprocessor interface (adaptable to Intel or Motorola interfaces)

The MT90220 can be separated into four major independent blocks and three support blocks.

The four major independent blocks are:

- the ATM Transmit Path
- the ATM Receive Path
- the PCM Interface
- the UTOPIA Interface

The three support blocks are:

- the Counter Block
- the Interrupt Block
- the Microprocessor Interface Block

2.0 The ATM Transmit Path

The transmit path corresponds to a cell flow from the ATM Layer towards the T1/E1 interface. The ATM cell path on the transmit side starts at the UTOPIA L2 Interface. Once ATM cells are received at the UTOPIA port, the device transfers these cells to the transmit block.

The MT90220 provides ATM cell mapping and transmission convergence blocks to transport ATM cell payloads over eight flexible PCM Interface ports. It uses these PCM Interface ports to communicate with most off-the-shelf T1 or E1 framers.

Each of the eight T1/E1 links can be assigned to either an IMA Group or to a UNI link. A single T1/E1 link cannot be assigned to more than one IMA Group.

The functional block diagram at Figure 3 illustrates the transmit function of the MT90220.

2.1 Cell_In_Control

In general terms, the MT90220 transmit input port has the following properties:

- cell level handshaking complies with the ATM Forum UTOPIA L2 Specification
- behaves like a UTOPIA MPHY Device
- each port can be enabled or disabled independently
- generates and optionally verifies the HEC for incoming cells
- includes the ATM Forum polynomial when generating the HEC (default option that can be disabled)
- either passes or removes incoming Idle cells
- either passes or removes incoming Unassigned cells
- provides a counter per UTOPIA port for the total number of Idle and Unassigned cells (24 bits)
- provides a counter per UTOPIA port for the total number of cells with wrong incoming HEC (24 bits)
- provides a counter per UTOPIA port for the total number of cells handled (24 bits)

The input port can be enabled to remove (filter) Unassigned or Idle cells. If Unassigned or Idle Cell Filtering is enabled, the device checks for and discards Unassigned or Idle cells. This function is programmed in the **UTOPIA Input Control** register.

Section 5 describes the UTOPIA Interface in more detail.

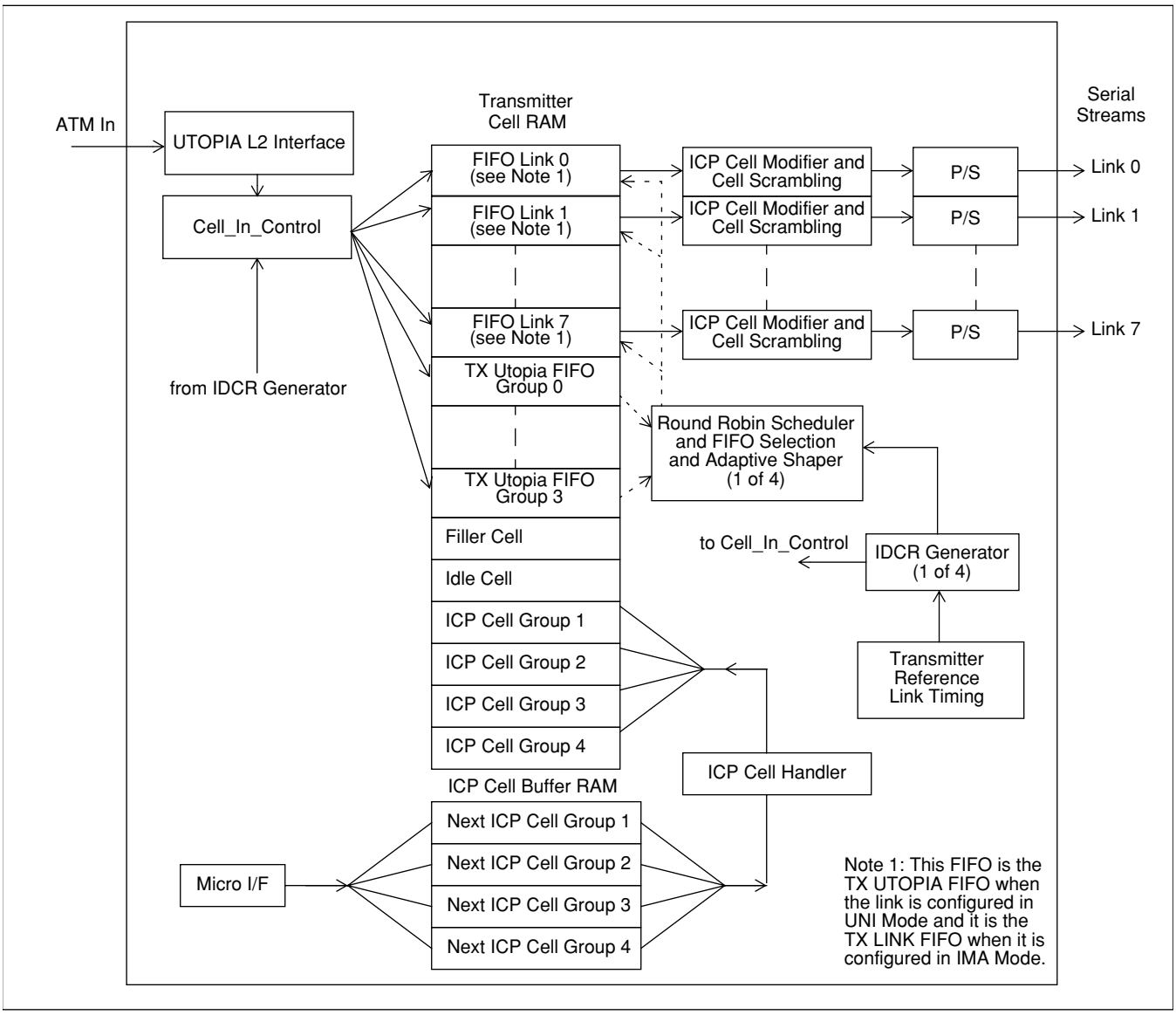


Figure 3 - Functional Block Diagram -Transmitter in IMA Mode

2.2 The ATM Transmission Convergence

The Transmit Convergence (TC) function is common for both the IMA and UNI modes. It integrates the circuitry to support ATM cell payload scrambling, HEC generation and the generation of Idle/Filler/ICP cells for use with the T1 and/or E1 trunks. Each of the eight MT90220 ATM TC circuits can use the polynomial $X^{43} + 1$ to scramble the ATM cell payload field. The MT90220 ATM cell payload scrambling function can be disabled.

The ITU I.432 polynomial $X^8 + X^2 + X + 1$ is used to generate the HEC field of the ATM cell. By default, the ATM Forum polynomial $X^6 + X^4 + X^2 + 1$ is added to the calculated HEC octet. The addition of the ATM Forum polynomial can be disabled.

The resulting calculation is then over-written on the HEC field and the ATM cell is ready (i.e., complies with the IMA transmit protocol) for transmission over the PCM Interface.

In cases where the TC block requests a cell to be transferred to any of the PCM Interfaces and the TX UTOPIA FIFO has no cell ready for transmission, then the TC block will automatically send an IDLE cell (in UNI) or a Filler cell (in IMA mode) to the line. The default values for the Idle and the Filler cells comply with the ATM IMA Specification and are pre-loaded in the MT90220 following a reset. The **TX Cell RAM Control** register can be used to re-initialize the TX Cell RAM.

2.2.1 TX Cell Ram and TX FIFO Length

The internal TX Cell Ram can hold up to 64 cells. The following six cells are reserved for MT90220 operation:

- one ICP cell for each IMA Group for a total of four cells

- one common Filler Cell used in IMA mode
- one Idle Cell used in UNI mode

The remaining 58 cells can be assigned to any of the 20 TX FIFOs. The TX FIFOs are divided in 12 TX UTOPIA FIFOs and 8 TX Link FIFOs.The MT90220 implements one TX UTOPIA FIFO for each link when used in UNI and one for each IMA Group for a total of 12 TX UTOPIA FIFOs. Each TX UTOPIA FIFO is associated with one TX UTOPIA Address. Please refer to the paragraph 5.0 UTOPIA Interface Operation for more details.

In addition, for each link to be used in IMA mode, an internal TX Link FIFO is utilized. These TX Link FIFOs are holding the cell streams that are to be sent on each TX serial port. There is a total of 8 TX Link FIFOs and their size is programmed on a per group basis using the **TX IMA Control** register. When a link is used in UNI mode, its corresponding TX Link FIFO is disabled and the TX UTOPIA FIFO is used.

TX UTOPIA FIFO Length Definition registers are used to set the TX UTOPIA FIFO size. A maximum of 15 cells can be assigned to any single FIFO. The size of unused TX UTOPIA FIFOs should be set to zero. The recommended size for the IMA Group TX UTOPIA FIFO is 1.

In IMA Mode, the ATM User Cells are first placed in the IMA TX UTOPIA FIFO and then transferred, by the internal round robin scheduler, to the proper TX Link FIFO. The TX UTOPIA FIFO length for each link configured in IMA mode should be set to zero.

The **TX IMA Control** registers are used to set the size of the internal TX Link FIFO. An upper and lower level limit must be set for the internal TX Link FIFO.

In UNI Mode, the ATM User Cells are queued in the TX UTOPIA FIFO until sent over the T1/E1 link.

The recommended upper limit value for the internal TX Link FIFO is five and the recommended lower limit is one when operating in ITC clocking mode. When operating in CTC mode, the recommended upper limit value for the internal TX Link FIFO is six and the recommended lower limit is one. In the case where CTC mode is used and when the ICP cells on all the links are sent with the same ICP cell offset and when carrying a CBR-type traffic, an upper value of 7 may be required.

2.3 Parallel to Serial PCM Interface

ATM cell octet byte alignment conforms to ITU G.804 recommendations for T1 or E1 framer parallel to serial format conversion.

The **TX PCM Control** and **RX PCM Control** registers are used to select the T1 or E1 mode of operation. Refer to Section 4, Description of the PCM Interface, for more details.

2.4 ATM Transmit Path in IMA Mode

The MT90220 supports up to four independent IMA Groups. Each of the eight T1/E1 trunks can be assigned to any one of these IMA Groups. A T1/E1 trunk cannot be assigned to more than one IMA Group. Refer to Figure 3 for a functional block diagram of the transmitter.

The IMA transmitter splits the incoming stream into N sub-streams, where $1 \leq N \leq 8$. Each sub-stream is passed to a separate line interface device that transmits the cells on a physical link.

The physical line rate is either 1.544 Mbps (T1) or 2.048 Mbps (E1). The transmitter inserts so-called ICP cells in the various outgoing streams according to the IMA specification. The ICP cells are inserted every M ATM cells on each link. This is the task of the scheduler.

2.4.1 IMA Frame Length (M)

The IMA frame length (value of M) can be 256, 128, 64, or 32. The value of M for each IMA Group is set by the **TX Group Control Mode** registers. M is fixed once an IMA Group is setup and should remain unchanged so long as that group is operational.

2.4.2 Position of the ICP Cell in the IMA Frame

The **TX ICP Cell Offset** registers control the position of the ICP cell in the IMA frame for each link. This parameter should remain unchanged so long as that group is operational.

2.4.3 Transmit Clock Operation

The MT90220 supports both the Common Transmit Clock (CTC) and Independent Transmit Clock (ITC) modes of operation. The desired mode is specified by writing to the **TX Group Control Mode** register. A reference link must be specified in the **TX Group Control Mode** register. The MT90220 introduces a Stuff cell on the reference link every 2048 cells and determines the appropriate time to insert a Stuff cell on the remaining group links. See paragraph 2.4.4, Stuff Cell Rate, for more details.

The clocking mode and reference link are fixed once an IMA Group is setup and should remain unchanged so long as that group is operational. The reference link should not change unless problems are reported with the link.

2.4.4 Stuff Cell Rate

The Stuff event algorithm differs between CTC and ITC modes. In CTC mode, the Stuff event is typically fixed and appears in the same IMA frame on all IMA Group links. In ITC mode, the Stuff event is determined using an adaptive algorithm that relates the level of the internal TX Link FIFO to that of the TX link FIFO of the Reference link.

The MT90220 implements 2 different stuffing algorithms: a fixed stuffing rate and an adaptive stuffing rate. The Stuffing events do not happen more frequently than once every five IMA frames.

TX Group Control Mode register bit 3 selects either the adaptive or fixed algorithm. Bit 4 determines the timing mode declared in the ICP cell.

There are three possible combinations:

- CTC Mode with internal Fixed algorithm
- CTC Mode with internal Adaptive algorithm
- ITC Mode with internal Adaptive algorithm

In CTC mode, when using the Fixed algorithm, the Stuff event is periodic and will appear in the same IMA frame, once every 2048 cells, on each link that is part of the IMA Group.

In CTC mode, when using the Adaptive algorithm, the Stuff event will occur at an average rate of once every 2048 cells on each link and may not occur in the same IMA Frame on all the links.

In ITC mode, the Stuff event is determined using the adaptive algorithm that relates the level of the internal TX Link FIFO with that of the TX Link FIFO of the Reference link. The reference link has one Stuff event every 2048 cells.

The state of bit seven in the **TX IMA Control** register determines whether a Stuff indication is generated in the first or first four frames preceding a Stuff event.

2.4.5 IMA Data Cell Rate

The MT90220 computes the internal TX IMA Data Cell Rate (IDCR) for each IMA Group. The cell rate for the IMA Group reference link, specified in the **TX Group Control Mode** register, is integrated over a programmable period of time. The preferred integration period is programmed in the TX IDCR Integration register and the value is indicated in Table 1.

PCM Mode	Preferred Value TX IDCR Integration register
T1 ISDN (23 channels)	0x09 (2^{16} clocks)
T1 (24 channels)	0x0B (2^{18} clocks)
E1(30 channels)	0x0C (2^{19} clocks)

Table 1 - IDCR Integration Register Value

2.4.6 IMA Controller (RoundRobin Scheduler)

The IMA controller produces the cell stream to be sent to the PCM blocks using the following four cell types:

- Data cells received from the UTOPIA port (User cells)
- Filler cells
- IMA ICP cells with Link status information
- Stuff cells

At an IDCR clock tick, the RoundRobin scheduler inserts either an ICP cell, a User cell or a Filler cell into the TX Link FIFO of the next link of the IMA group, based on ascending link ID numbers. An ICP cell is inserted every M cells and a stuff event is inserted when indicated by the stuffing algorithm.

If it is not time for an ICP cell and if the traffic is not enabled for the link (see bit 6 of the **TX Link Control** register), then a Filler cell is inserted in the TX Link FIFO. If the traffic is enabled and there is a User cell in the TX Utopia FIFO, then the User cell is transferred from the TX UTOPIA FIFO to the TX Link FIFO. If there is no User cell in the TX UTOPIA FIFO, then a Filler cell is inserted in the TX Link FIFO.

2.4.7 ICP Cell Generator

Once per IMA frame, an ICP cell is transmitted on each link of the IMA Group. The content of the ICP cell is controlled both by MT90220 and software. The software content of the ICP cell bytes is stored in buffer RAM. A copy of the ICP cell for each group is kept in the internal Transmitter Cell RAM.

The ICP cell to be transmitted on each link is assembled on an as required basis under the control of the internal RoundRobin scheduler and ICP Cell Modifier.

Hardware controls the following bytes of the ICP cell:

- Byte 5 - the HEC is always calculated and inserted by the MT90220
- Byte 6 - the **TX OAM** Label is defined by the software and the value contained in this location is transmitted in all ICP cells, Stuff

Byte	Description	Control Source
1-5	ICP Cell Header	Content of Header is under S/W control. The HEC is calculated by H/W.
6	OAM label	S/W control
7	Cell ID, Link ID	The Link ID is programmed through other registers and inserted by H/W
8	IMA Frame Sequence	Hardware Control
9	ICP Cell Offset	H/W Control. (Programmed by S/W through other registers)
10	Link Stuff Indication	H/W Control
11	Status Change Indic.	H/W Control
12	IMA ID	S/W Control
13	Group Status and Control	S/W Control except for value of M
14	Sync. Info.	H/W Control (Programmed by S/W through other registers)
15	Test Control	S/W Control
16	TX Test Pattern	S/W Control
17	RX Test Pattern	S/W Control
18-49	Link Status and Control	S/W Control
50	Unused	S/W Control
51	End-to-End Channel	S/W Control
52-53	CRC Error Control	H/W Calculation

Table 2 - ICP Cell Description

Cells and Filler cells sent on all the links that are part of the corresponding TX IMA group

- Byte 7 - the **TX Link ID** register is used to set the Link Logical ID and the cell type is determined by the internal controller on a per link basis
- Byte 8 - the frame sequence number is controlled by an internal counter
- Byte 9 - the **TX ICP Cell Offset** register is used to set the value. This value is inserted on a per link basis
- Byte 10 - the link Stuff indication is inserted automatically and the advance indication option is programmed by the **TX IMA Control** register on a per link basis
- Byte 11 - the SCCI is controlled by internal circuitry. The SCCI is incremented by one for each transfer of the TX ICP cell from the buffer area to the TX Cell RAM.
- Byte 13 - the value of M is programmed through the **TX Group Control Mode** register
- Byte 14 - the **TX Group Control Mode** register is used to set the Transmit Timing Information and define the reference link
- Bytes 52 and 53 - the calculated CRC-10 Error Control bits are inserted automatically

Software controls all remaining bytes of the ICP cells. It also maintains and updates all bytes that are not directly controlled by the MT90220. A dedicated address is reserved for each ICP cell byte for each of the four IMA Groups. This permits direct access to any of the bytes stored in each of the four **ICP Cell** registers. Refer to Table 2, ICP Cell Description, for details on the ICP cell byte contents.

To avoid updating or corruption problems, the internal copy of the ICP Cell cannot be directly accessed. ICP cells are prepared in a buffer area (RAM inside the MT90220) and transfer commands are issued to copy the content of the ICP cell into the internal Cell RAM area and to start using this new ICP cell. The MT90220 uses a flag (status bit) to indicate that this transfer is underway. Changes should not be made to the content of the ICP cell in the buffer area until the transfer to the internal memory is complete. The status bit is cleared during the transfer and returns to '1' on completion of the transfer. IMA Groups are controlled independently. When access to the ICP cell of one group is prohibited, the other ICP cell buffer areas can still be updated. The **TX ICP Cell Handler** and **TX ICP Interrupt Enable** registers are used to initiate a transfer and enable an optional interrupt to indicate when the process is complete.

The SCCI field is incremented by one for each transfer command performed which includes a change in at least one byte of the ICP cell.

2.4.8 IMA Frame Programmable Interrupt

An optional interrupt is provided at the end of an IMA frame to simplify software implemented changes in the Group Control and Status field. This interrupt can be enabled on an as required and per group basis to implement a frame counter. The **TX ICP Cell Handler** and **TX ICP Interrupt Enable** registers are used for the transfer ready and frame interrupt.

2.4.9 Filler Cell Definition

The content of the Filler cell is pre-initialized and conforms with the IMA Specification.

2.4.10 TX IMA Group Start-Up

Initialize the TX IMA Group start-up as follows:

(Note: The startup procedure below is given indicating the most important steps. A more detailed and complete sequence can be found in the MT90220/221 Programmer's Manual and example code).

- Configure the TX PCM port(s) by writing to the **TX PCM Link Control** register 1 and 2.
- Write the value of M, the Timing Mode and the reference link number to the **TX Group Control** register corresponding to the IMA Group number to be initialized.
- Write the Link ID (LID is between 0-31) to **TX Link ID** registers for each link to be used in the IMA Group. LID should not be changed when a group is operational. Ensure each link that is part of an IMA group has a unique LID (note that the MT90220 does not verify LIDs).
- Write the ICP Cell Offset value to **TX ICP Cell Offset** registers. This value depends on the value of M. Typically, the reference link will have a delay of 0 cells in the IMA Frame and the ICP cell in each other link will be evenly spaced in a multiple of M/N cells (where M is defined in the IMA specification and N is the number of links). The offset value for an operational group should not be changed.
- Write to the **TX Link Control** registers to put the link(s) in IMA mode and to enable the transfer of ATM User Cells when required.

2.4.11 TX Link Addition

The MT90220 supports software controlled link addition to the existing IMA group. Link addition is used to increase the available bandwidth. The **TX PCM Link Control register 1** and **2, the TX Link ID** and **TX ICP Cell Offset** registers are initialized first with the proper IMA Group information. The link is assigned to a TX IMA group by writing to the lower 2 bits of the **TX Link Control** register. The bit 3, 1 and 0 of the **Test 2** register have to be written with the proper value. The link is then configured in IMA mode by writing to the bit 2 of the **TX Link Contro**l register. The **TX IMA Mode** Status register is monitored to detect when the link is reported in IMA mode. When the link is in IMA mode, then the bit 3, 1 and 0 of the Test 2 register are reset to 0. **TX Link control** register bit 6 determines when ATM User cells can be sent. Note that the **Test 2** register cannot be used as a read/modify/write register. The values that are written and the values that are read are independant. Note also that the bit 6 of the **Test 2** register should always be set to 1.

2.4.12 TX Link Deletion

There are two reasons to remove a link: the required bandwidth decreases or a link becomes faulty. The MT90220 supports link deactivation under software control.

A link stops transmitting User cells when bit 6 of the **TX Link Control register** is set to 0. Filler and ICP cells will still be sent on the link. The link is removed from an IMA group by first setting the bit 2 of the **TX Link Control register** to 1 while keeping the original IMA group number. The IMA group number can be changed only when the link is in UNI mode as

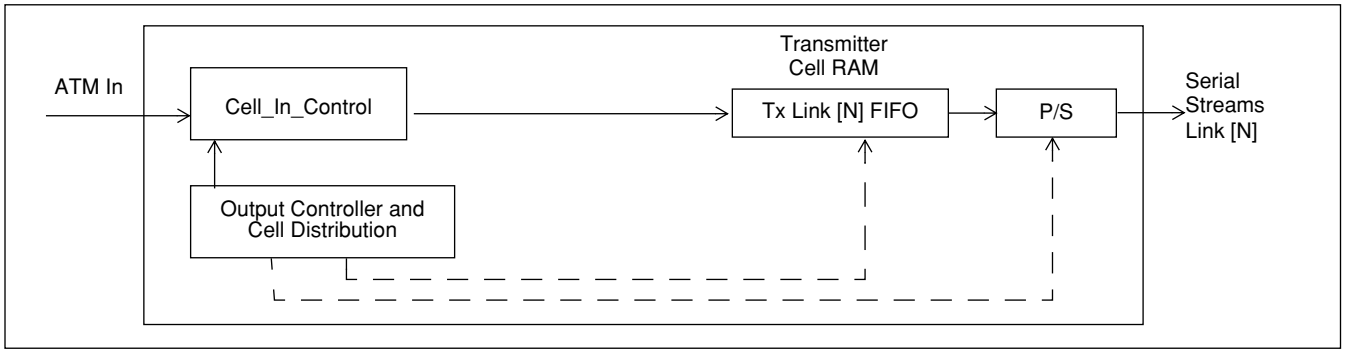


Figure 4 - Functional Block Diagram of the Transmitter in UNI Mode (For Link[N] where 1 ≤ N ≤ 8)

reported in the **TX IMA Mode Status register**. It then can be assigned to another IMA group.

When removing the last link of a TX IMA group, the **TX Utopia FIFO** has to be empty. This can easily be done by first disabling the source of ATM cells (ATM Utopia contoller), then disabling the **TX Utopia Port** using the UTOPIA input Link or Group PHY enable registers while still keeping the "Send User Cell" bit of the TX Link Control Centre register set to 1. The level of the **TX Utopia FIFO** can be monitored using **TX Utopia FIFO Level register**. The above procedure can then be applied to assign the link in UNI mode.

When the link is configured in UNI mode, IDLE cells are transmitted. Writing to the **TX PCM Link Control** registers either turns off the transmitter or reconfigures the link into another mode.

2.5 ATM Transmit Path in UNI Mode

A maximum of eight independent T1/E1 interfaces can be selected in UNI mode. Figure 4 gives a functional block diagram of the transmitter in UNI mode.

ATM cells received from the ATM port are placed in a TX UTOPIA FIFO, waiting to be transmitted. If the Idle/Unassigned cell removal option is selected, these cells are dropped. If the TX UTOPIA FIFO is empty, an Idle cell is sent to the output link. The content of the Idle cell is pre-initialized with the header bytes set at 0x00, 0x00, 0x00 and 0x01. The payload bytes are set to 0x6A.

TX UTOPIA FIFO Length Definition registers are used to set the TX UTOPIA FIFO size. The total number of cells in all the TX UTOPIA FIFOs and TX Link FIFO (includes the links used in IMA Mode and the links used in UNI Mode) is limited to 58.

Idle Cells are transmitted on the UNI PCM Interface until the bit corresponding to the link in the **UTOPIA Input Link PHY Enable** register is set. Then, the ATM User cells are transferred from the Input UTOPIA port to the TX PCM port.

3.0 The ATM Receive Path

The receive path corresponds to the cell flow from the T1/E1 interfaces to the ATM UTOPIA Interface. The MT90220 provides cell delineation and optional cell filtering to discard Unassigned or Idle cells on each link. The incoming cells are stored in the external RAM required in IMA mode to perform cell recovery due to delay variation between the links introduced by the network.

3.1 Cell Delineation Function

This block provides the circuitry necessary to perform functions such as Cell Delineation (CD), cell payload de-scrambling, HEC verification and filtering of Idle (UNI) cells. The CD circuit delineates ATM cells received from the payload of the T1 or E1 frame through the PCM Interface.

When performing delineation, correct HEC calculations are interpreted to indicate cell boundaries. The CD circuit performs a sequential byte by byte hunt for a correct HEC sequence. While performing this hunt, the cell delineation state machine is in the HUNT state. Figure 5 depicts a state diagram of the cell delineation operation.

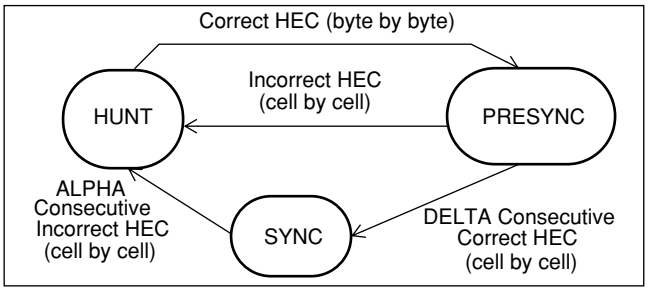


Figure 5 - Cell Delineation State Diagram

When a correct HEC is found, the CD circuit locks on the cell boundary and enters the PRESYNC state. The PRESYNC state keeps checking the HEC to ensure that the previous indication was not false.

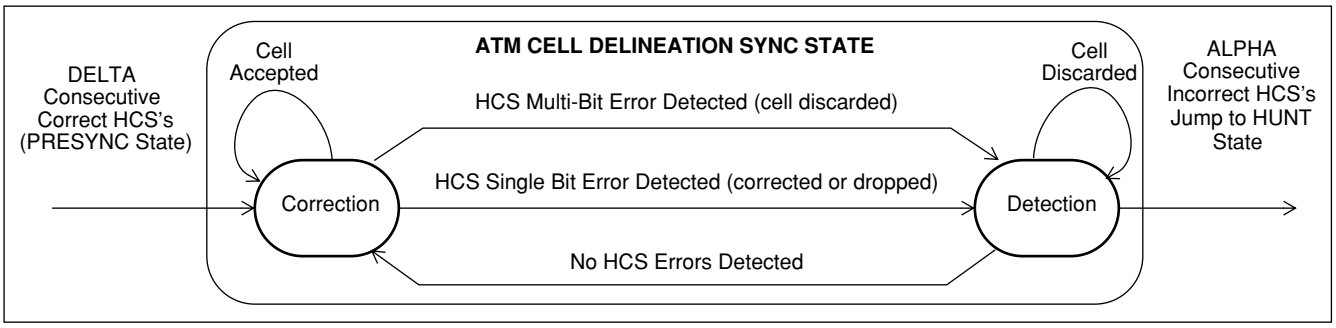


Figure 6 - SYNC State Block Diagram

False indications are interpreted to mean the circuit is not tracking good ATM cells. After entering the PRESYNC state, the first false indication triggers a transition back to HUNT state.

If the PRESYNC state HEC is correct, then a transition to the SYNC state occurs after *"δ"* cells (DELTA in ITU I.432) are correctly received. In the SYNC state, the CD circuit treats the incoming ATM cell stream as stable and the MT90220 functions normally.

While in the SYNC state, if an incorrect HEC is obtained *"a"* consecutive times (ALPHA in ITU I.432), cell delineation is considered lost and a transition is made back to the HUNT state (see Figure 6).

As defined by the ITU I.432 recommendations, the value of ALPHA and DELTA determine the robustness of the delineation method. The value of ALPHA and DELTA for the Cell Delineation state machine are defined in the **Cell Delineation** register. Only one set of values is defined for the eight Cell Delineation state machines. The status of the CD state machine for each link is available in bits 0 and 1 of the **RX Cell Delineation State** register.

The ITU I.432 suggested values are: ALPHA = 7; and DELTA = 6.

Loss of Cell Delineation (LCD) is detected by counting the number of incorrect cells while in HUNT state. The MT90220 provides an internal **Loss Cell Delineation** register to set the threshold for this count. A value of 360 in the LCD register would correspond to 79 msec for E1 and 100 msec for T1 applications. The LCD state for each link is available in bit 1 of the **IRQ LinkStatus** registers, and in bit 6 of the **RX Link ID Number** register.

The LCD status bit is reporting the current condition of the Cell Delineation State Machine at the time it is read and cannot not be programmed to generate an interrupt when exiting the LCD condition. The software has to poll the status bit to determine when the condition is cleared.

Table 3 provides the time, in microseconds, for the CD circuit to receive a full ATM cell from the T1 and E1 frame payloads.

Format	Average Cell Acquisition Time (μs)
T1	276
E1	221

Table 3 - Cell Acquisition Time

While the cell delineation state machine is in the SYNC state, the verification circuit implements the state machine shown in Figure 6.

In normal operation, the HEC verification state machine remains in the 'correction' state. Incoming cells containing no HEC errors are passed to the receive IMA block (RX IMA). Incoming single-bit errors can be corrected if required by the application (i.e., single bit error correction can be enabled or disabled).

After correction (when enabled), the resulting ATM cell is passed to the RX IMA block for IMA sequencing control.

If a single or multi bit error occurs, the state machine goes to the 'detection' state. When a cell with a good HEC is detected, the state machine returns to the 'correction' state. The HEC calculation normally includes the ATM FORUM polynomial ($X^6 + X^4 + X^2 + 1$). The use of the polynomial can be disabled by writing to bit 1 of the **RX Link Control** register.

3.2 De-Scrambling and ATM Cell Filtering

The CD circuit can de-scramble the cell payload field. The de-scrambling algorithm can be enabled or disabled using bit 5 of the **RX Link Control** registers.

The MT90220 can be programmed, using the **RX Link Control** registers, to discard received ATM cells with HEC error.

HEC error correction is optional and can be enabled by the CPU. When the option to correct an incoming HEC value with 1 bit error is selected, the HEC is corrected and the cell is not counted as a cell with a bad HEC. If the option to remove the cells that are received with a bad HEC is selected, then the incoming cells are replaced by a Filler cell in IMA mode. The cell is simply discarded when in UNI mode. The counter is not incremented if the HEC value is corrected, when the option is enabled.

Incoming Idle and Unassigned cells can be detected and dropped automatically.

3.3 ATM Receive Path in IMA Mode

The block diagram at Figure 7 illustrates the MT90220 IMA mode receive path. The receiver must rearrange the incoming bit streams from N-links ($1 \leq N \leq 8$) into a single UTOPIA cell stream.

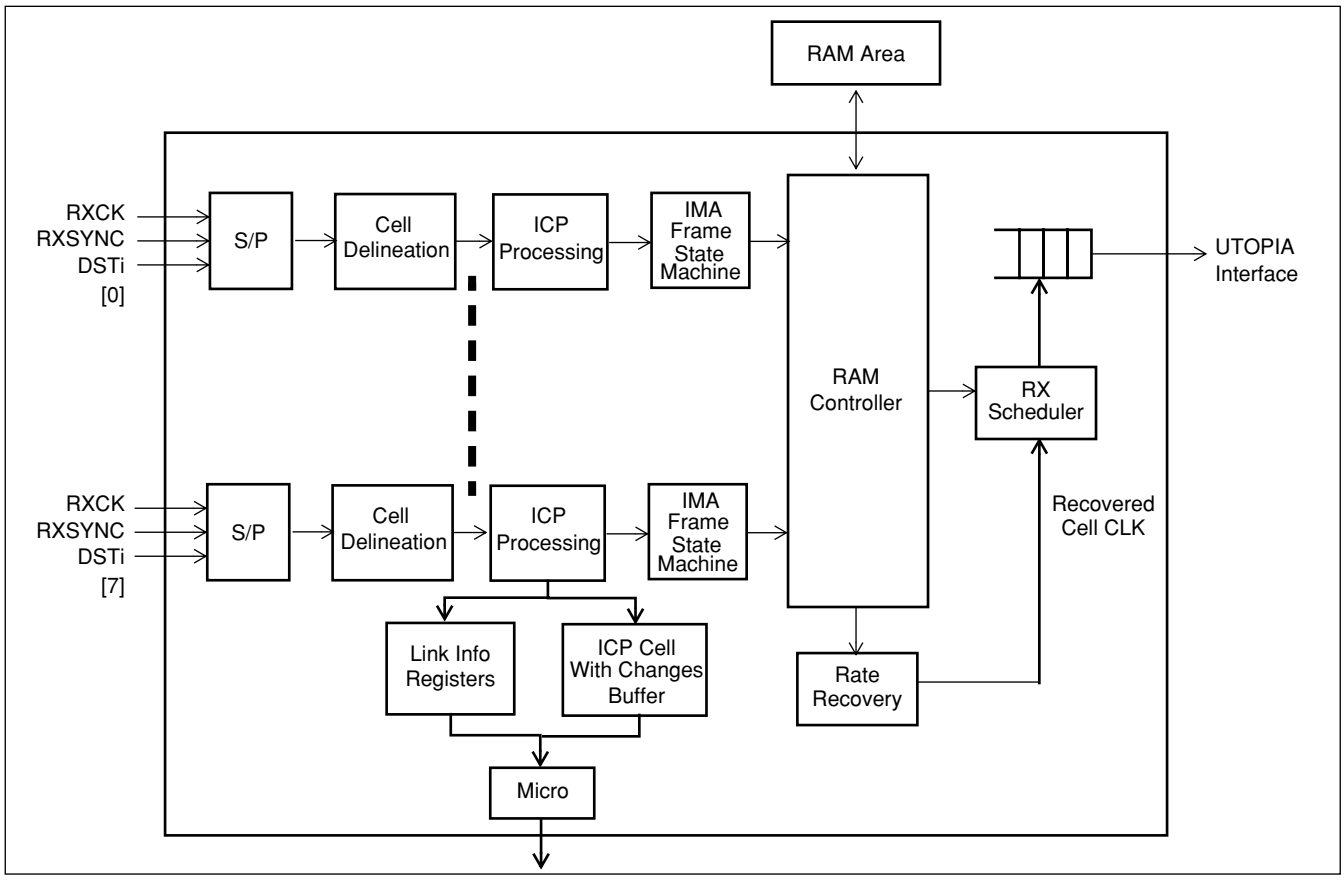


Figure 7 - The MT90220 Receiver Circuit in IMA Mode

3.3.1 ICP Cell Processor

In IMA mode, the transmitter inserts special ICP cells in the various outgoing streams every M ATM cells to comply with the IMA specification. The receive block is using these ICP cells to synchronize with the Far End transmit side and to reconstruct the ATM cell original sequence.

3.3.1.1 IMA Frame Synchronization

The MT90220 implements IMA Frame Synchronization State Machines (IFSM) for each link, as described in Section 11 of the IMA Specification. The values of Alpha, Beta and Gamma are programmable through the **Frame Delineation** register. Their values are the same for all links.

After the link is programmed to be in IMA mode by writing to the **RX Link Control** register, the IMA Frame State Machine is enabled. At the same time, the parameter's value of the RX link are latched in internal reference registers and are used to determine if the received ICP cell meets the valid ICP cell criteria to determine IMA frame synchronization. Refer to section 3.3.1.2 and 3.3.1.3 for the list of link's parameters.

Incoming ICP cells are automatically detected by the ICP Processing block. As soon as one valid ICP cell is received, the IMA Frame State Machine moves to the IMA PRESYNC state. When Gamma-valid ICP cells are received, the state machine moves to the IMA SYNC state. In the IMA PRESYNC state, one errored or missing ICP cell causes the state machine to return to the IMA HUNT state. In the IMA SYNC state, the state machine is forced to the IMA HUNT state by any of the following events:

- one missing ICP cell
- Alpha consecutive invalid ICP cells
- Beta consecutive errored ICP cells

Bits 3 and 2 of the **RX State** register report the IMA Frame State Machine state for a selected link. When in IMA HUNT mode, the information required to perform the verification is extracted from the ICP cells received.

After the received information is validated, the IMA Group is configured by writing to the **RX Reference Link Control**, the **RX Link Control** and **RX Recombiner** registers.

3.3.1.2 Link Information

All required verification and link validation information is extracted from the ICP received cells. The IMA ID, Link ID (LID), Reference Link Number, ICP Cell Offset and Frame Length can be read and validated before enabling an IMA Group link. Software obtains this information by writing to the **RX Load Values** register to select a link and by reading the **RX Link IMA ID**, **RX Link ICP Offset**, **RX Link ID and Reference** and **RX State** registers. This information can also be obtained by collecting all the received ICP cells in the RX ICP Cell Buffer and then processing the content of the ICP cell (i.e., writing to the **RX ICP Cell Type RAM** register and then reading from the RX ICP cell buffer).

The contents of the link information registers should be read after enabling the RX PCM link in the **RX PCM Link Control** register and before enabling the IMA mode. The link information can be accessed when a link is either in UNI or IMA mode.

3.3.1.3 RX OAM Label

The RX OAM Label is treated differently than the other link's parameters. Four registers, the **RX OAM Label** registers, 1 per RX IMA Group, are used to defined the RX OAM Label. Its value is written by the software and can be changed at any point in time. However, the RX OAM Label has to match the value contained in the RX ICP cell for the IMA Frame State Machine to reach the ACTIVE state.

3.3.2 Out of IMA Frame (OIF) Condition

Status bits in the **RX OIF Status** register, one bit per link, is reporting OIF conditions. The status bit is latching an OIF condition which corresponds to a transition of the IFSM from SYNC to HUNT. The OIF condition is reported as a status bit only and cannot generate an interrupt. The status bit is cleared by writing a 0 to the corresponding bit.

There are 8 OIF counters, one per link. For each OIF transition, the 8-bit counter associated with the link is incremented by one. The counter can be read with indirect access when issuing a load command with the **RX Load Values** register. The counter can be cleared by writing to the **RX OIF Counter Clear Command** register.

3.3.3 Link Out Of IMA Frame (LIF) Synchronization

A link is declared out of IMA Frame (LIF) synchronization state when the IFSM goes in HUNT mode for 'gamma +2' frames after it was in SYNC state. This condition is latched in bit 2 of the **IRQ Link Status** register. Refer to 6.2.2 IRQ Link Status and IRQ Link Enable Registers for more details.

The LIF status bit is reporting the current condition of the IMA Frame State Machine at the time it is read and cannot not be programmed to generate an interrupt when exiting the LIF condition. The software has to poll the LIF status bit to determine when the condition is cleared.

3.3.4 Filler Cell Handling

The MT90220 scans each incoming cell received for the Filler Cell Indication code. Filler cells are written to external RAM to keep the IMA frame aligned. They are automatically discarded after being read from the external RAM by the recombiner.

3.3.5 Stuff Cell Handling

Each incoming ICP cell received is scanned for the Stuff Indication Code. Stuff cells are inserted at the transmit end as two identical and consecutive ICP cells with the Link Stuff Indication Bits set as defined in the IMA specification. The MT90220 automatically discards one of the two Stuff cells without storing it in external RAM. The other is kept and processed as a regular ICP cell. IMA Frame synchronization is maintained for all cases (except case 7, O-19 optional requirements) as described in Figure 20 of the IMA Specification.

3.3.6 Received ICP Cell Buffer

An internal buffer is implemented to collect cells from the RX PCM links for analysis by the software. This storage unit is a circular buffer for each link and contains up to three cells per link. The buffer can selectively collect:

- all valid cells coming on a RX PCM port
- all valid ICP cells
- all valid ICP cells which contain new information (as indicated by the SCCI field, valid only when the link is in IMA mode).

The type of cells collected is defined in the **RX ICP Cell Type RAM** registers. A status bit and a maskable IRQ alerts the software when a new cell is waiting for processing in a specific link. These are found in the **IRQ Link Status** and **Enable** registers. Valid ICP cells when a link is in UNI mode is determined by a valid HEC byte. When in IMA mode, a valid ICP cell must meet the criteria defined in Table 16 of the ATM IMA spec.

Software can directly access the cells in the RX buffer through a two-cell-wide access window. This access window can be advanced, one cell at a time, by issuing a command to move the internal pointer to the next cells. Since the window accesses two cells,

the last processed cell can be accessed at the window's base address and the new cell at the base address plus 0x40.

The **RX ICP Cell Level FIFO** register is used to read the level of any of the 8 RX ICP Cell buffers. A '0' in this register signifies that no new cell has been received. A '2' indicates the possibility that one or more cells have been missed (overflow condition).

The cell in the last entry of the circular buffer is the last cell that was meeting the selection criteria. If the Cell FIFO level is 2, it is constantly overwritten by any new valid incoming cell.

The cell that is at the window's base address when the level is 0 is never overwritten as it is kept for reference.

The **RX ICP Cell Buffer Increment Read Pointer** register is used to advance the access window by 1 cell at a time. Upon the command, the Buffer level is decreased by 1. When the level reaches 0, the window is not advanced anymore.

During the start-up phase, the software can select to collect all valid ICP cells coming in a RX PCM port and determine if the parameters are acceptable to proceed and start-up an IMA group.

In normal IMA operating mode, the software will select to collect only valid ICP with changes. The Status and Control Change Indication (SCCI) is monitored for all valid ICP cells received. If the SCCI field indicates a change in the ICP cells, they are put aside for processing by software.

To accelerate the processing of ICP cells that contain changes, any byte of the last and next processed ICP cell can be accessed directly. To reduce the total processing time by the software, only those bytes that need to be read are accessed. The storage unit keeps the last read ICP cell and has room for up to three new ICP cells.

3.3.7 Rate Recovery

The MT90220 computes the internal RX IMA Data Cell Rate (IDCR) for each IMA Group. The cell rate of the reference link is integrated over a programmable period of time. Software must specify the reference link for the IMA Group in the **RX Reference Link Control** register and the period of integration in the **RX IDCR Integration** register. Refer to TX IMA Data Cell Rate in Section 2.4.5.

As an option, the reference link can be extracted automatically from the received ICP cell. This option is selected by bit 4 of the **RX Reference Link Control** registers. When this option is enabled, the **RX Reference Link** is always updated to reflect the content of the last valid RXICP cell that was received.

3.3.8 Cell Buffer/RAM Controller

The received cells are temporarily stored in external memory buffers until they can be correctly re-ordered for output. Memory size depends on the number of links and the maximum delay allowed between the links. The memory requirements for different configurations is listed in Table 4. The memory is organized in blocks of 64 bytes. Each block can hold one cell. The following equation can be used to determine the maximum delay value or the required RAM size for a determined delay:

Memory Size (Kbytes)	Delay (msec)	
	T1 links	E1 links
32Kb	16	13
64Kb	34	27
128Kb	69	55
256Kb	140	112
512Kb	281	225
1024Kb	560	451
Note: Assuming a Guardband of 4 cells		

Table 4 - Differential Delay for Various Memory Configuration

$$MaxDelay = \frac{[RAMsize]}{64}\left[\frac{1}{8}\right][1CellTime]$$

To simplify the RAM interface and pin loading, the MT90220 supports the following six, **SRAM Control** register selectable, external memory configurations:

- one 32 KByte SRAM device
- two 32 KByte SRAM devices
- one 128 KByte SRAM device
- two 128 KByte SRAM devices
- one 512 KBytes SRAM
- two 512 KBytes SRAM devices.

To enable the correct memory access, the **Test Mode Enable** register bit 7 has to be set to 1, the value 0x10 should be written to the **RX Delay Link Number** register, the bit 3 of the **RX External SRAM Control** register has to be set to 1 and the bit 6 of **Test 2** register has to be set to 1.

3.3.9 Cell Sequence Recovery

When an IMA Group is active, the IMA recombiner manages the pointers to the external RAM write and read location for the stored ATM cells. A cell is read out from the buffer located in the external RAM corresponding to the lowest link ID (LID) of the IMA Group and placed in the RX UTOPIA FIFO. After a

complete cell read, a read pointer is set to the buffer corresponding to the next LID. At the following IDCR clock cycle, the next available cell is read. ICP cells are skipped and Filler cells are discarded. This operation is done in a RoundRobin fashion based on the LID value for each IMA Group link. Faulty conditions (i.e., buffer overflow, excessive delay) are reported through the **IRQ Link Status** and **IRQ UTOPIA Status** registers.

3.3.10 Delay Between Links

The delay values between links are reflecting the various transit delays though the network. In order to rebuild the original ATM cell sequence, the link that exhibits less transport delay has to be stored until the data from the slowest link (link having the largest transport delay) has arrived. The link that exhibits the largest transport delay will be the link that requires the least cells to be stored. Conversely, the line that exhibits the least transport delay is the link that requires the largest number of cells to be stored.

Indirect access is provided to internal registers which hold the various link delay values. The link number and delay type are first selected by writing to the **RX Delay Select** register. After 2 system clock cycles, the 14-bit value in the **RX Delay MSB** and **LSB** and the **RX Delay Link Number** registers are updated and can be read. The valid delay types are: the **Maximum Delay over Time**, **the Current Maximum Delay** and **the Current Minimum Delay** for an IMA group and the **Current Delay** values for any links.

The delay values can be converted to time values by multiplying the number of cells by the conversion factor listed in the Table 5.

Link Type	Time per cell (msec)
T1 ISDN (23 ch. per frame)	0.288
T1 (24 ch. per frame)	0.276
E1 (30 ch. per frame)	0.221

Table 5 - Conversion Factors Time/Cell (msec)

3.3.10.1 RX Recombiner Delay Value

The ICP Cell from each link of the same IMA Group is used to determine the external SRAM read and write pointers. The distance between the read and write pointers is referred to as the recombiner delay. Setting the recombiner delay to the maximum acceptable delay results in a fixed recombiner delay that is not optimum. For example, setting recombiner delay to 25 msec when the worst case delay is 12 msec results in an additional, unnecessary delay of 13 msec.

The minimum recombiner delay would be the current worst case differential delay. In the example above, the recombiner delay would be set to 12 msec. In this case, a link with larger transport delay than the current worst value cannot be added to an existing IMA group: the cells from this slower link have not arrived when the cells sequence is rebuilt, as the read pointer was set using the previous worst case link. If this slower link is to be added, then the recombiner process has to stop for the time required to receive the cells on the slower link and then the recombiner process can resume. This causes disruption in the operation of the recombiner and will affect the Cell Delay Variation (CDV).

To provide an optimal recombiner delay, the MT90220 adds a guardband delay to the current worst case recombination delay when the IMA Group is first started up. Guardband delay is programmable and minimizes the number of disruptions that would otherwise occur in accommodating link delays exceeding the current worst case. The guardband delay is added to the minimum recombiner delay, when the recombiner process is enabled for the first link of an IMA group. The operational delay corresponds to the guardband delay added to the current worst case delay value.

The guardband delay value is specified for each IMA group by writing to the **Guardband/Delta Delay** register. It should be the smallest value possible consistent with minimizing the disruptions and the smallest allowed value is 4. When operational, the value of the guardband delay corresponds to the delay value of the link having the greater transport delay (the link where the data is the last to arrive to the MT90220).

3.3.10.2 RX Maximum Operational Delay Value

The various delays on links of the same IMA Group are measured and compared to the programmed 'maximum allowable value' stored in the **RX Maximum Operational Delay** register for the IMA Group. This value corresponds to the worst delay value that is expected. This value cannot be larger than the number of cells that can be stored in the external memory. The smallest 'maximum allowable value' is four cells. These values are independently established for each of the four IMA Groups.

3.3.10.3 Link Out of Delay Synchronization (LODS)

If a link to be added is slower and cannot be accommodated by the present guardband, an LODS signal is generated and the link delay value is reported negative. A delay is negative when the 2 most significant bits are set to "1". The value reported is with respect to the read pointer and

represents the minimum number of cells that has to be added to the present guardband before adding the link in the IMA group. See paragraph 3.3.10.6 Incrementing/Decrementing the Recombiner Delay for more details.

If a link to be added is faster and would cause its write pointer to be set beyond the **RX Maximum operational Delay** programmed value, then the link is reported to be faulty through an LODS condition. The recombination process will not be affected as long as the amount of delay is not larger than the total number of cells in the external memory.

LODS will also be reported if, during operation, the delay of a link is changing to exhibits higher or lower delay which result in a negative delay value or beyond the RX Maximum Operating Delay value.

LODS events are reported by the **IRQ Link Status** register and the selected **Current Maximum Delay** register for an IMA Group.

3.3.10.4 Negative Delay Values

If the recombiner process is enabled for a link that is exhibiting a negative delay value then the recombiner process will be suspended until the write pointers are moved in such a way that the delay is reported with a positive value of 4. At this time, the recombiner process will resume. No cells are lost. The same behavior applies if the delay value of a link which is part of the round robin process (recombiner bit ON) goes negative: the recombiner process will be suspended until the delay value becomes positive with a value of 4. The latter condition can happen under severe error conditions if the recombiner process of the faulty link is not disabled.

3.3.10.5 Measured Delay Between Links

The values and delay type for a selected link(s) or IMA Group can be read using the **RX Delay Select** register.

IMA Group delay types include: the **Maximum Delay over time**; the **Current Maximum Delay** and the **Current Minimum Delay** of an IMA Group. **Current Link Delay** reports the **Current Delay** of a link. These values are all reported through a common **RX Delay** register. The value is in number of cells. All the delay values include the guardband delay value. The **RX Delay Link Number** register is reporting the link number associated with the delay value that is currently in the **RX Delay** registers, with the exception for the Maximum Delay over time value, where the link number reported is not valid (reports value of 0).

The **Maximum Delay over time** value can be reset at any time by writing a clear command to bit 5 in the **RX Delay Select** register. The differential delays can be easily obtained by subtracting the delay values of the links.

3.3.10.6 Incrementing/Decrementing the Recombiner Delay

If a link to be added has a delay value which falls beyond the worst current delay value, then there are 2 options: either reject the link or re-adjust the pointers. To readjust the pointers, the number of cells to be added (delta) is specified and corresponds to the amount of extra delay to be added to the current recombination delay. The additional delay is first programmed in the **Guardband**/**Delta Delay** register and then a command to increase the delay is issued (using the **Increment**/**Decrement Delay Control** register). The MT90220 device stops the recombiner process for the amount of time specified and then resumes the recombiner process. No cells are lost but there is an effect on the CDV. The increment process is completed when the control bit in the **Increment**/**Decrement Delay Control** register is returned to a 0 value.

If the link exhibiting the longest transmission delay is removed, the recombiner delay can be reduced accordingly. When such a correction occurs, the number of cells corresponding to the delay correction will be lost. To reduce the impact of this correction, its implementation can either be immediate or delayed. The **Increment**/**Decrement Delay Control** register is used for this purpose. The amount of delay to be removed (i.e., number of cells) in the recombiner process is controlled by the **Guardband**/**Delta Delay** register. Alternatively, the links can all be placed in blocking mode for the transition period to avoid losing any cells.

If a decrement delay command is issued which would result in a negative delay value on one or more links, the following action will take place: the read pointer is re-adjusted as required by the decrease delay command and since the delay is negative, the recombiner process is suspended until the delay on all the link are at least reaching a positive value of 4. Then, the recombiner process will resume.

3.3.11 RX IMA Group Start-Up

A quick initialization sequence for the RX IMA Group could be as follows (default values can be used for some registers).

(Note: The startup procedure below is given indicating the most important steps. A more detailed and complete sequence can be found in the

MT90220/221 Programmer's Manual and example code).

- Configure the SRAM parameters using the **SRAM Control, RX External SRAM Control** and **Test Mode Enable** registers
- Configure the Cell delineation and IMA Frame State Machines parameters by writing to the **Cell Delineation, Loss Cell Delineation** and **IMA Frame Delineation** registers
- Write to the **RX Link Control** register to select the RX options
- Configure the RX PCM port(s) by writing to the **RX PCM Link Control** register
- Configure the RX UTOPIA port by writing to the **UTOPIA Output Group PHY Enable** and **UTOPIA OutputGroup Address** registers
- Validate the IMA parameter values received over the PCM links and configure the link in IMA mode using the **RX Recombiner** and the **RX Link Control** register
- When ready, start the recombiner process by writing to the **RX Recombiner** register

3.3.12 Link Addition

The MT90220 supports software controlled link addition to the existing RX link group. Such an addition can be used to increase available bandwidth. The added link receives Filler cells until the Far End (FE) TX side is active. During this time, the new link's delay is measured and compared with the current operating limits. The link is either rejected or accepted. The operational delay can be corrected if required as described in 3.3.10.6 Incrementing/ Decrementing the Recombiner Delay. After synchronization is achieved, the added link can be included in the recombiner algorithm using bit 2 of the **RX Recombiner** register. The link will be effectively included in the IMA Group when the corresponding bit in the **Enable Recombination Status** register is set.

A link may also be added to an IMA Group when the first User cell is received. This is done by writing to the **RX Recombiner Delay Control** register.

3.3.13 Link Deletion

There are two reasons to deactivate a link:

- the bandwidth required decreases or
- an existing link becomes faulty.

Both link deactivation procedures specified in the IMA specification are supported under the control of software.

The command to disable the recombination process for a link is issued by writing to bit 2 of the **RX Recombiner** register.

If the delay of the link to be removed is not the worst delay, then no pointer correction is required and the recombiner bit (i.e., bit 2 of **RX Recombiner** register) for the removed link should be set to 0.

If it is the worst case delay, then the pointer values should be corrected to reduce the amount of additional delay introduced by the recombiner. The pointers need to be changed (advanced). This results in reducing the number of cells (the amount of time) required for the recombiner process.

To reduce the impact of this correction, its implementation can either be immediate or delayed. A command in the **Increment/Decrement Delay Control** register is used for this purpose (refer to 3.3.10.6 Incrementing/Decerementing the Recombiner Delay, for more details).

3.3.14 Disabling an IMA Group

Before an IMA Group can be disabled, the software should ensure that no User cells are left in memory. As part of the higher level handshaking, the TX FE should have sent Filler cells for a while for the RX side to process all the User cells that could be in the external memory.

The procedure to follow is to stop the recombination process and then, wait for the enable process to be reported inactive (in the **Enable Recombination Status** register) before re-assigning the link to another IMA group or to UNI Mode.

3.4 The ATM Receive Path in UNI

Up to eight incoming T1/E1 lines can be connected to the MT90220 receiver and forwarded to the UTOPIA L2 interface served by an external ATM-Layer device. Figure 8 illustrates four of the eight possible UTOPIA ports that can be addressed through the UTOPIA Interface.

The size of the RX UTOPIA FIFO is fixed. The Idle cells are automatically removed at the RX PCM block and all other valid received cells are transferred to the RX UTOPIA FIFO.

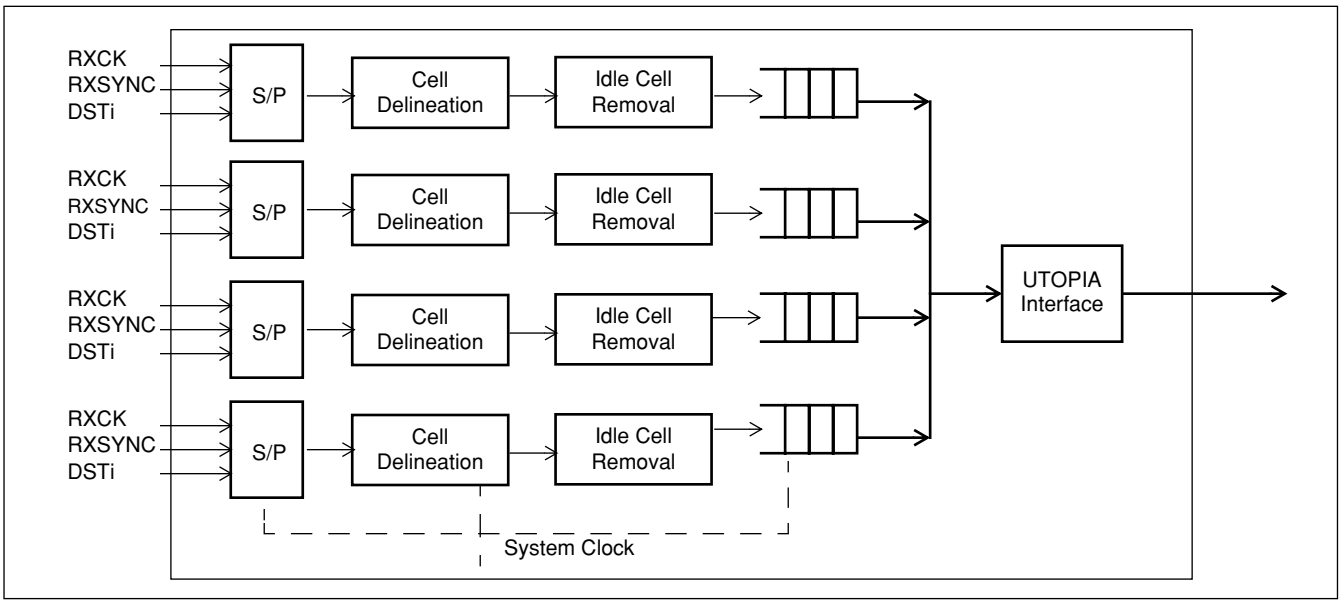


Figure 8 - Example of UNI Mode Operation
(Using Four of Eight Possible UTOPIA-Output Ports)

4.0 Description of the PCM Interface

To provide support for the IMA Asymmetrical mode, the Transmit PCM blocks are independent from the Receive PCM blocks. The TX port of a framer can be connected to any of the MT90220 TX UTOPIA Input ports and the RX port of a framer can be connected to any of the MT90220 RX UTOPIA Output ports.

4.1 Serial to Parallel (S/P) and Parallel to Serial (P/S) Converters

Each T1/E1 link has a S/P and P/S unit assigned. The P/S unit takes a byte from the cell RAM and converts it to a serial bit stream. The S/P unit takes a byte from the DSTi input and converts it to parallel format for use by the Cell Delineation block.

The system interface supports both the ST-BUS (2.048 Mbps bus) and generic PCM Interface. Note that the ST-BUS is compatible with the so-called MVIP mode that is supported by some T1 or E1 framer manufacturers.

The MT90220 generates and receives the PCM channels only (24 or 23 with T1, 30 with E1). The control/status channels of the framers and the signaling channels are *not supported by the MT90220.*

P/S and S/P units can be set-up differently on a per port and per direction basis (i.e. the transmit and receive function of the same port can use different configurations). The following features are supported:

- programming links as T1 or E1
- using ST-BUS and Generic PCM modes
- enabling/disabling the P/S and S/P units (if they are disabled the associated outputs are Tri-stated)
- mapping T1 links, on a per port and per direction basis, to use either the first 24 channels or 3 of every 4 channels (when ST-BUS or 2.048 clock modes are selected)
- programming T1 links to ignore timeslot 24 and reserve it for signaling (since only 23 timeslots are used to carry the ATM cells, this option should be applied to all links of the same IMA Group)
- independently programming the polarity of RXCK, TXCK, RXSYNC and TXSYNC signals (Generic PCM mode only)
- generating/accepting TXSYNC and TXCLK signals to support most T1 and E1 framers (depending on the programmed mode)
- monitoring RXSYNC signal period and reporting the unexpected occurrence of a synchronization signal (see 4.3.1 Verification of the RXSYNC Period, for more details)
- monitoring TXSYNC signal period (when defined as input) and reporting the unexpected occurrence of a synchronization signal (see 4.3.2 Verification of the TXSYNC Period, for more details)
- generating a TXSYNC pulse on every PCM frame when defined as output
- assigning any TX or RX link to any IMA Group

When the TXCK and TXSYNC signals are outputs, the source for the TXCLK is software selectable from any of the eight RXCK inputs or any of the four external REFCKs. The TXSYNC signal is generated

from the TXCK and is independent from (not aligned with) the RXSYNC or other TXSYNC signals.

4.2 PCM System Interface Modes

There are 8 major modes of operation for the PCM interface. The only difference between modes 1 to 4 and modes 5 to 8 is in the direction of the TXCK and TXSYNC signals. In the PCM modes 5 to 8, the direction is the opposite of what is defined in modes 1 to 4. The direction of the TXCK and TXSYNC signals is defined by the bit 4 in the **TX PCM Link Control Register #2** and the PCM mode is defined in the **TX PCM Link Control Register #1**

- Mode 1: Generic PCM interface for T1 applications, TXCK and TXSYNC outputs
- Mode 2: ST-BUS interface for T1 applications, TXCK and TXSYNC inputs
- Mode 3: Generic PCM interface for E1 applications, TXCK and TXSYNC outputs
- Mode 4: ST-BUS interface for E1 applications, TXCK and TXSYNC inputs
- Mode 5: Generic PCM interface for T1 applications, TXCK and TXSYNC inputs
- Mode 6: ST-BUS interface for T1 applications, TXCK and TXSYNC outputs
- Mode 7: Generic PCM interface for E1 applications, TXCK and TXSYNC inputs
- Mode 8: ST-BUS interface for E1 applications, TXCK and TXSYNC outputs

T1 with ISDN services operation is available in PCM Modes 1, 2, 5 and 6. Channel 24 is not used to carry the ATM cells and is reserved for signaling. In this case, 23 channels are used to carry the ATM cells over the links and all the links in the IMA Group must have the same option selected. The signaling channel is always channel 24 in the T1 frame and its position will vary with the PCM frame length.

In PCM Mode 1 and 5, the clock can be either 1.544 or 2.048 MHz. If a 2.048 MHz clock is selected, the mapping of the 24 channels can be either grouped (the first 24 consecutive timeslots starting with the Frame Pulse) or spaced (3 of every 4 timeslots, starting with the second timeslot of the 32 timeslot frame).

In PCM Modes 1, 3, 5 and 7, polarity of clock and synchronization signals (TXCK, TX SYNC, RXCK and RX SYNC) can be set as either positive or negative. In the ST-BUS mode 2, 4, 6 and 8, the

PCM Major Modes	TX PCM Control Registers 1 & 2			Description		
	Reg 1 bit 6	Reg 1 bit 5	Reg 2 bit 4	E1/T1	ST-BUS/ Generic	TXCK/TXSYNC (Input/Output)
Mode 1	0	0	0	T1	Generic	Output
Mode 2	0	1	0	T1	ST-BUS	Input
Mode 3	1	0	0	E1	Generic	Output
Mode 4	1	1	0	E1	ST-BUS	Input
Mode 5	0	0	1	T1	Generic	Input
Mode 6	0	1	1	T1	ST-BUS	Output
Mode 7	1	0	1	E1	Generic	Input
Mode 8	1	1	1	E1	ST-BUS	Output

Table 6 - PCM Modes

PCM Mode	ST-BUS			GENERIC			
Clock Frequency	4.096 MHz			1.544MHz	2.048 MHz		
Mapping	Grouped[a]	Spaced[b]	Fixed[c]	Fixed	Grouped	Spaced	Fixed
T1 ISDN (23 channels)	Yes	Yes	--	Yes	Yes	Yes	--
T1 Clear Channel (24 channels)	Yes	Yes	--	Yes	Yes	Yes	--
E1 (30 channels)	--	--	Yes	--	--	--	Yes

Table 7 - PCM Clock and Mapping Options

a. "Grouped" corresponds to the use of the first 23 or 24 channels (timeslots) from the 32 timeslots available in a frame.
b. "Spaced" corresponds to the use of 3 channels every 4 channels (timeslots) from the 32 timeslots available in a frame.
c. "Fixed" corresponds to the use of channels 1-15 and 17-31 leaving channels (timeslots) 0 and 16 not used.

clock and frame pulse are fixed and must conform to the ST-BUS specification.

The RXCK and RXSYNC pins are always defined as inputs and are generated by external circuitry.

4.2.1 Mode 2 and 6: ST-BUS Interface for T1

In PCM Mode 2 the TXCK and TXSYNC pins are defined as Inputs and in PCM Mode 6, the TXCK and TXSYNC are defined as outputs. The RXCK and RXSYNC are always defined as input pins.

In T1 applications, a DS-1 frame is 193 bits long and corresponds to 1 framing bit and 192 payload bits. The 192 payload bits are divided as 24 channels or time slots of 8 bits each.

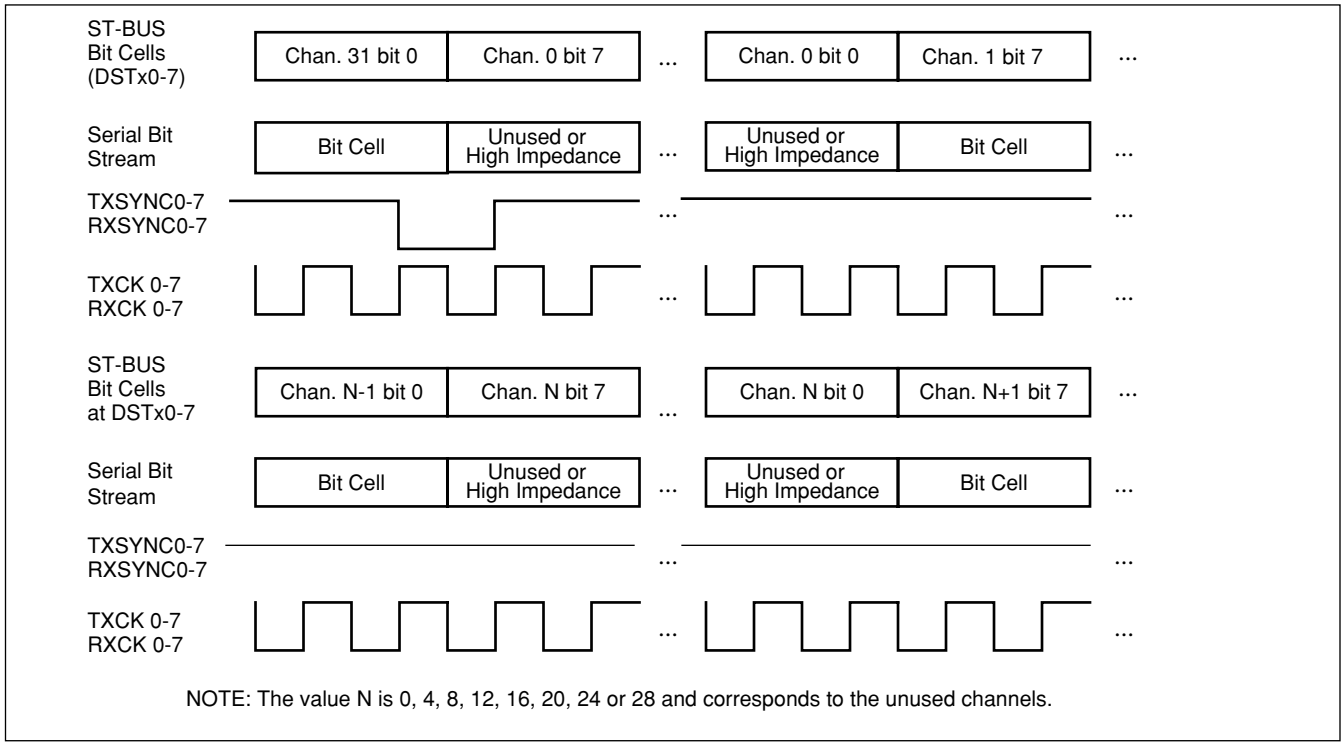
The Zarlink ST-BUS has 32 channels numbered 0 to 31. Two different mapping schemes are selectable. The spaced mapping scheme uses 3 of every 4 channels. The grouped scheme uses the first 24 channels. Refer to Table 8 for details of Spaced DS-1 mapping, Table 9 for Grouped DS1 mapping. All unused channels are tri-state.

The Zarlink ST-BUS clock value is 4.096 MHz. The frame pulse is 8 kHz and should be as defined in Figure 9 or Figure 10 (see Zarlink Application Note MSAN-126).

In the PCM Mode 6, the TXCK and TXSYNC pins are defined as outputs. The source for the TXCK is selected using **TX PCM Link Control** register number 2 and can be any of the eight RXCK or four external REFCK clocks. As there is no PLL inside the MT90220, the source frequency has to be a valid ST-

DS1 Time slots	-	1	2	3	-	4	5	6	-	7	8	9	-	10	11	12
Voice/Data Channels (DSTi/o) ST-BUS	0x	1	2	3	4x	5	6	7	8x	9	10	11	12x	13	14	15
DS1 Time slots	-	13	14	15	-	16	17	18	-	19	20	21	-	22	23	24
Voice/Data Channels (DSTi/o) ST-BUS	16x	17	18	19	20x	21	22	23	24x	25	26	27	28x	29	30	31

Table 8 - T1Channel Mapping Using 3 Channels Every 4 Channels



NOTE: The value N is 0, 4, 8, 12, 16, 20, 24 or 28 and corresponds to the unused channels.

Figure 9 - PCM Mode 2 and 6: ST-BUS Interface for T1 (Spaced Mapping)

DS1 Time slots	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Voice/Data Channels (DSTi/o) ST-BUS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DS1 Time slots	17	18	19	20	21	22	23	24	-	-	-	-	-	-	-	-
Voice/Data Channels (DSTi/o) ST-BUS	16	17	18	19	20	21	22	23	24x	25x	26x	27x	28x	29x	30x	31x

Table 9 - T1 Channel Mapping Using 24 Consecutive Channels

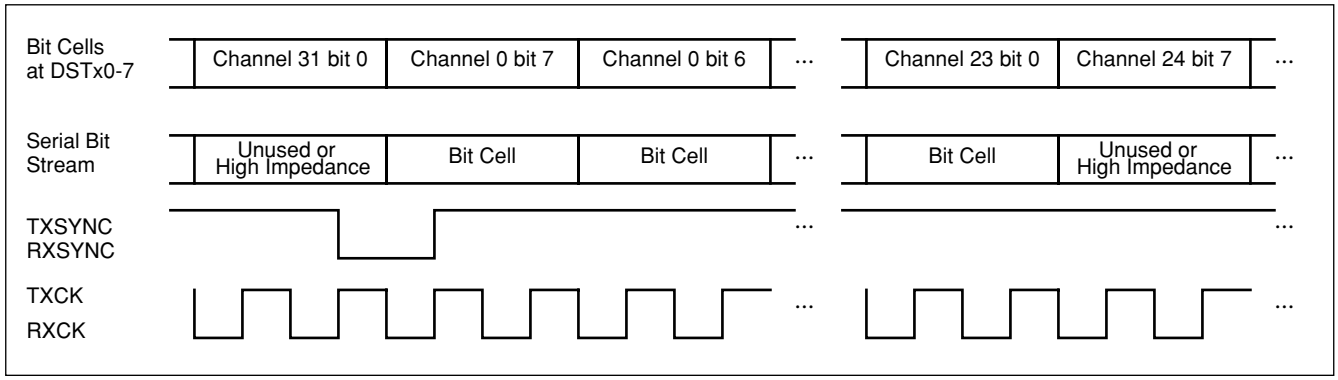


Figure 10 - PCM Mode 2 and 6: ST-BUS Interface for T1 (Grouped Mapping)

BUS Clock signal (i.e., 4.096 MHz). The TXSYNC signal is generated by the MT90220 and meets the ST-BUS format. It is not synchronized with any other RXSYNC or TXSYNC signal.

4.2.1.1 Detailed ST-BUS Spaced Mapping (3 of Every 4 Channels)

DS1 (T1) links contain 24 bytes of serial voice/data channels distributed over the 32 ST-BUS channels. One mapping option uses 3 of every 4 channels. The channels 0, 4, 8, 12, 16, 20, 24 and 28 of the ST-BUS are not used. The MT90220 tri-states the DSTo lines during the unused time-slots. See Figure 9.

4.2.1.2 Detailed ST-BUS Grouped Mapping (24 Consecutive Channels)

In this option, the 24 bytes of serial voice/data channels of the DS-1 use the first 24 consecutive channels over the 32 ST-BUS channels. The MT90220 tri-states the DSTo lines for the unused channels (25 - 31). Refer to Table 9.

4.2.1.3 Detailed ST-BUS ISDN Mapping (T1 ISDN Modes)

When the T1 ISDN modes are selected, channel 24 is not used to carry bytes from ATM cells. This byte is not used in the receive direction. In the transmit direction it is set to a high impedance state. The ST-BUS mapping is identical as in the T1 (DS1) 'clear channel' set-up except for the last channel of the T1 (DS1) frame. This last channel is reserved for signaling.

4.2.2 Mode 4 and 8: ST-BUS Interface for E1

The Zarlink ST-BUS has 32 channels, numbered 0 to 31. The PCM-30 payload is mapped to 30 of the 32 ST-BUS timeslots. Channels 0 and 16 are used for framing and signaling information. See Figure 11 and Table 10.

In E1 PCM Modes 4 and 8, the Zarlink ST-BUS clock value is 4.096 MHz. The frame pulse is 8 kHz and should be as defined in Figure 11.

In PCM Mode 4, the TXCK and TXSYNC pins are defined as inputs and are generated by external circuitry. In the PCM Mode 8, the TXCK and TXSYNC pins are defined as outputs. The source for the TXCK is selected using **TX PCM Link Control** register number 2 and can be any of the eight RXCK or four external REFCK clocks. As there is no PLL inside the MT90220, the source frequency has to be a valid ST-BUS Clock signal (i.e., 4.096 MHz). The TXSYNC signal is generated by the MT90220 and meets the ST-BUS format. It is not synchronized with any other RXSYNC or TXSYNC signal.

4.2.3 Mode 1 and 5: Generic PCM Interface for T1

In PCM Modes 1 and 5, the TXCK clock frequency can be either 1.544 or 2.048 MHz. In the PCM Mode

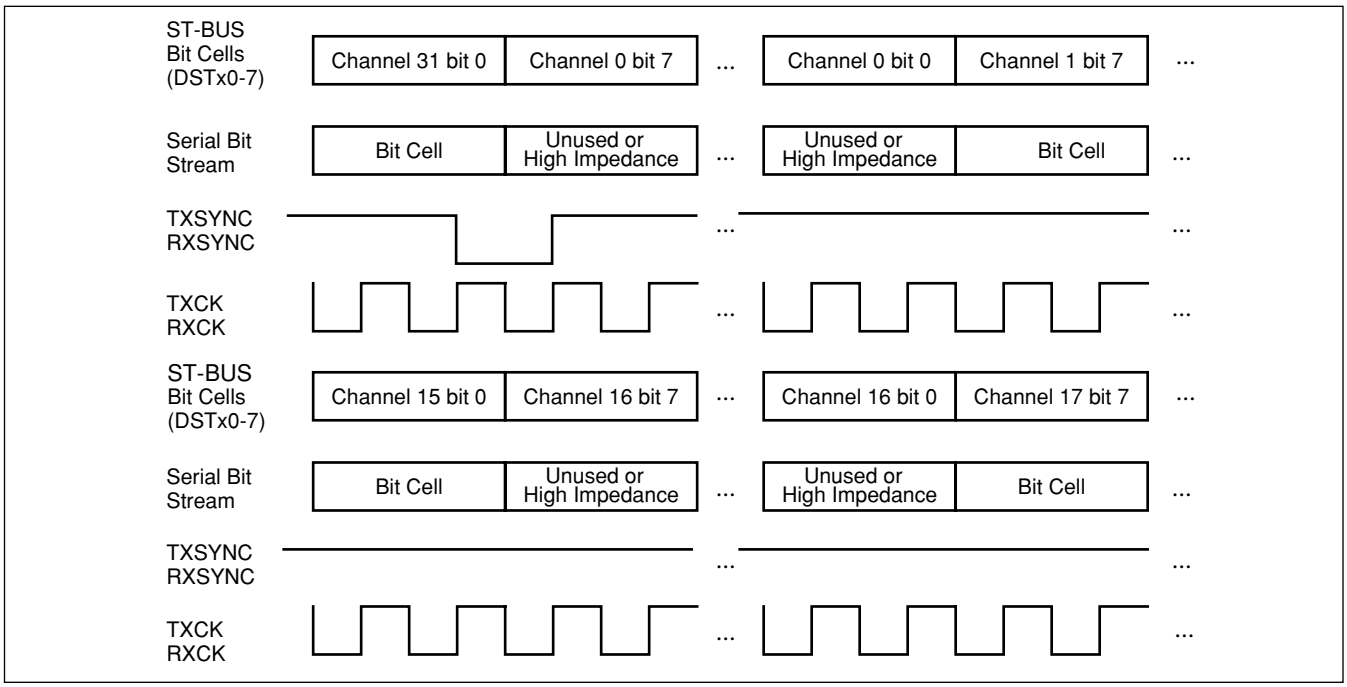


Figure 11 - PCM Mode 4 and 8: ST-BUS Interface for E1

E1 Time-Slots	-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Voice/Data Channels (DSTi/o)	0x	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
E1 Time-Slots	-	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Voice/Data Channels (DSTi/o)	16x	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Table 10 - Channel Mapping from ST-BUS to E1

1, the TXCK and TXSYNC pins are outputs. In the PCM Mode 5, the TXCK and TXSYNC pins are defined as inputs.

4.2.3.1 1.544 MHz Clock

In this sub-mode, (selected by clearing the bit 4 of the TX PCM Control Register 1,) the serial PCM Interface rate is equal to the line bit rate. When selected to operate in this sub-mode, the interface clock is 1.544 MHz and the DSTo and DSTi the data lines transport only 24 time-slots plus the DS1 framing bit for a total of 193 bits per frame.

The frequency value for TXSYNC and RXSYNC is 8 kHz. The frequency for the TXCK and RXCK is 1.544 Mhz.

The edge of the RXCK and TXCK signals used to sample incoming data and transmit the outgoing data is fully programmable on a per link basis. This allows the MT90220 to operate with the majority of available off-the-shelf T1 framers.

When operating in the generic PCM system Interface at 1.544 MHz, the MT90220 does not use the first bit of the PCM frame (i.e., the T1 framing bit) to perform the G.804 recommended transmission convergence function (see Figure 12). This frame bit is also ignored on the receive side. The position of the frame bit is indicated by the TXSYNC and RXSYNC signals.

4.2.3.2 2.048 MHz Clock

In this sub-mode (selected by setting the bit 4 of the TX PCM Control Register 1) the channel/timeslot mapping for this mode is similar to the ST-BUS mode for T1. The same PCM mapping schemes (grouped or spaced) are supported. The TXCLK and RXCLK are 2.048 MHz signal and the TXSYNC and RXSYNC are a frame pulse of one full bit duration that occurs at the beginning of the frame. The frame rate is 8 KHz. The polarity of the TXCK, RXCK, TXSYNC and RXSYNC and their active edge is programmable using **TX PCM Link Control** register number 1 and **RX PCM Link Control** register.

4.2.4 Mode 3 and 7: Generic PCM Interface for E1

The channel/timeslot mapping in this mode is similar to the ST-BUS mode for E1. The differences are:

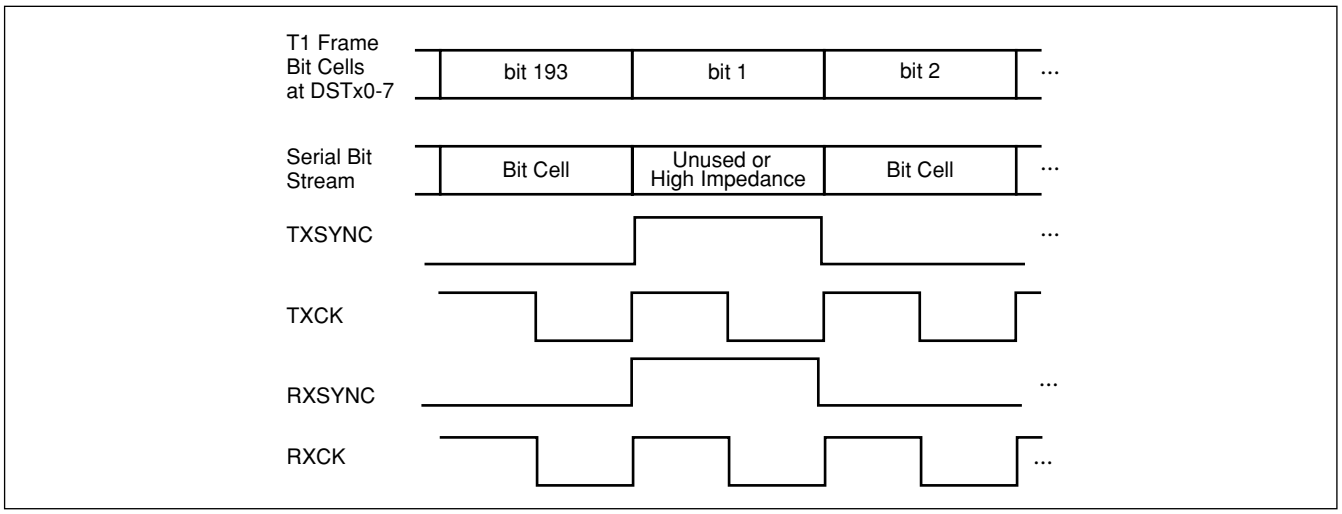


Figure 12 - Mode 1 and 5: Generic PCM Interface for T1

- the interface clocks (RXCK and TXCK) operate at 2.048 MHz only
- the synchronization signals (TXSYNC and RXSYNC) are valid for one clock cycle (488 nsec) during the first bit of the frame
- In PCM Mode 3, the TXCK and TXSYNC pins are defined as outputs.
- In PCM Mode 7, the TXCK and TXSYNC are defined as inputs.

The edge of the RXCK and TXCK signals that is used to sample the incoming, and transmit the outgoing, data is fully programmable on a per link basis. This allows the MT90220 to operate with the majority of off-the-shelf E1 framers.

The MT90220 does not use timeslots 0 and 16 to perform the G.804 transmission convergence function (see Figure 13).

4.2.5 TXSYNC Signal in Mode 5 and 7

The TXSYNC signal is defined as an input in PCM mode 5 and 7 and is sampled at the bit boundary. A positive delay of 10 nsec is expected between the TXCLK signal at the bit boundary and the time the TXSYNC changes. This may cause some inter-operability problems when the MT90220 is connected to some off-the-shelf framers as the TXSYNC can be slightly ahead of the TXCLK signal. In this case, the TXSYNC signal need to be delayed to ensure proper operation of the TX PCM port.

4.3 Clocking Options

In PCM Modes 2, 4, 5 and 7, the TXCK and TXSYNC are inputs and are generated by external circuitry.

In PCM Modes 1, 3, 6 and 8, the TXCK and TXSYNC are outputs. TXCK source is software selectable and can be any of the eight RXCK signals or four external REFCK inputs (see Figure 14). The TXSYNC is generated from the TXCK signal.

The RXCK pins are always defined as inputs and the proper signal must be provided to each input.

4.3.1 Verification of the RXSYNC Period

The RXSYNC signal is used to align the incoming DSTi data to retrieve all the T1 or E1 channels. The RXSYNC pulse can be present for each PCM frame (8Khz) or once per Superframe (every 12 or 24 PCM frames). The period and position of the RXSYNC is verified for each receive block independently. A status bit (1 per link) in the **RX Sync Status** register is set if the synchronization pulse occurs at an unexpected time in the frame. The RX block will be re-aligned with this new synchronization pulse.

4.3.2 Verification of the TXSYNC Period

The TXSYNC signal is used to align the outgoing DSTo data to retrieve all the T1 or E1 channels. When defined as input, the TXSYNC pulse can be present for each PCM frame (8Khz) or once per Superframe (every 12 or 24 PCM frames). The period and position of the TXSYNC is verified for each transmit block independently. A status bit (1 per link) in the **TX Sync Status** register is set if the synchronization pulse occurs at an unexpected time in the frame. The TX block will be re-aligned with this new synchronization pulse.

4.3.3 Primary and Secondary Reference Signals

Two output pins are provided to simplify the external circuitry required when using an external PLL. These two pins, PLLREF0 and PLLREF1, re-route any of the eight RXCK signals and drive the primary and secondary reference signals of a PLL under software

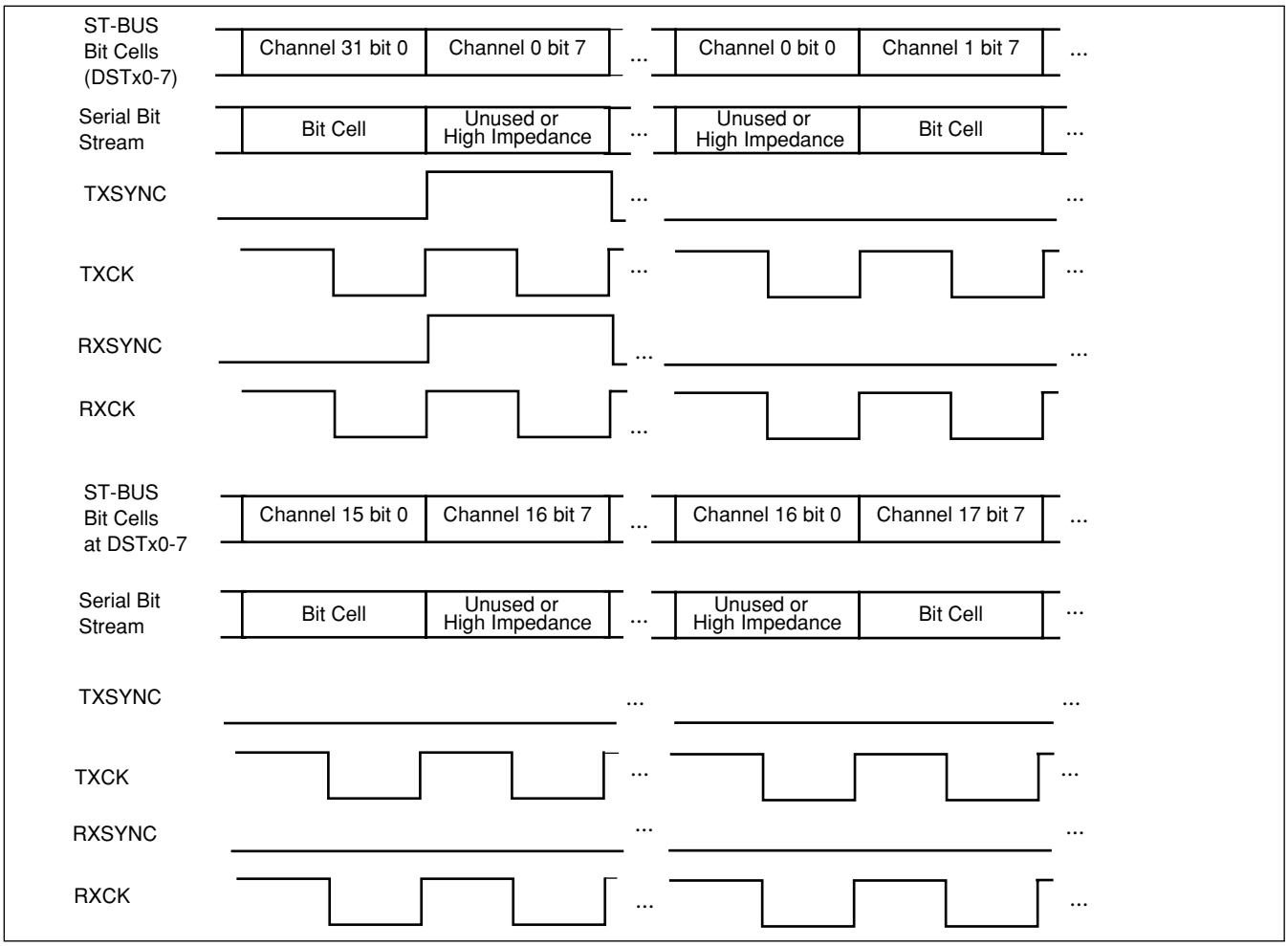


Figure 13 - Mode 3 and 7: Generic PCM Interface for E1

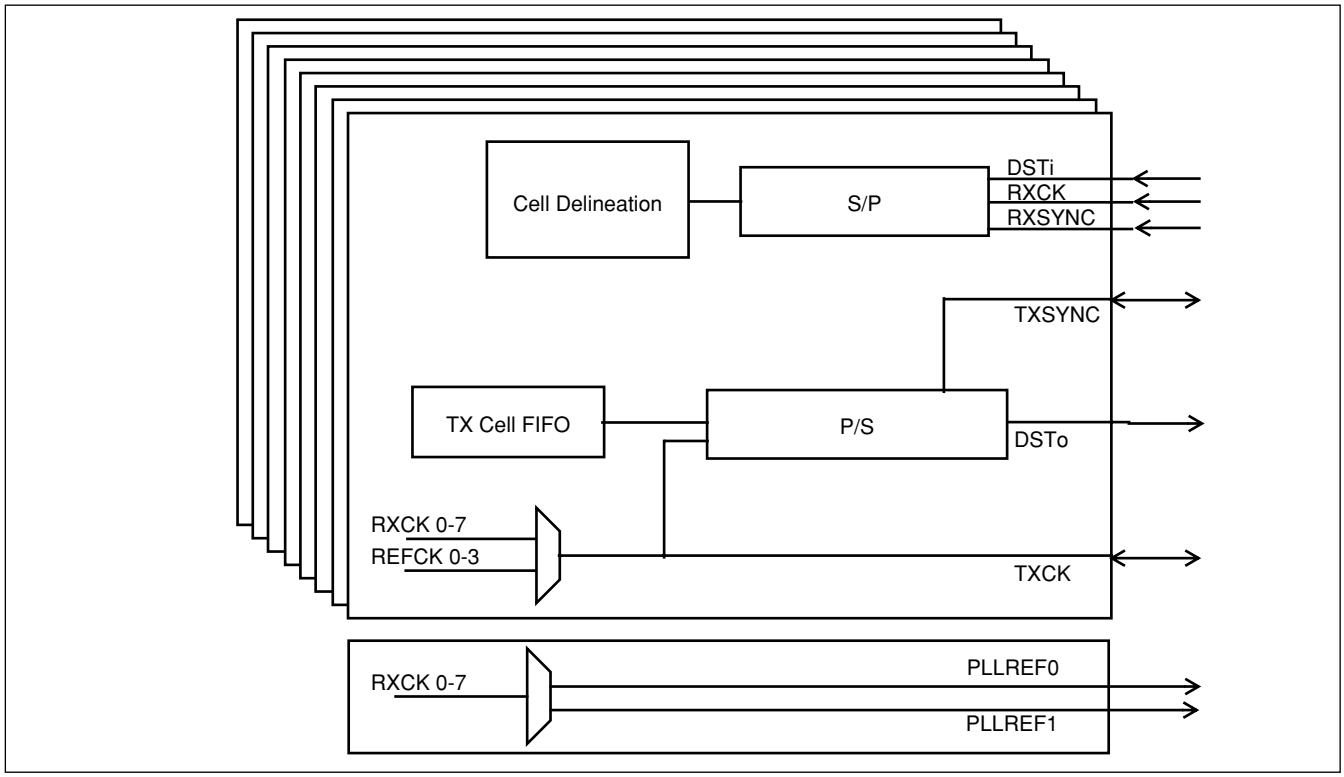


Figure 14 - TXCK and TXSYNC Output Pin Source Options

control. Refer to Section 8, Application Notes, for examples.

4.3.4 Verification of Clock Activity

The MT90220 implements circuitry to determine whether or not a selected clock signal is active. This feature is used to ensure a clock is operational before using it as a source for one or more transmit links. The identity of the clock source to be verified is written to the **Clock Activity** register. A read of the same register indicates clock activity if bit 7 is '1'. A value of '0' for bit 7 means that no transition was observed on this clock. This circuitry does not measure the frequency of a clock signal, it only detects activity on the eight RXCK, eight TXCK and four REFCK signals.

4.3.5 Clock Selection

In normal operation, the clock selection circuitry selects the desired clock signal and ensures a smooth, glitch free, transition between the current clock source and the new clock source.

However, if the current clock source is inactive (i.e., no clock transitions), the clock select circuitry must be reset before another clock can be used as reference. Clock select circuitry is reset by writing a 1 to bit 7 of the **PLL Reference Control** register. Clock source activity can be verified using the **Clock Activity** register as described in 4.3.4 Verification of Clock Activity.

5.0 UTOPIA Interface Operation

The MT90220 supports the UTOPIA L2 Mode for cell level handshake only. Each port can be assigned an address ranging from 0 to 30. The address value of 31 is reserved and should not be used for any MT90220 port.

The TX and RX paths of each IMA Group and each link in UNI has its own PHY address. These PHY addresses are defined in the **UTOPIA Input link Address** registers 1 to 8, **UTOPIA Input Group Address** register 1 to 4, **UTOPIA Output link Address** registers 1 to 8, and the **UTOPIA Output Group Address** registers 1 to 4. The **UTOPIA Input LINK PHY Enable** and the **UTOPIA Output Link PHY Enable** registers are used to enable the **PHY Address** of the links in UNI. The **UTOPIA Input Group PHY Enable** register and the **UTOPIA Output Group PHY Enable** registers are used to enable the PHY Address of the IMA Groups.

The MT90220 port uses handshaking signals to process data streams. The start of a cell (SOC) is marked by the UTOPIA SOC sync signal. This signal is active during the transfer of the first byte of a cell. The 52 bytes that follow the arrival of the first byte of a cell are interpreted as belonging to the same cell and are stored accordingly (note that SOC sync signals received during the loading of these 52 bytes are ignored).

The cell available satus line (Clav) is used to communicate to the ATM controller if the MT90220 has space for a cell in the PHY address that was polled in the previous cycle. Whenever there is space for a cell in teh TX direction or a cell ready in the RX direction, the TXClav and/or RXClav signal will be driven High or Low. When the address does not correspond to any enabled PHY address inside the MT90220, the TXClav and RXClav signal are in High impedance mode. The use of an external pull-down may be required for the proper operation of the Utopia bus in MPHY mode.

It should be noted that the bit 6 and 5 of the **Test 1** register have to be set to 1 for the proper operation of the RX Utopia port in MPHY mode.

5.1 ATM Input Port

The UTOPIA interface input clock TxClk is independent of the system clock. The UTOPIA TxClk can be up to 25MHz. The incoming cell is stored directly in the internal TX Cell RAM where the TX UTOPIA FIFOs are implemented.

The TX byte clock (TxClk) can be up to 25 MHz and is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 2 of the **General Status** register will be set. This bit is cleared by overwriting it with 0.

The total space for the UTOPIA input cells for all IMA Groups and links in UNI mode is 58. These 58 cells are shared between 12 TX UTOPIA FIFOs and 8 TX Link FIFOs. The size (length) of each TX UTOPIA FIFO is defined by writing to the **TX UTOPIA FIFO Length Definition** registers. The maximum value is 15 and the minimum value is 0 (in the case the PHY port is not to be used). The size of the TX Link FIFO is defined on a per group using the TX IMA Control registers.

The device will not accept a cell from the UTOPIA Interface if the internal Cell Ram is full. Status bit 0 in the **General Status** register is set to 1 to indicate the 'no free cell in TX Cell RAM' condition. The status bit can be cleared by overwriting it with 0.

The UTOPIA Input block has the option to verify the HEC of the cell coming from the ATM layer. Four

different options are available and are selected by bit 1 and 0 of the **UTOPIA Input Control** register.

- The ’00’ option is used to always accept a cell from the ATM layer. The HEC is verified and if wrong, the UTOPIA Input counter associated with the UTOPIA port for cells with bad HEC is incremented. The MT90220 will re-generate a valid HEC based on the content of the 4-byte header that was received.
- The ’01’ option is used to verify the HEC of an incoming cell. If the HEC value is wrong and if it can be corrected (1 bit error), then the cell is corrected and accepted as a good cell. The bad HEC counter is not incremented if the HEC is corrected. The bad HEC counter is incremented if the HEC value cannot be corrected. In this mode, the cell is always accepted. The MT90220 will re-generate a valid HEC based on the content of the 4-byte header that was received.
- The ’10’ option is used to verify the HEC on the incoming cell and discard the cell if the HEC value is wrong. The bad HEC counter is incremented if a cell is discarded.
- The ’11’ option is similar to mode ’01’ except that if the HEC value cannot be corrected, then the cell is discarded. If the HEC value is corrected, the bad HEC counter is not incremented.

5.2 ATM Output Port

The MT90220 supports a 53 byte cell stream via the ATM output port. Cells received at the ATM output port are stored in the RX UTOPIA FIFO before being processed by the UTOPIA Interface. The output of the UTOPIA Interface can be stopped by the ATM Layer device by de-asserting the $\overline{\text{RxEnb}}$* signal.

The start of a cell is marked with the SOC signal, which is active during the transmission of the first byte of a cell. The following 52 bytes are expected to belong to the same cell.

The RX byte clock (RxClk) can be up to 25 MHz and is checked against the system clock. If the incoming byte clock frequency is lower than 1/128 of the system clock, bit 3 of the **General Status** register will be set. This bit is cleared by overwriting it with 0.The RxClk signal has to be synchronized with the System Clock for the proper operation of the MT90220. Typically, both frequencies are equal but the RxClk frequency can be lower.

Overflow conditions in the RX UTOPIA FIFO associated with any of the 12 PHY RX Addresses cause a status bit to be set in either the **IRQ UTOPIA UNI Overflow Status** or **IRQ IMA Group Overflow Status** register. These status bits are cleared by overwriting them with 0. Additionally, for each status bit there is an Interrupt Enable bit in the associated **RX UTOPIA Link FIFO Overflow Enable** or **RX UTOPIA IMA Group FIFO Overflow Enable** register. When enabled, the status bit is reported in an Interrupt register. See 6.2 Interrupt Block for more details.

The size of the RX UTOPIA FIFO is fixed at two cells for the UNI PHY Addresses and four cells for the IMA Group PHY Addresses.

5.3 UTOPIA Operation With a Single PHY

A single ATM layer device with a UTOPIA L2 MPHY port can be connected to the ATM input port of one MT90220. Another ATM-Layer device using the UTOPIA L2 MPHY input interface is used to receive ATM cells from the MT90220.

The address pins should be set to the value programmed by the management interface.

In this mode, the bit 6 and 5 of the **Test 1** register are not to be set to 1 for the proper operation of the RX Utopia port.

5.4 UTOPIA Operation with Multiple PHY

When more than one MT90220 are connected to a single ATM Layer device the single TxClav and RxClav scheme is used. Direct Status Indication and Multiplexed Status Polling schemes are not supported. The necessary polling is performed by the ATM-Layer device.

The UTOPIA Interface transmit and receive addresses, provided by the ATM-Layer device, are used to de-multiplex the ATM-cell stream to as many as eight MT90220s. The maximum available bandwidth for eight E1 lines served by each MT90220 device is 2 MBytes/s.

5.5 UTOPIA Operation in UNI Mode

In UNI Mode, each Utopia port inside an MT90220 corresponds to a physical T1 or E1 line. Up to eight PHY ports can be supported by one MT90220. Up to eight MT90220 can be connected to a UTOPIA bus. The ports in the same device represent only one electrical load on the UTOPIA bus. The UTOPIA Interface supports up to 31 PHY addresses so a maximum of 31 PHY addresses are supported by the MT90220.

The MPHY address at the input port of MT90220 (TxAddr[4:0]) is used to store the cell in one specific TX UTOPIA FIFO.

The MPHY address at the output port (RxAddr[4:0]) is used to retrieve the cells from the proper RX UTOPIA FIFO.

5.6 UTOPIA Operation in IMA Mode

In IMA mode, up to eight MT90220s, with up to four UTOPIA ports each (one port per IMA Group), can be served by an external UTOPIA L2 ATM-Layer device. This provides up to 31 different logical IMA-channels. Note that port 31 (1F in hexadecimal format) is reserved.

5.7 Examples of UTOPIA Operation Modes

Figure 15 shows the connection of one ATM Device with one MT90220.

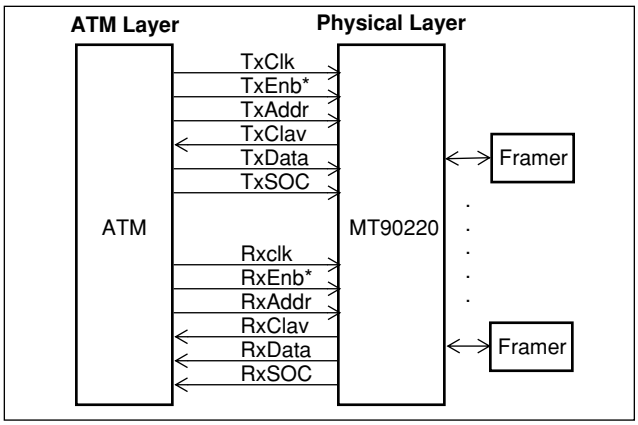


Figure 15 - ATM Interface to MT90220

Figure 16 shows the connection of one ATM Device with more than one MT90220.

Figure 17 illustrates the implementation of a mixed mode using only 1 MT90220. Links that are not used for IMA Groups are available in UNI mode. Unused links are programmed to set their outputs to high impedance mode.

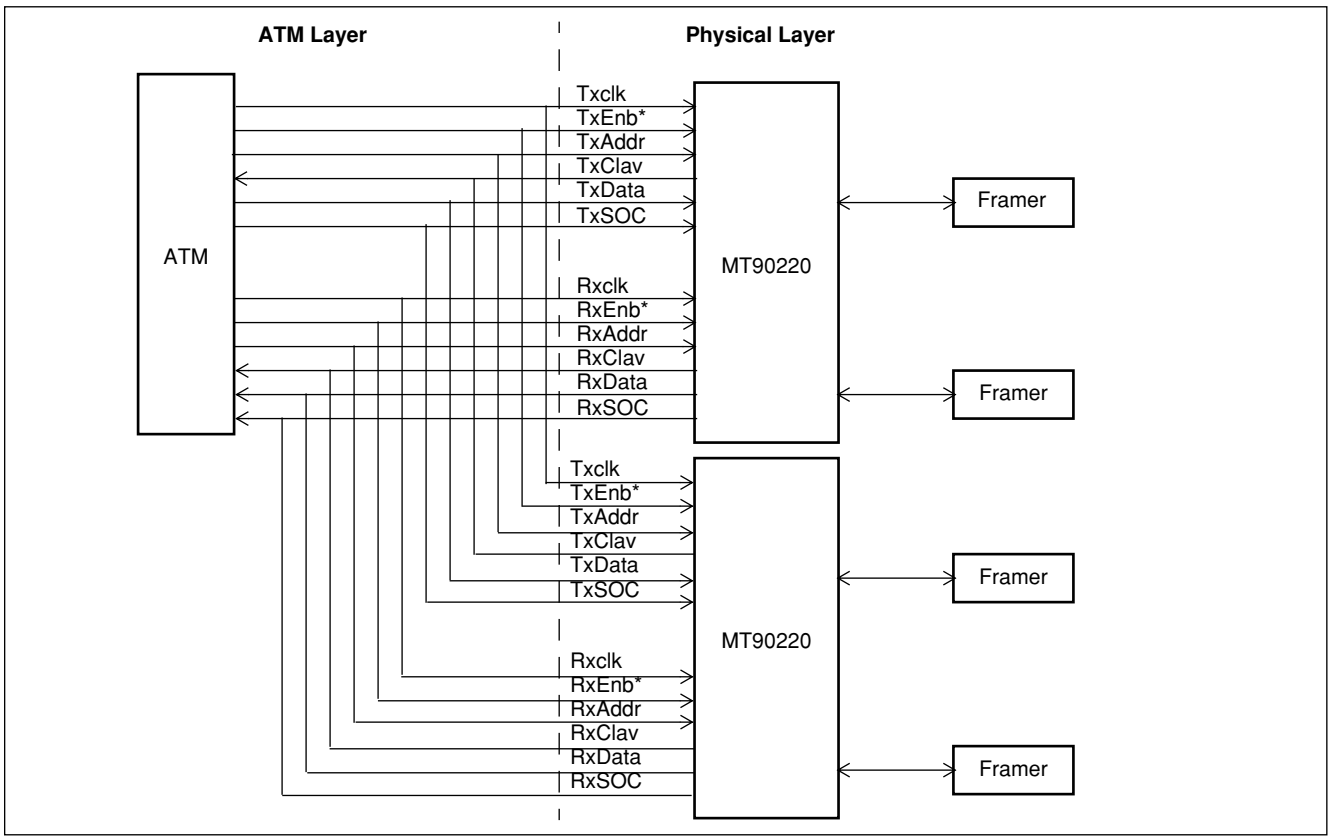


Figure 16 - ATM Interface to Multiple MT90220s

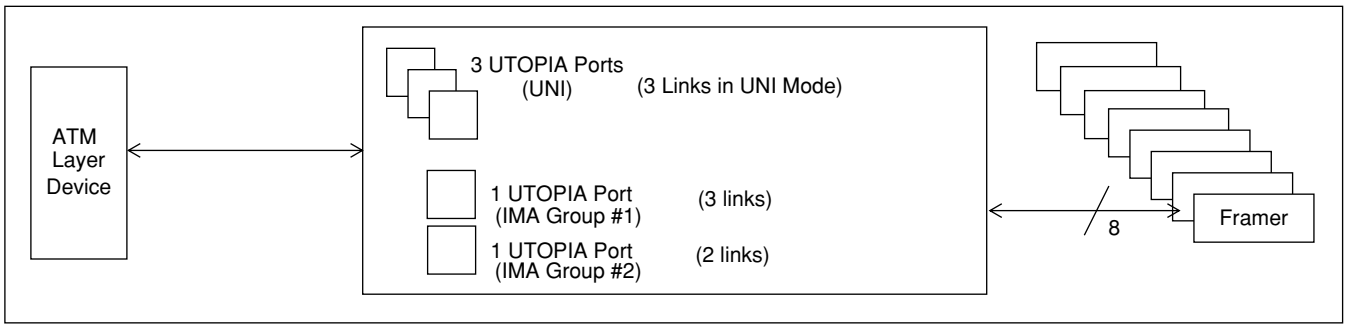


Figure 17 - ATM Mixed-Mode Interface to One MT90220

6.0 Support Blocks

6.1 Counter Block

The MT90220 includes 112 24-bit counters to provide statistical information on the device's operation. All the counters are cleared by a hardware reset. A maskable interrupt can be generated when the counter overflows.

A predetermined value can also be loaded in a counter. This feature can be used to generate an interrupt after a specified number of cells is processed. Counter values are incremented by 1 for every event occurrence and, when the count goes to all 1's, will overflow (to all 0's).

6.1.1 UTOPIA Input I/F counters

There are four counters associated with the each of the 12 UTOPIA Inputs (from ATM layer to the MT90220) for a total of 48 counters. These counters record the following information:

- the total number of cells received at the UTOPIA Input I/F
- the total number of Idle Cells received at the UTOPIA Input I/F, removed or not
- the total number of Unassigned Cells received at the UTOPIA Input I/F, removed or not
- the number of cells having a single or multiple bit error in the HEC, removed or not but not including the cells where the HEC is corrected

6.1.2 Transmit PCM I/F Counters

There are four counters associated with the each of the eight transmit PCM links for a total of 32 Transmit counters. These counters record the following information:

- the total number of cells sent through the PCM link
- the total number of Idle/Filler cells sent through the PCM link
- the total number of Stuff cells sent through the PCM link
- the total number of ICP cells sent through the PCM link

6.1.3 Receive PCM I/F Counters

There are four counters associated with each of the eight receive PCM links for a total of 32 Receive counters. These counters record the following information and are active as soon as the RX PCM port is enabled:

- the total number of cells received through the PCM link or total number of Stuff events received on the link (option selected in **RX Link Control** registers)
- the total number of Idle/Filler cells received through the PCM link, , with good or bad HEC
- the total number of ICP Cells with violation received through the PCM link
- the total number of cells with wrong HEC received through the PCM link but not including the cells where the HEC is corrected

6.1.4 Access to the Counters

Accessing (READ) counters is a three step function. First, the desired counter must be selected by writing to the **Counter Select Register**. Second, the READ command ('0x00x101') is written to the **Counter Transfer Command** register. This command causes the current three byte count value to be copied from the specified counter to the three byte-wide **Counter Bytes** registers (note that this value is unchanged until another counter read command is issued). And third, the **Counter Bytes** registers are read to obtain the three byte count value of the selected counter.

Pre-loading (WRITE) a counter is also a three step function. First, the three byte, pre-load value, is written to the three byte-wide **Counter Bytes** registers. Second, the identification of the counter to be pre-loaded is written to the **Counter Select Register**. And third, the WRITE command ('0x00x001') is written to the **Counter transfer Command** register.

The IRQ enable bit of a counter is set, or reset, by selecting the counter and writing to the appropriate bit of the **Counter Transfer Command** register. The value '0x001010' enables the counter IRQ and 'xxx00010' disables (masks) it.

6.2 Interrupt Block

The MT90220 can generate interrupts from many sources. All interrupt sources can be enabled or disabled. Write action is required to clear the source of interrupt. Interrupts are grouped on a per link basis, with six sub-categories for each link and two special types for the IMA Group configuration. These special interrupts are only present in the Link 0 IRQ Status register. Refer to Figure 18 for a representation of the interrupt register hierarchy.

6.2.1 IRQ Master Status and IRQ Master Enable Registers

There is a **Master IRQ Status** register that reports interrupts generated by any event on any of the eight links. Each bit of this register corresponds to a link. A '1' in a bit position indicates that the associated link is reporting an interrupt condition. For each bit in the **IRQ Master Status** register, there is a corresponding bit in the **IRQ Master Enable** register. When any IRQ source is active and the corresponding Enable bit is '1', then the $\overline{\text{IRQ}}$ pin will go LOW (active).

The **IRQ Master Status** register always reports the current state of the source(s) of interrupt. It does not latch the interrupt request(s); it only reports that one or more bit(s) in one or more **IRQ Link Status** register(s) is (are) set.

The bits that are read as active ('1' value) are cleared when the source of the interrupt is cleared or when the corresponding bit(s) in the **IRQ Link Enable** register(s) is (are) set to 0. Writing to or reading from the **IRQ Master Status** register has no effect on the level of the interrupt pin.

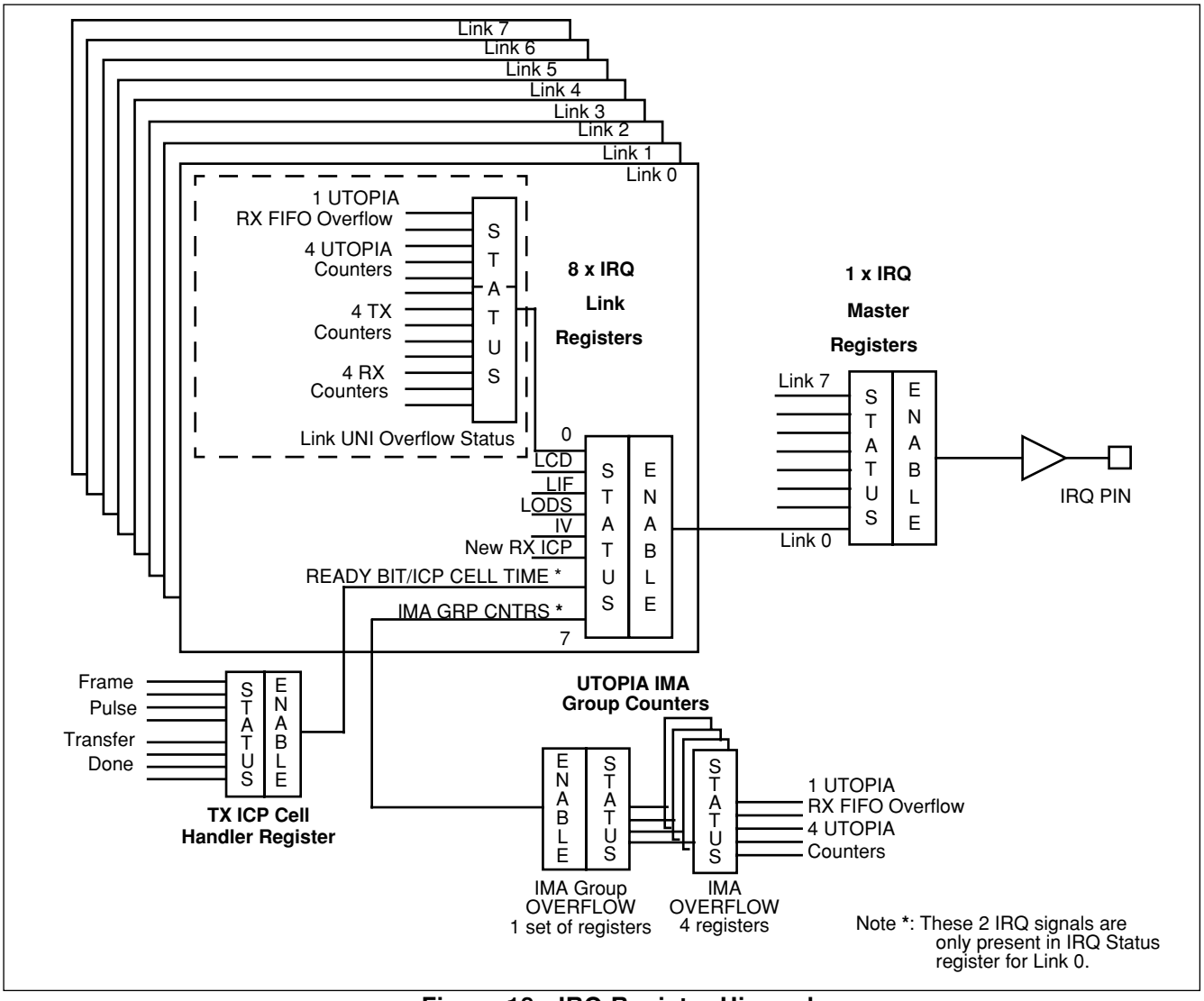


Figure 18 - IRQ Register Hierarchy

6.2.2 IRQ Link Status and IRQ Link Enable Registers

There are eight **IRQ Link Status** and eight **IRQ Link Enable** registers; one of each per link. The following six types of interrupts are reported (in the six least significant bits of the **IRQ Link Status** registers) for each link:

- Bit 5 latched: reports that an ICP Cell with changes was received on a RX PCM link.
- Bit 4 latched: reports an IV (ICP Cell violation) condition on a RX PCM link.
- Bit 3 latched: reports an LODS (Link is Out of Delay Synchronization) condition on a RX PCM link.
- Bit 2 latched: reports an LIF (Loss of IMA Frame) condition on a RX PCM link.
- Bit 1 latched: reports an LCD (Loss of Cell Delineation) condition on a RX PCM link.

Bit 0 (LSB) is a status bit. It reports an interrupt for an overflow condition in one or more of the 12 counters associated with the link. It is also used to report an overflow condition in the UTOPIA RX FIFO associated with a PCM link in UNI mode. If enabled, a counter generates an interrupt request when it overflows (i.e starts over from 0 after reaching the maximum counter value). 6.1 Counter Block paragraph for more details on the operation of the counters. These 13 sources of overflow can be identified through the **IRQ Link FIFO Overflow** and **IRQ UTOPIA FIFO Overflow** status registers. Refer to section 6.2.3 IRQ Link UNI Overflow and IRQ UTOPIA Input UNI Overflow Status Registers for more details.

Reading the **IRQ Link Status** register does not clear the source of interrupt. The bit 0 status is reset by any one of the following procedures:

- disabling (masking) the IRQ for this specific counter
- clearing the overflow status bit in the **IRQ Link UNI Overflow** and **IRQ UTOPIA UNI Overflow Status** registers
- disabling the interrupt in the **RX UTOPIA Link FIFO Overflow Enable** or in the corresponding Link (in UNI mode) Counter registers.

Bits 1, 2, 3, 4 and 5 of the **IRQ Link Status** register are latches that report the source of an interrupt. Writing a '0' these bits will reset the status bit (will reset the latch). Writing '0' to bit 0 has no effect on the status bit.

Writing a '1' has no effect on the bits 0 to 5 of the **IRQ Link Status** register.

Each one of these six interrupt sources can be enabled by writing a '1' in the **IRQ Link Enable** register to the bit corresponding to the interrupt source.

In some situations, an interrupt source can be masked as part of an interrupt service routine. This makes it possible to detect further interrupts of higher priority. For example, if an interrupt for a counter is received, the source of the interrupt can be masked by writing 0 to the bit 0 and then starting a separate process, outside of the Interrupt Service Routine. The independent process would read, reload and re-enable the counter to produce another interrupt service request, if necessary. At the end of this process, the enable bit in the **IRQ Link Enable** register would be set to '1' to detect any future interrupt requests.

6.2.2.1 Bit 7 and 6 of IRQ Link 0 Status and IRQ Link 0 Enable Registers

Bits 7 (MSB) and 6 of the **IRQ Link 0 Status** register have a special meaning.

Bit 7 reports an overflow condition in any of the counters or UTOPIA RX FIFOs associated with one of the four IMA Groups. Refer to 6.2.4 IRQ IMA Group Overflow Status and Enable Registers for more details. Bit 7 is a status bit and is cleared by disabling the IRQ for this specific counter or disabling (masking) the FIFO overflow condition by writing to the **RX UTOPIA IMA Group FIFO Overflow Enable** register.

Bit 6 is used to report the following two event types:

- the ICP cell internal transfer is complete (reported by any IMA Group TX ICP Cell Ready bit)
- the end of an IMA frame on the reference link of an IMA Group

The second type of event assists in implementing the software counter required to verify that Group Status and Control field information is sent for at least 2 consecutive IMA frames.

The eight interrupt sources are enabled independently by writing to the **TX ICP Cell Handler Enable** register.

There is also an associated Control/Status register (**TX ICP Cell Handler** register) that reports the interrupt source and the state of the transfer of an ICP Cell or the occurrence of the end of an IMA frame. The Frame status bits are cleared by writing 0 to the bit. The Ready bit is set to 1 when the transfer is complete. Bit 6 is a latched bit in the **IRQ Link 0 Status** register and is cleared by overwriting it with 0.

Each of these two interrupt sources can be masked by writing a '1' to the bit corresponding to the interrupt source in the **IRQ Link 0 Enable** register.

6.2.3 IRQ Link UNI Overflow and IRQ UTOPIA Input UNI Overflow Status Registers

The **IRQ Link UNI Overflow** and the **IRQ UTOPIA Input UNI Overflow Status** registers report the overflow condition from any of the counters associated with the TX PCM link, the RX PCM link or the TX UTOPIA I/F. They also report the overflow condition from the level of the UTOPIA RX FIFO when the link is used in UNI mode. The 13 interrupt sources are organized in the following two registers:

- an 8-bit register that reports the overflow condition from the eight counters associated with a TX or RX PCM link (the **IRQ Link UNI Overflow Status** registers)
- a 5-bit register that reports the overflow condition from the four counters associated with the UTOPIA TX I/F to the PCM link used in UNI mode as well as an overflow condition from the RX UTOPIA FIFO associated to a RX PCM link when in UNI mode (the **IRQ UTOPIA Input UNI Overflow Status** registers)

The five bits in the **IRQ UTOPIA Input UNI Overflow Status** registers are latched to report an overflow condition. The status bit is cleared by overwriting it with a 0. Reading the registers or writing a '1' to these registers will not change the content of the registers.

There is no enable register directly associated to the **IRQ Link UNI Overflow Status** registers. The source of the interrupt request can be controlled either by enabling the interrupt from the counters or from the **RX UTOPIA Link FIFO Overflow Enable** register. Refer to 6.1 Counter Block paragraph for more details on the operation of the counters.

6.2.4 IRQ IMA Group Overflow Status and Enable Registers

There are 20 sources of IMA Group overflow conditions organized in two levels of registers:

- four low level, 5-bit registers (one register per IMA Group)
- one intermediate 4-bit register that is used to report the overflow conditions for each IMA Group to minimize the number of accesses to identify the source of an overflow condition

The **IRQ IMA Group Overflow Status** register indicates which one of the four IMA Groups is reporting an overflow condition. When enabled, the bits in this status register reflect any overflow condition reported by the **IRQ IMA Overflow Status** registers.

The **IRQ IMA Group Overflow Enable** register is used to enable any overflow conditions for a specific IMA Group. Each of the four bits correspond to one of the four IMA Groups. A value of '1' enables the report of the overflow condition to the upper IRQ levels.

6.2.5 IRQ IMA Overflow Status and RX UTOPIA IMA Group FIFO Overflow Enable Registers

There are five possible sources of overflow conditions that can be reported for each of the 4 IMA Groups.

The **IRQ IMA Overflow Status** register captures (latches) the overflow condition from any of the four counters associated with the UTOPIA TX I/F when the PCM link is used in IMA mode. It also latches when an overflow condition occurs in the RX UTOPIA FIFO associated to a PCM link when in IMA mode.

The status bit is cleared by overwriting it with a 0. Reading the registers or writing a '1' to these registers will not change the content of the registers. A counter generates an interrupt request, if not masked, when the counter overflows (i.e. starts over from 0 after reaching the maximum counter value - refer to paragraph 6.1 for more details on the operation of the counters). An interrupt request can also be generated, if not masked, when an overflow condition is detected in the UTOPIA RX FIFO associated with an IMA Group.

There is one enable register used to enable the generation of an interrupt by the overflow condition of the RX UTOPIA FIFO associated with an IMA Group. This is the **RX UTOPIA IMA Group FIFO Overflow Enable** register.

6.3 Register and Memory Map

6.3.1 Access to the Various Registers

Since the MT90220 and microprocessor operate from two different clock sources, access to a MT90220 register is asynchronous. Data is synchronized between the MT90220 and the microprocessor using either direct or indirect (synchronized) methods of access.

The direct method is used during a read access whenever data does not change or data changes do not represent any problem. There is no register that clears status bits upon a read access. A write action is always required to clear a status bit.

The indirect method is identified with 'S' (indirect and need to synchronize with a ready bit) whereas the direct access is identified with a 'D' in the register tables.

6.3.2 Direct Access

Direct access registers can be written or read directly by the microprocessor, without having to use otherregisters. Upon a write access to the MT90220 internal registers, the data is stored in an internal latch and transferred to the destination register within 2.5 system clock cycles (100 nsec at 25 MHz). No specific action is required if the microprocessor provides at least 100 nsec (with Chip Select signal inactive) between 2 consecutive write accesses or between a write and a read back of the same register. If the microprocessor is faster, then consecutive accesses must be inhibited or wait state(s) introduced (this option is available on most MCUs).

6.3.3 Indirect Access

Indirect access registers cannot be accessed directly by the microprocessor. The value is transferred back and forth using registers which hold a copy of the information (data) and internal address of the register. This is required to stabilize the read value. Consider for example the transfer of a TX ICP cell that requires almost 200 system clock cycles. A dedicated ready bit which can optionally generate an interrupt is implemented for this type of transfer. Accessing any of the 24 bit counters provides another example. A ready bit is implemented in the Counter Transfer Command register when the transfer is completed.

When accessing indirect registers specified by the **RX Delay Select** or **RX Load Values**/**Link Select** registers, the value in the indirect registers can be read when the write to the selection register is effectively done (i.e. 2.5 system clock cycles after the write cycle is completed). There is no additional delay required.

6.3.4 Clearing of Status Bits

The status bits will remain set until cleared by a specific write action from the microprocessor. Status bits are cleared by overwriting a zero to the corresponding position in the source register. Each input status register has a related interrupt enable register. When enabled, setting a bit in the interrupt enable register causes an interrupt to occur in the corresponding status register bit.

6.3.4.1 Toggle Bit

Some registers include a toggle bit. Toggle bits are used to indicate a write action to any internal register has taken place. Typically, this bit is toggled 2.5 system clock cycles after performing the write action. To use the toggle bit, its state (either 0 or 1) must be read (polled) and its state is changed (toggled) when a write command is completed. This bit is particularly useful when the processor clock is much faster than the MT90220 system clock.

6.3.5 Test Modes

Access is provided to the External SRAM from the microprocessor using a special test mode and test registers (i.e., to assist in debugging or verification). The test mode is enabled by writing to bit 7 of the **Test Mode Enable** register, writing 0x10 to the **RX Delay Link Number** register and by writing 0x29 to the **RX External SRAM Control** register. Indirect access is provided using the **RX External SRAM Read**/**Write Data** register for the data to be written or read and the **RX SRAM External Address 0**, **1** and **2** registers for the address of the SRAM location. The write transfer command is issued using the **RX External SRAM Control** register. Bit 7 of the **RX External SRAM Control** is cleared (set to 0) and then returned to 1 when the write action is completed.

7.0 Register Descriptions

Address (Hex)	Access Type	Reset Value (Hex)	Table #	Description
000 - 007	D	00	12	UTOPIA Input Link Address Registers
008 - 00B	D	00	13	UTOPIA Input Group Address Registers
00C	D	00	14	UTOPIA Input Link PHY Enable Register
00D	D	00	15	UTOPIA Input Group PHY Enable Register
00E	D	00	16	UTOPIA Input Control Register.
040 - 047	D	00	17	UTOPIA Output Link Address Registers
048 - 04B	D	00	18	UTOPIA Output Group Address Registers
04C	D	00	19	UTOPIA Output Link PHY Enable Register
04D	D	00	20	UTOPIA Output Group PHY Enable Register
205	D	00	21	RX UTOPIA IMA Group FIFO Overflow Enable Register
221	D	00	22	RX UTOPIA Link FIFO Overflow Enable Register
140	D	00	23	TX Cell RAM Control Register
150	D	00	24	TX UTOPIA FIFO Level
14A	D	33	25	TX FIFO Length Definition Register 1
14B	D	33	26	TX FIFO Length Definition Register 2
14C	D	33	27	TX FIFO Length Definition Register 3
14D	D	33	28	TX FIFO Length Definition Register 4
14E	D	33	29	TX FIFO Length Definition Register 5
14F	D	33	30	TX FIFO Length Definition Register 6
0C0 - 0C3	D	58	31	TX Group Control Mode Register
0DD - 0E4	D	link #	32	TX Link ID Registers
0C4 - 0CB	D	link #	33	TX ICP Cell Offset Registers
200 - 203	D	05	34	TX IDCR Integration Registers
0CC - 0D3	D	04	35	TX Link Control Registers
0D4-0D7	D	29	36	TX IMA Control Register
0EF	D	00	37	TX IMA Mode Status Register
148	D	0F	38	TX ICP Cell Handler Register
149	D	00	39	TX ICP Cell Interrupt Enable Register
300, 340, 380, 3C0	D	SEE TABLE	40	TX ICP Cell Registers (access to ICP cell bytes)
100 - 107	D	0C	41	RX Link Control Registers
109	D	67	42	Cell Delineation Register
108	D	0C	43	Loss Cell Delineation Register
10A	D	91	44	IMA Frame Definition Register
10C - 10F	D	01	45	RX OAM Label
115	D	00	46	RX OIF Status Register
116	D	00	47	RX OIF Counter Clear Command Register
117	D	00	48	RX Load Values/Link Select Register
118	D	00	49	RX Link IMA ID Registers

Table 11 - Register Summary

Address (Hex)	Access Type	Reset Value (Hex)	Table #	Description
119	D	00	50	RX ICP Cell Offset Register
11A	D	00	51	RX Link Frame Sequence Number Registers
11B	D	00	52	RX Link SCCI Sequence Number Registers
11C	D	00	53	RX Link OIF Counter Value Register
11D	D	20	54	RX Link ID Number Registers
11E	D	00	55	RX State Register
1C0	D	00	56	RX ICP Cell Type RAM Register 1
1C1	D	00	57	RX ICP Cell Type RAM Register 2
1C6	D	00	58	RX ICP Cell Buffer Increment Read Pointer Register
1C7	D	00	59	RX ICP Cell Level FIFO Status Register
1C3	S	00	60	Test Mode Enable Register
292	D	08	61	SRAM Control Register
283	S	00	62	RX External SRAM Read/Write Data
291	S	00	63	RX External SRAM Read/Write Address 0
290	S	00	64	RX External SRAM Read/Write Address 1
28F	S	00	65	RX External SRAM Read/Write Address 2
280	S	80	66	RX External SRAM Control Register
281	D	00	67	Increment/Decrement Delay Control Register
29D	D	00	68	RX Delay Select Register
284	D	00	69	RX Delay MSB Register
285	D	04	70	RX Delay LSB Register
286	D	00	71	RX Delay Link Number Register
288, 28A, 28C, 28E	D	04	72	RX Guardband/Delta Delay LSB Register, 1 per IMA Group
287, 289, 28B, 28D	D	00	73	RX Guardband/Delta Delay MSB Register, 1per IMA Group.
296, 298, 29A, 29C	D	00	74	RX Maximum Operational Delay LSB Register, 1 per IMA Group.
295, 297, 299, 29B	D	00	75	RX Maximum Operational Delay MSB Register
180 - 187	D	00	76	RX Recombiner Registers
282	D	00	77	RX Recombiner Delay Control Register
29F	D	00	78	Enable Recombination Status
188 - 18B	D	00	79	RX Reference Link Control Registers
18C - 18F	D	05	80	RX IDCR Integration Register
080 - 087	D	00	81	TX PCM Link Control Register #2
088 - 08F	D	00	82	TX PCM Link Control Register #1
090 - 097	D	00	83	RX PCM Link Control Register
098	D	00	84	PLL Reference Control register
099	D	00	85	Clock Activity Register
09A	D	00	86	RX Sync. Status Register

Table 11 - Register Summary

Address (Hex)	Access Type	Reset Value (Hex)	Table #	Description
09E	D	00	87	TX Sync. Status Register
09C	D	00	88	TX Clock Disabled Status
09D	D	10	89	PLL REF Clock Disabled Status/Device Rev.
214	S	00	90	Counter Byte #3 Register
215	S	00	91	Counter Byte #2 Register
216	S	00	92	Counter Byte #1 Register
217	S	00	93	Select Counter register
207	S	00	94	Counter Transfer Command Register
232	D	00	95	IRQ Master Status Register
218	D	00	96	IRQ Master Enable Register
222 - 229	D	00	97	IRQ Link Status Registers
219 - 220	D	00	98	IRQ Link Enable Registers
235	D	00	99	IRQ IMA Group Overflow Status Register
204	D	00	100	IRQ IMA Group Overflow Enable Register
210 - 213	D	00	101	IRQ IMA Overflow Status Registers
208 - 20F	D	00	102	IRQ UTOPIA UNI Overflow Status Registers
22A - 231	D	00	103	IRQ Link UNI Overflow Status Registers
206	D	00	104	General Status Register
04E	D	00	105	Test1 register
0DA	D	00	106	Test2 register
400, 440	D	00		Base address for the 2 RX ICP Cell with changes, link 0
480, 4C0	D	00		Base address for the 2 RX ICP Cell with changes, link 1
500, 540	D	00		Base address for the 2 RX ICP Cell with changes, link 2
580, 5C0	D	00		Base address for the 2 RX ICP Cell with changes, link 3
600, 640	D	00		Base address for the 2 RX ICP Cell with changes, link 4
680, 6C0	D	00		Base address for the 2 RX ICP Cell with changes, link 5
700, 740	D	00		Base address for the 2 RX ICP Cell with changes, link 6
780, 7C0	D	00		Base address for the 2 RX ICP Cell with changes, link 7

Table 11 - Register Summary

7.1 Utopia Register Description

Tables 12 to 22 describe the **UTOPIA** registers.

Address (Hex):	**000 - 007**
Direct access	**1 register per link in UNI mode. The TxClk signal must be active for correct register operation.**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of Link N when in UNI.

Table 12- UTOPIA Input Link Address Registers

Address (Hex):	**008 - 00B**
Direct access	**11 reg. per IMA Group. The TxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of IMA Group N.

Table 13 - UTOPIA Input Group Address Registers

Address (Hex):	**00C**
Direct access	**1 register to enable the links in UNI mode. The TxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7	R/W	Enable UTOPIA PHY address of link 7. A 1 enables the PHY port Address. UNI mode.
6	R/W	Enable UTOPIA PHY address of link 6. A 1 enables the PHY port Address. UNI mode.
5	R/W	Enable UTOPIA PHY address of link 5. A 1 enables the PHY port Address. UNI mode.
4	R/W	Enable UTOPIA PHY address of link 4. A 1 enables the PHY port Address. UNI mode.
3	R/W	Enable UTOPIA PHY address of link 3. A 1 enables the PHY port Address. UNI mode.
2	R/W	Enable UTOPIA PHY address of link 2. A 1 enables the PHY port Address. UNI mode.
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address. UNI mode.
0	R/W	Enable UTOPIA PHY address of link 0. A 1 enables the PHY port Address. UNI mode.

Table 14 - UTOPIA Input Link PHY Enable Register

Address (Hex):	**00D**
Direct access	**1 register to enable the IMA Groups. The TxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7-4	R/W	Reserved. Write all 0's.
3	R/W	Enable UTOPIA PHY address of IMA Group 3. A 1 enables the PHY port Address.
2	R/W	Enable UTOPIA PHY address of IMA Group 2. A 1 enables the PHY port Address.
1	R/W	Enable UTOPIA PHY address of IMA Group 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of IMA Group 0. A 1 enables the PHY port Address.

Table 15 - UTOPIA Input Group PHY Enable Register

Address (Hex):	**00E**
Direct access	**1 register for all the UTOPIA Input ports. The TxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7	R	Reserved.
6	R/W	UTOPIA Input Reset. A 1 will reset the UTOPIA Input State Machine. All other user programmable registers are not cleared. A 0 is used for normal operation.
5	R/W	Reserved. Write 0.
4	R/W	Unassigned Cell Filter. A 1 signifies that the Unassigned[a] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.
3	R/W	Idle Cell Filter. A 1 signifies that the Idle[b] cells coming from the ATM layer will be discarded. The Unassigned/Idle cell counter is incremented for each cell discarded.
2	R/W	ATM Forum Polynomial. A 1 disables the addition of the ATM Forum Polynomial calculation on the HEC calculated as per I.432. A 0 means that the closest value is included in the HEC value.
1-0	R/W	HEC Verification. 11: Enable HEC error correction if 1 bit is wrong, discard cell if more than 1 bit are wrong. 10: Discard cell if HEC is wrong, no HEC correction. 01: Enable HEC error correction if 1 bit is wrong, no correction if more than 1 bit wrong, cell is not discarded if HEC is wrong. 00: No verification of HEC.

Table 16 - Utopia Input Control Register

a. Unassigned Cells have a fixed header corresponding to 00000000 00000000 00000000 0000xxx0.
b. Idle Cells have a fixed header corresponding to 00000000 00000000 00000000 00000001

Address (Hex):	**040 - 047**
Direct access	**1 register per link in UNI mode. The RxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of link N when in UNI (non-IMA) mode.

Table 17 - UTOPIA Output Link Address Registers

Address (Hex):	**048 - 04B**
Direct access	**1 reg. per IMA Group.link. The RxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R	Unused. Read all 0's.
4:0	R/W	UTOPIA PHY Address of IMA Group N.

Table 18 - UTOPIA Output Group Address Registers

Address (Hex):	**04C**
Direct access	**1 register to enable the links in UNI mode. The RxClk signal must be active for correct register operation**
Reset Value (Hex):	**00**

Bit #	Type	Description
7	R/W	Enable UTOPIA PHY address of link 7. A 1 enables the PHY port Address. UNI mode
6	R/W	Enable UTOPIA PHY address of link 6. A 1 enables the PHY port Address. UNI mode
5	R/W	Enable UTOPIA PHY address of link 5. A 1 enables the PHY port Address. UNI mode
4	R/W	Enable UTOPIA PHY address of link 4. A 1 enables the PHY port Address. UNI mode
3	R/W	Enable UTOPIA PHY address of link 3. A 1 enables the PHY port Address. UNI mode
2	R/W	Enable UTOPIA PHY address of link 2. A 1 enables the PHY port Address. UNI mode
1	R/W	Enable UTOPIA PHY address of link 1. A 1 enables the PHY port Address. UNI mode
0	R/W	Enable UTOPIA PHY address of link 0. A 1 enables the PHY port Address. UNI mode

Table 19 - UTOPIA Output Link PHY Enable Register

Address (Hex):	**04D**
Direct access	**1 register to enable the IMA Groups. The RxClk signal must be active for correct register operation**
Reset Value (Hex):	**X0000000**

Bit #	Type	Description
7	R	Watch clock. This bit reflects the level present on the RX UTOPIA Clock pin when this register is read.
6	R/W	Reserved, write 0 for normal operation.
5	R/W	Reset UTOPIA RX state machines when set to 1.
4	R/W	Reserved, write '0' for normal operation.
3	R/W	Enable UTOPIA PHY address of IMA Group 3. A 1 enables the PHY port Address.
2	R/W	Enable UTOPIA PHY address of IMA Group 2. A 1 enables the PHY port Address.
1	R/W	Enable UTOPIA PHY address of IMA Group 1. A 1 enables the PHY port Address.
0	R/W	Enable UTOPIA PHY address of IMA Group 0. A 1 enables the PHY port Address.

Table 20 - UTOPIA Output Group PHY Enable Register

Address (Hex):	205
Direct access	1 register to enable interrupts from IMA Groups. The RxClk signal must be active for correct register operation
Reset Value (Hex):	00

Bit #	Type	Description
7-4	R	Unused. Read all 0's.
3	R/W	When set to 1, the corresponding bit in the Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. IMA Group 3.
2	R/W	When set to 1, the corresponding bit in the Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. IMA Group 2.
1	R/W	When set to 1, the corresponding bit in the Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. IMA Group 1.
0	R/W	When set to 1, the corresponding bit in the Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. IMA Group 0.

Table 21 - RX UTOPIA IMA Group FIFO Overflow Enable Register

Address (Hex):	221
Direct access	1 register to enable interrupts from the links in UNI mode. The RxClk signal must be active for correct register operation
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link7.
6	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 6.
5	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 5.
4	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 4.
3	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link3.
2	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 2.
1	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 1.
0	R/W	When set to 1, the corresponding bit in the IRQ UTOPIA UNI Overflow Status register can generate an interrupt. A value of 0 inhibits the generation of an interrupt. Link 0.

Table 22 - RX UTOPIA Link FIFO Overflow Enable Register

7.2 TX Registers Description

Tables 23 to 37 describe the **Transmit** registers.

Address (Hex):	**140**
Direct access	**Used for initialization of the TX Cell RAM (Filler, Idle Cells etc.)**
Reset Value (Bin):	**1X000000**

Bit #	Type	Description
7	R	Goes to 0 during initialization and returns to 1 on completion of initialization.
6	R/W	Reserved, write 0 for normal operation.
5	R/W	Reserved. Write 0 for normal operation.
4:1	R/W	Reserved, write 0's for normal operation.
0	R/W	Reserved. Write 0 to initialize the Cell RAM.

Table 23 - TX Cell RAM Control Register

Address (Hex):	**150**
Direct access	
Reset Value (Hex):	**00**

Bit #	Type	Description
7:4	W	Write 0 for normal operation.
3:0	W	Write 1000 to load the TX Utopia FIFO level of IMA group 0 Write 1001 to load the TX Utopia FIFO level of IMA group 1. Write 1010 to load the TX Utopia FIFO level of IMA group 2. Write 1011 to load the TX Utopia FIFO level of IMA group 3.
7:5	R	Reserved, read 0's.
4:0	R	Level of selected FIFO.

Table 24 - TX UTOPIA FIFO Level Register

Address (Hex):	**14A**
Direct access	
Reset Value (Hex):	**33**

Bit #	Type	Description
7:4	R/W	TX FIFO Length Link 1.
3:0	R/W	TX FIFO Length Link 0.

Table 25 - TX FIFO Length Definition Register 1

Address (Hex):	**14B**
Direct access	
Reset Value (Hex):	**33**

Bit #	Type	Description
7:4	R/W	TX FIFO Length Link 3.
3:0	R/W	TX FIFO Length Link 2.

Table 26 - TX FIFO Length Definition Register 2

Address (Hex):	14C
Direct access	
Reset Value (Hex):	33

Bit #	Type	Description
7:4	R/W	TX FIFO Length Link 5.
3:0	R/W	TX FIFO Length Link 4.

Table 27 - TX FIFO Length Definition Register 3

Address (Hex):	14D
Direct access	
Reset Value (Hex):	33

Bit #	Type	Description
7:4	R/W	TX FIFO Length Link 7.
3:0	R/W	TX FIFO Length Link 6.

Table 28 - TX FIFO Length Definition Register 4

Address (Hex):	14E
Direct access	
Reset Value (Hex):	33

Bit #	Type	Description
7:4	R/W	TX FIFO Length IMA Group 1.
3:0	R/W	TX FIFO Length IMA Group 0.

Table 29 - TX FIFO Length Definition Register 5

Address (Hex):	14F
Direct access	
Reset Value (Hex):	33

Bit #	Type	Description
7:4	R/W	TX FIFO Length IMA Group 3.
3:0	R/W	TX FIFO Length IMA Group 2.

Table 30 - TX FIFO Length Definition Register 6

Address (Hex):	0C0 - 0C3
Direct access	1 register per TX IMA Group
Reset Value (Hex):	58

Bit #	Type	Description
7	R/W	Reserved, write 0 for normal operation.
6-5	R/W	Value of M. These 2 bits specifies the value of M for the IMA Group. 00: M=32, 01: M=64, 10: M=128 11: M=256
4	R/W	Timing Mode inserted in ICP cell. A 0 means that the ITC timing mode is inserted in the ICP cell and a 1 means that the CTC timing mode is inserted in the ICP cell.
3	R/W	Timing Mode in RoundRobin scheduler. A 0 means that the ITC timing mode (adaptive) algorithm is selected and a 1 means that the CTC timing mode (fixed) algorithm is selected for internal operation.
2:0	R/W	Reference Link. These 3 bits define which physical link is to be used as reference for timing purposes.

Table 31 - TX Group Control Mode Registers

Address (Hex):	0DD- 0E4
Direct access	1 register per link, used in IMA mode only.
Reset Value (Hex):	0DD: 00, 0DE: 01 0DF: 02, 0E0: 03, 0E1: 04, 0E2: 05, 0E3: 06, 0E4: 07

Bit #	Type	Description
7:5	R/W	Reserved, must write 0 for normal operation.
4:0	R/W	Link ID for the link N. The value can be between 0 and 31. This is the logical value associated to a physical link. Used in IMA mode only.

Table 32 - TX Link ID Registers

Address (Hex):	0C4 - 0CB
Direct access	1 register per link, used in IMA mode only
Reset Value (Hex):	0C4: 00, 0C5: 01 0C6: 02, 0C7: 03, 0C8: 04, 0C9: 05, 0CA: 06, 0CB: 07

Bit #	Type	Description
7:0	R/W	Defines the ICP cell offset of link N. The value of M determines which significant bits are used as follows: M=256; bits 7-0 are used, M=128; bits 6-0 are used; M=64; bits 5-0 are used; M=32; bits 4-0 are used.

Table 33 - TX ICP Cell Offset Registers

Address (Hex):	200 - 203
Direct access	1 register per TX IMA Group
Reset Value (Hex):	05

Bit #	Type	Description
7:4	R	Unused. Read all 0's.
3-0	R/W	Defines the integration period for an IMA Group: 1111: Reserved, do not use 1110: 2^{21} clock cycles 1101: 2^{20} clock cycles 1100: 2^{19} clock cycles (preferred value for E1) 1011: 2^{18} clock cycles (preferred value for T1 - 24 channels) 1010: 2^{17} clock cycles 1001: 2^{16} clock cycles (preferred value for T1 - 23 channels) 1000: 2^{15} clock cycles 0111: 2^{14} clock cycles 0110: 2^{13} clock cycles 0101: 2^{12} clock cycles 0100: 2^{11} clock cycles 0011: 2^{10} clock cycles 0010: 2^{09} clock cycles 0001: 2^{08} clock cycles 0000: 2^{07} clock cycles

Table 34 - TX IDCR Integration Registers

Address (Hex):	0CC - 0D3
Direct access	1 register per link
Reset Value (Hex):	04

Bit #	Type	Description
7	R/W	Reserved, write 0 for normal operation.
6	R/W	Set to 1 to start sending User Cells in IMA mode. Set to 0 to send always Filler and ICP cells in IMA mode (Note: in UNI mode, the control to send User cells is implemented with the UTOPIA Input Link PHY Enable register).
5	R/W	Coset value. A 0 will generate HEC with Coset value, when 1, Coset is not added.
4	R/W	Cell Scrambling. A 1 enables the scrambling of the cells on the link N.
3	R/W	Reserved, must write a 0 for normal operation.
2	R/W	Set to 1 for UNI mode and clear to 0 for IMA mode. Select the IMA group number BEFORE enabling the IMA mode.
1:0	R/W	Defines IMA group number when the link is configured in IMA mode. Select the IMA group number BEFORE enabling the IMA mode. When configuring the link in UNI mode after it was in IMA mode, do not change the IMA group number until the link is reported in UNI mode (refer to TX IMA Mode Status Register).

Table 35 - TX Link Control Registers

Address (Hex):	0D4- 0D7
Direct access	1 register per IMA Group
Reset Value (Hex):	29

Bit #	Type	Description
7	R/W	0 for Stuff Indication 1 frame before Stuff event. 1 for Stuff Indication 4 frames before stuff event.
6:3	R/W	Level overflow limit. Default is 5.
2:0	R/W	Level underflow limit. Default is 1.

Table 36 - TX IMA Control Registers

Address (Hex):	0EF
Direct access	
Reset Value (Hex):	FF

Bit #	Type	Description
7	R	1 means Link 7 is not in IMA mode.
6	R	1 means Link 6 is not in IMA mode.
5	R	1 means Link 5 is not in IMA mode.
4	R	1 means Link 4 is not in IMA mode.
3	R	1 means Link 3 is not in IMA mode.
2	R	1 means Link 2 is not in IMA mode.
1	R	1 means Link 1 is not in IMA mode.
0	R	1 means Link 0 is not in IMA mode.

Table 37 - TX IMA Mode Status Register

7.3 TX ICP Register Description

Tables 38 to 40 describe the **TX ICP** registers.

Address (Hex):	**148**
Direct access	**Controls the transfer of TX ICP cells and frame pulse indication**
Reset Value (Hex):	**0F**

Bit #	Type	Description
7	R/W	When 1 indicates the end of a frame was detected in IMA Group #3. Cleared by writing 0.
6	R/W	When 1 indicates the end of a frame was detected in IMA Group #2. Cleared by writing 0.
5	R/W	When 1 indicates the end of a frame was detected in IMA Group #1. Cleared by writing 0.
4	R/W	When 1 indicates the end of a frame was detected in IMA Group #0. Cleared by writing 0.
3	R/W	When 1 indicate that the transfer of the TX ICP cell for IMA Group #3 is complete. Write 0 to initiate a transfer.
2	R/W	When 1 indicate that the transfer of the TX ICP cell for IMA Group #2 is complete. Write 0 to initiate a transfer.
1	R/W	When 1 indicate that the transfer of the TX ICP cell for IMA Group #1 is complete. Write 0 to initiate a transfer.
0	R/W	When 1 indicate that the transfer of the TX ICP cell for IMA Group #0 is complete. Write 0 to initiate a transfer.

Table 38 - TX ICP Cell Handler Register

Address (Hex):	**149**
Direct access	**Interrupt Enable register for the TX ICP Handler register**
Reset Value (Hex):	**00**

Bit #	Type	Description
7	R/W	Write a 1 will enable the generation of an interrupt from the end of a frame detection for IMA Group 3. A 0 will inhibit the generation of an interrupt.
6	R/W	Write a 1 will enable the generation of an interrupt from the end of a frame detection for IMA Group 2. A 0 will inhibit the generation of an interrupt.
5	R/W	Write a 1 will enable the generation of an interrupt from the end of a frame detection for IMA Group 1. A 0 will inhibit the generation of an interrupt.
4	R/W	Write a 1 will enable the generation of an interrupt from the end of a frame detection for IMA Group 0. A 0 will inhibit the generation of an interrupt.
3	R/W	Write a 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 3 is completed. A 0 will inhibit the generation of an interrupt.
2	R/W	Write a 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 2 is completed. A 0 will inhibit the generation of an interrupt.
1	R/W	Write a 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 1 is completed. A 0 will inhibit the generation of an interrupt.
0	R/W	Write a 1 will enable the generation of an interrupt when the transfer of the TX ICP cell for the IMA Group 0 is completed. A 0 will inhibit the generation of an interrupt.

Table 39 - TX ICP Cell Interrupt Enable Register

Address (Hex):	**300, 340, 380, 3C0 for IMA Group 0, 1, 2 and 3 respectively**
Direct access	**Access these locations directly then use transfer command to copy to internal memory**
Reset Value (Hex):	**These registers need to be initialized for proper operation**

Cell Byte #	Address Offset	Type	Description
1-4	00-03	R/W	Header of ICP Cell. The values should be set to Byte 0: 0x00, byte 1: 0x00, byte 2: 0x00, byte 3: 0x0B.
5	04	R/W	HEC is always calculated and inserted by the MT90220.
6	05	R/W	OAM, should be set to 0x01
7	06	R/W	Cell ID, Link ID. The bit 7 (Cell ID) is controlled by the MT90220, the Link ID is provided by the TX Link ID Register.
8	07	R/W	IMA Frame Sequence Number. Inserted by the MT90220.
9	08	R/W	ICP Cell Offset. Inserted by the MT90220 based on the Link Offset register info.
10	09	R/W	Link Stuff Indication. Inserted by the MT90220.
11	0A	R/W	Status & Control Change Indication. Inserted by the MT90220.
12	0B	R/W	IMA ID
13	0C	R/W	Group Status and Control
14	0D	R/W	Synchronization Information. Inserted by the MT90220 based on the TX Group Control Mode Register.
15	0E	R/W	Tx Test Control
16	0F	R/W	Tx Test Pattern
17	10	R/W	Rx Test Pattern
18-49	11-30	R/W	Status and Control of links with LID in the range 0-31
50	31	R/W	Unused
51	32	R/W	End-to-End channel
52-53	33-34	R/W	CRC Error Control. Inserted by the MT90220

Table 40 - TX ICP Cell Registers

7.4 RX Registers Description

Tables 41 to 55 describe the **Receive** registers.

Address (Hex):	**100 -107**	
Direct access	**1 register per link**	
Reset Value (Hex):	**0C**	
Bit #	**Type**	**Description**
7	R/W	A Value of 0 select to count the number of Stuff cells received by the physical link. A value of 1 selects to count the total number of cells received by the link.
6	R/W	A value of 1 enables the IMA mode for this link. A value of 0 enables the UNI mode for the link.
5	R/W	A value of 1 enables the descrambling of the cell for the link
4	R/W	A value of 1 means that the Unassigned cells are discarded upon reception. UNI mode only.
3	R/W	A value of 1 means that the Idle cells are discarded upon reception. UNI mode only.
2	R/W	A value of 1 enables the discard option of the cells with wrong HEC. A value of 0 will disables the discard option, all the cells will be written to the receive buffer.
1	R/W	A value of 1signifies that the ATM Forum polynomial value (coset) is not to be added to the HEC before the verification. A value of 0 means that the HEC as per I.432 only is calculated and compared (i.e. including the coset).
0	R/W	A value of 1 enables the correction of the cells with a wrong HEC. A value of 0 disable the correction of the HEC.

Table 41 - RX Link Control Registers

Address (Hex):	**109**	
Direct access	**1 register for all 8 cell delineation state machines**	
Reset Value (Hex):	**67**	
Bit #	**Type**	**Description**
7:4	R/W	DELTA parameter value for the Cell Delineation register. The number of consecutive cells with correct HEC to leave the PRESYNC state to go to the SYNC state. The default value is 6.
3:0	R/W	ALPHA parameter value for the Cell Delineation register. The number of consecutive cells with incorrect HEC to leave the SYNC state to go to the HUNT state. The default value is 7.

Table 42 - Cell Delineation Register

Address (Hex):	**108**	
Direct access	**1 reg. for all 8 cell delineation state machines**	
Reset Value (Hex):	**0C**	
Bit #	**Type**	**Description**
7:0	R/W	Contains the number of consecutive cell periods that the CD circuit will count before the incoming ATM cell stream to be considered in LCD state. Each count will be done on a cell by cell basis. The value of this register is multiplied by 2 before being loaded in the internal counter. (The internal counter value can be from 0 to 512). Note that a value of 0 is not allowed as an LCD condition would be generated.

Table 43 - Loss of Delineation Register

Address (Hex):	10A
Direct access	1 reg. for all 4 IMA Frame state machines
Reset Value (Hex):	91

Bit #	Type	Description
7:6	R/W	ALPHA parameter value for the IMA Frame Delineation.state machine. The number of consecutive invalid ICP cells to leave the IMA SYNC state to go to the IMA HUNT state.The default value is 2.
5:3	R/W	BETA parameter value for the Cell Delineation.state machine. The number of consecutive errored ICP cells to leave the IMA SYNC state to go to the IMA HUNT state. The default value is 2.
2:0	R/W	GAMMA parameter value for the Frame Delineation state machine. The number of consecutive valid ICP cells to leave the IMA PRESYNC state to go to the IMA SYNC state. The default value is 1.

Table 44 - IMA Frame Delineation Register

Address (Hex):	10C - 10F
Direct access	1 register per RX IMA group
Reset Value (Hex):	01

Bit #	Type	Description
7:0	R/W	RX OAM label value (defines the working RX IMA version).

Table 45 - RX OAM Label Register

Address (Hex):	115
Direct access	1 register for the 8 RX links
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	An OIF state was detected on the physical link 7. Cleared by writing a 0.
6	R/W	An OIF state was detected on the physical link 6. Cleared by writing a 0.
5	R/W	An OIF state was detected on the physical link 5. Cleared by writing a 0.
4	R/W	An OIF state was detected on the physical link 4. Cleared by writing a 0.
3	R/W	An OIF state was detected on the physical link 3. Cleared by writing a 0.
2	R/W	An OIF state was detected on the physical link 2. Cleared by writing a 0.
1	R/W	An OIF state was detected on the physical link 1. Cleared by writing a 0.
0	R/W	An OIF state was detected on the physical link 0. Cleared by writing a 0.

Table 46 - RX OIF Status Register

Address (Hex):	116
Direct access	1 register for the 8 RX links
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	Write a 0 to clear the OIF counter for physical link 7.
6	R/W	Write a 0 to clear the OIF counter for physical link 6.
5	R/W	Write a 0 to clear the OIF counter for physical link 5.
4	R/W	Write a 0 to clear the OIF counter for physical link 4.
3	R/W	Write a 0 to clear the OIF counter for physical link 3.
2	R/W	Write a 0 to clear the OIF counter for physical link 2.
1	R/W	Write a 0 to clear the OIF counter for physical link 1.
0	R/W	Write a 0 to clear the OIF counter for physical link 0.

Table 47 - RX OIF Counter Clear Command Register

Address (Hex):	117
Direct access	1 register to select the link from which to extract the RX ICP cells values shown in following registers
Reset Value (Hex):	00

Bit #	Type	Description
7:4	R	Unused. read all 0's.
3	R	Reserved.
2:0	R/W	Selects the RX physical link number to update the values from the RX ICP cell. This is used when the RX Link is enabled but in UNI mode to collect the values received over the ICP cells.

Table 48 - RX Load Values/Link Select Register

Address (Hex):	118
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	00

Bit #	Type	Description
7:0	R	This register stores the value of the IMA ID extracted from the valid RX ICP cell received on the link selected in the RX Load Values/Link Select register.

Table 49 - RX Link IMA ID Registers

Address (Hex):	119
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	00

Bit #	Type	Description
7:0	R	Defines the ICP cell offset of the link selected in the RX Load Values/Link Select register. The significant bits are used depending on the value of M. M=256; bits 7-0 are used, M=128; bits 6-0 are used; M=64; bits 5-0 are used; M=32; bits 4-0 are used.

Table 50 - RX ICP Cell Offset Register

Address (Hex):	11A
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	01

Bit #	Type	Description
7:0	R	This register reports the IMA Frame sequence number as reported in the last received valid ICP cell of the selected link.

Table 51 - RX Link Frame Sequence Number Register

Address (Hex):	11B
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	00

Bit #	Type	Description
7:0	R	This register reports the SCCI sequence number as reported in the last received valid ICP cell of the link selected in the RX Load Values/Link Select register.

Table 52 - RX Link SCCI Sequence Number Register

Address (Hex):	11C
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	00

Bit #	Type	Description
7:0	R	Content of the OIF counter for the link selected in the RX Load Values/Link Select register.

Table 53 - RX Link OIF Counter Value Register

Address (Hex):	11D
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	20

Bit #	Type	Description
7	R	LIF state of the link selected in the RX Load Values/Link Select register.
6	R	LCD state of the link selected in the RX Load Values/Link Select register.
5	R	A value of 1 means that the link selected in the RX Load Values/Link Select register is a reference link for his IMA Group.
4:0	R	These bits report the link ID number for the link selected in the RX Load Values/Link Select register.

Table 54 - RX Link ID Number Register

Address (Hex):	11E
Direct access	The value is updated on completion of the write action in the RX Load Values register
Reset Value (Hex):	00

Bit #	Type	Description
7:6	R	Unused. Read all 0's.
5:4	R	Frame length (value of M) of the link selected in the RX Load Values/Link Select register.
3:2	R	IMA Frame State: 00: Hunt 01: Presync 10: Sync. 11: Stuffed Frame event.
1:0	R	Cell Delineation State: 00: Hunt 01: Presync 10: Sync. 11: Unused.

Table 55 - RX State Register

7.5 RX ICP Cell Registers Description

Tables 56 to 60 describe the **RX ICP** registers

Address (Hex):	**1C0**
Direct access	**Access for RX link 3-0**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:6	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 3. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
5:4	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 2. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
3:2	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 1. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
1:0	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 0. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.

Table 56 - RX ICP Cell Type RAM Register 1

Address (Hex):	1C1
Direct access	Access for RX link 7-4
Reset Value (Hex):	00

Bit #	Type	Description
7:6	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 7. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
5:4	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 6. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
3:2	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 5. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.
1:0	R/W	These 2 bits select the type of cells stored in the RX ICP Cell buffer for physical link 4. 00: valid RX ICP Cells with changes. 01: All valid RX ICP Cells. 10: All valid RX Cells. 11: No cell written into RX buffer.

Table 57 - ICP Cell Type RAM Register 2

Address (Hex):	1C6
Direct access	1 reg. for all 8 RX link FIFO
Reset Value (Hex):	00

Bit #	Type	Description
7	W	A value of 1 will increment the position of the read pointer for the physical link 7. A 0 has no effect.
6	W	A value of 1 will increment the position of the read pointer for the physical link 6. A 0 has no effect.
5	W	A value of 1 will increment the position of the read pointer for the physical link 5. A 0 has no effect.
4	W	A value of 1 will increment the position of the read pointer for the physical link 4. A 0 has no effect.
3	W	A value of 1 will increment the position of the read pointer for the physical link 3. A 0 has no effect.
2	W	A value of 1 will increment the position of the read pointer for the physical link 2. A 0 has no effect.
1	W	A value of 1 will increment the position of the read pointer for the physical link 1. A 0 has no effect.
0	W	A value of 1 will increment the position of the read pointer for the physical link 0. A 0 has no effect.

Table 58 - RX ICP Cell Buffer Increment Read Pointer Register

Address (Hex):	1C7	
Direct access	Write to bit 2:0 of this register to select the specific link RX ICP Cell FIFO. The value is immediately updated for a read	
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
7:6	R	Unused. Read all 0's.
5:4	R	Level of RX ICP Cell FIFO.
3:2	R	FIFO write pointer position
1:0	R	FIFO read pointer position
2:0	W	Select link number for FIFO Status.

Table 59 - RX ICP Cell Level FIFO Status Register

Address (Hex):	1C3	
Synchronized access	Set Address for an indirect access to write to ICP Cell RAM	
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
7	R/W	0: External SRAM Test Mode is disabled, 1: External SRAM Test Mode is enabled.
6	R/W	Reserved, write 0 for normal operation.
5	R/W	Reserved, write 0 for normal operation.
4	R/W	Reserved, write 0 for normal operation.
3	R/W	Reserved, write 0 for normal operation.
2:0	R/W	Reserved, write 0's for normal operation.

Table 60 - Test Mode Enable Register

7.6 External SRAM Register Description

Tables 61 to 65 describe the **External SRAM** registers.

Address (Hex):	**292**
Direct access	**Defines the external SRAM configuration**
Reset Value (Hex):	**08**

Bit #	Type	Description
7	R/W	Write a 1 to reset the receiver. 0 means no action.
6	R/W	Write a 1 to reset the transmitter. 0 means no action.
5	R/W	Reserved, write 0 for normal operation.
4:3	R/W	Write 00 for normal operation
2:0	R/W	These 3 bits define the size of the external receive memory: 101: 2 banks of 512K x 8 bits 100: 1 bank of 512K x 8 bits 011: 2 banks of 128K x 8 bits 010: 1bank of 128K x 8 bits 001: 2 banks of 32K x 8 bits 000: 1bank of 32K x 8 bits

Table 61 - SRAM Control Register

Address (Hex):	**283**
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R/W	RX External SRAM Read/Write data register.

Table 62 - RX External SRAM Read/Write Data

Address (Hex):	**291**
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R/W	RX External SRAM Read/Write Address bit 7:0.

Table 63 - RX External SRAM Read/Write Address 0

Address (Hex):	**290**
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R/W	RX External SRAM Read/Write Address bit 15:8.

Table 64 - RX External SRAM Read/Write Address 1

Address (Hex):	**28F**
Synchronized access	**Set address before the transfer is initiated with the RX External SRAM Control register**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R	Unused. Read all 0's
4	R/W	Reserved, write 0 for normal operation.
3:0	R/W	RX External SRAM Read/Write Address bit 19:16.

Table 65 - RX External SRAM Read/Write Address 2

7.7 RX Delay Registers Description

Tables 66 to 75 describe the **RX Delay** registers.

Address (Hex): 280 **Synchronized access** **Reset Value (Bin):** 1X000000		
Bit #	**Type**	**Description**
7	R	Upon a write to this register, the bit will go to 0 and will return to 1 when the transfer is completed
6	R	Toggle Bit.
5	R/W	Write 0 to initiate a transfer from the MT90220 registers to the external RAM. Write 1 to initiate a transfer from the external RAM to the MT90220 registers.
4	R/W	Reserved, write 0 for normal operation.
3	R/W	When Test Mode bit is 1; write 1 to enable the direct addressing mode to the External SRAM.
2	R/W	When Test Mode bit is 1; write 0 for normal operation.Write 1 for disabling all access to the external RAM except for the uP port (for RAM test purposes)
1:0	R/W	When bit 1 is 1, there is no access to the external RAM (no reset or read or write action done). When bit 1 is 0 and bit 0 is 0, then the external RAM is initialized. When bit 1 is 0 and bit 0 is 1, then a read or write access to the external RAM is performed, as defined by bit 5.

Table 66 - RX External SRAM Control Register

Address (Hex): 281 **Direct access** **Used to increment or decrement the recombiner delay for an IMA Group. The value is in the Guardband/Delta Delay register** **Reset Value (Hex):** 00		
Bit #	**Type**	**Description**
7	R/W	Write a 1 to decrement the recombiner delay of IMA Group #3. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
6	R/W	Write a 1 to increment the recombiner delay of IMA Group #3. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
5	R/W	Write a 1 to decrement the recombiner delay of IMA Group #2. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
4	R/W	Write a 1 to increment the recombiner delay of IMA Group #2. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
3	R/W	Write a 1 to decrement the recombiner delay of IMA Group #1. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
2	R/W	Write a 1 to increment the recombiner delay of IMA Group #1. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
1	R/W	Write a 1 to decrement the recombiner delay of IMA Group #0. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.
0	R/W	Write a 1 to increment the recombiner delay of IMA Group #0. The bit will return to 0 when the delay is adjusted. Writing a 0 has no effect.

Table 67 - Increment/Decrement Delay Control Register

Address (Hex):	**29D**
Direct access	**Used to initiate an update of the RX Delay registers based on the link and delay value to read**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:6	R/W	00: normal delay, 01: read pointer, 10: write pointer.
5	R/W	Writing a 1 will reset the value of the maximum delay over time register for the selected IMA Group (see bits 1:0).
4:3	R/W	Delay register: 11: Maximum Delay over time 10: Current Maximum Delay for an IMA Group 01: Current Minimum Delay for an IMA Group 00: Current Delay for a link
2:0	R/W	Bits 2:0 are used to specify the physical link number. Bits 1:0 are used to specify the IMA Group number.

Table 68 - RX Delay Select Register

Address (Hex):	**284**
Direct access	**This register contains the delay value (in number of cells) selected by the RX Delay Select Register. The value always include the current guardband delay**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:6	R/W	Unused. Read all 0's.
5:0	R/W	Delay Value (MSB)

Table 69 - RX Delay MSB Register

Address (Hex):	**285**
Direct access	**This register contains the delay value (in number of cells) selected by the RX Delay Select Register. The value always include the current guardband delay.**
Reset Value (Hex):	**04**

Bit #	Type	Description
7:0	R/W	Delay Value (LSB).

Table 70 - RX Delay LSB Register

Address (Hex):	**286**
Direct access	**This register contains the link number associated with the RX Delay value Register.**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:5	R/W	Reserved, write 0's for normal operation.
4:3	R/W	Write 1 to bit 4 and 0 to bit 3 for normal operation.
2:0	R	Number of the physical link associated with the value in the RX Delay register. This value is not valid when reading the Maximum Delay over time value is read.

Table 71 - RX Delay Link Number Register

Address (Hex):	**288, 28A, 28C, 28E**
Direct access in number of cells)	**1 value for each IMA Group to use for start-up and adding/removing delay (value**
Reset Value (Hex):	**04**

Bit #	Type	Description
7:0	R/W	LSB of the Guardband/Delay value Bits 7:0.

Table 72 - RX Guardband/Delta Delay LSB Register

Address (Hex):	**287, 289, 28B, 28D**
Direct access	**1 value for each IMA Group to use for start-up and adding/removing delay (value in number of cells)**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:6	R/W	Unused. Read 0 after reset.
5:0	R/W	MSB of the Guardband/Delay value Bits 13:8.

Table 73 - RX Guardband/Delta Delay MSB Register

Address (Hex):	**296, 298, 29A, 29C**
Direct access	**1 register per IMA Group (value in number of cells)**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R/W	LSB of the Maximum Operational Delay value Bits 7:0.

Table 74 - RX Maximum Operational Delay LSB Register

Address (Hex):	**295, 297, 299, 29B**
Direct access	**1 reg. per IMA Group (value in number of cells)**
Reset Value (Hex):	**00**

Bit #	Type	Description
7:6	R/W	Unused. Read 0 after reset.
5:0	R/W	MSB of the Maximum Operational Delay value Bits 13:8.

Table 75 - RX Maximum Operational Delay MSB Register

7.8 RX Recombiner Registers Description

Tables 76 to 80 describe the **RX Recombiner** registers.

Address (Hex):	**180 - 187**	
Direct access	**1 register per RX link**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:3	R	Unused. Read all 0's.
2	R/W	Recombiner Control: 1 to enable the recombiner and a 0 to disable. This bit works in conjunction with the RX Recombiner Delay register.
1:0	R/W	These 2 bits specify which IMA Group the link belongs to: 00: IMA Group #0 01: IMA Group #1 10: IMA Group #2 11: IMA Group #3.

Table 76 - RX Recombiner Registers

Address (Hex):	**282**	
Direct access	**1 register for all links. Note: the first link of a group SHALL NOT be enabled in delayed recombination mode**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 7 to the recombiner process. A 0 will include the link 7 in the recombiner as soon as it is enabled in the RX Recombiner register.
6	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 6 to the recombiner process. A 0 will include the link 6 in the recombiner as soon as it is enabled in the RX Recombiner register.
5	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 5 to the recombiner process. A 0 will include the link 5 in the recombiner as soon as it is enabled in the RX Recombiner register.
4	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 4 to the recombiner process. A 0 will include the link 4 in the recombiner as soon as it is enabled in the RX Recombiner register.
3	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 3 to the recombiner process. A 0 will include the link 3 in the recombiner as soon as it is enabled in the RX Recombiner register.
2	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 2 to the recombiner process. A 0 will include the link 2 in the recombiner as soon as it is enabled in the RX Recombiner register.
1	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 1 to the recombiner process. A 0 will include the link 1 in the recombiner as soon as it is enabled in the RX Recombiner register.
0	R/W	A 1 enables the circuitry to wait for the first User cells to be received before adding the link 0 to the recombiner process. A 0 will include the link 0 in the recombiner as soon as it is enabled in the RX Recombiner register.

Table 77 - RX Recombiner Delay Control Registers

Address (Hex):	29F
Direct access	
Reset Value (Hex):	00

Bit #	Type	Description
7:0	R/W	Each bit reports the recombination status for a link. A 1 means that the recombination is enabled. The bit 7 reports for link 7 and so on so forth. Do not write to this register.

Table 78 - Enable Recombination Status

Address (Hex):	188 - 18B
Direct access	1 register per IMA Group
Reset Value (Hex):	00

Bit #	Type	Description
7	R	Unused. Read 0.
6:4	R	Reserved.
3	R/W	When set to 1, it enables the automatic selection of the Reference link for the Group. When 0, the link specified in bits 2-0 is used as the reference link.
2:0	R/W	These 3 bits specify which physical link is to be used as the reference link for the IMA Group.

Table 79 - RX Reference Link Control Registers

Address (Hex):	18C - 18F
Direct access	1 register per IMA Group
Reset Value (Hex):	05

Bit #	Type	Description
7:4	R	Unused. Read all 0s.
3:0	R/W	Defines the integration period for an IMA Group 1111: Reserved. Do not use. 1110: 2^{21} clock cycles 1101: 2^{20} clock cycles 1100: 2^{19} clock cycles (preferred value for E1) 1011: 2^{18} clock cycles (preferred value for T1 - 24 channels) 1010: 2^{17} clock cycles 1001: 2^{16} clock cycles (preferred value for T1 - 23 channels) 1000: 2^{15} clock cycles 0111: 2^{14} clock cycles 0110: 2^{13} clock cycles 0101: 2^{12} clock cycles 0100: 2^{11} clock cycles 0011: 2^{10} clock cycles 0010: 2^{09} clock cycles 0001: 2^{08} clock cycles 0000: 2^{07} clock cycles

Table 80 - RX IDCR Integration Registers

7.9 TX/RX and PLL Control Registers Description

Tables 81 to 89 describe the **TX/RX and PLL Control** registers.

Address (Hex):	**080 - 087**	
Direct access	**1 reg. per TX link**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:5	R	Unused. Read all 0's.
4	R/W	TXCK and TXSYNC Direction: When the bit is 0 (default value) Mode 1: TXCK and TXSYNC are outputs Mode 2: TXCK and TXSYNC are inputs Mode 3: TXCK and TXSYNC are outputs Mode 4: TXCK and TXSYNC are inputs When the bit is 1 Mode 5: TXCK and TXSYNC are inputs Mode 6: TXCK and TXSYNC are outputs Mode 7: TXCK and TXSYNC are inputs Mode 8: TXCK and TXSYNC are outputs
3:0	R/W	These 4 bits are used to select the source for the TXCK for the link: The valid combinations are: 0000: RXCK0 0001: RXCK1 0010: RXCK2 0011: RXCK3 0100: RXCK4 0101: RXCK5 0110: RXCK6 0111: RXCK7 1000: REFCK0 1001: REFCK1 1010: REFCK2 1011: REFCK3

Table 81 - TX PCM Link Control Register Number 2

Address (Hex):	088 - 08F
Direct access	1 reg. per TX link
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	PCM port tri-state control. TXCLK, TXSYNC and DSTO outputs are active when the bit is 1. The outputs of the Port is in tri-state if the bit is 0.
6:5	R/W	00: T1, Generic Mode, 1.544MHz or 2.048 MHz Clk, (Mode 1 or 5) 01: T1, ST-BUS Mode, 4.096MHz Clk, (Mode 2 or 6) 10: E1, Generic Mode, 2.048 MHz clk, (Mode 3 or 7) 11: E1, ST-BUS Mode, 4.096MHz Clk, (Mode 4 or 8) The direction of the TXCK and TXSYNC signals (i.e.; input or output) is defined using the TX PCM Link Control register #2 bit 4.
4	R/W	This bit defines the PCM clock rate when one of the 2 T1 generic modes is selected. A 1 signifies that a 2.048 MHz clock is used and a 0 signifies that a 1.544 MHz clock is used. This bit is valid only for T1 Generic modes (PCM Mode 1 or 5).
3	R/W	This bit defines the position of the PCM channels over the PCM Stream. A value of 1 means that the 24 channels are grouped and transmitted in the first 24 channels on the PCM stream. A value of 0 corresponds to using 3 channels every 4 channels. This bit is valid only for T1 type link, in ST-BUS or Generic mode with a TXCK frequency of 2.048MHz. It is not applicable for T1, Generic mode with TXCK frequency of 1.544MHz.
2	R/W	T1 Signaling channel. A value of 1 disables the use of the channel 24 and reserves it for signaling. A value of 0 enables the use of the 24 channels to carry the cells. Valid only for T1 mode.
1	R/W	TX Clock polarity: Rising edge of TXCK is used to output new data on DSTo if bit is 1. Falling edge of TXCK is used to output new data on DSTo if bit is 0. Valid in Generic PCM mode only
0	R/W	TX frame pulse polarity. Positive if bit is 1, negative if bit is 0. Valid in Generic PCM mode only.

Table 82 - TX PCM Link Control Register Number 1

Address (Hex):	090 - 097
Direct access	1 register per RX link
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	PCM Input port control. Data present at input port is sent to the Cell Delineation block when the bit is 1. The data at the input port is ignored if the bit is 0.
6	R/W	Link Type: A value of 1 selects the E1 link type and 0 select T1 type.
5	R/W	PCM format: A value of 1 selects the ST-BUS mode and a 0 selects the Generic PCM mode.
4	R/W	This is the PCM clock rate when the generic mode is selected. A 1 signifies a 2.048 Mhz clock and a 0 signifies a 1.544 MHz clock. This is valid only for the T1 in Generic PCM mode.
3	R/W	This bit defines the position of the PCM channels over the PCM in Stream. A value of 1 means that the 24 channels are grouped and are received in the first 24 channels on the PCM stream. A value of 0 corresponds to 3 channels every 4 channels. Valid only for T1 type link, ST-BUS mode or Generic PCM mode with a bit rate of 2.048 Mbps.
2	R/W	T1 Signaling channel. A value of 1 disables the use of the channel 24 and reserves it for signaling. A value of 0 enables the use of the 24 channels to carry the cells. Valid only for T1 mode.
1	R/W	RX Clock polarity: Falling edge is used to sample data at DST if bit is 1. Rising edge of RXCK is used to sample data at DSTi if bit is 0. Valid in Generic PCM mode only
0	R/W	RX frame pulse polarity. Positive if bit is 1. Negative if bit is 0. Valid in Generic PCM mode only.

Table 83 - RX PCM Link Control Register

Address (Hex): 098 Direct access Reset Value (Hex): 00		
Bit #	**Type**	**Description**
7	R/W	Writing a 1 forces the deselecting of the selected clock when it failed.
6	R/W	Reserved. Set to 0 for normal operation.
5:3	R/W	These 3 bits are used to select the source for the signal at PLLREF1: The valid combinations are: 000: RXCK0 001: RXCK1 010: RXCK2 011: RXCK3 100: RXCK4 101: RXCK5 110: RXCK6 111: RXCK7
2:0	R/W	These 3 bits are used to select the source for the signal at PLLREF0: The valid combinations are: 000: RXCK0 001: RXCK1 010: RXCK2 011: RXCK3 100: RXCK4 101: RXCK5 110: RXCK6 111: RXCK7

Table 84 - PLL Reference Control Register

Address (Hex): 099 Direct access Reset Value (Hex): 00		
Bit #	**Type**	**Description**
7	R	Clock Running Status: Cleared by writing to this register, set by the running clock
6	R	Toggle on every transition of the selected clock
5	R/W	Reserved.Write 0 for normal operation.
4:0	R/W	These 5 bits are used to select the clock that is to be verified: The valid combinations are: 00000: REFCK0 00001: REFCK1 00010: REFCK2 00011: REFCK3 00100: TXCK0 00101: TXCK1 00110: TXCK2 00111: TXCK3 01000: TXCK4 01001: TXCK5 01010: TXCK6 01011: TXCK7 01100: RXCK0 01101: RXCK1 01110: RXCK2 01111: RXCK3 10000: RXCK4 10001: RXCK5 10010: RXCK6 10011: RXCK7

Table 85 - Clock Activity Register

Address (Hex): 09A Direct access 1 reg. for all 8 RX links Reset Value (Hex): 00		
Bit #	**Type**	**Description**
7	R/W	PCM RX Sync signal faulty on link 7. Cleared by writing ’0’.
6	R/W	PCM RX Sync signal faulty on link 6. Cleared by writing ’0’.
5	R/W	PCM RX Sync signal faulty on link 5. Cleared by writing ’0’.
4	R/W	PCM RX Sync signal faulty on link 4. Cleared by writing ’0’.
3	R/W	PCM RX Sync signal faulty on link 3. Cleared by writing ’0’.
2	R/W	PCM RX Sync signal faulty on link 2. Cleared by writing ’0’.
1	R/W	PCM RX Sync signal faulty on link 1. Cleared by writing ’0’.
0	R/W	PCM RX Sync signal faulty on link 0. Cleared by writing ’0’.

Table 86 - RX Sync. Status Register

Address (Hex):	09E
Direct access	1 reg. for all 8 RX links
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	PCM TX Sync signal faulty on link 7. Cleared by writing ’0’.
6	R/W	PCM TX Sync signal faulty on link 6. Cleared by writing ’0’.
5	R/W	PCM TX Sync signal faulty on link 5. Cleared by writing ’0’.
4	R/W	PCM TX Sync signal faulty on link 4. Cleared by writing ’0’.
3	R/W	PCM TX Sync signal faulty on link 3. Cleared by writing ’0’.
2	R/W	PCM TX Sync signal faulty on link 2. Cleared by writing ’0’.
1	R/W	PCM TX Sync signal faulty on link 1. Cleared by writing ’0’.
0	R/W	PCM TX Sync signal faulty on link 0. Cleared by writing ’0’.

Table 87 - TX Sync. Status Register

Address (Hex):	09C
Direct access	
Reset Value (Hex):	FF

Bit #	Type	Description
7	R	A ’1’ signifies that the TX Clock, link 7 is disabled.
6	R	A ’1’ signifies that the TX Clock, link 6 is disabled.
5	R	A ’1’ signifies that the TX Clock, link 5 is disabled.
4	R	A ’1’ signifies that the TX Clock, link 4 is disabled.
3	R	A ’1’ signifies that the TX Clock, link 3 is disabled.
2	R	A ’1’ signifies that the TX Clock, link 2 is disabled.
1	R	A ’1’ signifies that the TX Clock, link 1 is disabled.
0	R	A ’1’ signifies that the TX Clock, link 0 is disabled.

Table 88 - TX Clock Disabled Status

Address (Hex):	09D
Direct access	
Reset Value (Hex):	03

Bit #	Type	Description
7:2	R	Unused. Read 0’ss
1	R	A ’1’ signifies that the PLLREF1 Clock is disabled.
0	R	A ’1’ signifies that the PLLREF0 Clock is disabled.

Table 89 - PLL REF Clock Disabled Status/Device Rev

7.10 Counter Registers Description

Tables 90 to 94 describe the **Counter** registers

Address (Hex):	**214**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:0	R/W	A read accesses the MSB (byte 3) of the Counter selected in the Select Counter register. A write will hold the value to be written to the selected counter.

Table 90 - Counter Byte Number 3 Register

Address (Hex):	**215**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:0	R/W	A read accesses the byte #2 of the Counter that was selected in the Select Counter register. A write will hold the value to be written to the selected counter.

Table 91 - Counter Byte Number 2 Register

Address (Hex):	**216**	
Synchronized access	**The value in this register is used for internal access to the counter when the transfer command is issued**	
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:0	R/W	A read accesses the byte #1 (Least Significant Byte) of the Counter that was selected in the Select Counter register. A write will hold the value to be written to the selected counter.

Table 92 - Counter Byte Number 1 Register

Address (Hex):	217
Synchronized access	The value in this register is used for internal access to the counter when the transfer command is issued
Reset Value (Hex):	00

Bit #	Type	Description
7:4	R/W	The valid bit combinations are: 1011: UTOPIA Input, counter of all cells for link 1010: UTOPIA Input, counter of Idle cells for link 1001: UTOPIA Input, counter of Unassigned cells for link 1000: UTOPIA Input, counter of cell with HEC error, single or multiple bit error 0111: TX Link, total number of cells, 0110: TX Link, number of Idle/Filler cells, 0101: TX Link, number of Stuff cells, 0100: TX Link, number of ICP cells, 0011: RX Link, total number of cells (or stuff cells), 0010: RX Link, number of Idle/Filler cells, 0001: RX Link, number of cells with HEC errors, 0000: RX Link, number of bad ICP cells.
3:0	R/W	The valid bit combinations are: 1011: IMA Group 3 when UTOPIA Input counter access 1010: IMA Group 2when UTOPIA Input counter access 1001: IMA Group 1when UTOPIA Input counter access 1000: IMA Group 0when UTOPIA Input counter access 0111: Link 7 0110: Link 6 0101: Link 5 0100: Link 4 0011: Link 3 0010: Link 2 0001: Link 1 0000: Link 0

Table 93 - Select Counter Register

Address (Hex):	207
Synchronized access	
Reset Value (Bin):	0XX00000

Bit #	Type	Description
7	R/W	Write: 0 for normal operation. Read: 1 when the transfer is done, 0 when the transfer is pending.
6	R/W	Reserved, write 0 for normal operation.
5	R/W	Reserved, write 0 for normal operation.
4	R/W	Reserved, write 0 for normal operation.
3	R/W	Value to write to the Enable bit. 1 to enable, 0 to mask interrupt. This value is transferred when the bit 1:0 are 10.
2	R/W	0 will enable the transfer from the uP to the selected counter. 1 will enable the transfer from the selected counter to the uP.
1:0	R/W	00: Reserved. Do not use. 01: initiate a read or write of the counter value. 10: initiate a read or write of the IRQ enable counter bit. 11: not used.

Table 94 - Counter Transfer Command Register

7.11 Interrupt Registers Description

Tables 95 to 103 describe the **Interrupt** registers.

Address (Hex):	**232**
Direct access	
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R	Each bit represents a link. A ’1’ means that the corresponding link has a valid request for interrupt. The level of the IRQ pin is controlled by the bits in this register and the corresponding bits in the IRQ Master Enable Register. A write does not have any affect on the bits in this register. The status bit is not latched and changing the mask bit in the IRQ Master Register has a direct effect on the level of the IRQ pin.

Table 95 - IRQ Master Status Register

Address (Hex):	**218**
Direct access	
Reset Value (Hex):	**00**

Bit #	Type	Description
7:0	R/W	Each bit represents a link. A ’1’ means that the interrupt form the corresponding link is enabled and that the level of the IRQ pin is low if the corresponding bit in the IRQ Master Register is set. A ’0’ means that the IRQ level is not affected by the corresponding bit.

Table 96 - IRQ Master Enable Register

Address (Hex):	**222 - 229**
Direct access	**1 Status register per link**
Reset Value (Hex):	**00**

Bit #	Type	Description
7[a]	R	A ’1’ in this bit means that at least one of the IRQ sources from the IMA Group Overflow Status Register is requesting service. This bit can be cleared only by service the source of the IRQ. This bit is valid only for the IRQ Link 0 Status register and is reading always a 0 for the IRQ Link 1-7 Status registers.
6[b]	R/W	A 1 in this bit means that at least one of the Ready bit used to initiate a transfer of a TX ICP cell for at least 1 of the IMA Group is returned to 1 (meaning that the transfer of the TX ICP cell is complete) or a frame pulse was detected for an IMA Group. This bit is cleared by writing a 0 to it. This bit is valid only for the IRQ Link 0 Status register and is reading always a 0 for the IRQ Link 1-7 Status registers.
5	R/W	ICP Cell with changes received. The link has received an ICP cell which contain one or more changes in it. This status bit can be cleared by writing a ’0’ to it. This bit is set when an ICP cell is stored in RX ICP cell buffer as defined in RX ICP cell type RAM register 1or 2.
4	R/W	IV. The Link has received an ICP cell which contain a violation as defined in Table 16 of IMA Spec. This status bit can be cleared by writing a ’0’ to it.
3	R/W	LODS. The Link is Out of Delay Synchronization. This status bit can be cleared by writing a ’0’ to it.
2	R/W	LIF. Loss of IMA Frame. This status bit can be cleared by writing a ’0’ to it.
1	R/W	LCD Loss of Cell Delineation. This status bit can be cleared by writing a ’0’ to it.
0	R	Link Counter Overflow Interrupt. One or more counters associated with the link overflowed. This status bit can be cleared only by reading or writing to the counter(s) which is (are) the source for the IRQ.

Table 97 - IRQ Link Status Registers

a. Bit 7 is present only for Link 0. In all other Link Status Registers, this bit is set to 0.
b. Bit 6 is present only for Link 0. In all other Link Status Registers, this bit is set to 0.

Address (Hex):	219 - 220	
Direct access	1 Enable register per link Status reg	
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
7:0	R/W	Each bit set to '1' will enable the generation of the interrupt when the corresponding bit in the IRQ Link Status register is set.

Table 98 - IRQ Link Enable Registers

Address (Hex):	235	
Direct access		
Reset Value (Hex):	XD	
Bit #	**Type**	**Description**
7:4	R	Reserved.
3:0	R/W	Each bit set to '1' represent an overflow condition from the IMA Group associated with the bit. There is one bit for each IMA Group. A bit is set when one or more of the 4 counters or the RX UTOPIA FIFO associated with an IMA Group overflows.

Table 99 - IRQ IMA Group Overflow Status Register

Address (Hex):	204	
Direct access		
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
7:4	R	Unused. Should read 0's.
3:0	R/W	Each bit set to '1' will enable the generation of the interrupt when the corresponding bit in the IRQ IMA Group Overflow Status register is set. There is one bit for each status bit.

Table 100 - IRQ IMA Group Overflow Enable Register

Address (Hex):	210 - 213	
Direct access	1 register per IMA Group. The RxClk and TxClk signals must be active for correct register operation	
Reset Value (Hex):	00	
Bit #	**Type**	**Description**
7:5	R	Unused. Should read 0's.
4	R/W	This bit is set when the RX UTOPIA FIFO associated with an IMA Group overflows. This bit is cleared by writing 0.
3	R/W	This bit is set when the counter for all cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
2	R/W	This bit is set when the counter for Idle Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
1	R/W	This bit is set when the counter for Unassigned Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.
0	R/W	This bit is set when the counter for HEC Errored Cells associated with an IMA Group overflows. (Input UTOPIA port). This bit is cleared by writing 0.

Table 101 - IRQ IMA Overflow Status Registers

Address (Hex):	208 - 20F
Direct access register operation	1 register per link. The RxClk and TxClk signals must be active for correct
Reset Value (Hex):	00

Bit #	Type	Description
7:5	R	Unused. Should read 0's.
4	R/W	This bit is set when the RX UTOPIA FIFO associated with a Link in UNI mode overflows. This bit is cleared by writing 0.
3	R/W	This bit is set when the UTOPIA Input counter for all cells (or all Stuff cells event) associated with a link used in UNI mode overflows. This bit is cleared by writing 0.
2	R/W	This bit is set when the UTOPIA Input counter for Idle Cells associated with a link used in UNI mode overflows. This bit is cleared by writing 0.
1	R/W	This bit is set when the UTOPIA Input counter for Unassigned Cells associated with a link used in UNI mode overflows. This bit is cleared by writing 0.
0	R/W	This bit is set when the UTOPIA Input counter for HEC Errored Cells associated with a link used in UNI mode overflows. This bit is cleared by writing 0.

Table 102 - IRQ UTOPIA UNI Overflow Status Registers

Address (Hex):	22A - 231
Direct access register operation	1 register per link. The RxClk and TxClk signals must be active for correct
Reset Value (Hex):	00

Bit #	Type	Description
7	R/W	This bit is set when the TX PCM Link counter for all cells associated with a link used in overflows.
6	R/W	This bit is set when the TX PCM Link counter for Idle or Filler Cells associated with a link overflows.
5	R/W	This bit is set when the TX PCM Link counter for TX Stuff Cells associated with a link overflows.
4	R/W	This bit is set when the TX PCM Link counter for TX ICP Cells associated with a link overflows.
3	R/W	This bit is set when the RX PCM Link counter for all cells (or all Stuff cells event) associated with a link overflows.
2	R/W	This bit is set when the RX PCM Link counter for Idle or Filler Cells associated with a link overflows.
1	R/W	This bit is set when the RX PCM Link counter for HEC Errored Cells associated with a link overflows.
0	R/W	This bit is set when the RX PCM Link counter for bad ICP Cells associated with a link overflows.

Table 103 - IRQ Link UNI Overflow Status Registers

7.12 Miscellaneous Registers Description

Tables 104 to 106 describe the **General Status** and **Test Register**.

Address (Hex):	**206**	
Direct access		
Reset Value (Hex):	**10**	
Bit #	**Type**	**Description**
7:4	R	Device Revision Number: reads 0001.
3	R/W	Set when the UTOPIA output clock is missing or too slow. This latched bit is cleared by writing a 0.
2	R/W	Set when the UTOPIA input clock is missing or too slow. This latched bit is cleared by writing a 0.
1	R/W	Overflow of 1 or more of the TX UTOPIA FIFO.
0	R/W	Set when there is no free cell in TX Cell RAM. This latched bit is cleared by writing a 0.

Table 104 - General Status Register

Address (Hex):	**O4E**	
Direct access		
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:0	R	Reserved (different than written values).
7:0	W	Write 0x60 for normal operation.

Table 105 - Test 1 Register

Address (Hex):	**0DA**	
Direct access		
Reset Value (Hex):	**00**	
Bit #	**Type**	**Description**
7:0	R	Reserved (different from written values).
7	W	Write 0 for normal operation.
6	W	Write 1 for normal operation.
5:4	W	Write 00 for normal operation
3	W	Write 1 before adding a link to an existing IMA group. Write 0 when the link is reported in IMA mode.
2	W	Write 0 for normal operation.
1:0	W	Write IMA group number before adding a link to an IMA group.

Table 106 - Test 2 Register

8.0 Application Notes

Inverse Multiplexing for ATM (IMA) divides a high-bandwidth stream of ATM cells in a round-robin fashion and sends them over grouped T1/E1 lines in a logical connection (on public or private networks) and recombines the cells to recover the original high-bandwidth stream at the receiving end. Zarlink's MT90220 is ideally suited to implement the IMA function.

8.1 Connecting the MT90220 to Various T1/E1 Framers

Many off-the-shelf T1/E1 framers require the generation of a 1.544 MHz (T1) or 2.048 MHz (E1) transmit clock reference signal at an input pin. The MT9042 can generate both these clocks and the ST-BUS back-plane signals (C4,F0). Figure 19 provides an example of PCM Modes 2 and 4 in an IMA implementation using existing T1/E1 framers and a common 2 Mbps ST-Bus backplane.

New generation Zarlink framers only require the ST-BUS 4.096 MHz (C4) clock and a Frame Pulse (F0i) at the transmit interface. An internal PLL generates the required 1.544 MHz (T1) or 2.048 MHz (E1) transmit clock. Figure 20 provides an example of PCM Modes 2 and 4 in an IMA implementation based on the Zarlink MT90220 and the Zarlink MT9074 framers. This configuration supports CTC mode. Although the MT9074 use the ST-Bus format but it is not configured as a common backplane.

Figure 21 exemplifies PCM Modes 2 and 4 in an IMA implementation supporting the asynchronous link operation mode. Each T1 or E1 framer uses independent clock and synchronization signals which corresponds to ITC mode.

Figure 22 exemplifies PCM Modes 1 and 3 in an IMA implementation supporting the asynchronous link operation mode. Each T1 or E1 framer uses independent clock and synchronization signals.

Figure 23 exemplifies PCM Mode 5 and 7 in an IMA implementation supporting the asynchronous link operation mode where the TXCLK signal is provided by the T1 interface. Each T1 framer uses independent clock and synchronization signals.

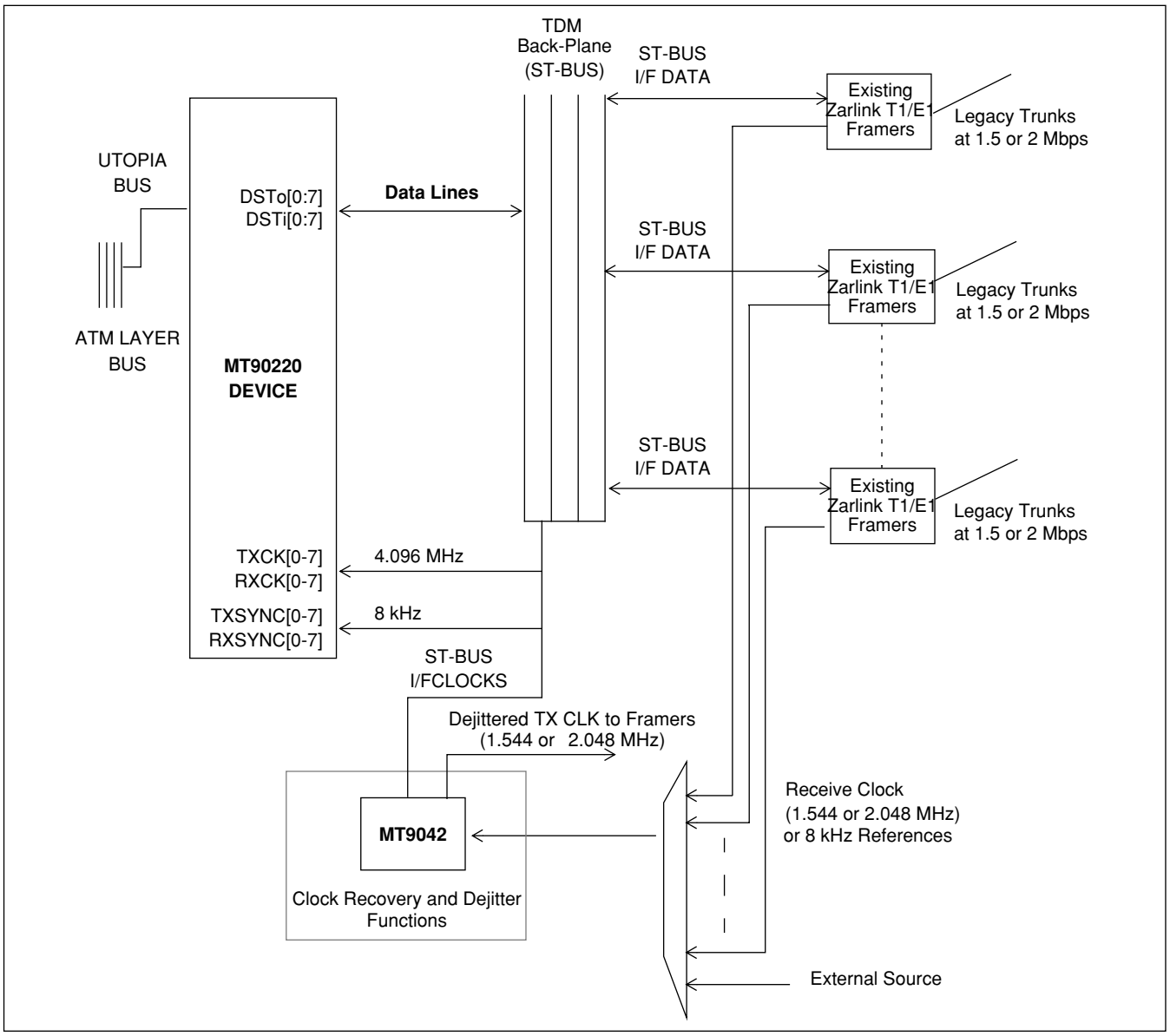


Figure 19 - PCM MODE 2 AND 4: Synchronous ST-BUS Mode (Using ST-BUS/2.048 Mbps Backplane Compatible Framers)

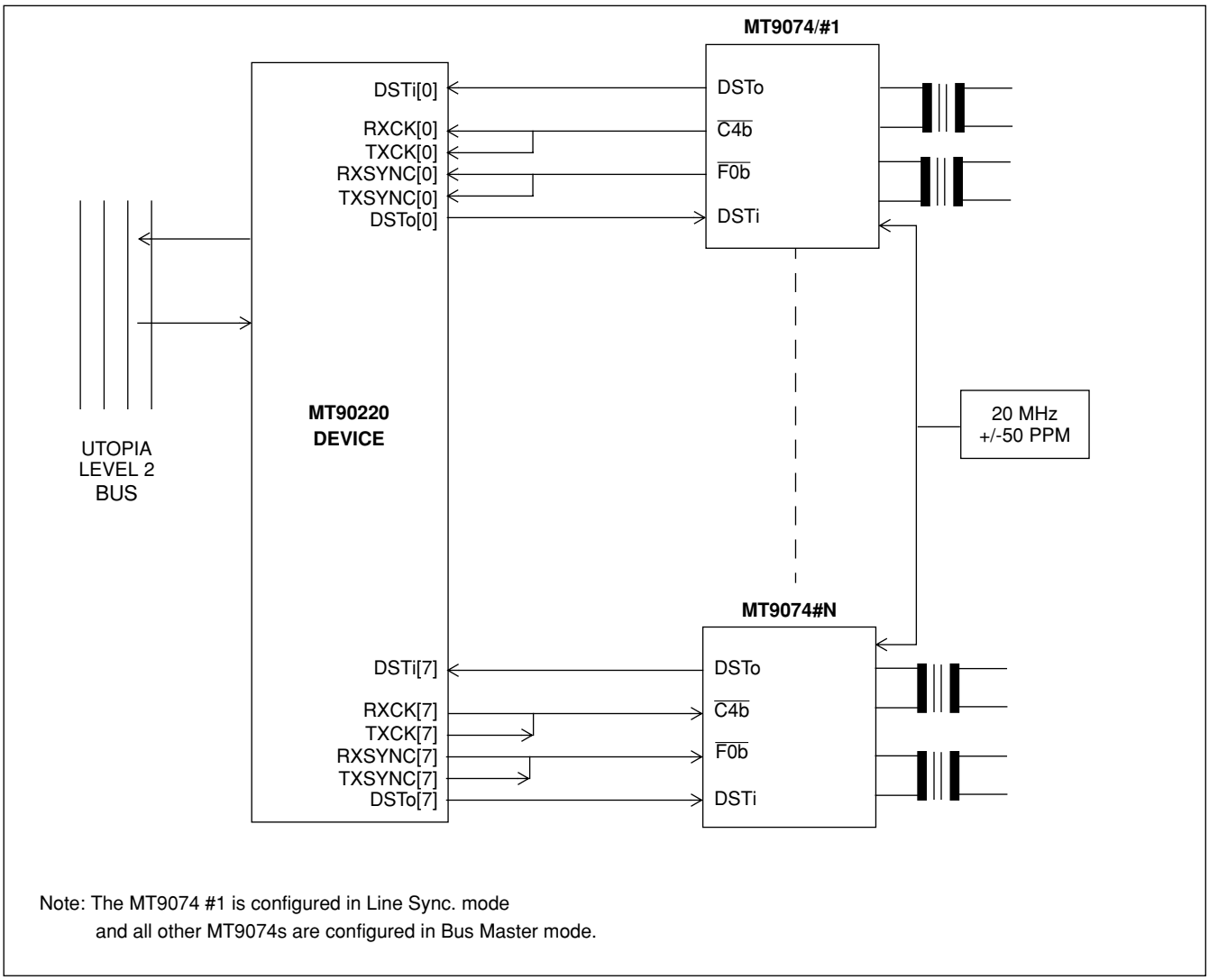


Figure 20 - PCM MODE 2 and 4 CTC Mode (Using MT9074 T1/E1 Single Chip Transceivers)

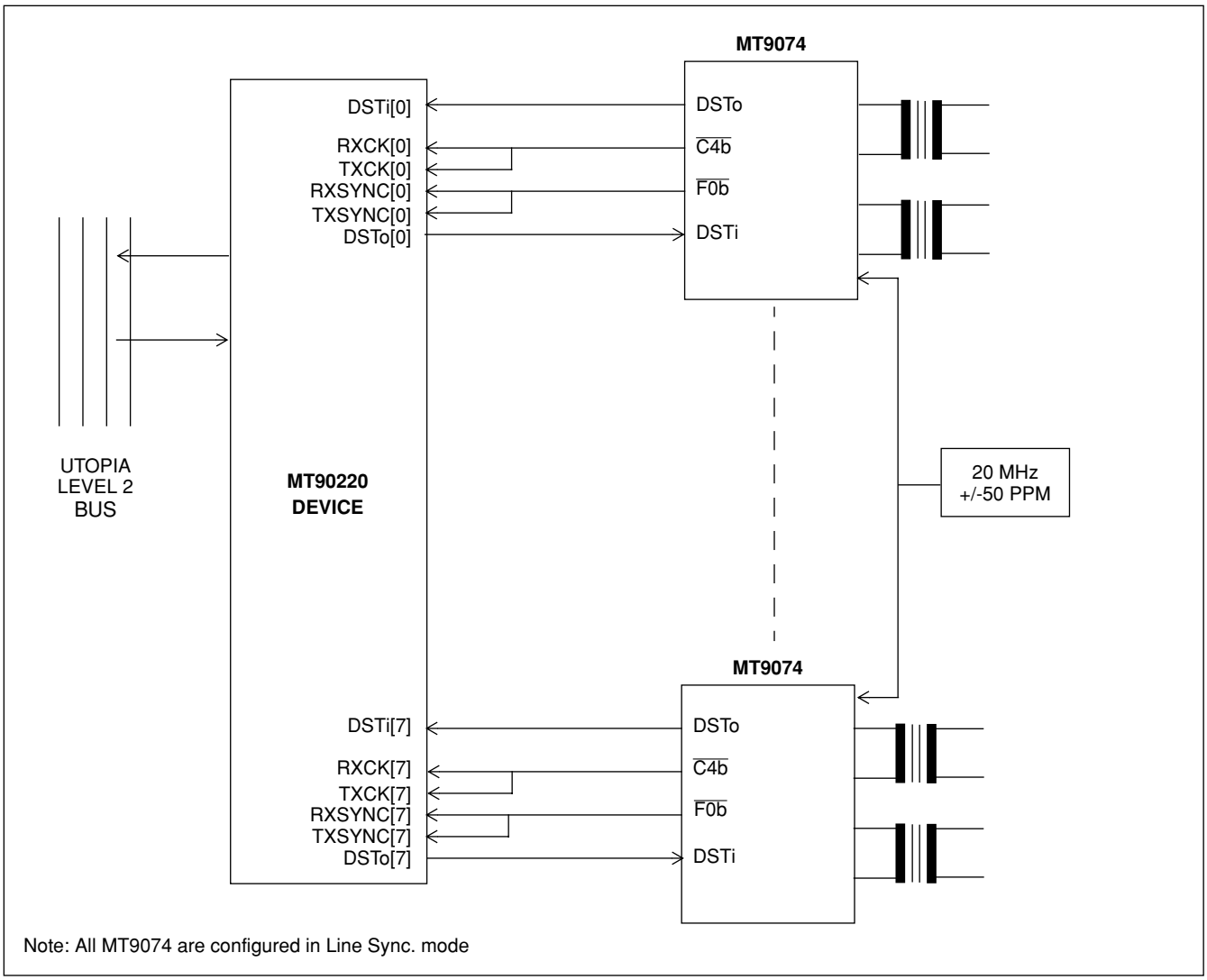


Figure 21 - PCM MODE 2 AND 4: ITC Mode
(Using Zarlink MT9074 T1/E1 Single Chip Transceivers)

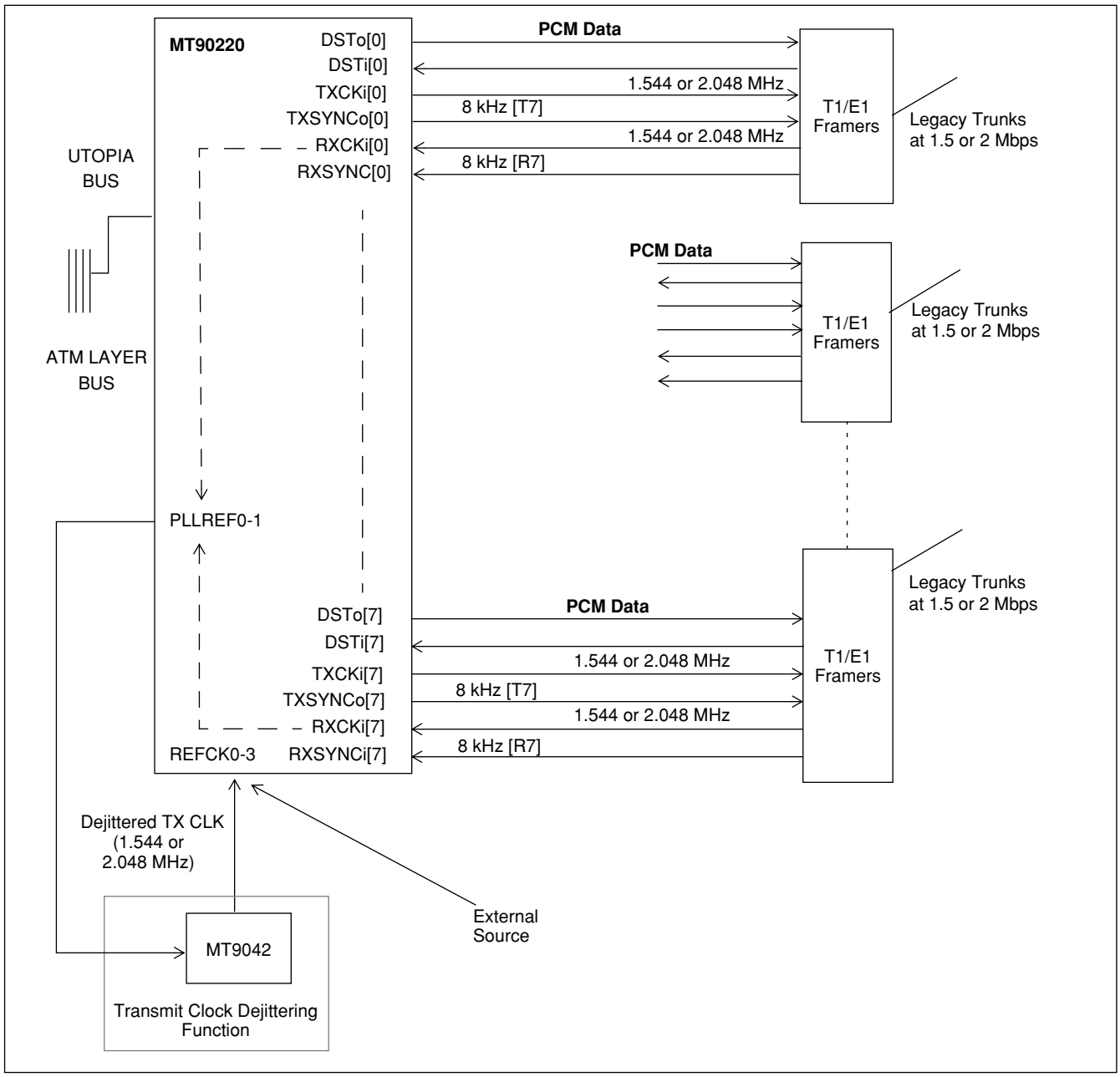
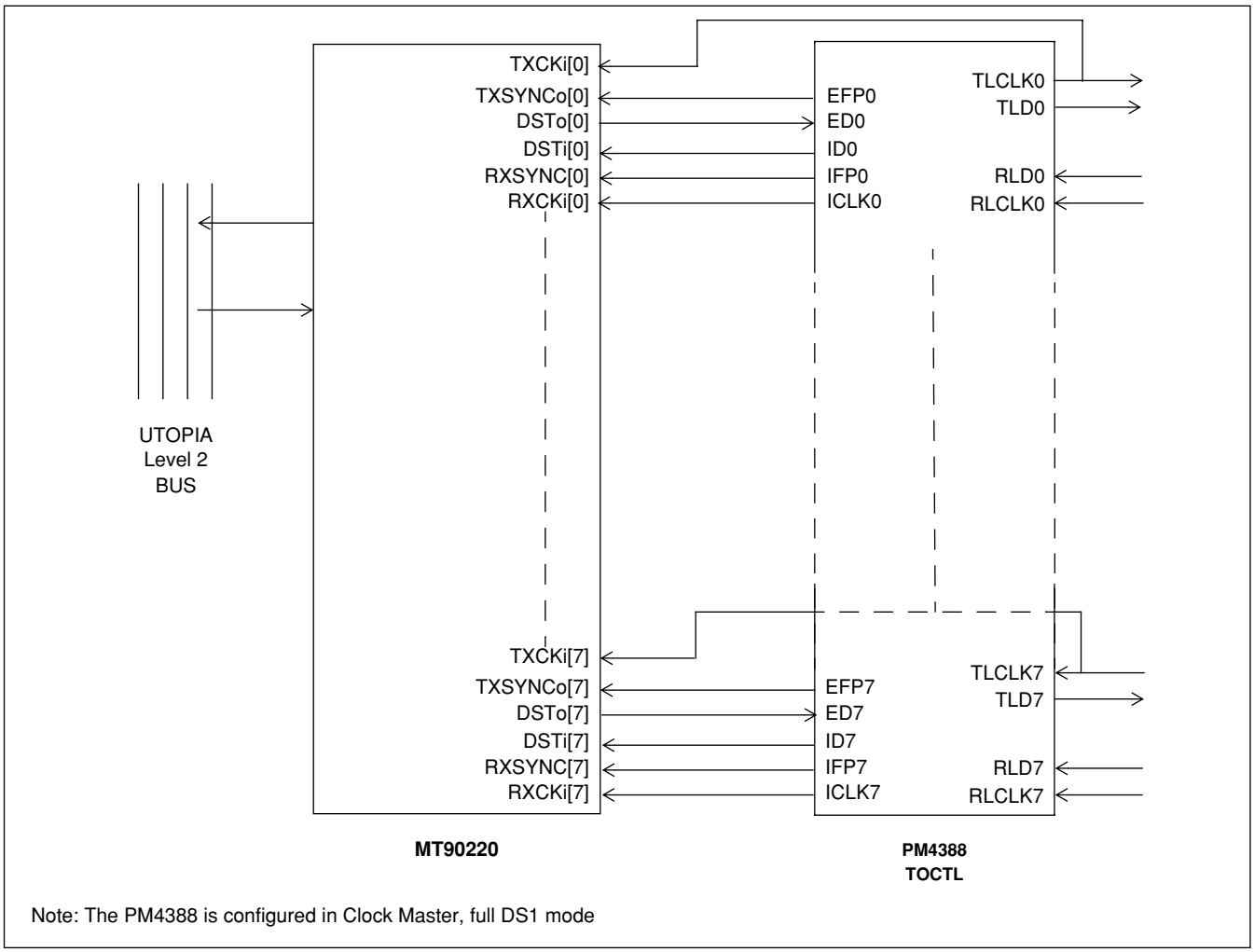


Figure 22 - PCM MODE 1 and 3: Generic PCM System Interface (For Applications with Asynchronous Lines)



Note: The PM4388 is configured in Clock Master, full DS1 mode

Figure 23 - PCM MODE 5 and 7: Asynchronous Operations (Using Octal T1 Framer)

9.0 AC/DC Characteristics

Absolute Maximum Conditions*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	3.9	V
2	Voltage at Digital Inputs	V_I	-1.0	6.5	V
3	Current at Digital Inputs	I_I	-10	10	mA
4	Storage Temperature	T_{ST}	-40	125	˚C

* Exceeding these values may cause permanent damage. Functional Operation under these conditions is not implied.
Note: Input pins are 5 Volt compatible type

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	˚C	
2	Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

‡ Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics* - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current	I_{DD}		150	300	mA	System Clock 25 MHz. PCM clock @ 2.048MHz
2	Input High Voltage (Digital Inputs)	V_{IH}	2.0		5.5	V	
3	Input Low Voltage (Digital Inputs)	V_{IL}	-0.5		0.8	V	
4	Input Leakage (Digital Inputs)	I_{IL}		1	10	µA	V_I = 0 to V_{DD}
5	Input Leakage	I_{IL}	-35	-115	-214	µA	For pins DSTi[7:0], REFCK[3:0], TXCKio[7:0], TXSYNC[7:0], RXSYNCi[7:0], RXCKi[7:0], TDI, TEST1, TMS, TCK
6	Input Leakage	I_{IL}	35	115	222	µA	For pin TEST2
7	Input Pin Capacitance	C_I			10	pF	
8	Output High Voltage (Digital Outputs)	V_{OH}	2.4			V	
9	Output High Current (Digital Outputs)	I_{OH}			-6	mA	Source V_{OH}=2.4 V, all output and bidirectional pins except External SRAM and PLLREF 0 and 1 interface pins.
10	Output High Current (Digital Outputs)	I_{OH}			-4	mA	Source V_{OH}=2.4 V, all External SRAM and PLLREF 0 and 1 interface pins
11	Output Low Voltage (Digital Outputs)	V_{OL}	V_{SS}		0.4	V	
12	Output Low Current (Digital Outputs)	I_{OL}	6			µA	Source V_{OL}=0.4 V, all output and bidirectional pins except External SRAM and PLLREF 0 and 1 interface pins.

DC Electrical Characteristics* - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
13	Output Low Current (Digital Outputs)	I_{OL}	4			mA	Source V_{OL}=0.4 V, all External SRAM and PLLREF 0 and 1 interface pins.
14	Output Pin Capacitance	C_O			10	pF	
15	High Impedance Leakage (Digital I/O)	I_{OZ}	-10	1	10	mA	V_O = 0 to V_{DD}

* DC Electrical Characteristics are over recommended temperature and supply voltage
‡ Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - PCM PORT ST-BUS Interface Mode - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristic	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C4i Clock Width High or Low	t_{4W}	110	122	134	ns	
2	C4i Clock Period	t_{4CYC}		244		ns	
3	Frame Pulse Setup	t_{FPS}	4			ns	
4	Frame Pulse Hold Time	t_{FPH}	1			ns	
5	DSTi 0-7 Serial Input Setup	t_{SIS}	3			ns	
6	DSTi 0-7 Serial Input Hold	t_{SIH}	0			ns	
7	DSTo 0-7 Serial Output Delay	t_{SOD}			25	ns	CL = 150pF
8	DSTo 0-7 Delay Active to High-Z	t_{DZ}			25	ns	CL = 150pF
9	DSTo 0-7 Serial High-Z to Active	t_{ZD}	0	10	25	ns	CL = 150pF

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

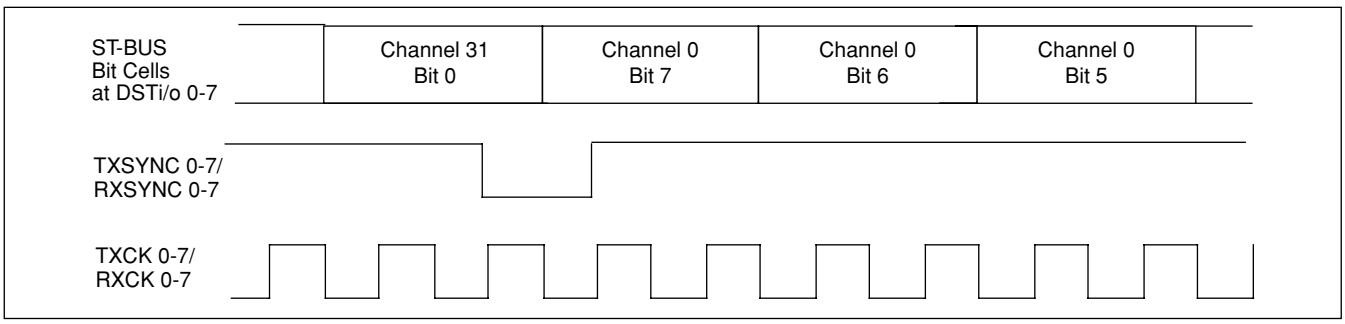


Figure 24 - ST-BUS Functional Timing Diagram

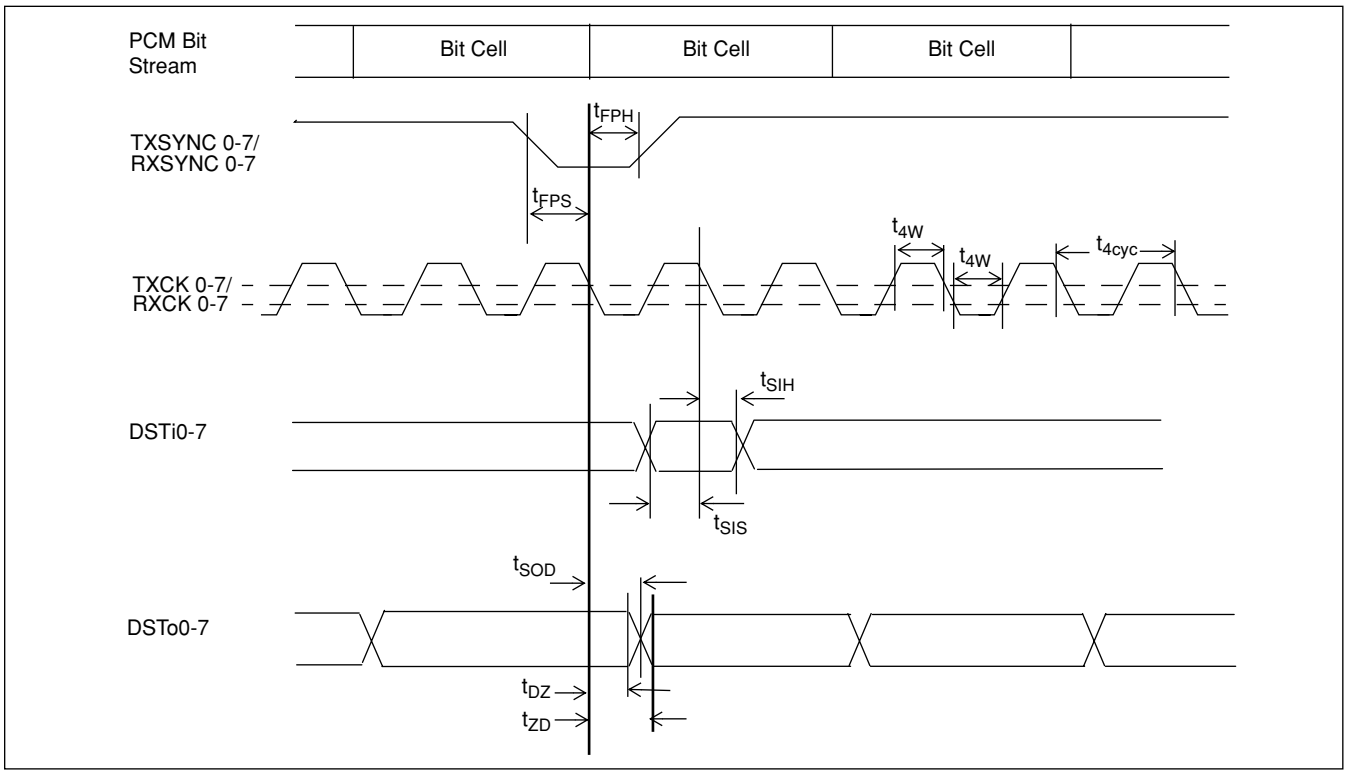


Figure 25 - ST-BUS Timing Diagram

AC Electrical Characteristics† - Generic PCM Interface Mode

	Characteristic	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TXCK/RXCK Clock period for T1, 1.544 MHz mode for E1, 2.048 MHz mode	tcyc		 648 488		ns	duty cycle 40 / 60%
2	TXCK/RXCK Clock Width High or Low for T1, 1.544 MHz mode for E1, 2.048 MHz mode	t_{4W}	 260 195			ns	
3	Frame Pulse Setup	t_{FPS}	4			ns	
4	Frame Pulse hold	t_{FPH}	1			ns	
5	DSTi 0-7 Serial Input Setup	t_{SIS}	3			ns	
6	DSTi 0-7 Serial Input Hold	t_{SIH}	0			ns	
7	DSTo 0-7 Serial Output Delay	t_{SOD}			25	ns	CL = 150pF
8	TXSYNC/RXSYNC Frame Pulse delay after TXCK/RXCK active border	t_{FPD}			25	ns	CL = 150pF
9	TXSYNC when input (PCM Mode 5 & 7) is sampled at the end of the bit period	t_{FPSi}	25ns		.5 t_{cyc}		
10	TXSYNC when input (PCM Mode 5 & 7) is sampled at the end of the bit period	t_{FPSH}			.5 t_{cyc}		

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=3.3V, and for design aid only: not guaranteed and not subject to production testing

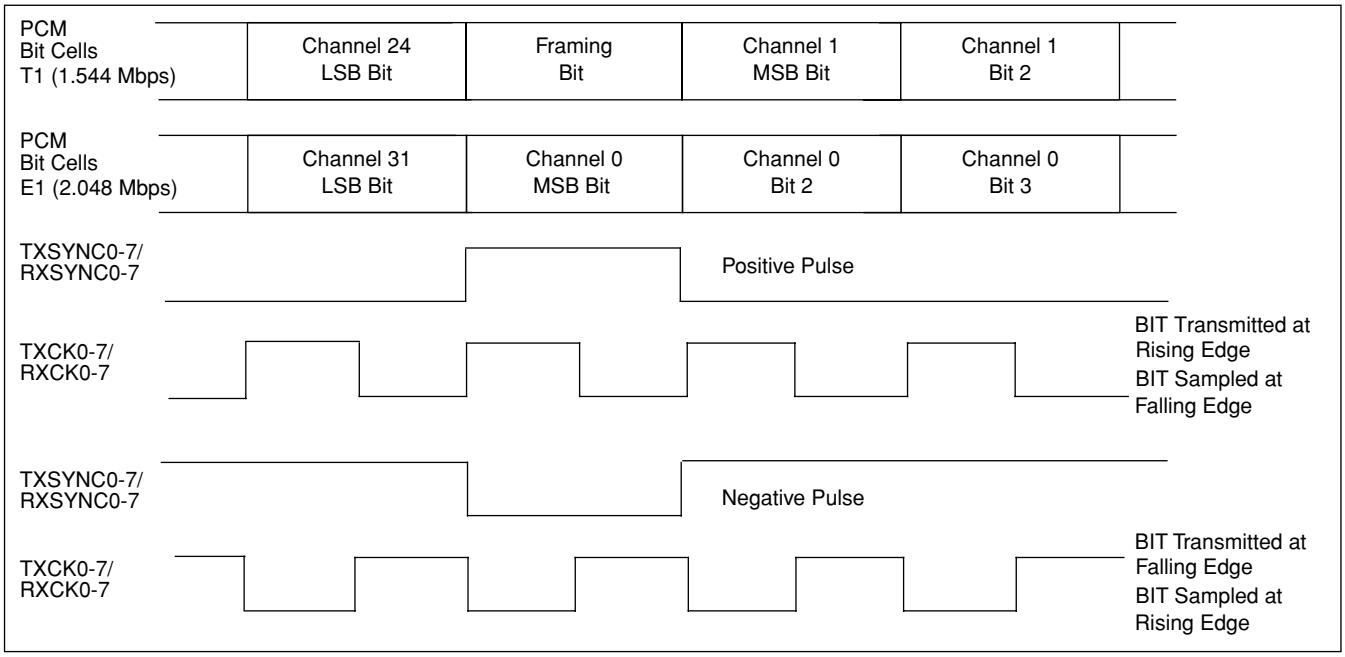


Figure 26 - Generic PCM Interface Timing Diagram (Frame Pulse Location)

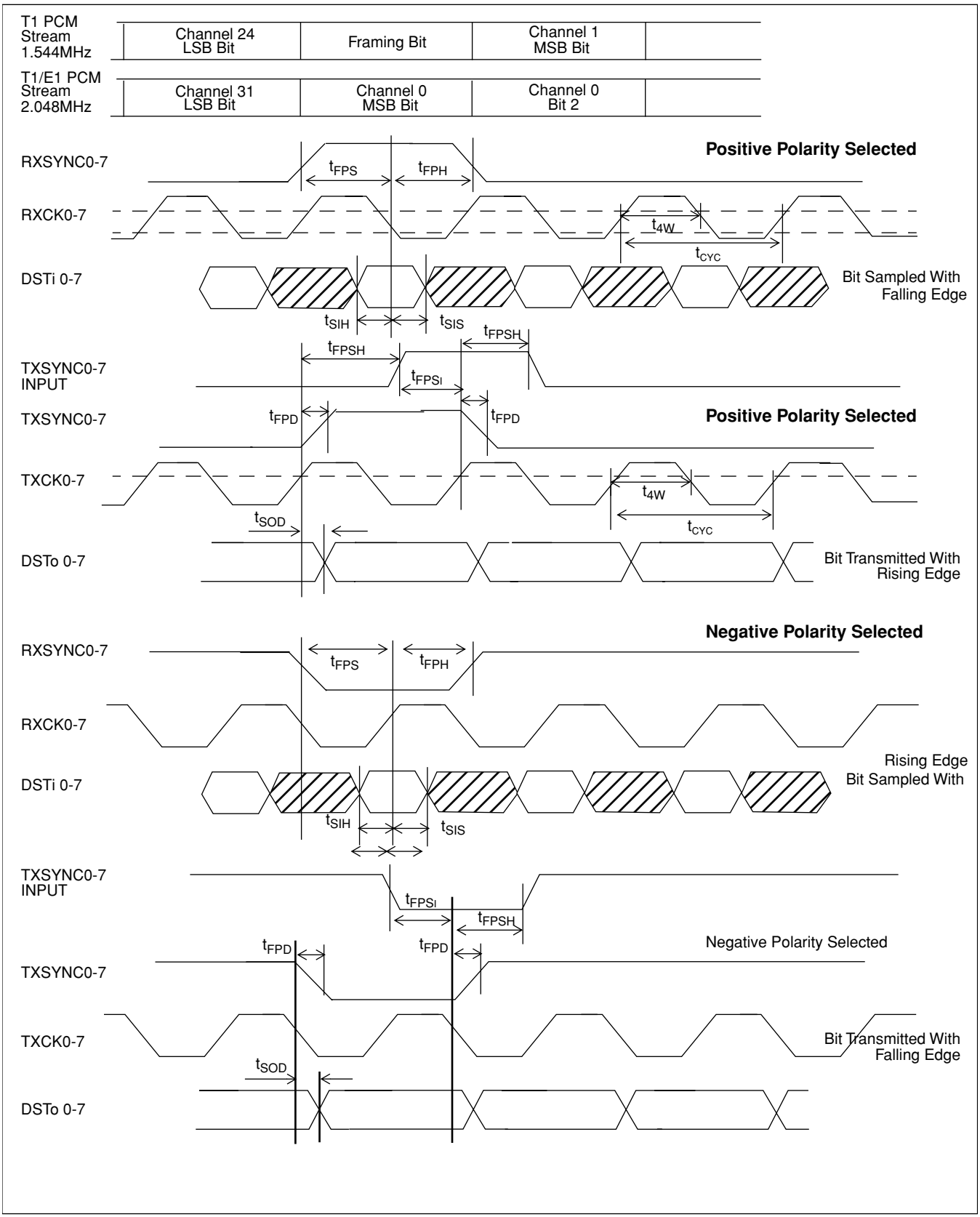


Figure 27 - Detailed Generic PCM Interface Timing Diagram

AC Electrical Characteristics - Utopia Interface Transmit Timing

Signal name	DIR	Item	Description	Min	Max
TxClk	A->P		TxClk frequency (nominal)	0	25 MHz
			TxClk duty cycle	40%	60%
			TxClk peak-to-peak jitter	-	5%
			TxClk rise/fall time	-	4 ns
TxData[7:0], TxSOC, $\overline{\text{TxEnb}}$*, TxAddr[4:0]	A->P	tT5	Input setup to TxClk	4 ns	-
		tT6	Input hold from TxClk	0 ns	-
TxClav[0]	A<-P	tT7	Input setup to TxClk	4 ns	-
		tT8	Input hold from TxClk	0 ns	-
		tT9	Signal valid	14 ns	-
		tT10	Signal going high impedance	14 ns	-
		tT11	Signal going low impedance from TxClk	3 ns	-
		tT12	Signal going high impedance from TxClk	3 ns	-

AC Electrical Characteristics - Receive Timing

Signal name	DIR	Item	Description	Min	Max
RxClk	A->P		RxClk frequency (nominal)	0	25 MHz
			RxClk duty cycle	40%	60%
			RxClk peak-to-peak jitter	-	5%
			RxClk rise/fall time	-	4 ns
$\overline{\text{RxEnb}}$*, RxAddr[4:0]	A->P	tT5	Input setup to RxClk	4 ns	-
		tT6	Input hold from RxClk	0 ns	-
RxData[7:0], RxSOC, RxClav[0]	A<-P	tT7	Input setup to RxClk	4 ns	-
		tT8	Input hold from RxClk	0 ns	-
		tT9[1]	Signal valid	18 ns	-
		tT10[1]	Signal going high impedance	18 ns	-
		tT11	Signal going low impedance from RxClk	3 ns	-
		tT12	Signal going high impedance from RxClk	3 ns	-

Note 1 - The RXCLK signal needs to be synchronous with the system clock refer to paragraph 5.2.

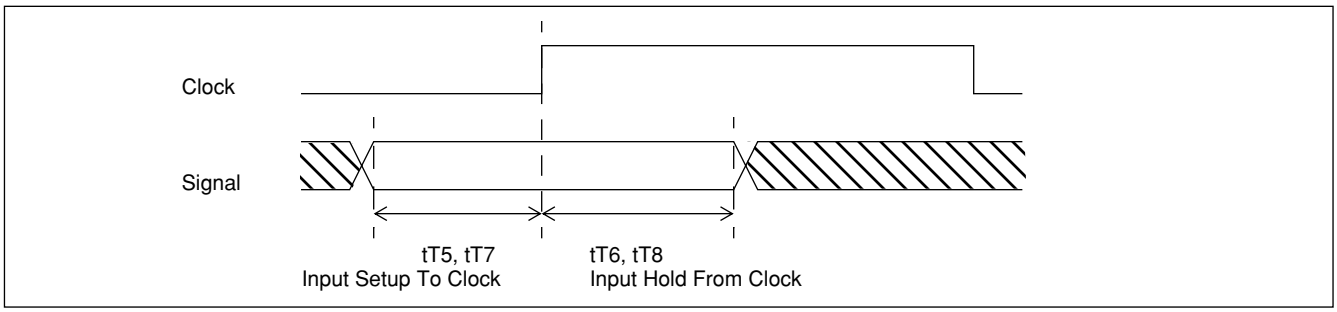


Figure 28 - Setup and Hold Time Definition

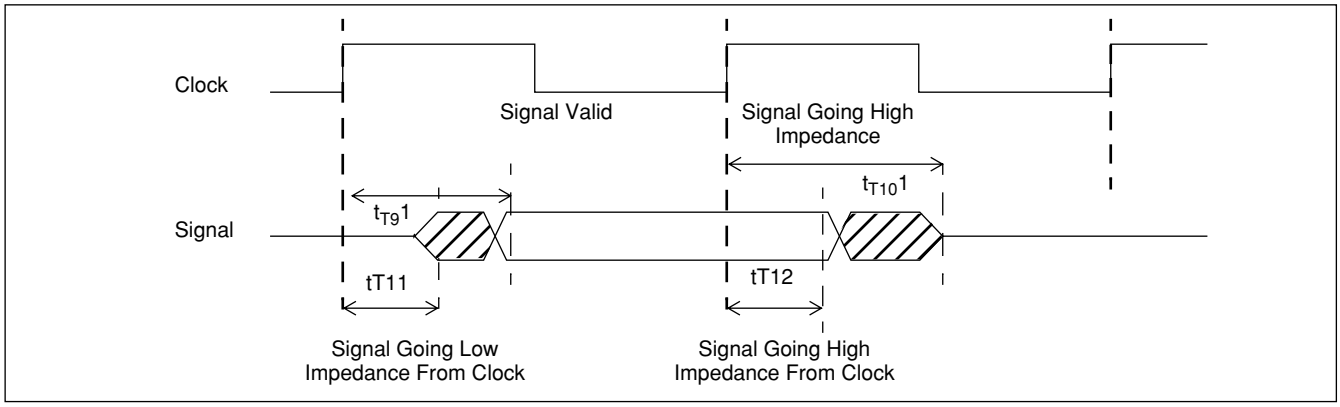


Figure 29 - Tri-State Timing

AC Electrical Characteristics - External Memory Interface Timing - Read Access

Item	Description	Min	Typ	Max
t_{CLK}	MT90220 System Clock Period	38 ns	40 ns	46 ns
t_{RC}	Read Cycle Time		30 ns	1 t_{CLK} -10 ns
t_{AVRS}	Address Setup Time			9 ns
t_{AVRH}	Address Hold Time	3 ns		
t_{CSRS}	Chip Select Setup Time			9 ns
t_{CSRH}	Chip Select Hold Time	3 ns		
t_{WERS}	Write Enable* Setup Time	9 ns		
t_{WERH}	Write Enable* Hold Time	3 ns		
t_{RDS}	Data Setup Time			0
t_{RDH}	Data Hold Time	3		

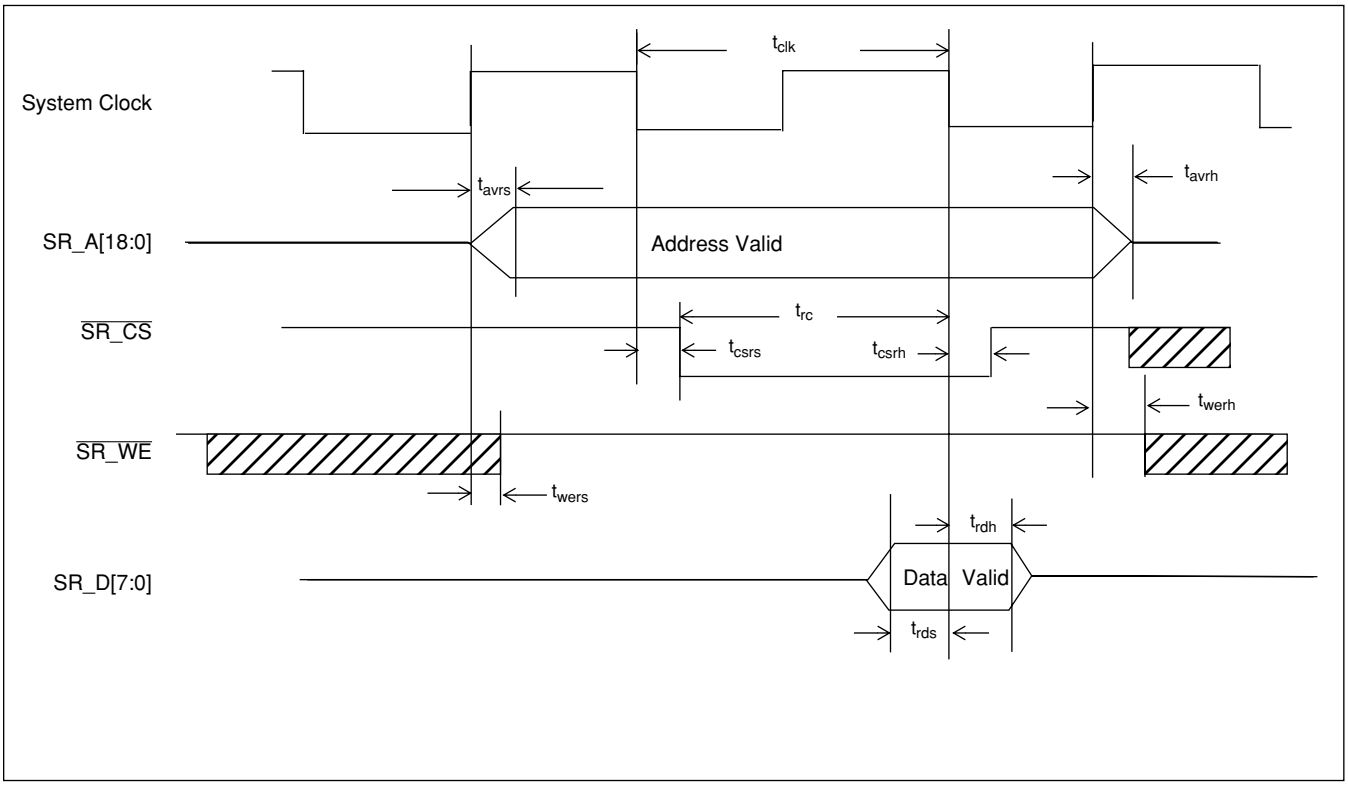
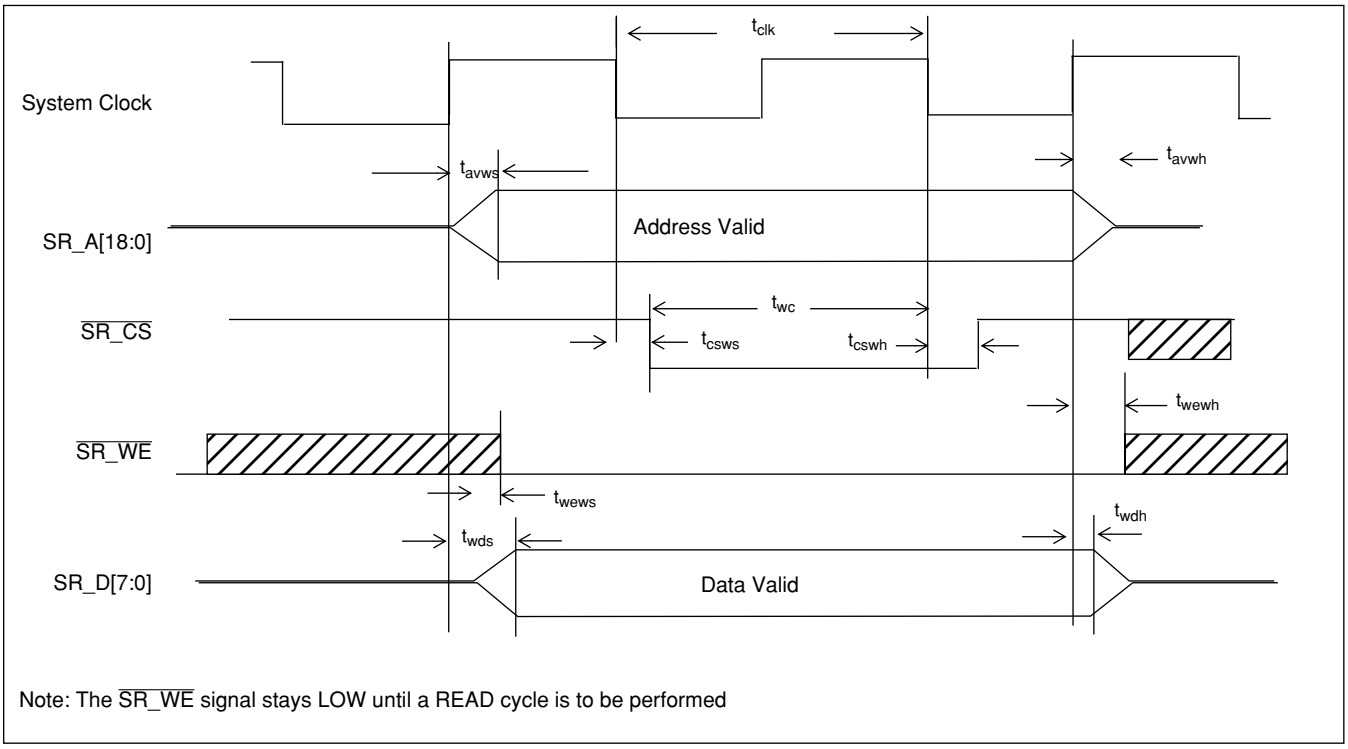


Figure 30 - External Memory Interface Timing - Read Cycle

AC Electrical Characteristics - External Memory Interface Timing - Write Access

Item	Description	Min	Typ	Max
t_{CLK}	System Clock Period	38	40 ns	46
t_{WC}	Write Cycle Time		30 ns	1 t_{CLK} -10 ns
t_{AVWS}	Address Setup Time			9 ns
t_{AVWH}	Address Hold Time	3 ns		
t_{CSWS}	Chip Select Setup Time			9 ns
t_{CSWH}	Chip Select Hold Time	3 ns		
t_{WEWS}	Write Enable* Setup Time	9 ns		
t_{WEWH}	Write Enable* Hold Time	3 ns		
t_{WDS}	Data Setup Time			13 ns
t_{WDH}	Data Hold Time	3 ns		



Note: The $\overline{SR\_WE}$ signal stays LOW until a READ cycle is to be performed

Figure 31 - External Memory Interface Timing - Write Cycle

9.1 CPU Interface Timing

The CPU Interface of the MT90220 supports both the Motorola and Intel timing modes. No Mode Select pin is required.

With Motorola devices, the Motorola R/W-signal is connected to the UP_R/W* pin and the UP_$\overline{OE}$* pin is tied to ground. There is no DS signal and the $\overline{UP\_CS}$* signal is taken to be qualified with the DS signal.

When used with Intel devices, the READ-signal is connected to the UP_$\overline{OE}$* pin and the WRITE-signal is connected to the UP_R/W* pin.

When performing a read operation, data is placed on the bus immediately after $\overline{UP\_CS}$* is LOW for the Motorola timing mode and after the $\overline{UP\_CS}$* and UP_$\overline{OE}$*signals are LOW for Intel timing.

When performing a write operation in Motorola timing mode, the data is clocked into an MT90220 pre-load register on the rising edge of the UP_CS* signal. In Intel timing mode, the data is clocked into MT90220 pre-load register on the rising edge of the UP_R/W* signal. Right after that transition, the data is transferred to the MT90220's internal register. Writing data into the this register can take up 2 system clock cycles.

AC Electrical Characteristics - CPU Interface Timing - Read Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	R/W set-up time to $\overline{\text{UP\_CS}}$* falling edge	t_{WS}	1			ns	
2	Data valid after UP_$\overline{\text{OE}}$*, $\overline{\text{UP\_CS}}$* or UP_AD	t_{ACC}			28	ns	
3	UP_AD or UP_R/W* hold time after $\overline{\text{UP\_CS}}$ rising edge	t_{AH}	0			ns	
4	Data hold time after rising edge of UP_CS or UP_$\overline{\text{OE}}$	t_{CH}	3			ns	
5	UP_D low impedance after falling edge of UP_$\overline{\text{OE}}$	t_{OE}	2.5		10	ns	

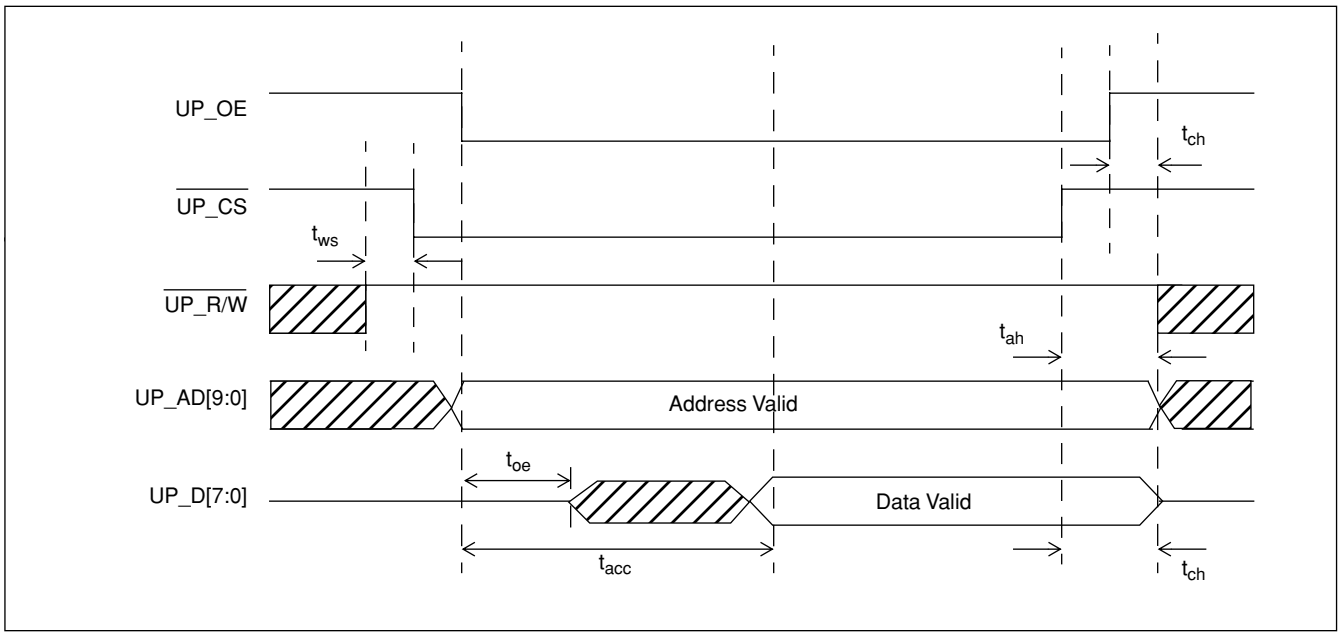


Figure 32 - CPU Interface Timing - Read Access

AC Electrical Characteristics - CPU Interface Motorola Timing - Write Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	UP_R/W* set-up time to $\overline{\text{UP\_CS}}$* falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of $\overline{\text{UP\_CS}}$*	t_{SU}	4			ns	
3	UP_AD and Data hold time after $\overline{\text{UP\_CS}}$ rising edge	t_{ADH}	0			ns	
4	UP_R/W low after rising edge or $\overline{\text{UP\_CS}}$	t_{WH}	1			ns	
5	$\overline{\text{UP\_CS}}$* high before next $\overline{\text{UP\_CS}}$ low	t_{CSH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

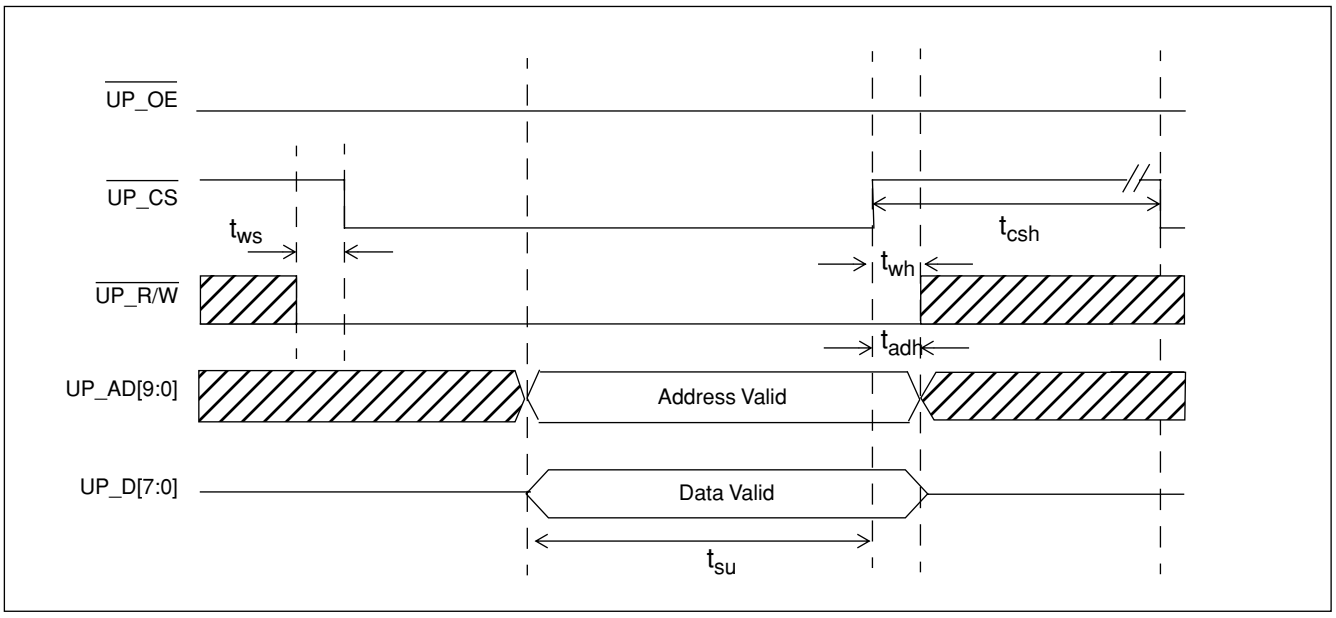


Figure 33 - CPU Interface Motorola Timing - Write Access

AC Electrical Characteristics - CPU Interface Intel Timing - Write Cycle

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	$\overline{\text{UP\_CS}}$* set-up time to UP_R/W* falling edge	t_{WS}	1			ns	
2	Address and Data set up before rising edge of UP_R/W	t_{SU}	4			ns	
3	UP_AD, $\overline{\text{UP\_CS}}$ and Data hold time after UP_R/W* rising edge	t_{ADH}	0			ns	
4	UP_R/W low after rising edge or $\overline{\text{UP\_CS}}$	t_{CSH}	1			ns	
5	$\overline{\text{UP\_CS}}$* high before next $\overline{\text{UP\_CS}}$ low	t_{WH}	2 (see Note 1)			cycle system clock	

Note 1 - For internal synchronization purposes, 2 system clock cycles are required between a write access and the next valid access.

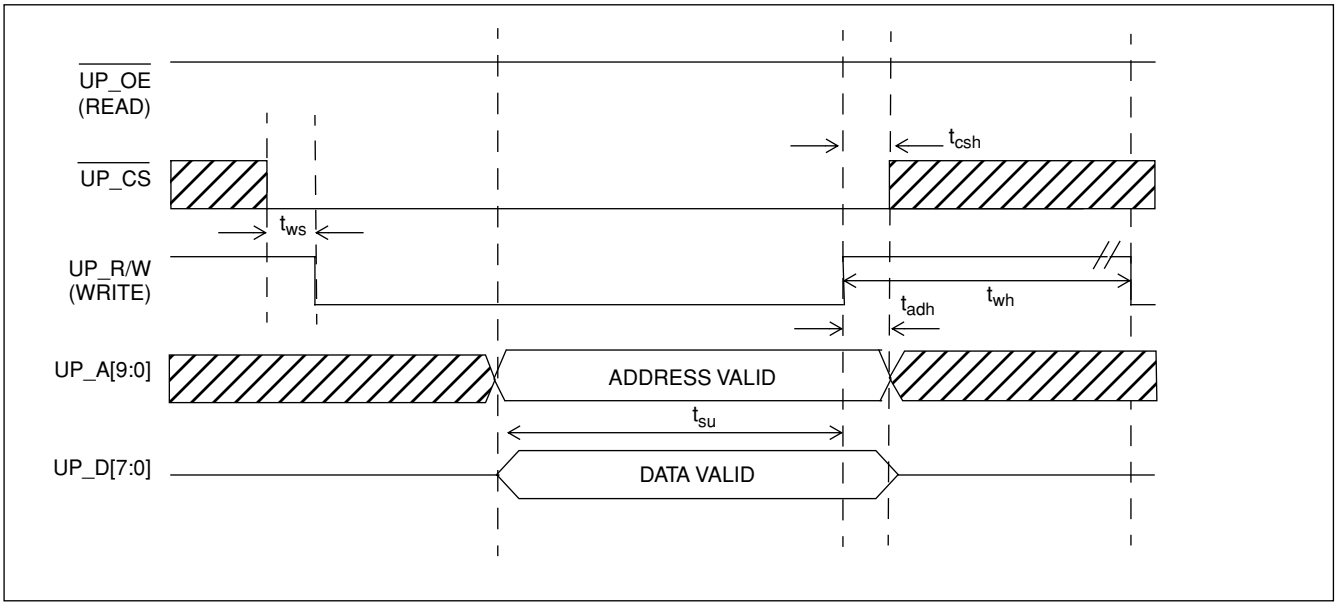


Figure 34 - CPU Interface Intel Timing - Write Access

AC Electrical Characteristics - JTAG Port and RESET Pin Timing

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
TCK period width	t_{TCLK}	100			ns	BSDL spec's 12 MHz
TCK period width LOW	t_{TCLKL}	40			ns	
TCK period width HIGH	t_{TCLKH}	40			ns	
TDI setup time to TCK rising	t_{DISU}	2			ns	
TDI hold time after TCK rising	t_{DIH}	33			ns	
TMS setup time to TCK rising	t_{MSSU}	2			ns	
TMS hold time after TCK rising	t_{MSH}	5			ns	
TDO delay from TCK falling	t_{DOD}			20	ns	C_L = 30 pF
$\overline{TRST}$ pulse width	t_{TRST}	15			ns	
RESET pulse width	t_{RST}	2			ms	70 MCLK cycles

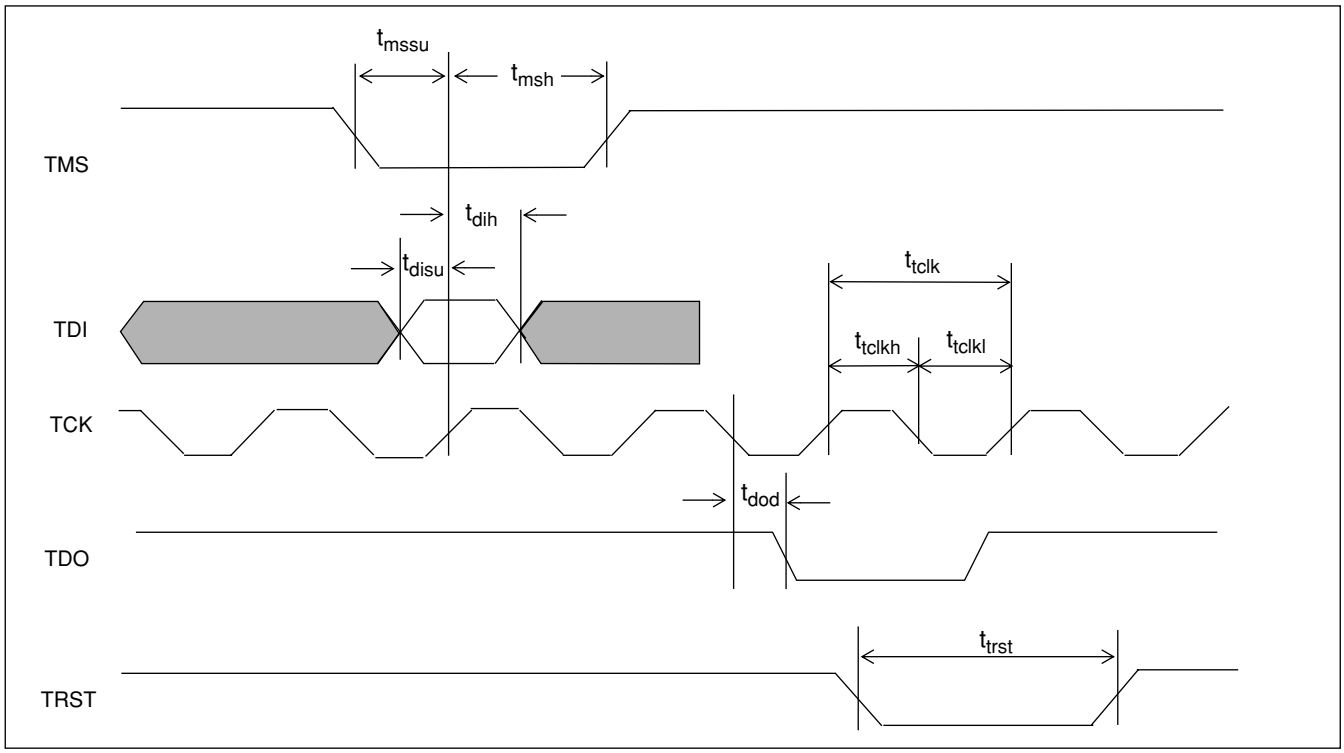


Figure 35 - JTAG Port Timing

AC Electrical Characteristics - System Clock and Reset

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
CLK period width	t_{TCLK}	38	40	46	ns	
CLK period width LOW	t_{TCLKL}		20		ns	
CLK period width HIGH	t_{TDKH}		20		ns	
CLK rising	t_{CLKR}			5	ns	
CLK falling	t_{CLKF}			5	ns	
$\overline{\text{RESET}}$ pulse width	t_{RST}	10			clk period	

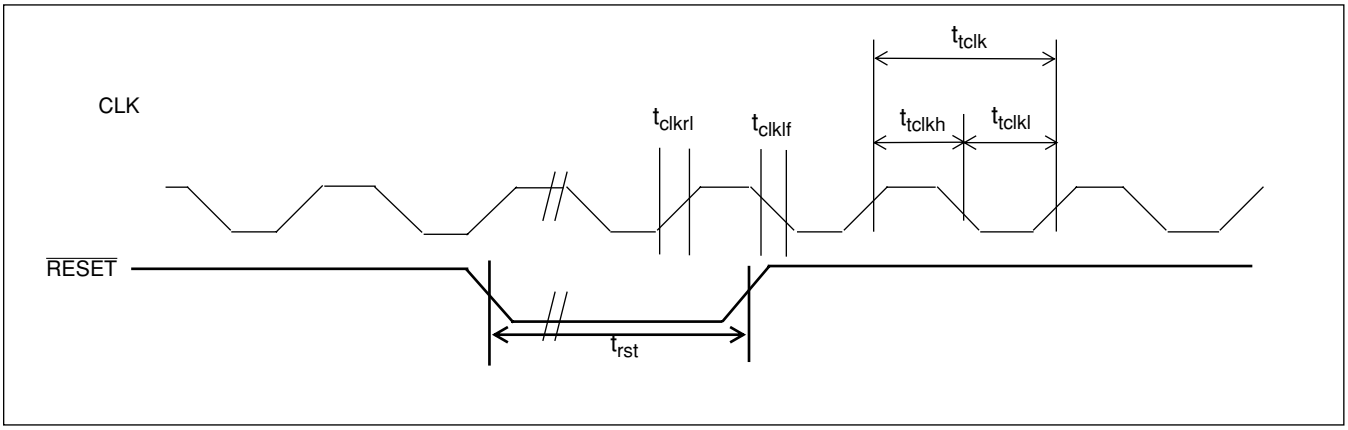
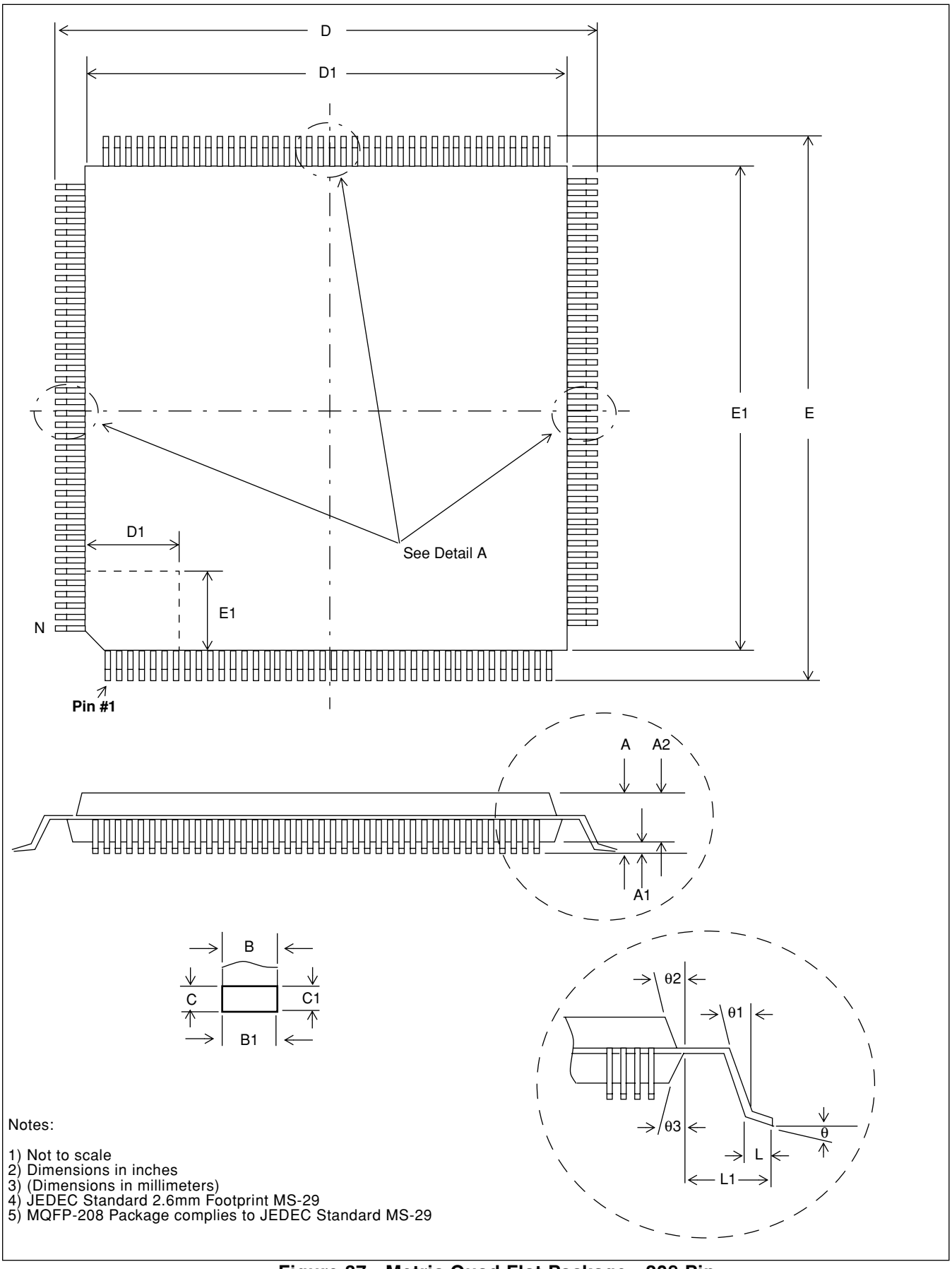


Figure 36 - System Clock and Reset



Notes:

1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) JEDEC Standard 2.6mm Footprint MS-29
5) MQFP-208 Package complies to JEDEC Standard MS-29

Figure 37 - Metric Quad Flat Package - 208 Pin

Dimensions	208-Pin	
	Min	Max
A		.161 (4.10)
A1	0.01 (0.25)	
A2	.126 (3.20)	.142 (3.60)
B	.007 (0.18)	.011 (0.28)
B1	.007 (0.18)	.009 (0.28)
C	.003 (0.076)	.008 (0.20)
C1	.003 (0.076)	.006 (0.152)
D	1.197 (30.40)	1.212 (30.80)
D1	1.098 (27.90)	1.106 (28.10)
e	.020 BSC (0.5 BSC)	
E	1.197 (30.40)	1.212 (30.80)
E1	1.098 (27.90)	1.106 (28.10)
L	.018 (0.45)	.030 (10.76)
L1	.051 REF (1.30 REF)	
θ	0	7
θ1	0	
θ2	5	16
θ3	5	16

Metric Quad Flat Package Dimensions

List of Changes

Page Numbers

Newer	Older	Change	Text
1	1	Replaced:	"Issue 3" with "Issue 4" and “3 April ” With: “4 December ”
2	2	Replaced:	“00 ” With: “001 ”
2	2	Replaced:	“0 ” With: “1 ”
3	3	Changed Content	
3	3	Inserted:	overbar above signals
4	4	Inserted:	overbar to TxEnb amd RxEnb
4	4	Deleted:	last line in Pin 203 Description
5	5	Inserted:	overbar to sr_we, sr_cs_1, 0, up_wr, up_oe, up_rd, up_cs, up_irq
5	5	Bolded Control Signal in Pin 198, 199	
5	5	Changed Interface in Pin 41 to Mode	
		Replaced:	the last sentence in Pin 41 to read, "De-asserting this signal to high will...
5	5	Replaced:	the last two sentences in Pin 39 to read, "De-asserting this signal to high will....
6	6	Replaced:	"2.048 Mbit/s" with "1.544 Mbps" and "1.533 Mbps" with "2.048 Mbits" in Pin 81, 88, 90, 97...
6	6	Replaced:	"2.048 Mbit/s" with "1.544 Mbps" and "1.533 Mbps" with "2.048 Mbits" in Pin 118, 124, 127...
6	6	Replaced:	"RXCK" with "TXCK"
6	6	Inserted :	"PCM in front of Section 4.2...in Pin 80, 87, 89....
6	6	Replaced:	"RXCK0" with "RXCKi" and replaced "C4" with "4.096 MHz" in Pin 120, 122, 129...
7	7	Replaced:	“TRISTATE ” With: “TMS ”
14	13	Replaced:	“The SCCI field is incremented …” With: “The SCCI field is incremented …”
14	14	Replaced:	“IMA Group ” With: “IMA ”
14	14	Inserted:	“(Note: The startup procedure …”
14	14	Replaced:	“sent.” With: “sent. Note that the Test …”
15	14	Replaced:	“disabling” With: “first disabling the source …”
16	16	Inserted:	“A value of 360 in …”
16	16	Inserted:	“The LCD status bit is …”
16	16	Deleted:	“A value of 360 in …”
18	17	Replaced:	“S/W ” With: “software ”
18	18	Inserted:	“The LIF status bit is …”
18	18	Replaced:	“7) ” With: “7, O-19 optional requirements) ”
18	18	Inserted:	"Valid ICP cell...."
19	19	Inserted:	“Mode ”
19	19	Replaced:	“register and ” With: “register, ”
19	19	Inserted:	“to 1 and the bit …”
19	19	Inserted:	"When this option... to the last paragraph of 3.3.7
20	20	Replaced:	“enable ” With: “enabled ”
20	20	Replaced:	“disruptions. ” With: “disruptions and the smallest allowed …”
20	20	Replaced:	“the ’programmed’” With: “the programmed ’”
20	20	Inserted:	"A delay is negative... after the first sentence in 3.3.10.3
21	20	Replaced:	“will go below the guardband ” With: “result in a negative delay ”
21	20	Inserted:	“Current ”
21	20	Replaced:	“delay ” With: “Delay ”
21	21	Replaced:	“registers):” With: “registers).”
21	21	Inserted:	“(Note: The startup procedure …”

22	21	Replaced:	“decreases” With: “decreases or”
22	22	Replaced:	“5 ” With: “6 ”
30	29	Replaced:	“used.” With: “used for any MT90220 port.”
30	30	Inserted:	“The cell available satus line (…”
30	30	Replaced:	“port. ” With: “port in MPHY mode. ”
31	31	Inserted:	“In this mode, the bit …”
34	32	Replaced:	“information:” With: “information and are active as …”
34	32	Replaced:	“link” With: “link, , with good or bad …”
38	37	Replaced:	“0EB” With: “0EF”
42	41	Replaced:	“ho ” With: “no ”
45	44	Replaced:	“Hex):” With: “Bin):”
47	46	Replaced:	“mode ” With: “mode (adaptive) algorithm ”
47	46	Replaced:	“mode ” With: “mode (fixed) algorithm”
51	51	Inserted:	"By the MT90220... in Cell Byte #14
60	59	Replaced:	“Write 01 ” With: “Write 00”
62	61	Replaced:	“Hex):” With: “Bin):”
75	73	Inserted:	"This bit is set... to Bit #5
79	77	Replaced:	"General Status register" with "General Status and Test Register
90	90	Updated:	Figure 27
93	91	Replaced:	“2 ” With: “1 ”
93	91	Removed:	2nd line of table
93	91	Figure updated for 2 clock cycles access time	
94	92	Replaced:	“2 ” With: “1 ”
94	92	Removed:	2nd line of table
94	92	Figure updated for 2 clock cycles access time	
99	97	Replaced:	“10” With: “5”
99	97	Replaced:	“10” With: “5”
99	97	Replaced:	“10 CLK period” With: “10”
99	97	Replaced:	“ns” With: “clk period”

List of Abbreviations and Acronyms

AAL	ATM Adaptation Layer
ATM	Asynchronous Transfer Mode
CBR	Constant Bit Rate
CDV	Cell Delay Variation
CPE	Customer Premises Equipment
CRC	Cyclic Redundancy Check
CTC	Common Transmit Clock
DSU	Data Service Unit
FE	Far End
GSM	Group State Machine
GTSM	Group Transmit State Machine
HEC	Header Error Control
IDCR	IMA Data Cell Rate
I/F	Interface
IFSM	Ima Frame State Machine
IMA	Inverse Multiplexing for ATM
ISDN	Integrated Services Digital Network
ITC	Independent Transmit Clock
LCD	Loss of Cell Delineation
LID	Link Identification
LIF	Loss of IMA Frame
LODS	Link Out of Delay Synchronization
LOF	Loss Of Frame
LOS	Loss of Signal
LSM	Link State Machines
M	IMA Frame Size
MIB	Management Information Base
MVIP	Multi-Vendor Integration Protocol
NE	Near End
OAM	Operations, Administration and Maintenance
OCD	Out of Cell Delineation (anomaly)
OIF	Out of IMA Frame (anomaly)
PDH	Plesiochronous Digital Hierarchy
PHY	Physical Layer
PMD	Physical Medium Dependent
QoS	Quality of Service
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
RFI	Remote Failure Indication
SAR	Segmentation and Reassembly
SCCI	Status and Control Change Indication
SOC	Start of Cell
TC	Transmission Convergence
TRL	Timing Reference Link
TRLCR	Timing Reference Link Cell Rate
UTOPIA	Universal Test and Operations Physical Interface for ATM
UNI	User Network Interface

ATM Glossary

Asynchronous Transfer Mode Adaptation Layer (AAL) - Standardized protocols used to translate higher layer services from multiple applications into the size and format of an ATM cell. Individual protocols are indexed as per the examples below:

AAL0 - Native ATM cell transmission proprietary protocol featuring 5-byte header and 48-byte user payload.

AAL1 - Used for the transport of constant bit rate, time-dependent traffic (e.g. voice, video); requires transfer of timing information between source and destination; maximum of 47-bytes of user data permitted in payload as an additional header byte is required to provide sequencing information.

AAL5 - Usually used for the transport of variable bit rate, delay-tolerant data traffic and signalling which requires little sequencing or error-detection support.

Active - This is a link state indicating the link is capable of passing ATM Layer cells in the specified direction.

Aligned - IMA Frames are said to be aligned if they are transmitted simultaneously.

Asynchronous

1. Not synchronous; not periodic.
2. The temporal property of being sourced from independent timing references, having different frequencies and no fixed phase relationship
3. In telecommunications, data which is not synchronized to the public network clock.
4. The condition or state of being unable to determine exactly when an event will transpire prior to its occurrence.

Asynchronous Transfer Mode (ATM) - A method of organizing information to be transferred into fixed-

length cells; asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic.

Note: Although ATM cells are transmitted synchronously to maintain the clock between sender and receiver, the sender transmits data cells on an as available basis and transmits empty cells when idle. The sender is not limited to transmitting data every Nth cell.

Blocked - The Blocked State is a Group State indicating that the Group has been inhibited.

Blocking - Blocking is a transitional state that allows graceful transition into the ***Unusable State*** without loss of ATM layer cells.

Cell - Fixed-size information package consisting of 53 bytes (octets) of data; of these, 5 bytes represent the cell header and 48 bytes carry the user payload and required overhead.

Cell Delay Variation (CDV) - a QoS parameter that measures the peak-to-peak cell delay through the network; results from buffering and cell scheduling.

Common Transmit Clock (CTC) Configuration - This is a configuration where the transmit clocks of all links within the IMA group are derived from the same clock source.

Constant Bit Rate - An ATM service category supporting a constant or guaranteed rate, with timing control and strict performance parameters. Used for services such as voice, video, or circuit emulation.

Filler Cell - A Filler Cell is used to fill in the IMA frame when no cells are available at the ATM layer. It is used for performing cell rate decoupling at the IMA sublayer (e.g., similar to the Idle Cell used in single link interfaces).

Header Error Control (HEC) - ATM equipment (usually the PHY) uses the fifth octet in the ATM cell header to check for an error and correct the contents of the header; CRC algorithm allows for single-error correction and multiple-error detection.

I.363 - ITU-T Recommendation specifying the AALs for B-ISDN.

IMA Frame - The IMA Frame is used as the unit of control in the IMA protocol. It is defined as M consecutive cells, on each of N links, where $1 \leq N \leq 32$ (determined by the UM and IMA link start-up procedure), in an IMA Group. One of the M cells on each of the N links is an ICP cell that occurs within the frame at the ICP cell offset position. This offset position may be different between links. The IMA Frame is ***Aligned*** on all links. Differential link delay can cause the reception to be 'mis-aligned' in time. Alignment can be recovered using a link delay synchronization mechanism. The ICP 'Stuff' mechanism is a controlled violation of the IMA consecutive frame definition.

IMA Group - The IMA Group is a 'group' of links at one end of a 'circuit' that establish an IMA virtual link to another end.

IMA Sublayer - The IMA Sublayer is part of the Physical Layer that is located between the interface specific Transmission Convergence Sublayer and the ATM Layer.

IMA Virtual Link - The IMA Virtual Link is a virtual circuit established between two IMA ends over a number of Physical Links (i.e., IMA Group).

Inhibiting - Inhibiting is a voluntary action that disables the capacity of a group or link to carry ATM Layer cells for reasons other than reported problems.

Insufficient Links - This is a Group State indicating that the group does not have sufficient links to be in the ***Operational*** State.

Independent Transmit Clock (ITC) Configuration - This is a configuration where the transmit clock of at least one link within the IMA Group is not derived from a common clock source.

Isochronous - The temporal property of an event or signal recurring at known periodic time intervals (e.g. 125 µs). Isochronous signals are dependent on some uniform timing, or carry their own timing information embedded as part of the signal. Examples are DS-1/T1 and E1. From the root words, "iso" meaning equal, and "chronous" meaning time.

ITU-T - International Telecommunications Union Telecommunications Standards Sector.

Layer Management Functions - The Layer Management Functions relate to processing of actions such as configuration, fault monitoring and performance monitoring within the group.

Loss of Cell Delineation (LCD) - The LCD defect is reported when the *OCD* anomaly persists for the period of time specified in ITU-T Recommendation I.432(30)$_3$. The LCD defect is cleared when the OCD anomaly has not been detected for the period of time specified in ITU-T Recommendation I.432.

LCD Remote Failure Indication (LCD-RFI) - The LCD-RFI is reported to the FE when a link defect is locally detected. The LCD-RFI defect is not always required on the link interface.

Link Delay Synchronization (LDS) - The LDS is an event indicating that the link is synchronized with the other links within the IMA Group with respect to differential delay.

Loss of IMA Frame (LIF) Defect - the LIF defect is the occurrence of persistent ***OIF*** anomalies for at least Gamma + 2 IMA Frames.

Link Out of Delay (LODS) Synchronization Defect - The LODS is a link event indicating that the link is not synchronized with the other links within the IMA Group.

Multi-Vendor Integration Protocol (MVIP) - MVIP standards are designed to support the inter-operability of products from different manufacturers and the portability of computer software between products from different manufacturers with the goal of facilitating new and improved applications of computer and communications equipment.

Out of Cell Delineation (OCD) Anomaly - As specified in ITU-T Recommendation I.432(30), an OCD anomaly is reported when ALPHA consecutive cells with incorrect HEC are received. It ceases to be reported when DELTA consecutive cells with correct HEC are received.

Out of IMA Frame (OIF) Anomaly - The OIF is the occurrence of an IMA anomaly as defined in the Inverse Multiplexing for ATM Specification.

Operational - The Operational State is a group state that has sufficient links in both the transmit and receive directions to carry ATM Layer cells.

Plesiochronous - The temporal property of being arbitrarily close in frequency to some defined precision. Plesiochronous signals occur at nominally the same rate, any variation in rate being constrained within specific limits. Since they are not identical, over the long term they will be skewed from each other. This will force a switch to occasionally repeat or delete data in order to handle buffer under-flow or overflow. (In telecommunications, this is known as a frame slip).

Physical Layer (PHY) - Bottom layer of the ATM Reference Model; provides ATM cell transmission over the physical interfaces that interconnect the various ATM devices.

Quality of Service (QoS) - ATM performance parameters that characterize the transmission quality over a given VC (e.g cell delay variation; cell transfer delay, cell loss ratio).

Stuff Event - The Stuff Event is the repetition of an ICP Cell over one IMA Link to compensate for a timing difference with other links within the IMA Group.

Synchronous 1. The temporal property of being sourced from the same timing reference. Synchronous signals have the same frequency, and a fixed (often implied to be zero) phase offset.

2. A mode of transmission in which the sending and receiving terminal equipment are operating continually at the same rate and are maintained in a desired phase relationship by an appropriate means.

Universal Test and Operations Physical Interface for ATM (UTOPIA) - A PHY-level interface to provide connectivity between ATM components.

Unusable - The Unusable State is a link state indicating that a link is not in use due to a fault, inhibition, etc.

Usable - The Usable State is a link state indicating the link is ready to operate in the specified direction, but is waiting to move to the ***Action*** State.

Virtual Channel (VC) - One of several logical connections defined within a virtual path (VP) between two ATM devices; provides sequential, unidirectional transport of ATM cells. Also *Virtual Circuit*.

Glossary References:

The ATM Glossary - ATM Year 97 - Version 2.1, March 1997

The ATM Forum Glossary - May 1997

ATM and Networking Glossary
(http://www.techguide.com/comm/index.html)

Zarlink Semiconductor Glossary of Telecommunications Terms - May 1995.

Notes:

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www.zarlink.com

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