National Semiconductor

August 1999

LMV821 Single/ LMV822 Dual/ LMV824 Quad Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

General Description

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.4 V/µs slew rate, the quiescent current is only 220 µA/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600 Ω Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5mV (Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

Features

(For Typical, 5 V Supply Values; Unless Otherwise Noted)

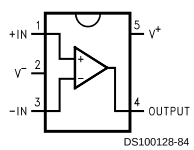
- Ultra Tiny, SC70-5 Package 2.0 x 2.0 x 1.0 mm
- Guaranteed 2.5 V, 2.7 V and 5 V Performance
- Maximum VOS 3.5 mV (Guaranteed)
- VOS Temp. Drift 1 uV/° C
- GBW product @ 2.7 V 5 MHz
- I_{Supply} @ 2.7 V 220 µA/Amplifier
- Minimum SR 1.4 V/us (Guaranteed)
- CMRR 90 dB
- PSRR 85 dB
- Rail-to-Rail (R-to-R) Output Swing
  — @600 Ω Load 160 mV from rail
  — @10 kΩ Load 55 mV from rail
- V_{CM} @ 5 V -0.3 V to 4.3 V
- Stable with High Capacitive Loads (Refer to Application Section)

Applications

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

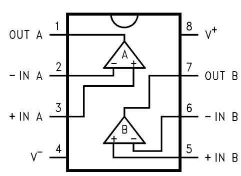
Connection Diagrams

5-Pin SC70-5/SOT23-5



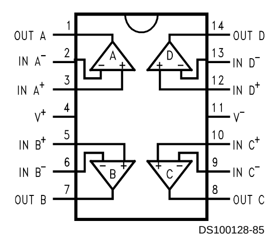
Top View

8-Pin SO/MSOP



Top View

14-Pin SO/TSSOP



Top View

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Ordering Information

Package	Temperature Range Industrial −40˚C to +85˚C	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC-70-5	LMV821M7	A15	1k Units Tape and Reel	MAA05
	LMV821M7X	A15	3k Units Tape and Reel	
5-Pin SOT23-5	LMV821M5	A14	1k UnitsTape and Reel	MA05B
	LMV821M5X	A14	3k Units Tape and Reel	
8-Pin SO	LMV822M	LMV822M	Rails	M08A
	LMV822MX	LMV822M	2.5k Units Tape and Reel	
8-Pin MSOP	LMV822MM	LMV822	1k Units Tape and Reel	MUA08A
	LMV822MMX	LMV822	3.5k Units Tape and Reel	
14-Pin SO	LMV824M	LMV824M	Rails	M14A
	LMV824MX	LMV824M	2.5k Units Tape and Reel	
14-Pin TSSOP	LMV824MT	LMV824MT	Rails	MTC14
	LMV824MTX	LMV824MT	2.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	$-40˚C \leq T_J \leq 85˚C$
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package 5-Pin Surface Mount	440 ˚C/W
Tiny SOT23-5 Package 5-Pin Surface Mount	265 ˚C/W
SO Package, 8-Pin Surface Mount	190 ˚C/W
MSOP Package, 8-Pin Mini Surface Mount	235 ˚C/W
SO Package, 14-Pin Surface Mount	145 ˚C/W
TSSOP Package, 14-Pin	155 ˚C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5 **4**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		μV/˚C
I_B	Input Bias Current		30	90 **140**	nA max
I_{OS}	Input Offset Current		0.5	30 **50**	nA max
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 1.7V$	85	70 **68**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$1.7V \leq V^+ \leq 4V$, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75 **70**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-1.0V \leq V^- \leq -3.3V$, V^+ =1.7V, V_O= 0V, V_{CM} = 0V	85	73 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V max
			2.0	1.9	V min
A_V	Large Signal Voltage Gain	Sourcing, R_L=600Ω to 1.35V, V_O=1.35V to 2.2V	100	90 **85**	dB min
		Sinking, R_L=600Ω to 1.35V, V_O=1.35V to 0.5V	90	85 **80**	dB min
		Sourcing, R_L=2kΩ to 1.35V, V_O=1.35V to 2.2V	100	95 **90**	dB min
		Sinking, R_L=2kΩ to 1.35, V_O=1.35 to 0.5V	95	90 **85**	dB min

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_O	Output Swing	V^+=2.7V, R_L= 600Ω to 1.35V	2.58	2.50 **2.40**	V min
			0.13	0.20 **0.30**	V max
		V^+=2.7V, R_L= 2kΩ to 1.35V	2.66	2.60 **2.50**	V min
			0.08	0.120 **0.200**	V max
I_O	Output Current	Sourcing, V_O=0V	16	12	mA min
		Sinking, V_O=2.7V	26	12	mA min
I_S	Supply Current	LMV821 (Single)	0.22	0.3 **0.5**	mA max
		LMV822 (Dual)	0.45	0.6 **0.8**	mA max
		LMV824 (Quad)	0.72	1.0 **1.2**	mA max

2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.5V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.25V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5 **4**	mV max
V_O	Output Swing	V^+=2.5V, R_L= 600Ω to 1.25V	2.37	2.30 **2.20**	V min
			0.13	0.20 **0.30**	V max
		V^+=2.5V, R_L= 2kΩ to 1.25V	2.46	2.40 **2.30**	V min
			0.08	0.12 **0.20**	V max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	1.5		V/µs
GBW	Gain-Bandwdth Product		5		MHz
Φ_m	Phase Margin		61		Deg.
G_m	Gain Margin		10		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	28		$\frac{nV}{\sqrt{Hz}}$

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
i_n	Input-Referred Current Noise	f = 1 kHz	0.1		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5 **4.0**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/˚C
I_B	Input Bias Current		40	100 **150**	nA max
I_{OS}	Input Offset Current		0.5	30 **50**	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V	90	72 **70**	dB min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75 **70**	dB min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ =1.7V, V_O = 0V, V_{CM} = 0V	85	73 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V max
			4.3	4.2	V min
A_V	Large Signal Voltage Gain	Sourcing, R_L=600Ω to 2.5V, V_O=2.5 to 4.5V	105	95 **90**	dB min
		Sinking, R_L=600Ω to 2.5V, V_O=2.5 to 0.5V	105	95 **90**	dB min
		Sourcing, R_L=2kΩ to 2.5V, V_O=2.5 to 4.5V	105	95 **90**	dB min
		Sinking, R_L=2kΩ to 2.5, V_O=2.5 to 0.5V	105	95 **90**	dB min
V_O	Output Swing	V^+=5V,R_L= 600Ω to 2.5V	4.84	4.75 **4.70**	V min
			0.17	0.250 **.30**	V max
		V^+=5V, R_L=2kΩ to 2.5V	4.90	4.85 **4.80**	V min
			0.10	0.15 **0.20**	V max

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 **Limit** (Note 6)	Units
I_O	Output Current	Sourcing, V_O=0V	45	20	mA
				15	min
		Sinking, V_O=5V	40	20	mA
				15	min
I_S	Supply Current	LMV821 (Single)	0.30	0.4	mA
				0.6	max
		LMV822 (Dual)	0.5	0.7	mA
				0.9	max
		LMV824 (Quad)	1.0	1.3	mA
				1.5	max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. V^+ = 5V, V^- = 0V, V_{CM} = 2V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	2.0	1.4	V/µs min
GBW	Gain-Bandwdth Product		5.6		MHz
Φ_m	Phase Margin		67		Deg.
G_m	Gain Margin		15		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	24		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.25		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series wth 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 45 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

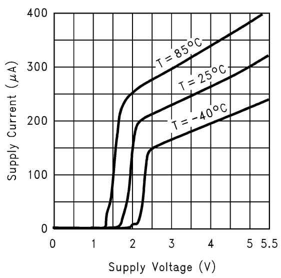
Note 7: V^+ = 5V. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Input referred, V^+ = 5V and R_L = 100 kΩ connected to 2.5V. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}.

5V AC Electrical Characteristics (Continued)

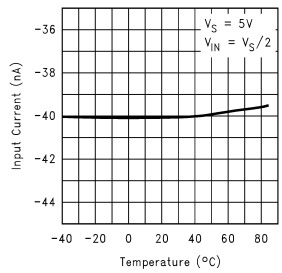
Typical Performance Characteristics
Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs Supply Voltage (LMV821)



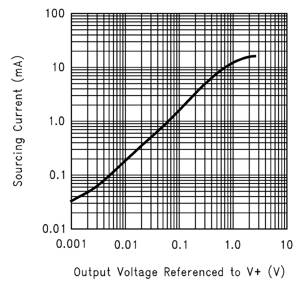
DS100128-1

Input Current vs Temperature



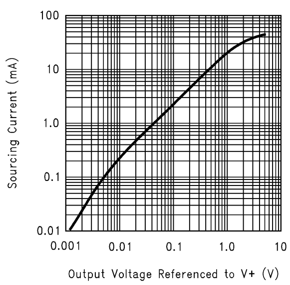
DS100128-2

Sourcing Current vs Output Voltage (V_S=2.7V)



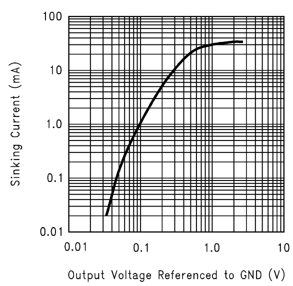
DS100128-3

Sourcing Current vs Output Voltage (V_S=5V)



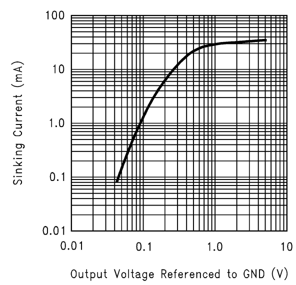
DS100128-4

Sinking Current vs Output Voltage (V_S=2.7V)



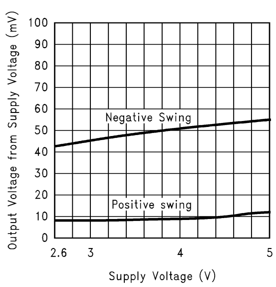
DS100128-5

Sinking Current vs Output Voltage (V_S=5V)



DS100128-6

Output Voltage Swing vs Supply Voltage (R_L=10kΩ)



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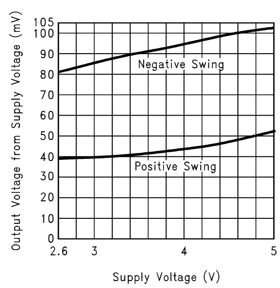
Output Voltage Swing vs Supply Voltage (R_L=2kΩ)



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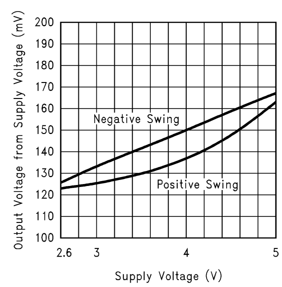
Output Voltage Swing vs Supply Voltage (R_L=600Ω)



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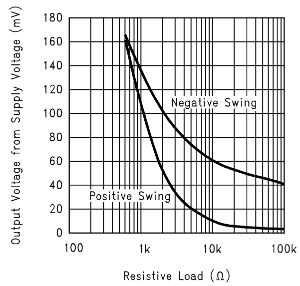
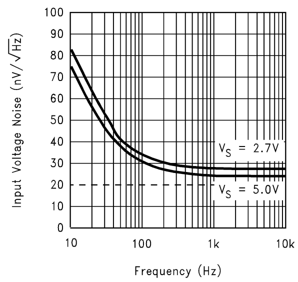
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Output Voltage Swing vs Load Resistance



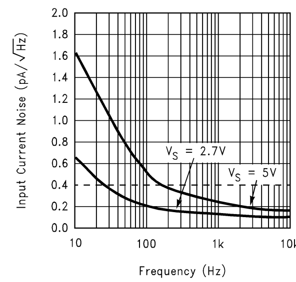
DS100128-87

Input Voltage Noise vs Frequency



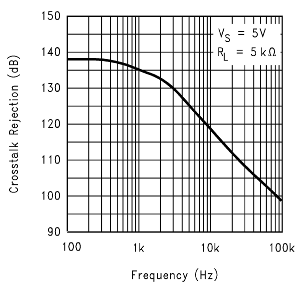
DS100128-18

Input Current Noise vs Frequency



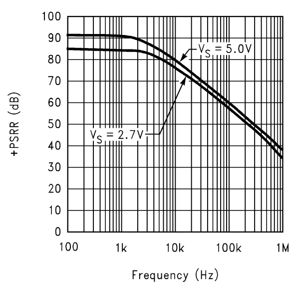
DS100128-17

Crosstalk Rejection vs Frequency



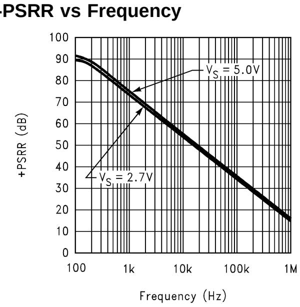
DS100128-93

+PSRR vs Frequency



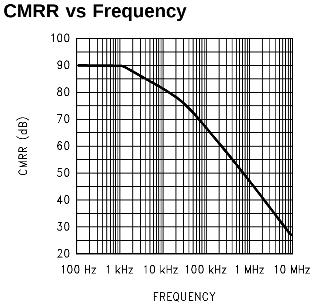
DS100128-9

-PSRR vs Frequency



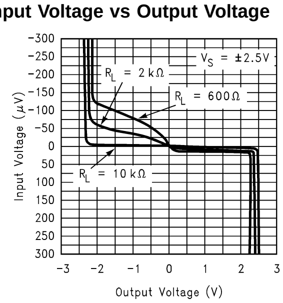
DS100128-10

CMRR vs Frequency



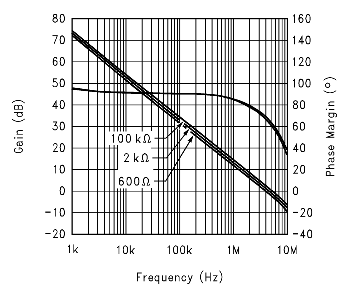
DS100128-47

Input Voltage vs Output Voltage



DS100128-88

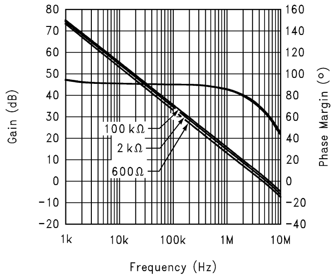
Gain and Phase Margin vs Frequency (R_L=100kΩ, 2kΩ, 600Ω) 2.7V



DS100128-11

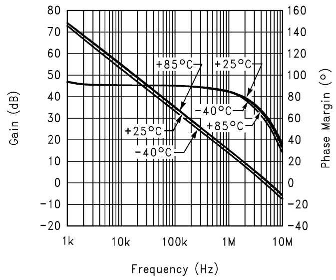
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Gain and Phase Margin vs Frequency (R_L=100kΩ, 2kΩ, 600Ω) 5V



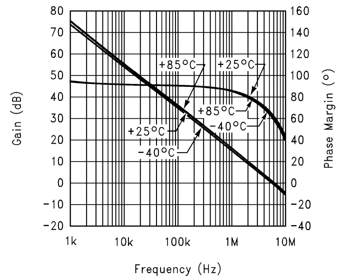
DS100128-12

Gain and Phase Margin vs Frequency (Temp.=25, -40, 85˚C, R_L= 10kΩ) 2.7V



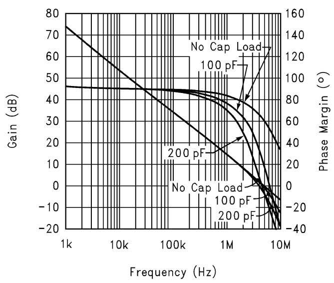
DS100128-13

Gain and Phase Margin vs Frequency (Temp.=25, -40, 85 ˚C, R_L=10kΩ) 5V



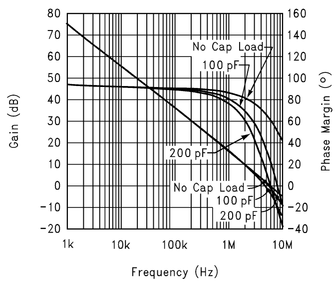
DS100128-14

Gain and Phase Margin vs Frequency (C_L=100pF, 200pF, 0pF, R_L=10kΩ)2.7V



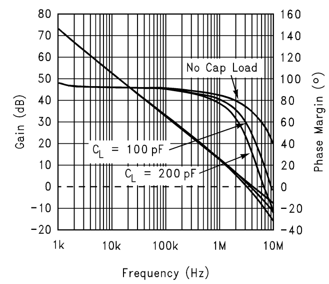
DS100128-15

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=10kΩ)5V



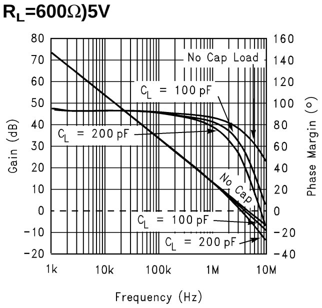
DS100128-16

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=600Ω)2.7V



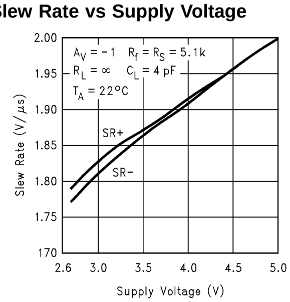
DS100128-19

Gain and Phase Margin vs Frequency (C_L=100pF,200pF,0pF R_L=600Ω)5V



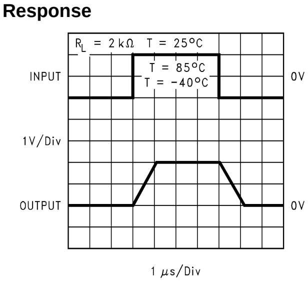
DS100128-20

Slew Rate vs Supply Voltage



DS100128-62

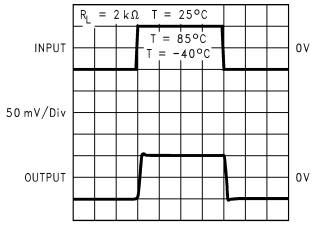
Non-Inverting Large Signal Pulse Response



DS100128-21

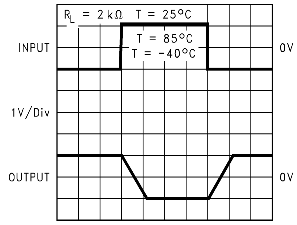
Typical Performance Characteristics Unless otherwise specified, V_S = +5V, single supply, T_A = 25˚C. (Continued)

Non-Inverting Small Signal Pulse Response



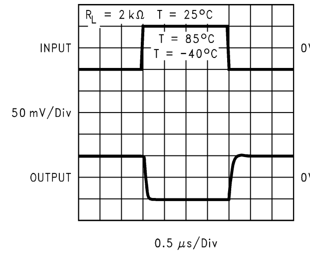
DS100128-24

Inverting Large Signal Pulse Response



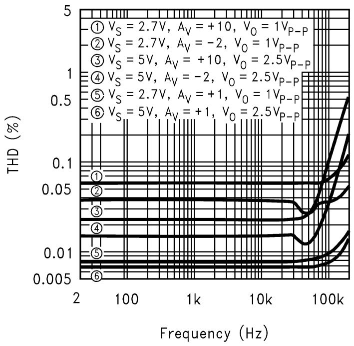
DS100128-27

Inverting Small Signal Pulse Response



DS100128-30

THD vs Frequency



DS100128-82

APPLICATION NOTE

This application note is divided into two sections: design considerations and Application Circuits.

1.0 Design Considerations

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

1.1 Frequency and Phase Response Considerations

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin (ϕ_m) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show ϕ_m for a no load condition. But ϕ_m changes with load. The Gain and Phase margin vs Frequency plots in the curve section can be used to graphically determine the ϕ_m for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

The bandwidth is also affected by load. The graphs of *Figure 1* and *Figure 2* provide a quick look at how various loads affect the ϕ_m and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both ϕ_m and bandwidth, while resistive loads reduce the bandwidth but increase the ϕ_m. Notice how a 600Ω resistor can be added in parallel with 220 picofarads capacitance, to increase the ϕ_m 20°(approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.

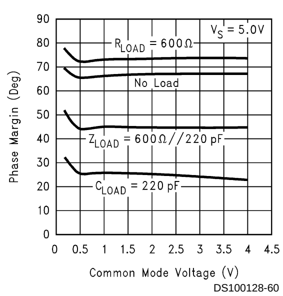


FIGURE 1. Phase Margin vs Common Mode Voltage for Various Loads

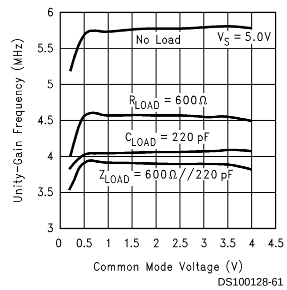


FIGURE 2. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

1.2 Unity Gain Pulse Response Considerations

A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600 Ω pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. *Figure 3* shows how to implement the pull-up resistor for more pulse response stability.

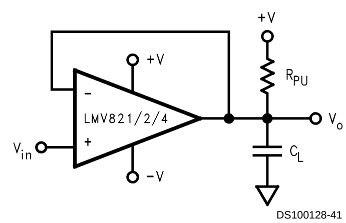


FIGURE 3. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in *Figure 4* .

Figure 5 shows the resulting pulse response from a LMV824, while driving a 10,000pF load through a 20 Ω isolation resistor.

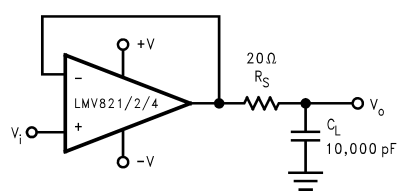
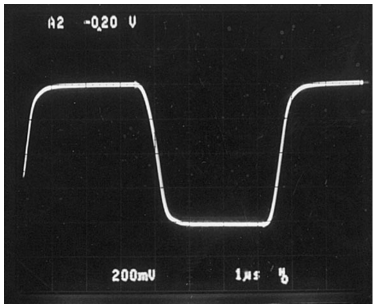


FIGURE 4. Using an Isolation Resistor to Drive Heavy Capacitive Loads

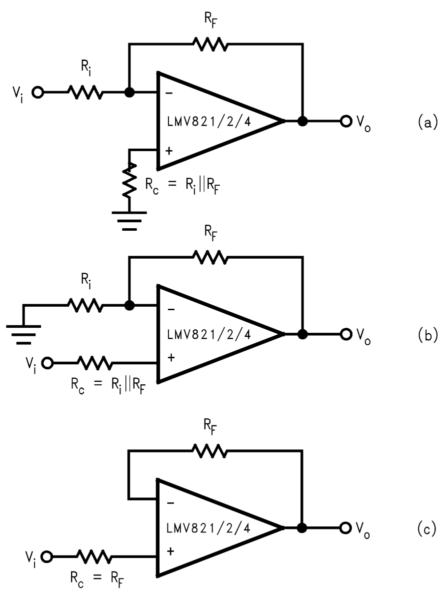


DS100128-54

FIGURE 5. Pulse Response per *Figure 4*

1.3 Input Bias Current Consideration

Input bias current (I_B) can develop a somewhat significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 90nA (max room) and R_F is 100 kΩ, then an offset of 9 mV will be developed (V_{OS}=I_Bx R_F).Using a compensation resistor (R_C), as shown in *Figure 6*, cancels out this affect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.



DS100128-59

FIGURE 6. Canceling the Voltage Offset Effect of Input Bias Current

2.0 APPLICATION CIRCUITS

This section covers the following application circuits:

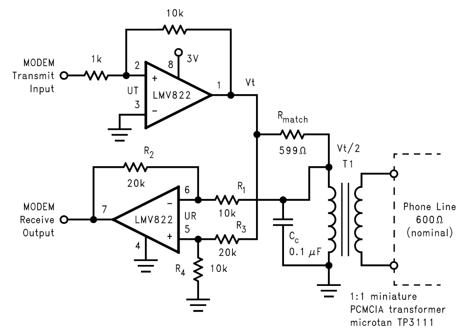
1. Telephone-Line Transceiver
2. “Simple” Mixer (Amplitude Modulator)
3. Dual Amplifier Active Filters (DAAFs)
- a. Low-Pass Filter (LPF)
- b. High-Pass Filter (HPF)

5. Tri-level Voltage Detector

2.1 Telephone-Line Transceiver

The telephone-line transceiver of *Figure 7* provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage (Vt) and Vt/2. This is because R_{match} is chosen to match the coupled telephone-line impedance; therefore dividing Vt by two (assuming R1 >> R_{match}). The differential configuration of UR has its resistors chosen to cancel the Vt and Vt/2 inputs according to the following equation:

$$V_O = V_T\left(\frac{R_3}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) - \frac{V_T}{2}\left(\frac{R_2}{R_1}\right) = V_T\,\frac{1}{3}\,(3) - \frac{V_T}{2}(2) = 0$$



DS100128-33

FIGURE 7. Telephone-line Transceiver for a PCMCIA Modem Card

Note that Cr is included for canceling out the inadequacies of the lossy, miniature transformer. Refer to application note AN-397 for detailed explanation.

2.2“Simple” Mixer (Amplitude Modulator)

The mixer of *Figure 8* is simple and provides a unique form of amplitude modulation. Vi is the modulation frequency (F_M), while a +3V square-wave at the gate of Q1, induces a carrier frequency (F_C). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at Vi results in the oscilloscope photo of *Figure 9*.

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude (/F_M-F_C/) is the key factor for determining an object’s velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object’s velocity.

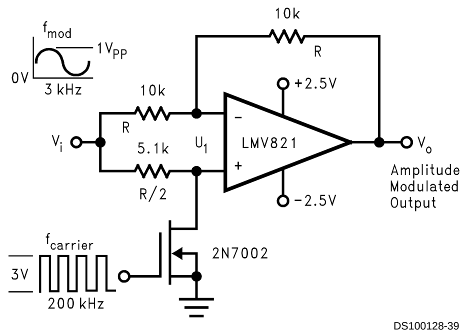


FIGURE 8. Amplitude Modulator Circuit

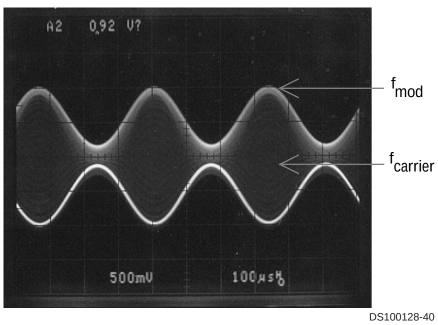


FIGURE 9. Output signal per the Circuit of ***Figure 8***

2.4 Dual Amplifier Active Filters (DAAFs)

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of *Figure 10* and *Figure 11* (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter's parameter such as cutoff frequency (Fc). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of *Figure 10* and *Figure 11* are well suited for high volume production.

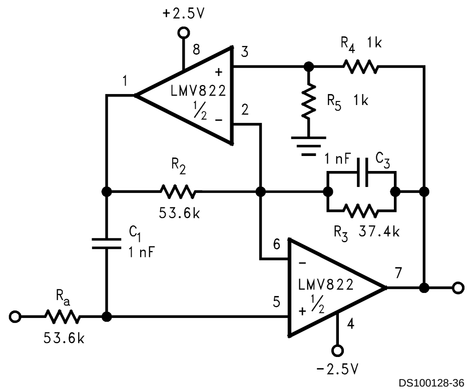


FIGURE 10. Dual Amplifier, 3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

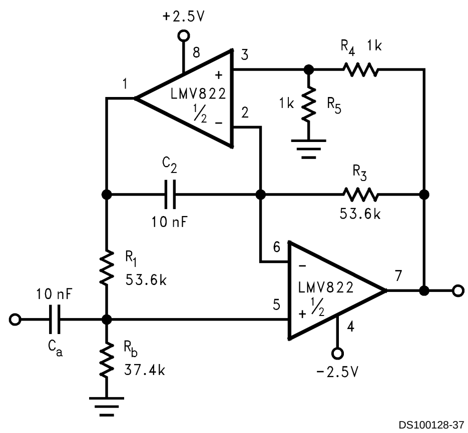


FIGURE 11. Dual Amplifier, 300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Table 1 provides sensitivity measurements for a 10 MΩ load condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for a 1 percent increase in component value, Fc decreases by 1.2 percent.

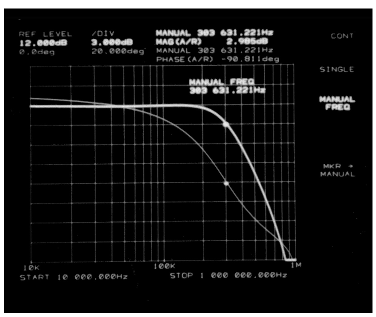
Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R_4 and R_5 of each circuit also caused variations in the pass band gain. Increasing R_4 by ten percent, increased the gain by 0.4 dB, while increasing R_5 by ten percent, decreased the gain by 0.4 dB.

TABLE 1.

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R_a	-1.2	C_a	-0.7
C_1	-0.1	R_b	-1.0
R_2	-1.1	R_1	+0.1
R_3	+0.7	C_2	-0.1
C_3	-1.5	R_3	+0.1
R_4	-0.6	R_4	-0.1
R_5	+0.6	R_5	+0.1

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of the filter response. *Figure 12* shows an impressive photograph of a network analyzer measurement (hp3577A). The measurement was taken from a 300kHz version of *Figure 10*. At 300 kHz, the open-loop to closed-loop gain ratio @ Fc is about 5 to 1. This is 10 times lower than the 50 to 1 "rule of thumb" for Single Amplifier Active Filters.



DS100128-92

FIGURE 12. 300 kHz, Low-Pass Filter, Butterworth Response as Measured by the HP3577A Network Analyzer

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equation calculate the Fc and the circuit Quality Factor (Q) for the LPF (*Figure 10*). The second two equations calculate the Fc and Q for the HPF (*Figure 11*).

$$\text{(LPF)} \quad F_C = \frac{\sqrt{R_5}}{2\pi\sqrt{R_a}\cdot\sqrt{R_2}\cdot\sqrt{R_4}\cdot\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$Q = 2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}$$

$$\text{(HPF)} \quad F_C = \frac{\sqrt{R_4}}{2\pi\sqrt{R_1}\cdot\sqrt{R_3}\cdot\sqrt{R_5}\cdot\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$Q = 2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}$$

To simplify the design process, certain components are set equal to each other. Refer to *Figure 10* and *Figure 11*. These equal component values help to simplify the design equations as follows:

$$\text{(LPF)} \quad R_a = R_2 = \frac{1}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$R_3 = \frac{Q}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$\text{(HPF)} \quad R_1 = R_3 = \frac{1}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$R_b = \frac{Q}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}$$

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (*Figure 10*) is designed as follows:

1. Choose $C_1 = C_3 = C = 1$ nF
2. Choose $R_4 = R_5 = 1$ kΩ
3. Calculate R_a and R_2 for the desired Fc as follows:

$$R_a = R_2 = \frac{1}{2\pi(F_C)C}$$

$$= \frac{1}{2\pi(3\text{ kHz})1\text{ nF}}$$

$$= 53.1\text{ k}\Omega$$

$$\cong 53.6\text{ k}\Omega \text{ (Practical Value)}$$

4. Calculate R_3 for the desired Q. The desired Q for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane). R_3 calculates as follows:

$$R_3 = \frac{Q}{2\pi(F_C)C}$$

$$= \frac{0.707}{2\pi(3\text{ kHz})1\text{ nF}}$$

$$= 37.5\text{ k}\Omega$$

$$\cong 37.4\text{ k}\Omega \text{ (Practical Value)}$$

Notice that R_3 could also be calculated as 0.707 of R_a or R_2.

The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

2.5 Tri-level Voltage Detector

The tri-level voltage detector of *Figure 13* provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage (V_O) is at V_{CC} for the Min-range. V_O is clamped at GND for the Mid-range. For the Max-range, V_O is at V_{ee}. *Figure 14* shows a V_O vs. V_I oscilloscope photo per the circuit of *Figure 13*.

Its operation is as follows: V_I deviating from GND, causes the diode bridge to absorb I_{IN} to maintain a clamped condition (V_O= 0V). Eventually, I_{IN} reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding *Figure 14*, shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

$$\Delta V = \frac{R}{R_1}(V_{CC} - V_{Diode})$$

DS100128-89

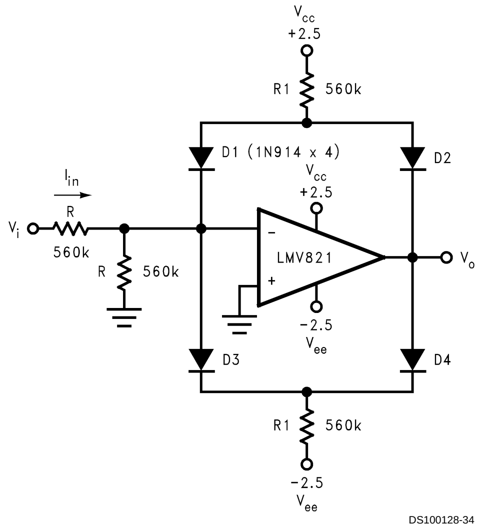


FIGURE 13. Tri-level Voltage Detector

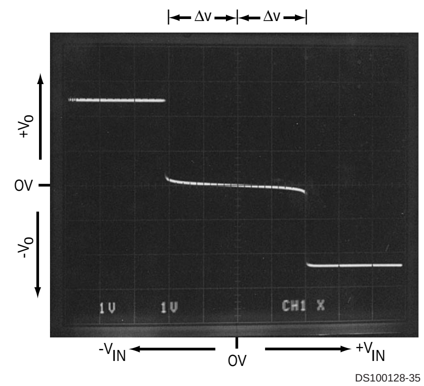
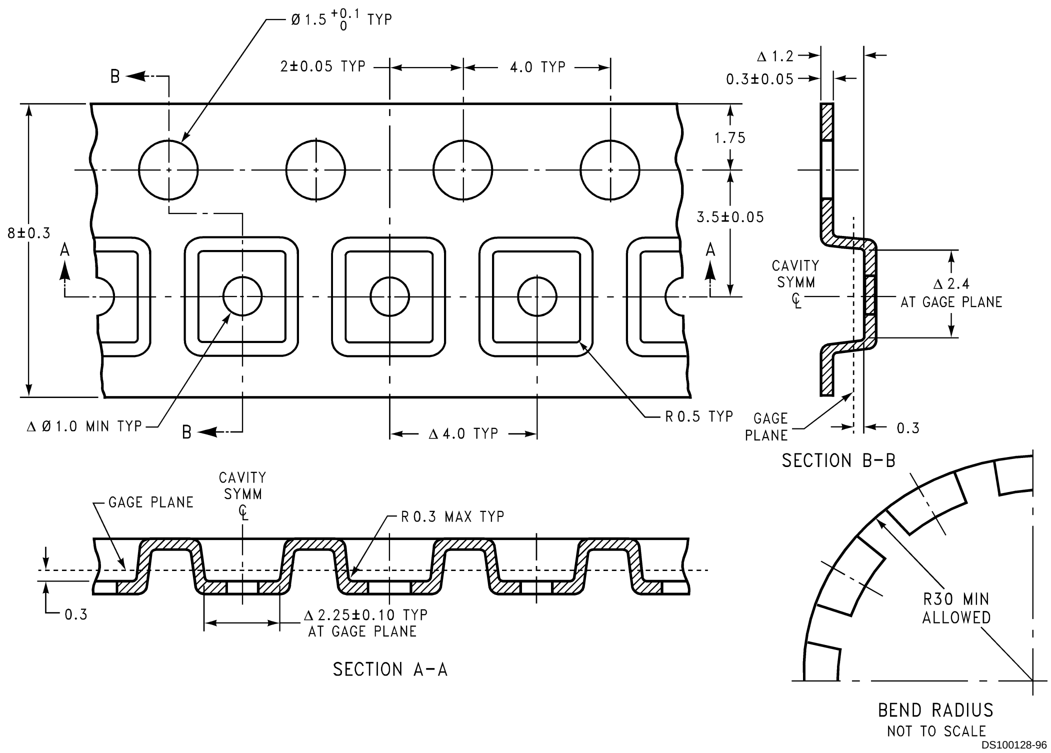


FIGURE 14. X, Y Oscilloscope Trace showing V_{OUT} vs V_{IN} per the Circuit of *Figure 13*

SC70-5 Tape and Reel Specification

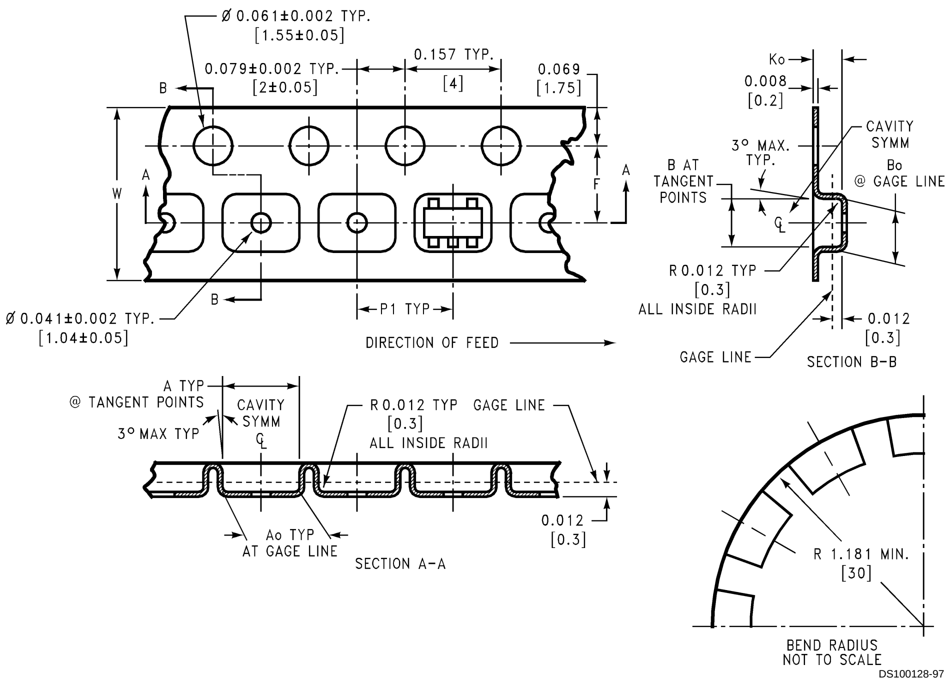


SOT-23-5 Tape and Reel Specification

Tape Format

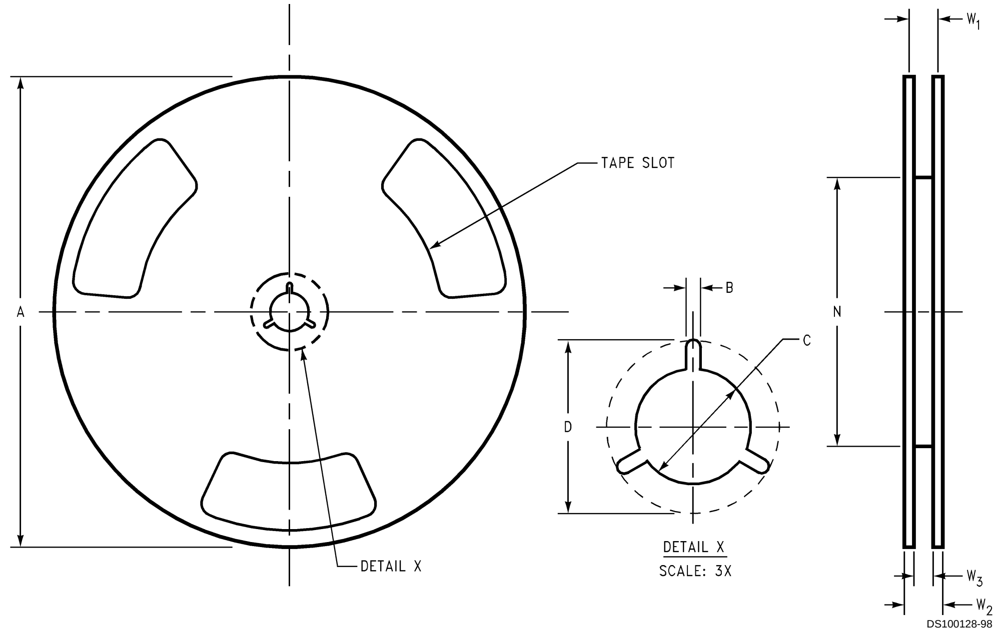
Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader	0 (min)	Empty	Sealed
(Start End)	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer	125 (min)	Empty	Sealed
(Hub End)	0 (min)	Empty	Sealed

Tape Dimensions



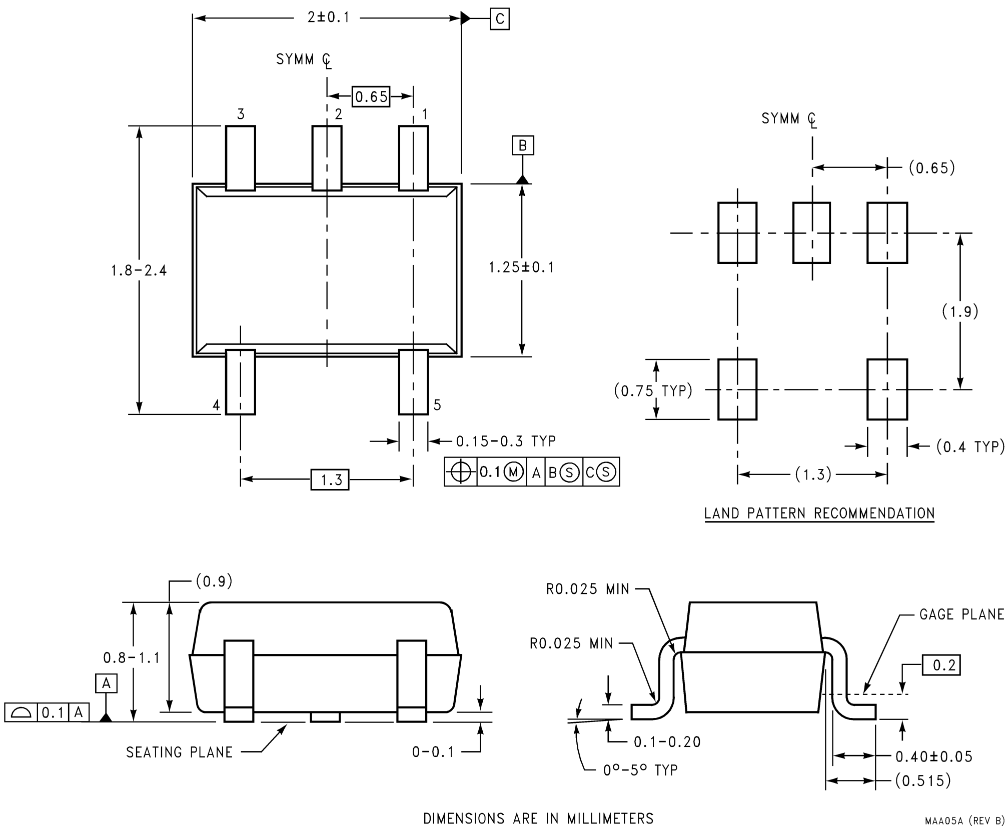
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

Reel Dimensions



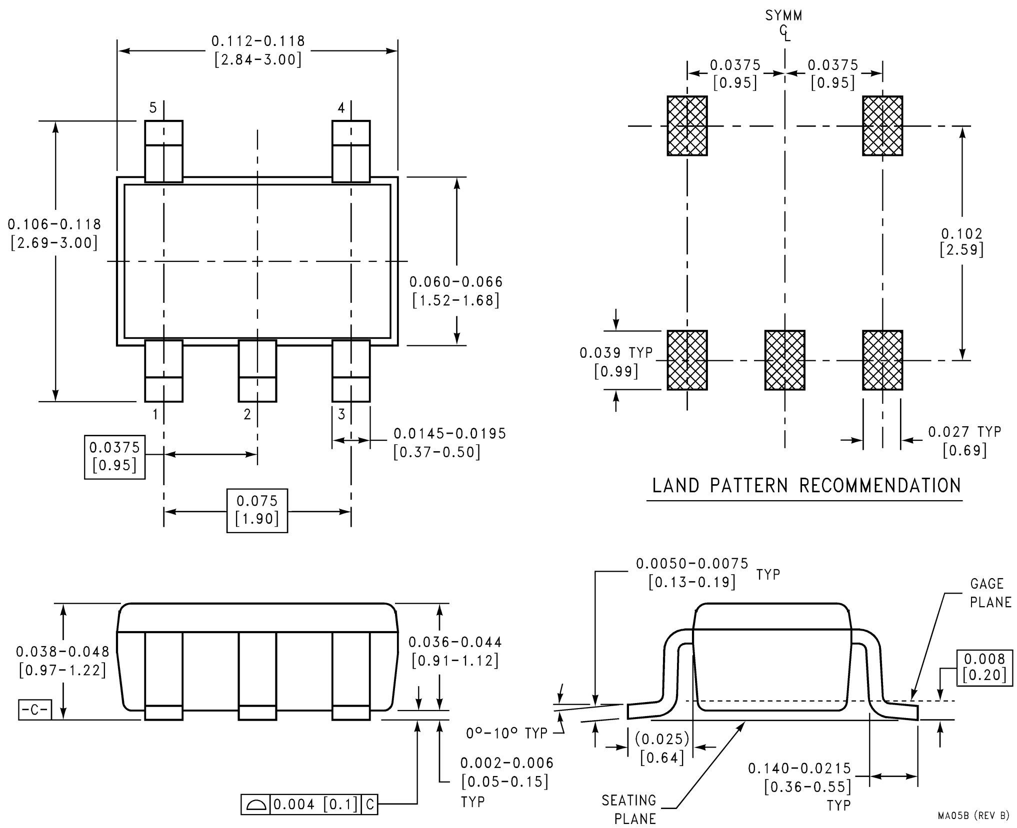
8 mm	**7.00** **330.00**	**0.059** **1.50**	**0.512** **13.00**	**0.795** **20.20**	**2.165** **55.00**	**0.331 + 0.059/−0.000** **8.40 + 1.50/−0.00**	**0.567** **14.40**	**W1+ 0.078/−0.039** **W1 + 2.00/−1.00**
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters) unless otherwise noted



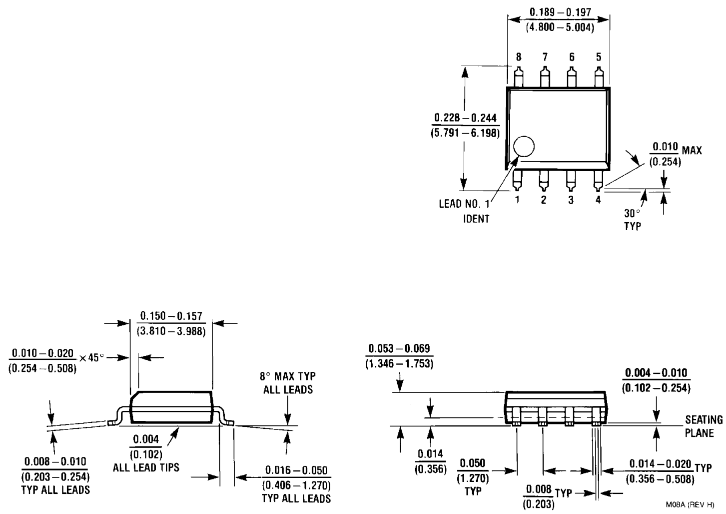
SC70-5
Order Number LMV821M7 or LMV821M7X
NS Package Number MAA05

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



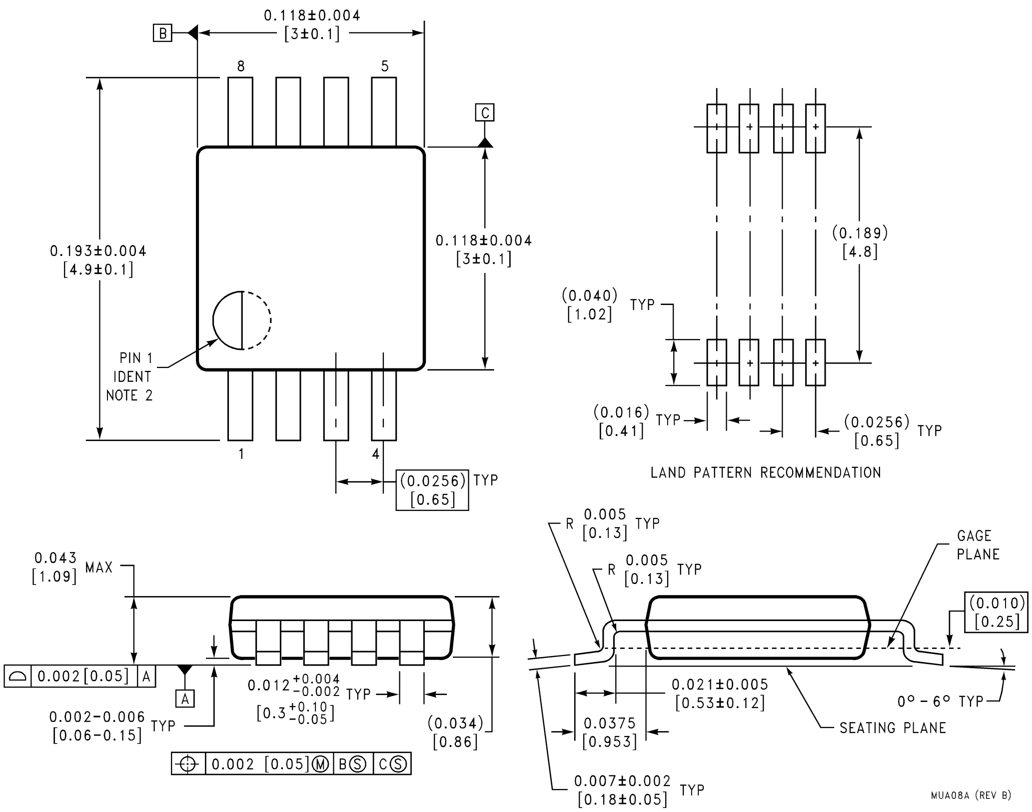
SOT 23-5
Order Number LMV821M5 or LMV821M5X
NS Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



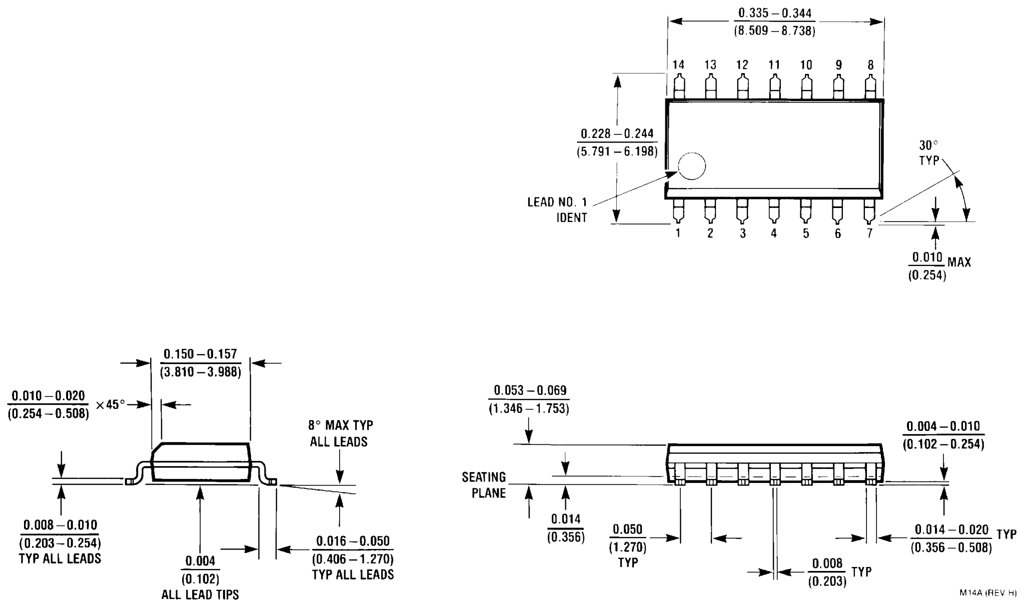
8-Pin Small Outline
Order Number LMV822M or LMV822MX
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



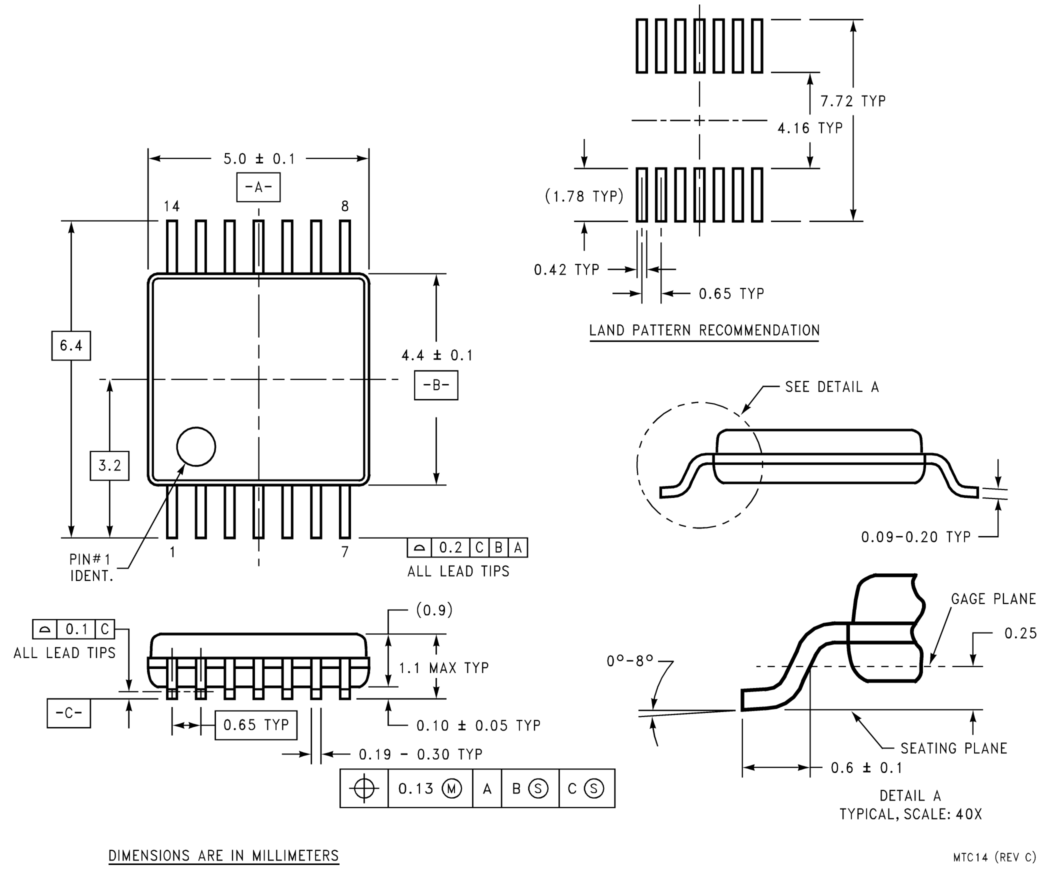
8-Pin MSOP
Order Number LMV822MM or LMV822MMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin Small Outline
Order Number LMV824M or LMV824MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin TSSOP
Order Number LMV824MTC or LMV824MTCX
NS Package Number MTC14

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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