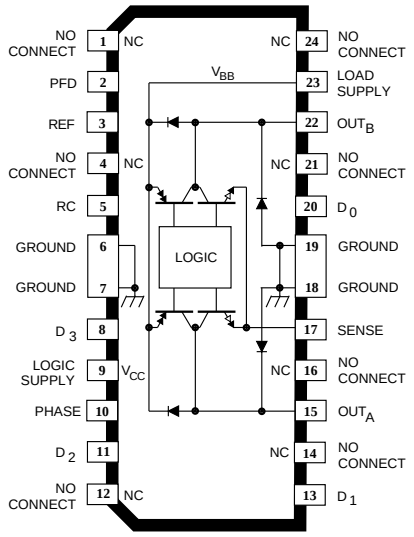
3957

Data Sheet
29319.44†

FULL-BRIDGE PWM MICROSTEPPING MOTOR DRIVER

A3957SLB



Dwg. PP-056-4

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} . . . . . **50 V**
Output Current, I_{OUT}
(Continuous) . . . . . **±1.5 A***
Logic Supply Voltage, V_{CC} . . . . . **7.0 V**
Logic/Reference Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{CC} + 0.3 V**
Sense Voltage, V_S . . . . . **1.0 V**
Package Power Dissipation (T_A = 25°C), P_D
A3957SA . . . . . **2.08 W†**
A3957SLB . . . . . **2.23 W†**
Operating Temperature Range,
T_A . . . . . **-20˚C to +85˚C**
Junction Temperature, T_J . . . . . **+150˚C**
Storage Temperature Range,
T_S . . . . . **-55˚C to +150˚C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

† Per SEMI G42-88 Specification, *Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages*..

The A3957SA and A3957SLB are designed for driving one winding of a bipolar stepper motor in a microstepping mode. The outputs are rated for continuous output currents to ±1.5 A and operating voltages to 50 V. Internal pulse-width modulated (PWM) current control combined with an internal four-bit nonlinear digital-to-analog converter allows the motor current to be controlled in full-, half-, quarter-, eighth-, or sixteenth-step (microstepping) modes. Nonlinear increments minimize the number of control lines necessary for microstepping. Microstepping provides for increased step resolution, and reduces torque variations and resonance problems at low speed.

Internal circuitry determines whether the PWM current-control circuitry operates in a slow (recirculating) current-decay mode, fast (regenerative) current-decay mode, or in a mixed current-decay mode in which the off time is divided into a period of fast current decay with the remainder of the fixed off time spent in slow current decay. The combination of user-selectable current-sensing resistor and reference voltage, digitally selected output current ratio; and slow, fast, or mixed current-decay modes provides users with a broad, variable range of motor control.

Internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover current protection. Special power-up sequencing is not required.

The A3957S— is supplied in a choice of two power packages; a 16-pin dual-in-line plastic package (suffix ‘A’), and a 24-lead plastic SOIC with copper heat-sink tabs (suffix ‘LB’). The power tab is at ground potential and needs no electrical isolation.

FEATURES

- ±1.5 A Continuous Output Current
- 50 V Output Voltage Rating
- Internal PWM Current Control
- 4-Bit Non-Linear DAC for 16-Bit Microstepping
- Satlington™ Sink Drivers
- Fast, Mixed Fast/Slow, and Slow Current-Decay Modes
- Internal Transient-Suppression Diodes
- Internal Thermal-Shutdown Circuitry
- Crossover-Current and UVLO Protection

Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JC}$	$R_{\theta JT}$
A3957SA	16-pin DIP	60°C/W	38°C/W	—
A3957SLB	24-lead batwing SOIC	56°C/W	—	6°C/W

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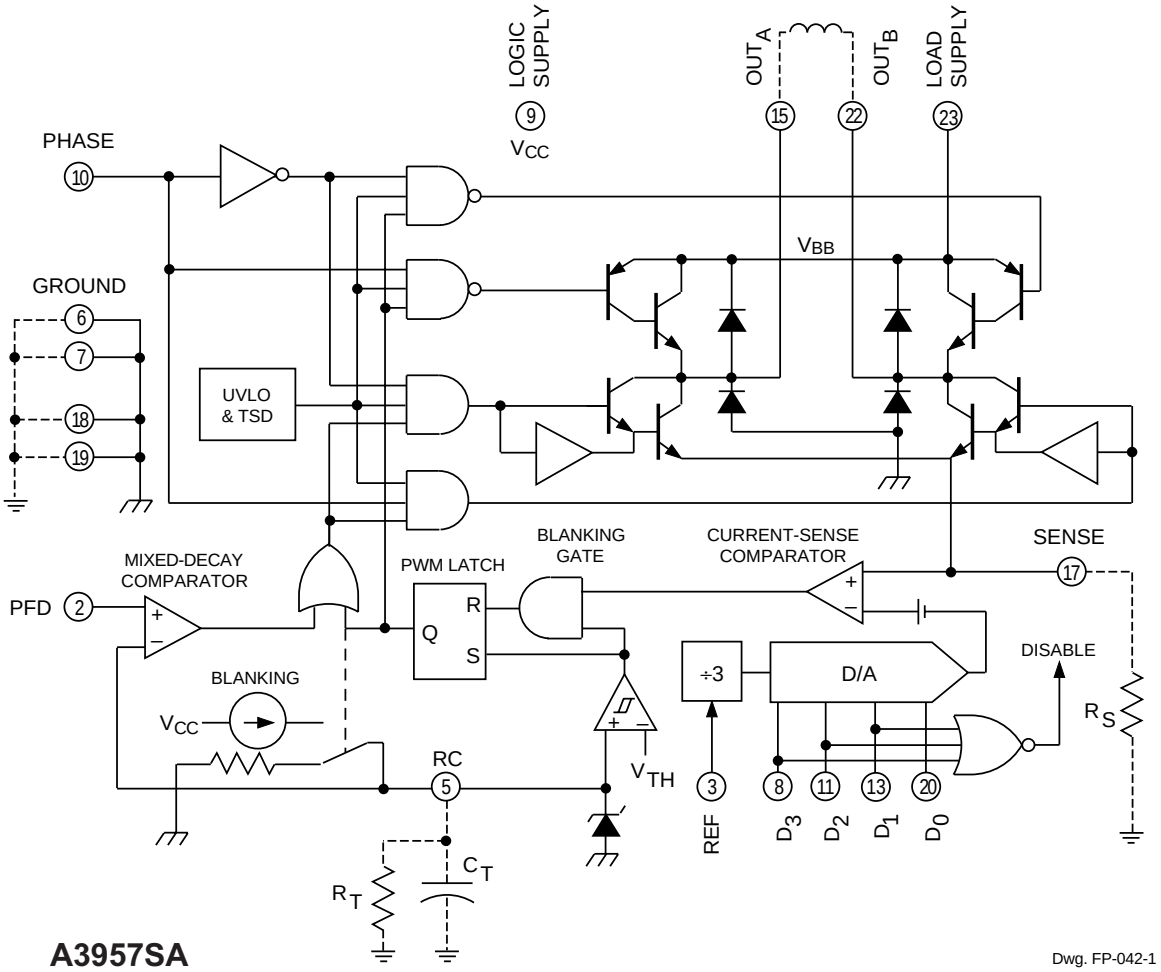
FUNCTIONAL BLOCK DIAGRAM (A3957SLB shown)



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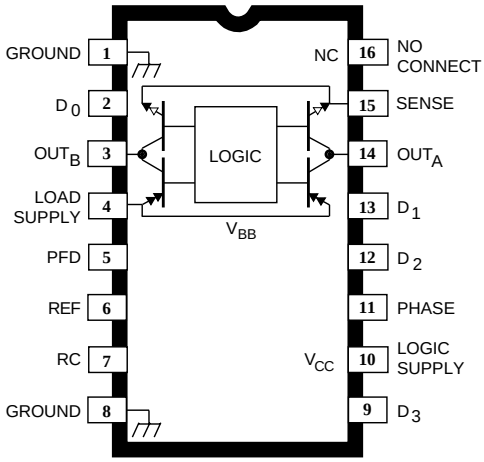
A3957SA



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For the 'A' package, pins 1 and 8 must be externally connected together.

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Table 1 — PHASE Truth Table

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

Table 2 — PFD Truth Table

V_{PFD}	Description
≥3.5 V	Slow Current-Decay Mode
1.2 V to 2.9 V	Mixed Current-Decay Mode
≤0.8 V	Fast Current-Decay Mode

Table 3 — DAC Truth Table

DAC Data				Current	
D_3	D_2	D_1	D_0	Ratio, %	V_{REF}/V_S
H	H	H	H	100	3.00
H	H	H	L	95.7	3.13
H	H	L	H	91.3	3.29
H	H	L	L	87.0	3.45
H	L	H	H	82.6	3.64
H	L	H	L	78.3	3.83
H	L	L	H	73.9	4.07
H	L	L	L	69.6	4.31
L	H	H	H	60.9	4.93
L	H	H	L	52.2	5.74
L	H	L	H	43.5	6.90
L	H	L	L	34.8	8.62
L	L	H	H	26.1	11.49
L	L	H	L	17.4	17.24
L	L	L	X	All Outputs Disabled	

where $V_S = I_{TRIP} \bullet R_S$. See Applications section.

ELECTRICAL CHARACTERISTICS at T_A = 25˚C, V_{BB} = 5 V to 50 V, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Power Outputs						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±1.5 A, L = 3 mH	V_{CC}	—	50	V
Output Leakage Current	I_{CEX}	V_{OUT} = V_{BB}	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<-1.0	-50	µA
Output Saturation Voltage (Forward or Reverse Mode)	$V_{CE(SAT)}$	V_S = 1.0 V:				
		Source Driver, I_{OUT} = -0.85 A	—	1.1	1.2	V
		Source Driver, I_{OUT} = -1.5 A	—	1.4	1.5	V
		Sink Driver, I_{OUT} = 0.85 A	—	0.5	0.7	V
		Sink Driver, I_{OUT} = 1.5 A	—	1.2	1.5	V
Sense Current Offset	I_{SO}	I_S - I_{OUT}, I_{OUT} = 850 mA, V_S = 0 V, V_{CC} = 5 V	20	30	40	mA
Clamp Diode Forward Volt. (Sink or Source)	V_F	I_F = 0.85 A	—	1.2	1.4	V
		I_F = 1.5 A	—	1.5	1.7	V
Motor Supply Current (No Load)	$I_{BB(ON)}$		—	2.0	4.0	mA
	$I_{BB(OFF)}$	D_0 = D_1 = D_2 = D_3 = 0.8 V	—	1.0	50	µA
Control Circuitry						
Logic Supply Voltage Range	V_{CC}	Operating	4.5	5.0	5.5	V
Reference Voltage Range	V_{REF}	Operating	0.5	—	2.5	V
UVLO Enable Threshold		V_{CC} = 0 → 5 V	3.35	3.70	4.05	V
UVLO Hysteresis			0.25	0.40	0.55	V
Logic Supply Current	$I_{CC(ON)}$		—	42	50	mA
	$I_{CC(OFF)}$	D_0 = D_1 = D_2 = D_3 = 0.8 V	—	14	17	mA
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-200	µA

Continued next page…

ELECTRICAL CHARACTERISTICS at T_A = 25˚C, V_{BB} = 5 V to 50 V, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Circuitry (continued)						
Mixed-Decay Comparator Trip Points	V_{PFD}	Slow Current-Decay Mode	3.5	—	—	V
		Mixed Current-Decay Mode	1.2	—	2.9	V
		Fast Current-Decay Mode	—	—	0.8	V
Mixed-Decay Comparator Input Offset Voltage	$V_{IO(PFD)}$		—	0	±20	mV
Mixed-Decay Comparator Hysteresis	$\Delta V_{IO(PFD)}$		5.0	25	55	mV
Reference Input Current	I_{REF}	V_{REF} = 0 V to 2.5 V	—	—	±5.0	µA
Reference Divider Ratio	V_{REF}/V_S	at trip, $D_0 = D_1 = D_2 = D_3$ = 2 V	—	3.0	—	—
Digital-to-Analog Converter Accuracy*	—	1.0 V < $V_{REF} \leq$ 2.5 V	—	—	±3.0	%
		0.5 V < $V_{REF} \leq$ 1.0 V	—	—	±4.0	%
Current-Sense Comparator Input Offset Voltage*	$V_{IO(S)}$	V_{REF} = 0 V	—	±16	—	mV
Step Reference Current Ratio	SRCR	$D_0 = D_1 = D_2 = D_3$ = 0.8 V	—	0	—	%
		D_1 = 2 V, $D_0 = D_2 = D_3$ = 0.8 V	—	17.4	—	%
		$D_0 = D_1$ = 2 V, $D_2 = D_3$ = 0.8 V	—	26.1	—	%
		D_2 = 2 V, $D_0 = D_1 = D_3$ = 0.8 V	—	34.8	—	%
		$D_0 = D_2$ = 2 V, $D_1 = D_3$ = 0.8 V	—	43.5	—	%
		$D_1 = D_2$ = 2 V, $D_0 = D_3$ = 0.8 V	—	52.2	—	%
		$D_0 = D_1 = D_2$ = 2 V, D_3 = 0.8 V	—	60.9	—	%
		D_3 = 2 V, $D_0 = D_1 = D_2$ = 0.8 V	—	69.6	—	%
		$D_0 = D_3$ = 2 V, $D_1 = D_2$ = 0.8 V	—	73.9	—	%
		$D_1 = D_3$ = 2 V, $D_0 = D_2$ = 0.8 V	—	78.3	—	%
		$D_0 = D_1 = D_3$ = 2 V, D_2 = 0.8 V	—	82.6	—	%
		$D_2 = D_3$ = 2 V, $D_0 = D_1$ = 0.8 V	—	87.0	—	%
		$D_0 = D_2 = D_3$ = 2 V, D_1 = 0.8 V	—	91.3	—	%
		$D_1 = D_2 = D_3$ = 2 V, D_0 = 0.8 V	—	95.7	—	%
		$D_0 = D_1 = D_2 = D_3$ = 2 V	—	100	—	%
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hyst.	ΔT_J		—	15	—	°C

* The total error for the V_{REF}/V_S function is the sum of the D/A error and the current-sense comparator input offset voltage.

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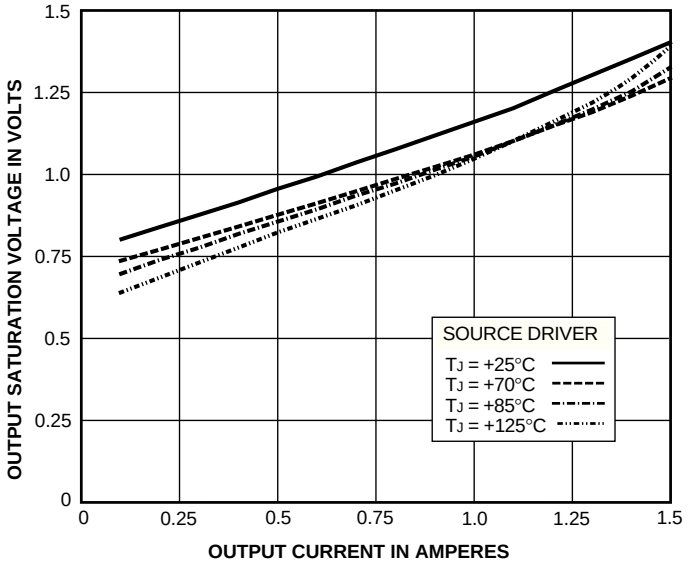
ELECTRICAL CHARACTERISTICS at T_A = 25˚C, V_{BB} = 5 V to 50 V, V_{CC} = 4.5 V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
AC Timing						
PWM RC Fixed Off-time	$t_{OFF\ RC}$	C_T = 470 pF, R_T = 43 kΩ	18.2	20.2	22.3	µs
PWM Turn-Off Time	$t_{PWM(OFF)}$	Current-Sense Comparator Trip to Source OFF, I_{OUT} = 100 mA	—	1.0	1.5	µs
		Current-Sense Comparator Trip to Source OFF, I_{OUT} = 1.5 A	—	1.4	2.5	µs
PWM Turn-On Time	$t_{PWM(ON)}$	I_{RC} Charge ON to Source ON, I_{OUT} = 100 mA	—	0.4	0.7	µs
		I_{RC} Charge ON to Source ON, I_{OUT} = 1.5 A	—	0.55	0.85	µs
PWM Minimum On Time	$t_{ON(min)}$	V_{CC} = 5.0 V, $R_T \geq$ 43 kΩ, C_T = 470 pF I_{OUT} = 100 mA	1.0	1.6	2.2	µs
Crossover Dead Time	t_{CODT}	1 kΩ Load to 25 V	0.3	1.5	3.0	µs

Typical Operating Characteristics

Source Driver Saturation Voltage



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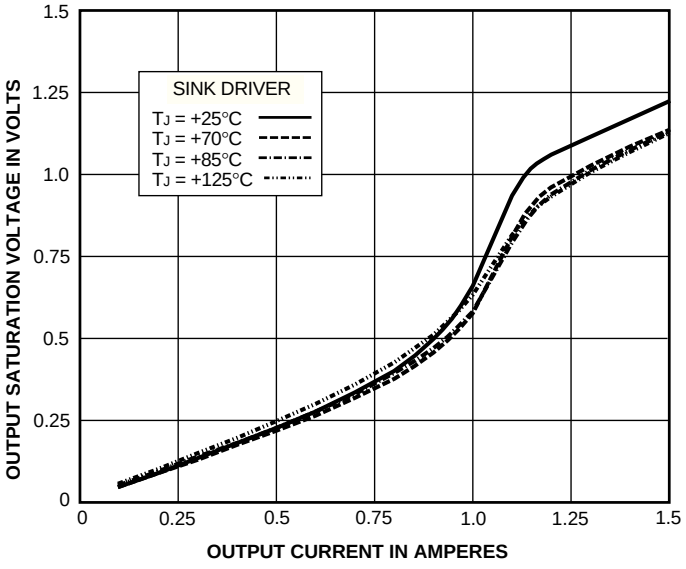
Satlington™ Sink Driver Saturation Voltage



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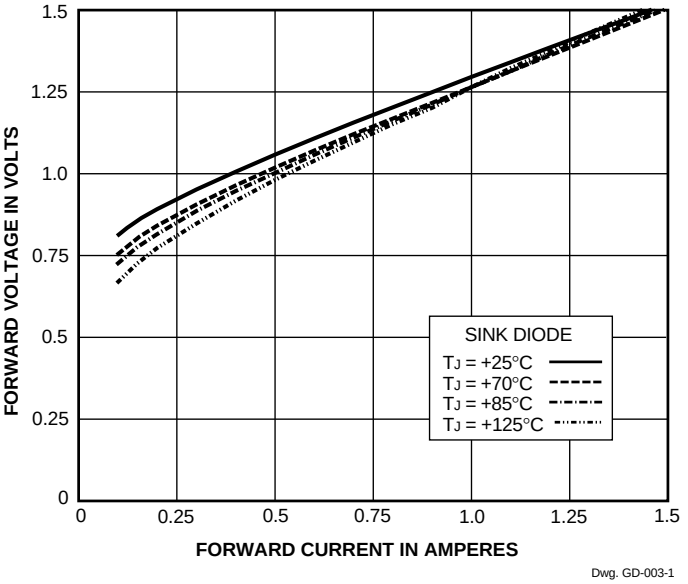
Clamp Diode Forward Voltage



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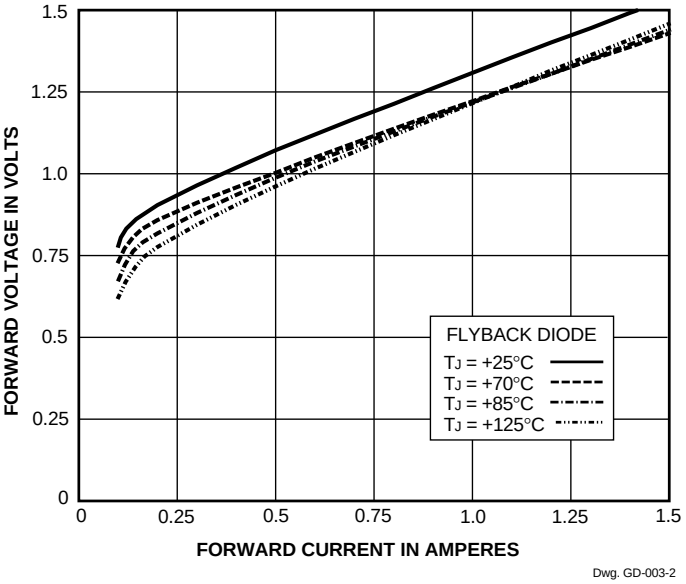
Flyback Diode Forward Voltage



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Terminal Functions

A3957SA Pin	A3957SLB Lead	Terminal Name	Description
–	1	NC	No internal connection.
5	2	PFD	(Percent Fast Decay) The analog input used to set the current-decay mode.
6	3	REF	(V_{REF}) The voltage at this input (along with the value of R_S and the states of DAC inputs D_0, D_1, and D_2) set the peak output current.
–	4	NC	No internal connection.
7	5	RC	The parallel combination of external resistor R_T and capacitor C_T set the off time for the PWM current regulator. C_T also sets the blanking time.
8*	6-7	GROUND	Return for the logic supply (V_{CC}) and load supply (V_{BB}); the reference for all voltage measurements.
9	8	D_3	($DATA_3$) One of four (MSB) control bits for the internal digital-to-analog converter.
10	9	LOGIC SUPPLY	(V_{CC}) Supply voltage for the logic circuitry. Typically = 5 V.
11	10	PHASE	The PHASE input determines the direction of current in the load.
12	11	D_2	($DATA_2$) One of four control bits for the internal digital-to-analog converter.
–	12	NC	No internal connection.
13	13	D_1	($DATA_1$) One of four control bits for the internal digital-to-analog converter.
–	14	NC	No internal connection.
14	15	OUT_A	One of two output load connections.
–	16	NC	No internal connection.
15	17	SENSE	Connection to the sink-transistor emitters. Sense resistor R_S is connected between this point and ground.
16	–	NC	No internal connection.
1*	18-19	GROUND	Return for the logic supply (V_{CC}) and load supply (V_{BB}); the reference for all voltage measurements.
2	20	D_0	($DATA_0$) One of four (LSB) control bits for the internal digital-to-analog converter.
–	21	NC	No internal connection.
3	22	OUT_B	One of two output load connections.
4	23	LOAD SUPPLY	(V_{BB}) Supply voltage for the load.
–	24	NC	No internal connection.

* For the ‘A’ package, pins 1 and 8 must be externally connected together.

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Functional Description

Two A3957S— full-bridge PWM microstepping motor drivers are needed to drive the windings of a bipolar stepper motor. Internal pulse-width modulated (PWM) control circuitry regulates each motor winding's current. The peak motor current is set by the value of an external current-sense resistor (R_S), a reference voltage (V_{REF}), and the digital-to-analog converter (DAC) data inputs (D_0, D_1, D_2, and D_3).

To improve motor performance, especially when using sinusoidal current profiles necessary for microstepping, the A3957S— has three distinct current-decay modes: slow decay, fast decay, and mixed decay.

PHASE Input. The PHASE input controls the direction of current flow in the load (table 1). An internally generated dead time of approximately 1.5 µs prevents crossover currents that could occur when switching the PHASE input.

DAC Data Inputs (D_0, D_1, D_2, D_3). A non-linear DAC is used to digitally control the output current. The output of the DAC is used to set the trip point of the current-sense comparator. Table 3 shows DAC output voltages for each input condition. When D_1, D_2, and D_3 are all logic low, all of the power output transistors are turned off.

Internal PWM Current Control. Each motor driver IC contains an internal fixed off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink transistors are enabled and current flows through the motor winding and R_S (figure 1).

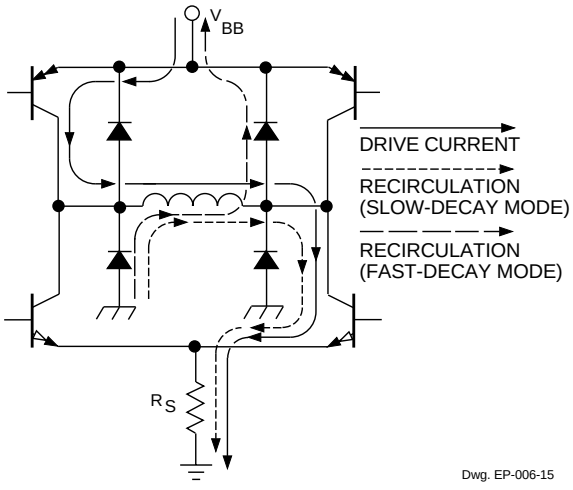


Figure 1 — Load-Current Paths

When the voltage across the sense resistor equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source drivers (slow-decay mode) or the sink and source drivers (fast- or mixed-decay mode).

With the DATA input lines tied to V_{CC}, the maximum value of current limiting is set by the selection of R_S and V_{REF} with a transconductance function approximated by:

$$I_{TRIP} \approx V_{REF}/3R_S = I_{OUT} + I_{SO}.$$

where I_{SO} is the sense-current offset due to the base-drive current of the sink transistor (typically 30 mA). The actual peak load current (I_{PEAK}) will be slightly higher than I_{TRIP} due to internal logic and switching delays. The driver(s) remain off for a time period determined by a user-selected external resistor-capacitor combination (R_TC_T). At the end of the fixed off time, the driver(s) are re-enabled, allowing the load current to increase to I_{TRIP} again, maintaining an average load current.

The current-sense comparator has a fixed offset of approximately 16 mV. With $R_S = 0.5\ \Omega$, the sense-current offset (I_{SO}) is effectively cancelled ($V_{IO(S)} \approx I_{SO} \bullet R_S$).

The DAC data input lines are used to provide up to eight levels of output current. The internal 4-bit digital-to-analog converter reduces the reference input to the current-sense comparator in precise steps (the step reference current ratio or SRCR) to provide half-step, quarter-step, eighth-step, or "microstepping" load-current levels.

$$I_{TRIP} \approx \text{SRCR} \times V_{REF}/3R_S$$

Slow Current-Decay Mode. When $V_{PFD} \geq 3.5$ V, the device is in slow current-decay mode (the source drivers are disabled when the load current reaches I_{TRIP}). During the fixed off time, the load inductance causes the current to recirculate through the motor winding, sink driver, ground clamp diode, and sense resistor (see figure 1). Slow-decay mode produces low ripple current for a given fixed off time (see figure 2). Low ripple current is desirable because the average current in the motor winding is more nearly equal to the desired reference value, resulting in increased motor performance in microstepping applications.

For a given level of ripple current, slow decay affords the lowest PWM frequency, which reduces heating in the motor and driver IC due to a corresponding decrease in hysteretic core losses and switching losses respectively. Slow decay also has the advantage that the PWM load current regulation can follow a more rapidly increasing reference before the PWM frequency drops into the audible range. For these reasons slow-decay mode is typically used as long as good current regulation can be maintained.

Under some circumstances slow-decay mode PWM can fail to maintain good current regulation:

1) The load current will fail to regulate in slow-decay mode due to a sufficiently negative back-EMF voltage in conjunction with the low voltage drop across the load during slow decay recirculation. The negative back-EMF voltage can cause the load current to actually increase during the slow decay off time. A negative back-EMF voltage condition commonly occurs when driving stepping motors because the phase lead of the rotor typically causes the back-EMF voltage to be negative towards the end of each step (see figure 3A).

2) When the desired load current is decreased rapidly, the slow rate of load current decay can prevent the current from following the desired reference value.

3) When the desired load current is set to a very low value, the current-control loop can fail to regulate due to its minimum duty cycle, which is a function of the user-selected value of t_{OFF} and the minimum on-time pulse width $t_{on(min)}$ that occurs each time the PWM latch is reset.

Fast Current-Decay Mode. When $V_{PFD} \le 0.8$ V, the device is in fast current-decay mode (both the sink and source drivers are disabled when the load current reaches I_{TRIP}). During the fixed off time, the load inductance causes the current to flow from ground to the load supply via the motor winding, ground-clamp and flyback diodes (see figure 1). Because the full motor supply voltage is across the load during fast-decay recirculation, the rate of load current decay is rapid, producing a high ripple current for a given fixed off time (see figure 2). This rapid rate of decay allows good current regulation to be maintained at the

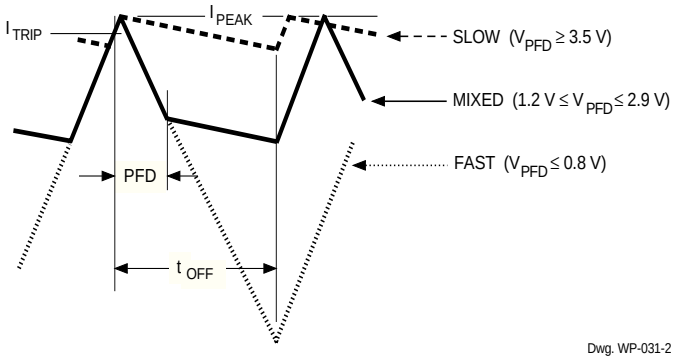
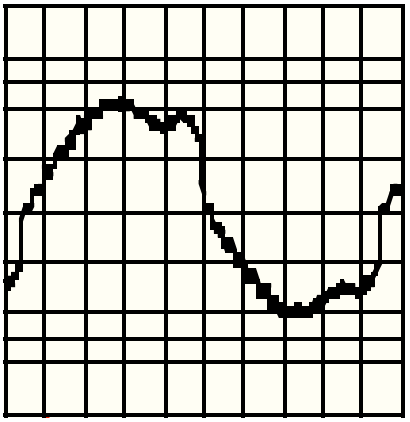
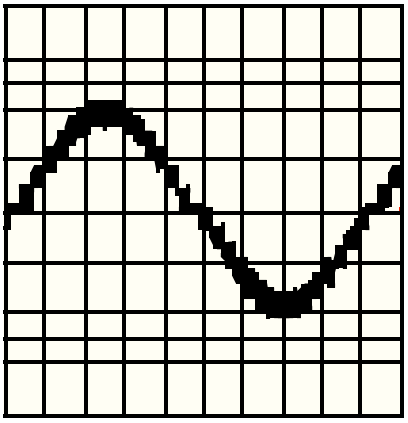


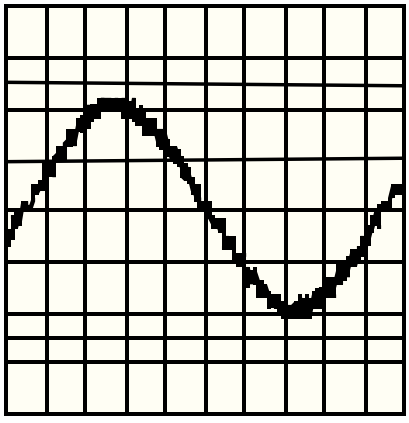
Figure 2 — Current-Decay Waveforms



A — Slow-Decay Mode



B — Fast-Decay Mode



C — Mixed-Decay Mode

Figure 3 — Sinusoidal Drive Currents

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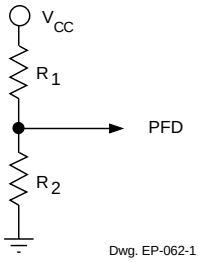
cost of decreased average current accuracy or increased driver and motor losses.

Mixed Current-Decay Mode. If V_{PFD} is between 1.2 V and 2.9 V, the device will be in a mixed current-decay mode. Mixed-decay mode allows the user to achieve good current regulation with a minimum amount of ripple current and motor/driver losses by selecting the minimum percentage of fast decay required for their application (see also Stepper Motor Applications).

As in fast current-decay mode, mixed-decay starts with the sink and source drivers disabled after the load current reaches I_{TRIP}. When the voltage at the RC terminal decays to a value below V_{PFD}, the sink drivers are re-enabled, placing the device in slow current-decay mode for the remainder of the fixed off time (figure 2). The percentage of fast decay (PFD) is user determined by V_{PFD} or two external resistors.

$$PFD = 100 \ln (0.6[R_1+R_2]/R_2)$$

where



Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one-shot off-time, t_{OFF}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminal to ground. The off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ, is approximated by:

$$t_{OFF} \approx R_T C_T.$$

When the load current is increasing, but has not yet reached the sense-current comparator threshold (I_{TRIP}), the voltage on the RC terminal is approximately $0.6V_{CC}$. When I_{TRIP} is reached, the PWM latch is reset by the current-sense comparator and the voltage on the RC terminal will decay until it reaches approximately $0.22V_{CC}$. The PWM latch is then set, thereby re-enabling the driver(s) and allowing load current to increase again. The PWM cycle repeats, maintaining the peak load current at the desired value.

With increasing values of $t_{OFF,}$ switching losses will decrease, low-level load-current regulation will improve, EMI will be reduced, the PWM frequency will decrease, and ripple current will increase. A value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} are chosen to be in the range of 15 µs to 35 µs.

RC Blanking. In addition to determining the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry (or by the PHASE input, or when the device is enabled with the DAC data inputs). The comparator output is blanked to prevent false over-current detections due to reverse recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{OFF} time, the comparator's output is blanked and C_T begins to be charged from approximately $0.22V_{CC}$ by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$. The blanking time, t_{BLANK}, can be calculated as:

$$t_{BLANK} = R_T C_T \ln (R_T/[R_T - 3\ k\Omega]).$$

When a transition of the PHASE input occurs, C_T is discharged to near ground during the crossover delay time (the crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$.

Similarly, when the device is disabled, via the DAC data inputs, C_T is discharged to near ground. When the device is re-enabled, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$. The blanking time, t_{BLANK}', can be calculated as:

$$t_{BLANK}' \approx 1900\ C_T.$$

The minimum recommended value for C_T is 470 pF ± 5 %. This value ensures that the blanking time is sufficient to avoid false trips of the comparator under normal operating conditions. For optimal regulation of the load current, this value for C_T is recommended and the value of R_T can be sized to determine t_{OFF}.

Thermal Considerations. Thermal-protection circuitry turns off all output transistors when the junction temperature reaches approximately +165°C. This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The output transistors are re-enabled when the junction temperature cools to approximately +150°C.

Stepper Motor Applications. The A3957SB or A3957SLB are used to optimize performance in microstepping/sinusoidal stepper-motor drive applications (see figures 4 and 5). When the load current is increasing, the slow current-decay mode is used to limit the switching losses in the driver and iron losses in the motor. This also improves the maximum rate at which the load current can increase (as compared to fast decay) due to the slow rate of decay during t_{OFF}. When the load current is decreasing, the mixed current-decay mode is used to regulate the load current to the desired level. This prevents tailing of the current profile caused by the back-EMF voltage of the stepper motor (see figure 3A).

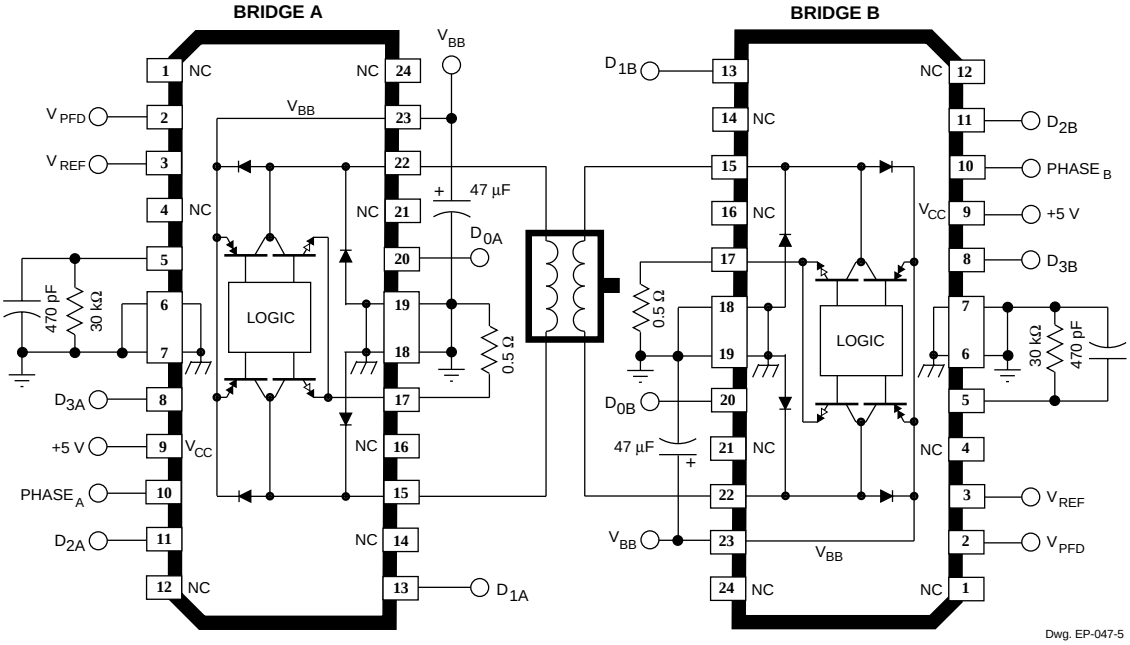


Figure 4 — Typical Application

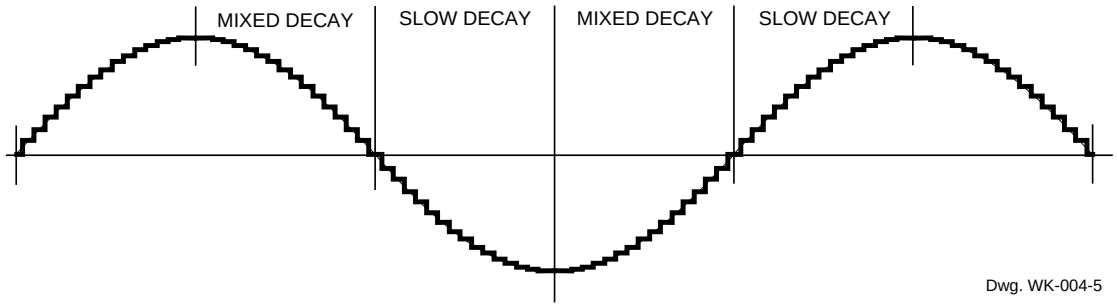


Figure 5 — Microstepping/Sinusoidal Drive Current

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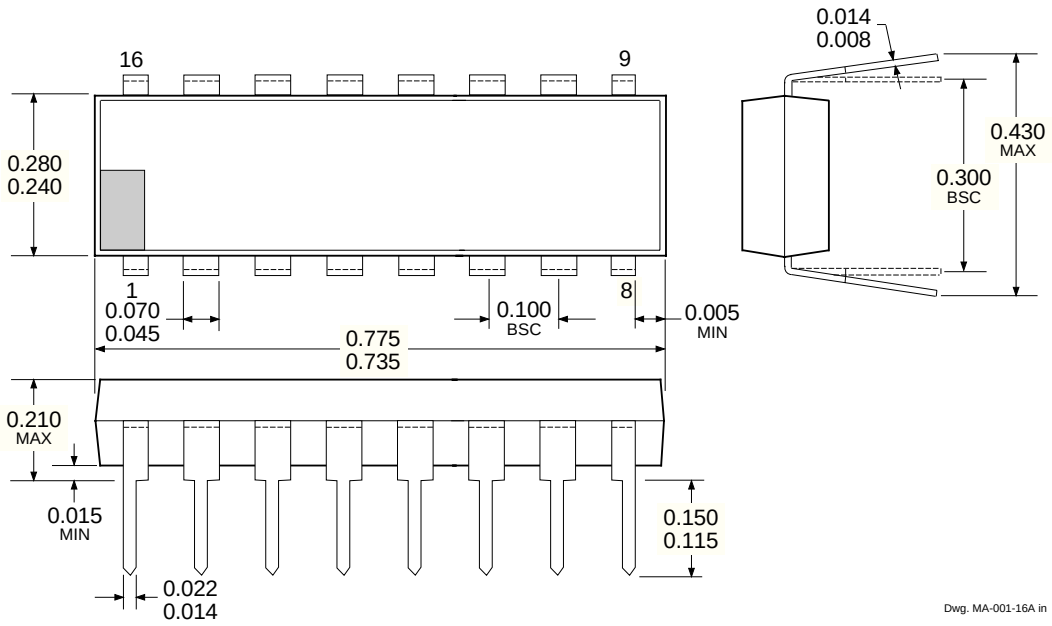
Table 4 — Step Sequencing

Full Step	1/2 Step	1/4 Step	1/8 Step	1/16 Step	Bridge A						Bridge B						Step angle
					$PHASE_A$	D_{3A}	D_{2A}	D_{1A}	D_{0A}	$I_{LOAD\ A}$	$PHASE_B$	D_{3B}	D_{2B}	D_{1B}	D_{0B}	$I_{LOAD\ B}$	
1	1	1	1	1	H	H	H	H	H	100%	X	L	L	L	X	0%	0°
				2	H	H	H	H	H	100%	H	L	L	H	L	17.4%	
			2	3	H	H	H	H	H	100%	H	L	L	H	H	26.1%	
				4	H	H	H	H	L	95.7%	H	L	H	L	L	34.8%	
		2	3	5	H	H	H	L	H	91.3%	H	L	H	L	H	43.5%	
				6	H	H	H	L	L	87.0%	H	L	H	H	L	52.2%	
			4	7	H	H	L	H	H	82.6%	H	L	H	H	H	60.9%	
				8	H	H	L	H	L	78.3%	H	H	L	L	L	69.6%	
	2	3	5	9	H	H	L	L	H	73.9%	H	H	L	L	H	73.9%	45°
				10	H	H	L	L	L	69.6%	H	H	L	H	L	78.3%	
			6	11	H	L	H	H	H	60.9%	H	H	L	H	H	82.6%	
				12	H	L	H	H	L	52.2%	H	H	H	L	L	87.0%	
		4	7	13	H	L	H	L	H	43.5%	H	H	H	L	H	91.3%	
				14	H	L	H	L	L	34.8%	H	H	H	H	L	95.7%	
			8	15	H	L	L	H	H	26.1%	H	H	H	H	H	100%	
				16	H	L	L	H	L	17.4%	H	H	H	H	H	100%	
2	3	5	9	17	X	L	L	L	X	0%	H	H	H	H	H	100%	90°
				18	L	L	L	H	L	-17.4%	H	H	H	H	H	100%	
			10	19	L	L	L	H	H	-26.1%	H	H	H	H	H	100%	
				20	L	L	H	L	L	-34.8%	H	H	H	H	L	95.7%	
		6	11	21	L	L	H	L	H	-43.5%	H	H	H	L	H	91.3%	
				22	L	L	H	H	L	-52.2%	H	H	H	L	L	87.0%	
			12	23	L	L	H	H	H	-60.9%	H	H	L	H	H	82.6%	
				24	L	H	L	L	L	-69.6%	H	H	L	H	L	78.3%	
	4	7	13	25	L	H	L	L	H	-73.9%	H	H	L	L	H	73.9%	135°
				26	L	H	L	H	L	-78.3%	H	H	L	L	L	69.6%	
			14	27	L	H	L	H	H	-82.6%	H	L	H	H	H	60.9%	
				28	L	H	H	L	L	-87.0%	H	L	H	H	L	52.2%	
		8	15	29	L	H	H	L	H	-91.3%	H	L	H	L	H	43.5%	
				30	L	H	H	H	L	-95.7%	H	L	H	L	L	34.8%	
			16	31	L	H	H	H	H	-100%	H	L	L	H	H	26.1%	
				32	L	H	H	H	H	-100%	H	L	L	H	L	17.4%	
3	5	9	17	33	L	H	H	H	H	-100%	X	L	L	L	X	0%	180°
				34	L	H	H	H	H	-100%	L	L	L	H	L	-17.4%	
			18	35	L	H	H	H	H	-100%	L	L	L	H	H	-26.1%	
				36	L	H	H	H	L	-95.7%	L	L	H	L	L	-34.8%	
		10	19	37	L	H	H	L	H	-91.3%	L	L	H	L	H	-43.5%	
				38	L	H	H	L	L	-87.0%	L	L	H	H	L	-52.2%	
			20	39	L	H	L	H	H	-82.6%	L	L	H	H	H	-60.9%	
				40	L	H	L	H	L	-78.3%	L	H	L	L	L	-69.6%	
	6	11	21	41	L	H	L	L	H	-73.9%	L	H	L	L	H	-73.9%	225°
				42	L	H	L	L	L	-69.6%	L	H	L	H	L	-78.3%	
			22	43	L	L	H	H	H	-60.9%	L	H	L	H	H	-82.6%	
				44	L	L	H	H	L	-52.2%	L	H	H	L	L	-87.0%	
		12	23	45	L	L	H	L	H	-43.5%	L	H	H	L	H	-91.3%	
				46	L	L	H	L	L	-34.8%	L	H	H	H	L	-95.7%	
			24	47	L	L	L	H	H	-26.1%	L	H	H	H	H	-100%	
				48	L	L	L	H	L	-17.4%	L	H	H	H	H	-100%	
4	7	13	25	49	X	L	L	L	X	0%	L	H	H	H	H	-100%	270°
				50	H	L	L	H	L	17.4%	L	H	H	H	H	-100%	
			26	51	H	L	L	H	H	26.1%	L	H	H	H	H	-100%	
				52	H	L	H	L	L	34.8%	L	H	H	H	L	-95.7%	
		14	27	53	H	L	H	L	H	43.5%	L	H	H	L	H	-91.3%	
				54	H	L	H	H	L	52.2%	L	H	H	L	L	-87.0%	
			28	55	H	L	H	H	H	60.9%	L	H	L	H	H	-82.6%	
				56	H	H	L	L	L	69.6%	L	H	L	H	L	-78.3%	
	8	15	29	57	H	H	L	L	H	73.9%	L	H	L	L	H	-73.9%	315°
				58	H	H	L	H	L	78.3%	L	H	L	L	L	-69.6%	
			30	59	H	H	L	H	H	82.6%	L	L	H	H	H	-60.9%	
				60	H	H	H	L	L	87.0%	L	L	H	H	L	-52.2%	
		16	31	61	H	H	H	L	H	91.3%	L	L	H	L	H	-43.5%	
				62	H	H	H	H	L	95.7%	L	L	H	L	L	-34.8%	
			32	63	H	H	H	H	H	100%	L	L	L	H	H	-26.1%	
				64	H	H	H	H	H	100%	L	L	L	H	L	-17.4%	

A3957SA

Dimensions in Inches

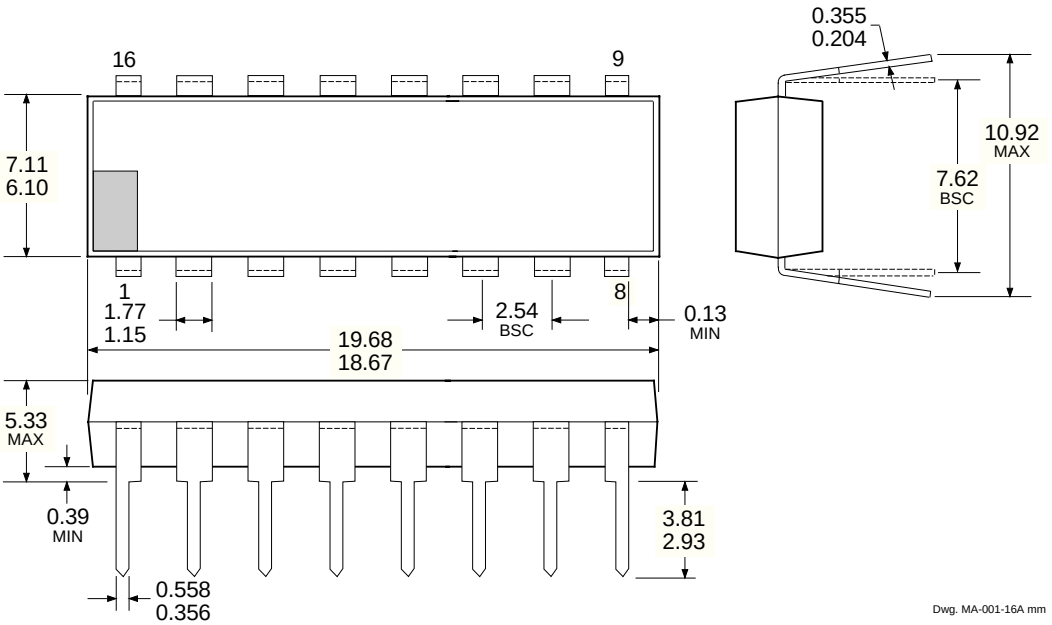
(controlling dimensions)



Dwg. MA-001-16A in

Dimensions in Millimeters

(for reference only)



Dwg. MA-001-16A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Lead thickness is measured at seating plane or below.

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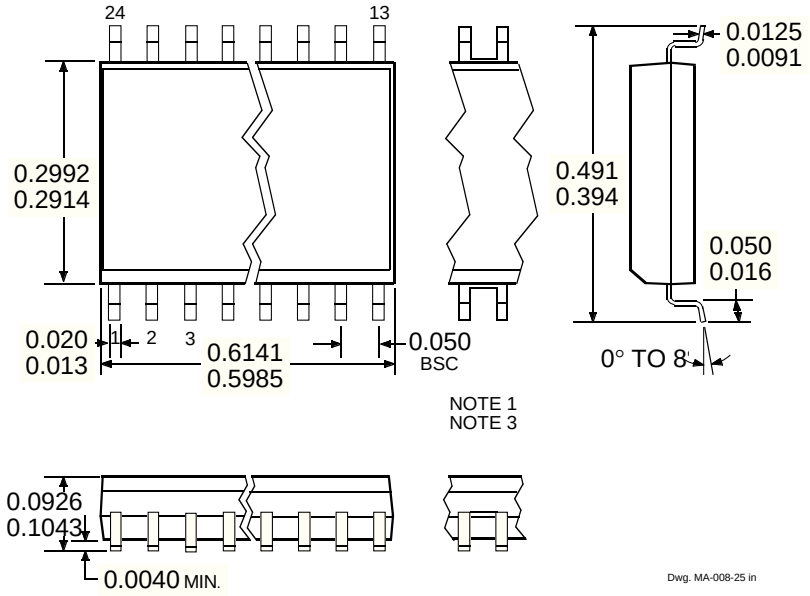
A3957SLB

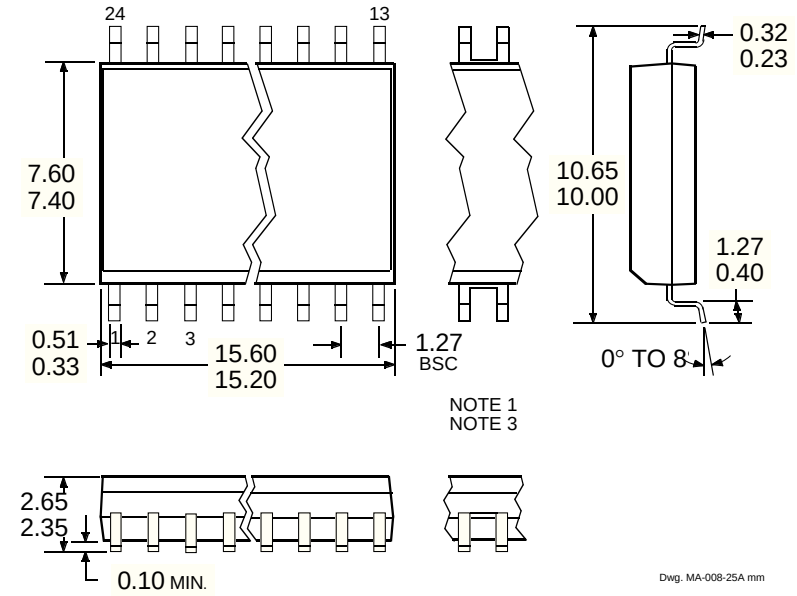
Dimensions in Inches

(for reference only)



Dimensions in Millimeters

(controlling dimensions)



NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Webbed lead frame. Leads 4, 5, 12, and 13 are internally one piece.

3957
FULL-BRIDGE PWM MICROSTEPPING MOTOR DRIVER

Allegro® MicroSystems, Inc.

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