32K x 36 Bit Synchronous Dual I/O, Dual Address SRAM

The MCM69D536 is a 1M–bit static random access memory, organized as 32K words of 36 bits. It features common data input and data output buffers and incorporates input and output registers on–board with high speed SRAM.

The MCM69D536 allows the user to concurrently perform reads, writes, or pass–through cycles in combination on the two data ports. The two address ports (AX, AY) determine the read or write locations for their respective data ports (DQX, DQY).

The synchronous design allows for precise cycle control with t<u>he use of</u> an external single clock (K). All signal pins except output enables (GX, GY) are registered on the rising edge of clock (K).

The pass-through feature allows data to be passed from one port to the other, in either direction. The PTX input must be asserted to pass data from port X to port Y. The PTY will likewise pass data from port Y to port X. A pass-through operation takes precedence over a read operation.

For the case when AX and AY are the same, certain protocols are followed. If both ports are read, the reads occur normally. If one port is written and the other is read, the read from the array will occur before the data is written. If both ports are written, only the data on DQY will be written to the array.

- Single 3.3 V ± 5% Power Supply
- Fast Access Times: 6/8 ns Max
- Throughput of 2.98 Gigabits/Second
- Single Clock Operation
- Address, Data Input, E1, E2, PTX, PTY, WX, WY, and Data Output Registers On–Chip
- 83 MHz Maximum Clock Frequency
- Self-Timed Write
- Two Bi-Directional Data Buses
- Can be Configured as Separate I/O
- Pass–Through Feature
- Asynchronous Output Enables (GX, GY)
- LVTTL Compatible I/O
- Concurrent Reads and Writes
- 176–Pin TQFP Package

Suggested Applications

- ATM
- Cell/Frame Buffers SNA Switches
- Ethernet Switches Routers
 SNA Switches Shared Memory

Product Family Configurations

Part Number	Dual Address	Single Address	Dual I/O	Separate I/O	Configuration	V _{DD}
MCM69D536	~	Note 1	~	Note 2	32K x 36	3.3 V
MCM69D618	~	Note 1	~	Note 2	64K x 18	3.3 V
MCM67Q709A		1		~	128K x 9	5.0 V
MCM67Q909		~		~	512K x 9	5.0 V

NOTES:

1. Tie <u>AX</u> and AY address ports together for <u>the</u> part to function as a single address part.

2. Tie GX high for DQX to be inputs and tie WY high and GY low for DQY to be outputs.

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MOTOROLA



MCM69D536

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Туре	Description	
65, 63, 61, 59, 57, 55, 169, 167, 145, 143, 68, 70, 72, 74, 76	AX0 – AX14	Input	Address Port X. Never allow floating addresses for inputs AX0 – AX14. A pullup resistor is needed.	
64, 62, 60, 58, 56, 54, 168, 166, 144, 142, 69, 71, 73, 75, 77	AY0 – AY14	Input	Address Port Y. Never allow floating addresses for inputs AY0 – AY14. A pullup resistor is needed.	
82, 86, 90, 94, 96, 100, 102, 106, 108, 113. 115, 119, 121, 125, 127, 131, 135, 139, 170, 174, 2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51	DQX0 – DQX35	I/O	Data Input/Output Port X.	
83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 134, 138, 171, 175, 3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50	DQY0 – DQY35	I/O	Data Input/Output Port Y.	
150	E1	Input	Synchronous Chip Enable: Active low.	
151	E2	Input	Synchronous Chip Enable: Active high.	
152	GX	Input	Asynchronous Output Enable Port X Input: Low — enables output buffers (DQXx pins). High — DQXx pins are high impedance.	
153	GY	Input	Asynchronous Output Enable Port Y Input: Low — enables output buffers (DQYx pins). High — DQYx pins are high impedance.	
156	к	Input	Clock: <u>Th</u> is signal registers the address, data in, and all control signals except G.	
146	PTX	Input	Pass-Through Port X.	
147	PTY	Input	Pass-Through Port Y.	
148	WX	Input	Synchronous Write Enable Port X.	
149	WY	Input	Synchronous Write Enable Port Y.	
4, 10, 16, 22, 28, 34, 40, 49, 67, 84, 92, 98, 104, 110, 116, 122, 128, 137, 155, 172	VDD	Supply	+ 3.3 V Power Supply.	
5, 11, 17, 23, 29, 35, 41, 48, 66, 85, 93, 99, 105, 111, 117, 123. 129, 136, 154, 173	VSS	Supply	Ground.	
1, 44, 45, 52, 53, 88, 89, 132, 133, 165, 176	V _{SSi}	Input	Bonded to die flag. No chip current flows through these pins.	
78–81, 140, 141, 157–164	NC	_	No Connection: There is no connection to the chip.	

TRUTH TABLE (See Notes 1 through 5)

	Input at t _n Clock							
Operation Number	E1	E2	wx	WY	РТХ	PTY	Operation	
1	Н	Х	Х	Х	Х	Х	Deselected	
2	Х	L	Х	Х	Х	Х	Deselected	
3	L	Н	0	Х	Х	Х	Write X Port	
4	L	Н	Х	0	Х	Х	Write Y Port	
5	L	Н	Х	Х	0	Х	Pass–Through X to Y	
6	L	Н	Х	Х	Х	0	Pass–Through Y to X	
7	L	Н	1	Х	1	1	Read X	
8	L	Н	Х	1	1	1	Read Y	

NOTE<u>S:</u>

1. GX/GY must be controlled to avoid bus contention issues during write and pass-through cycles.

2. Operation numbers 3-6 can be used in any combination.

3. Operation numbers 4 and 7, 3 and 8, 7 and 8 can be combined.

4. Operation number 5 can not be combined with operation number 7 or 8 because pass-through takes precedence over a read operation.

5. Operation number 6 can not be combined with operation number 7 or 8 because pass-through takes precedence over a read operation.



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V _{in} , V _{out}	– 0.5 to V _{DD} + 0.5	V
Output Current	l _{out}	± 20	mA
Power Dissipation	PD	TBD	W
Temperature Under Bias	T _{bias}	– 10 to + 85	°C
Operating Temperature	TA	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for *ALL* rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

PACKAGE THERMAL CHARACTERISTICS (See Note 1)

Rating		Symbol	TQFP	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single–Layer Board Four–Layer Board	R _{θJA}	40 35	°C/W	2
Junction to Board (Bottom)		R _{θJB}	23	°C/W	3
Junction to Case (Top)		R _θ JC	9	°C/W	4

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.

2. Per SEMI G38-87.

3. Indicates the average thermal resistance between the die and the printed circuit board.

4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC-883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V \pm 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit	
Supply Voltage (Operating Voltage Range)		V _{DD}	3.135	3.465	V
Input High Voltage		VIH	2.0	V _{DD} + 0.5**	V
Input Low Voltage		VIL	- 0.5*	0.8	V
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{DD})	l _{lkg(l)}	_	± 1.0	μΑ	
Output Leakage Current ($E = V_{IH}$, $V_{out} = 0$ to V_{DD})	I _{lkg(O)}	_	± 1.0	μΑ	
AC Supply Current ($I_{out} = 0 \text{ mA}$) ($V_{DD} = \max, f = f_{max}$)	MCM69D536–6 ns MCM69D536–8 ns	IDDA		300 300	mA
$\begin{array}{l} \mbox{CMOS Standby Supply Current (Deselected, Clock (K) \\ \mbox{Cycle Time} \geq t_{KHKH}, \mbox{All Inputs Toggling at CMOS Levels} \\ \mbox{V}_{in} \leq V_{SS} + 0.2 \ \mbox{V or} \geq V_{DD} - 0.2 \ \mbox{V}) \end{array}$	MCM69D536–6 ns MCM69D536–8 ns	I _{SB1}		100 100	mA
Output Low Voltage (I _{OL} = + 8.0 mA)	VOL	—	0.4	V	
Output High Voltage (I _{OH} = - 4.0 mA)		VOH	2.4	V _{DD}	V

* VIL \geq - 1.5 V for t \leq t_{KHKH}/2. ** VIH \leq VDD + 1.0 V for t \leq t_{KHKH}/2.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C _{in}	6	pF
Control Pin Input Capacitance	C _{in}	6	pF
Output Capacitance	Cout	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V \pm 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level		1.5 V
Input Pulse Levels	0 to	3.0 V
Input Rise/Fall Time		3 ns

 Output Timing Reference Level
 1.5 V

 Output Load
 Figure 1 Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

			MCM69D536-6		MCM69D536-8			
Paramo	eter	Symbol	Min	Max	Min	Max	Unit	Notes
Cycle Time		^t КНКН	12	—	15	—	ns	1
Clock Access Time		^t KHQV	—	6	-	8	ns	
Clock Low Pulse Width		^t KLKH	4	—	6	—	ns	
Clock High Pulse Width		^t KHKL	4	—	6	—	ns	
Clock High to Data Output Ac	tive	^t KHQX1	0	—	0	—	ns	
Clock High to Data Output Inv	valid	^t KHQX2	2	—	2	—	ns	
Clock High to Data Output High–Z		^t KHQZ	-	5	-	5	ns	2
Output Enable Low to Data Output Valid		^t GLQV	—	6	-	8	ns	
Output Enable Low to Data Output Low-Z		^t GLQX	0	-	0	—	ns	
Output Enable High to Data C	Dutput High–Z	^t GHQZ	-	5	-	8	ns	2
Setup Times:	AWR0 – AWR14 ARD0 – ARD <u>14</u> <u>W</u> PT E1, E2 D0 – D35	^t AVKH ^t AVKH ^t WVKH ^t PTVKH ^t EVKH ^t DVKH	2.5	_	3	_	ns	3
Hold Times:	AWR0 – AWR14 ARD0 – ARD1 <u>4</u> <u>W</u> PT E1, E2 D0 – D35	^t KHAX ^t KHAX ^t KHWX ^t KHPTX ^t KHEX ^t KHDX	0.5	_	1	_	ns	3 3 3 3 3 3, 4

NOTES:

1. All read and write cycles are referenced from K.

2. This parameter is sampled and not 100% tested.

3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for *ALL* rising edges of clock (K) while the device is selected.

4. t_{KHDX} minimum for Port Y only extends to 4.0 ns only for the special case when the Y- and X-address are identical on the same rising clock edge.



Figure 1. AC Test Load



NOTE: \overline{E} Low = $\overline{E1}$ Low and E2 High. \overline{E} High = $\overline{E1}$ High or E2 Low.



NOTE: \overline{E} Low = $\overline{E1}$ Low and E2 High. \overline{E} High = $\overline{E1}$ High or E2 Low.





COMBINATION READ/WRITE WITH SAME ADDRESS ON EACH PORT



 $\overline{\text{PTX}} = \overline{\text{PTY}} = \text{high.}$

D(Value) = Value is the input to the data port. Q(Value) = Value is the output from the data port.

ORDERING INFORMATION

(Order by Full Part Number)



PACKAGE DIMENSIONS

TQFP PACKAGE 176 LEAD CASE 1101-01











- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUMS -L-, -M-, AND -N- TO BE DETERMINED AT DATUM PLANE -H.
- -H-. -TH- DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A
- AND B DO INLCUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
- DATUM PLANE –H-. 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35 (0.014) MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD 0.07 (0.003).

	MILLIN	IETERS			
DIM	MIN MAX				
Α	24.00	BSC			
A1	12.00	BSC			
В	24.00	BSC			
B1	12.00	BSC			
С		1.60			
C1	0.05				
C2	1.35	1.45			
D	0.17	0.23			
E	0.45	0.75			
F	0.17	0.27			
G	0.50 BSC				
J	0.09	0.20			
K	0.50 REF				
Р	0.25 BSC				
R1	0.10	0.20			
S	26.00	BSC			
S1	13.00	BSC			
U	0.09	0.16			
۷	26.00 BSC				
V1	13.00 BSC				
W	0.20 REF				
Z	1,00 REF				
θ	0 °	7°			
<u>01</u>	0 0				
θ2	12°	REF			

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