CY7C4282V
CY7C4292V

64K/128Kx9 Low Voltage Deep Sync FIFOs w/ Retransmit & Depth Expansion

Features

- **3.3V operation for low power consumption and easy integration into low-voltage systems**
- **High-speed, low-power, first-in first-out (FIFO) memories**
- **64K x 9 (CY7C4282V)**
- **128K x 9 (CY7C4292V)**
- **0.35 micron CMOS for optimum speed/power**
- **High-speed, Near Zero Latency (True Dual-Ported Memory Cell), 100-MHz operation (10 ns read/write cycle times)**
- **Low power**
  - **— I_{CC} = 25 mA**
  - **— I_{SB} = 6 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, and Programmable Almost Empty and Almost Full status flags**
- **Retransmit function**
- **Output Enable ($\overline{OE}$) pin**
- **Independent read and write enable pins**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion Capability**
- **Depth Expansion Capability through token-passing scheme (no external logic required)**
- **64-pin 10x10 STQFP**
- **Pin-compatible 3.3V solution for CY7C4282/92**

Functional Description

The CY7C4282V/92V are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All devices are 9 bits wide. The CY7C4282V/92V can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, video and communications buffering.

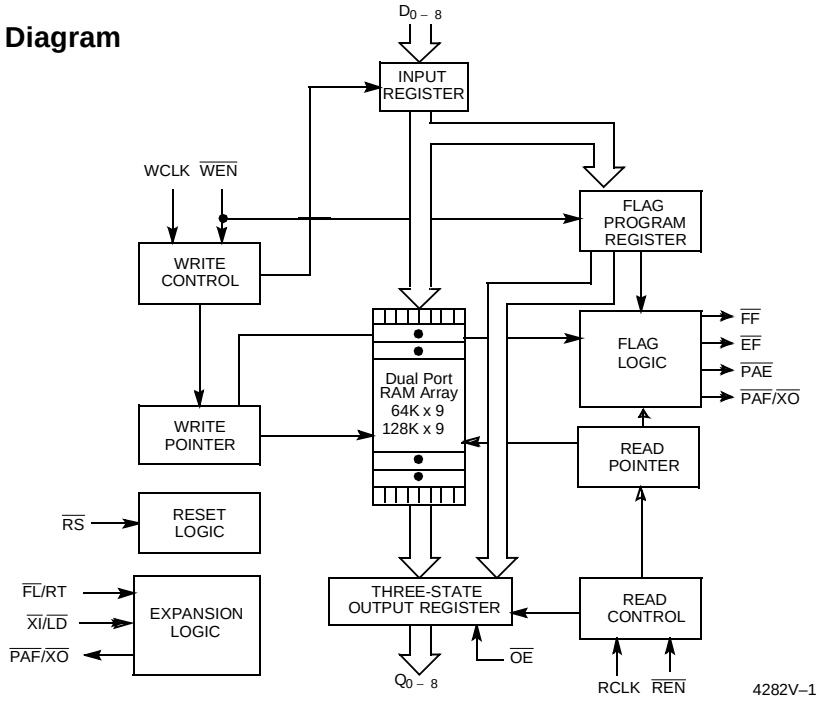
These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a Write Enable pin ($\overline{WEN}$).

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

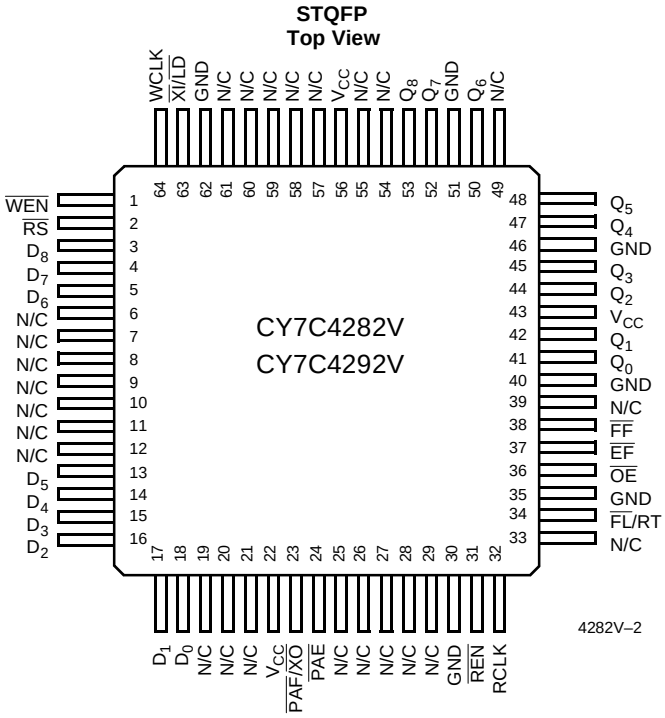
Depth expansion is possible using the Cascade Input ($\overline{XI}$), Cascade Output ($\overline{XO}$), and First Load ($\overline{FL}$) pins. The $\overline{XO}$ pin is connected to the $\overline{XI}$ pin of the next device, and the $\overline{XO}$ pin of the last device should be connected to the $\overline{XI}$ pin of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}

When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running Read Clock (RCLK) and a Read Enable pin ($\overline{REN}$). In addition, the CY7C4282V/92V have an Output Enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 67 MHz are achievable.

Logic Block Diagram



Pin Configuration



Functional Description (continued)

The CY7C4282V/92V provides four status pins: Empty, Full, Programmable Almost Empty, and Programmable Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty+7 and Full–7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.35µ CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C4282V/92V-10	7C4282V/92V-15	7C4282V/92V-25
Maximum Frequency (MHz)		100	66.7	40
Maximum Access Time (ns)		8	10	15
Minimum Cycle Time (ns)		10	15	25
Minimum Data or Enable Set-Up (ns)		3.5	4	6
Minimum Data or Enable Hold (ns)		0	0	1
Maximum Flag Delay (ns)		8	10	15
Active Power Supply Current (I_{CC}) (mA)	Commercial	25	25	25
	Industrial		30	

	CY7C4282V	CY7C4292V
Density	64k x 9	128k x 9
Package	64-pin 10x10 TQFP	64-pin 10x10 TQFP

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	Data Inputs for 9-bit bus.
Q_{0-8}	Data Outputs	O	Data Outputs for 9-bit bus.
$\overline{WEN}$	Write Enable	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted and $\overline{FF}$ is HIGH.
$\overline{REN}$	Read Enable	I	Enables the device for Read operation. $\overline{REN}$ must be asserted LOW to allow a Read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}/\overline{XO}$	Programmable Almost Full/ Expansion Output	O	Dual-Mode Pin: Cascaded - Connected to $\overline{XI}$ of next device. Not Cascaded - When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FL}$/RT	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded - The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standard mode or width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded - Retransmit function is available in stand-alone mode by strobing RT.
$\overline{XI}/\overline{LD}$	Expansion Input/Load	I	Dual-Mode Pin: Cascaded - Connected to $\overline{XO}$ of previous device. Not Cascaded - $\overline{LD}$ is used to write or read the programmable flag offset registers. $\overline{LD}$ must be asserted LOW during reset to enable standalone or width expansion operation. If programmable offset register access is not required, $\overline{LD}$ can be tied to $\overline{RS}$ directly.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to V_{CC} +0.5V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC}+0.5V

DC Input Voltage ..... –0.5V to V_{CC} +0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC} [2]
Commercial	0°C to +70°C	3.3V +/–300mV
Industrial[1]	–40°C to +85°C	3.3V +/–300mV

Notes:
1. T_A is the "instant on" case temperature.
2. V_{CC} Range for commercial -10 ns is 3.3V ± 150 mV.

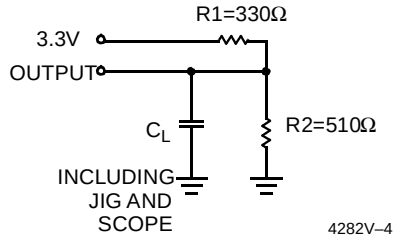
Electrical Characteristics Over the Operating Range

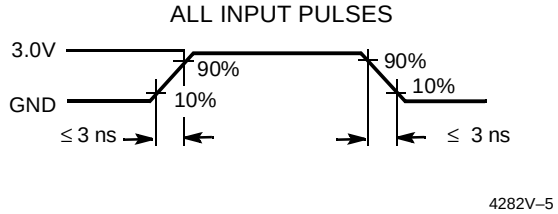
Parameter	Description	Test Conditions		7C4282V/92V -10		7C4282V/92V -15		7C4282V/92V -25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA V_{CC} = 3.0V, I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA V_{CC} = 3.0V, I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	µA
I_{CC1}[3]	Active Power Supply Current		Com'l		25		25		25	mA
			Ind				30			mA
I_{SB}[4]	Average Standby Current		Com'l		6		6		6	mA
			Ind				6			mA

Capacitance[5]

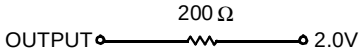
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms (-15 , -25) [6, 7]

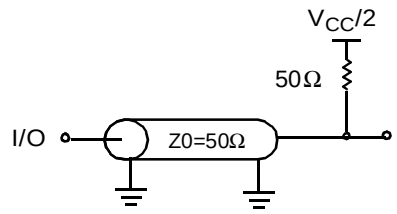


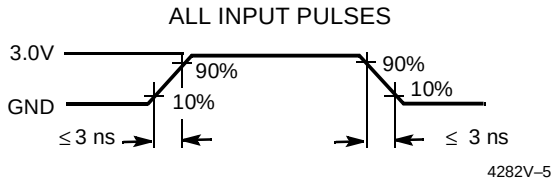


Equivalentto: THÉVENIN EQUIVALENT



AC Test Loads and Waveforms (-10)





Notes:

3. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.
4. All inputs = V_{CC} – 0.2V, except WCLK and RCLK (which are switching at frequency = 0 MHz). All outputs are unloaded.
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 30 pF for all AC parameters except for t_{OHZ}.
7. C_L = 5 pF for t_{OHZ}.

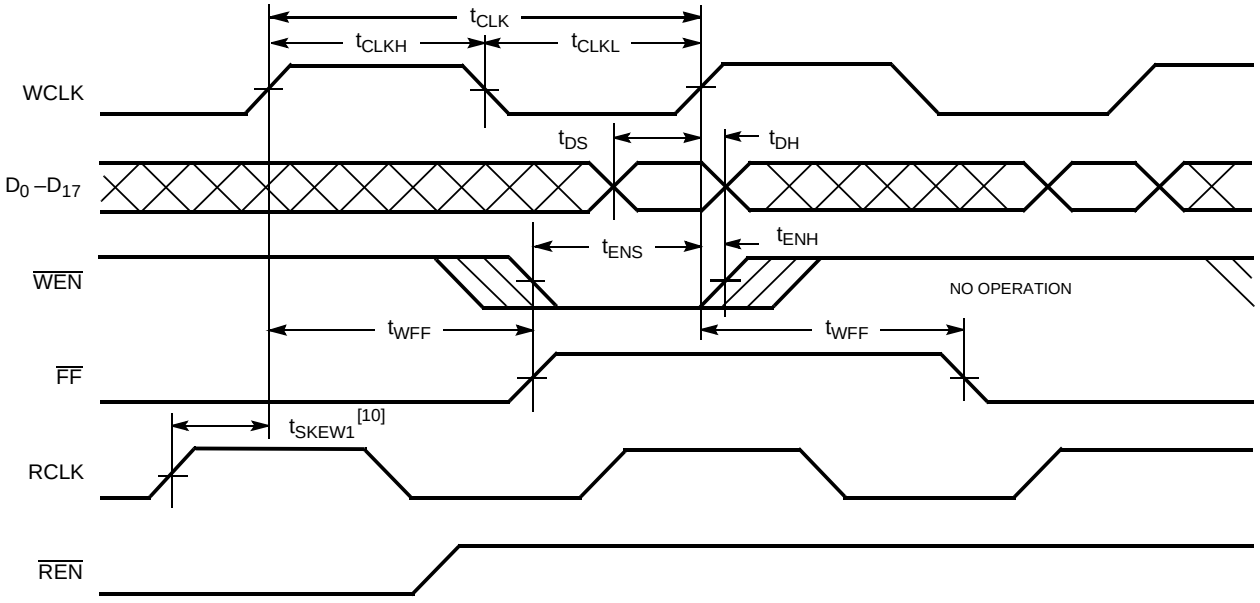
Switching Characteristics Over the Operating Range

Parameter	Description	7C4282V/92V -10		7C4282V/92V -15		7C4282V/92V -25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40	MHz
t_A	Data Access Time	2	8	2	10	2	15	ns
t_{CLK}	Clock Cycle Time	10		15		25		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		ns
t_{DS}	Data Set-Up Time	3.5		4		6		ns
t_{DH}	Data Hold Time	0		0		1		ns
t_{ENS}	Enable Set-Up Time	3.5		4		6		ns
t_{ENH}	Enable Hold Time	0		0		1		ns
t_{RS}	Reset Pulse Width[8]	10		15		25		ns
t_{RSS}	Reset Set-Up Time	8		10		15		ns
t_{RSR}	Reset Recovery Time	8		10		15		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25	ns
t_{PRT}	Retransmit Pulse Width	60		60		60		ns
t_{RTR}	Retransmit Recovery Time	90		90		90		ns
t_{OLZ}	Output Enable to Output in Low Z[9]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	10	3	12	ns
t_{OHZ}	Output Enable to Output in High Z[9]	3	7	3	8	3	12	ns
t_{WFF}	Write Clock to Full Flag		8		10		15	ns
t_{REF}	Read Clock to Empty Flag		8		10		15	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	10		15		18		ns

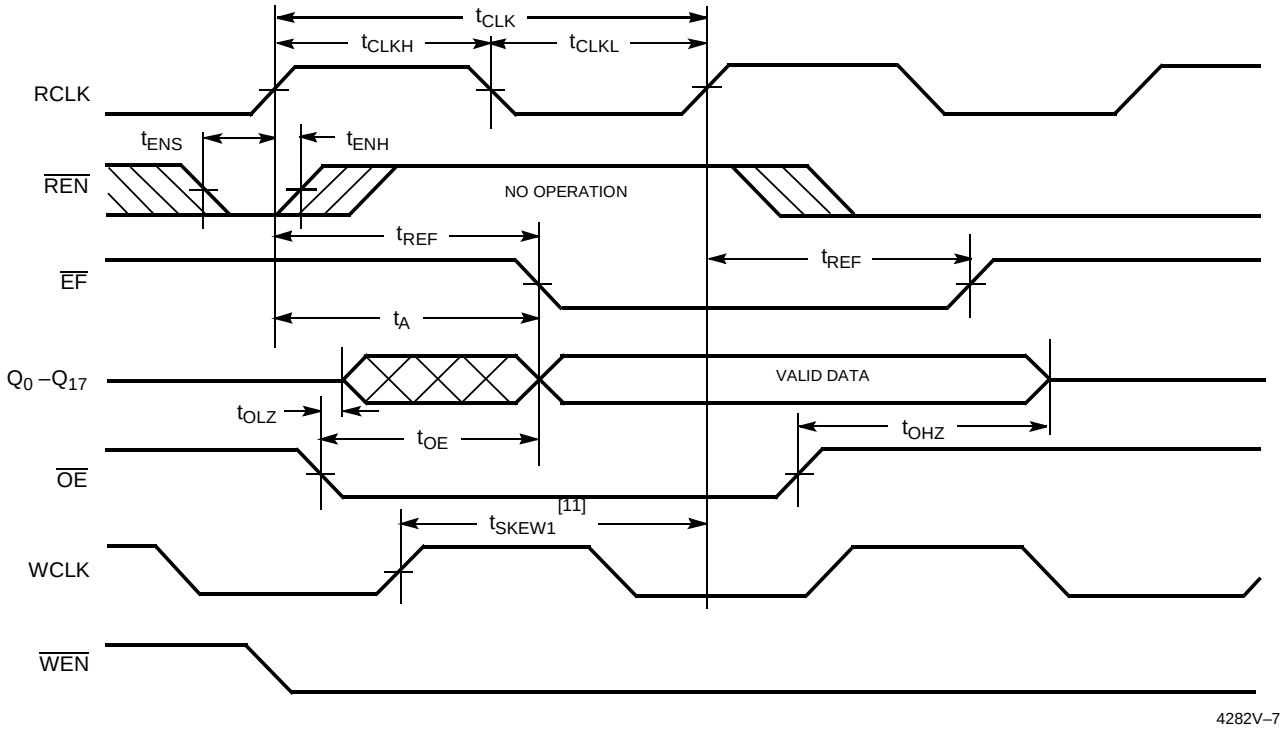
Notes:
8. Pulse widths less than minimum values are not allowed.
9. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

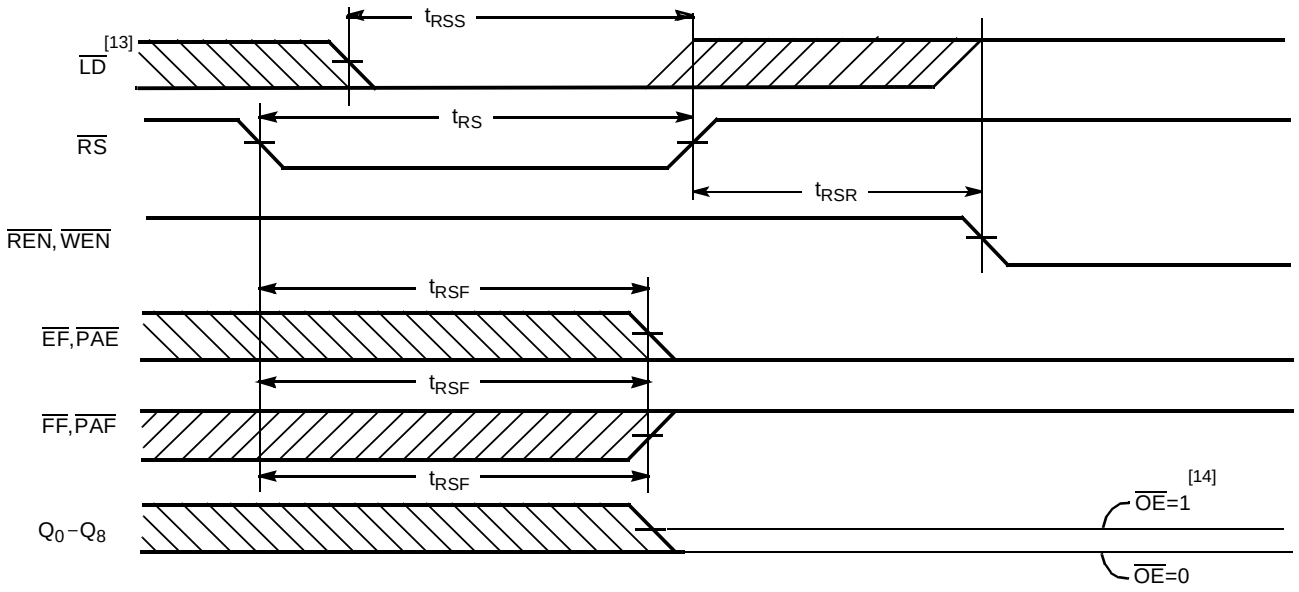


Notes:

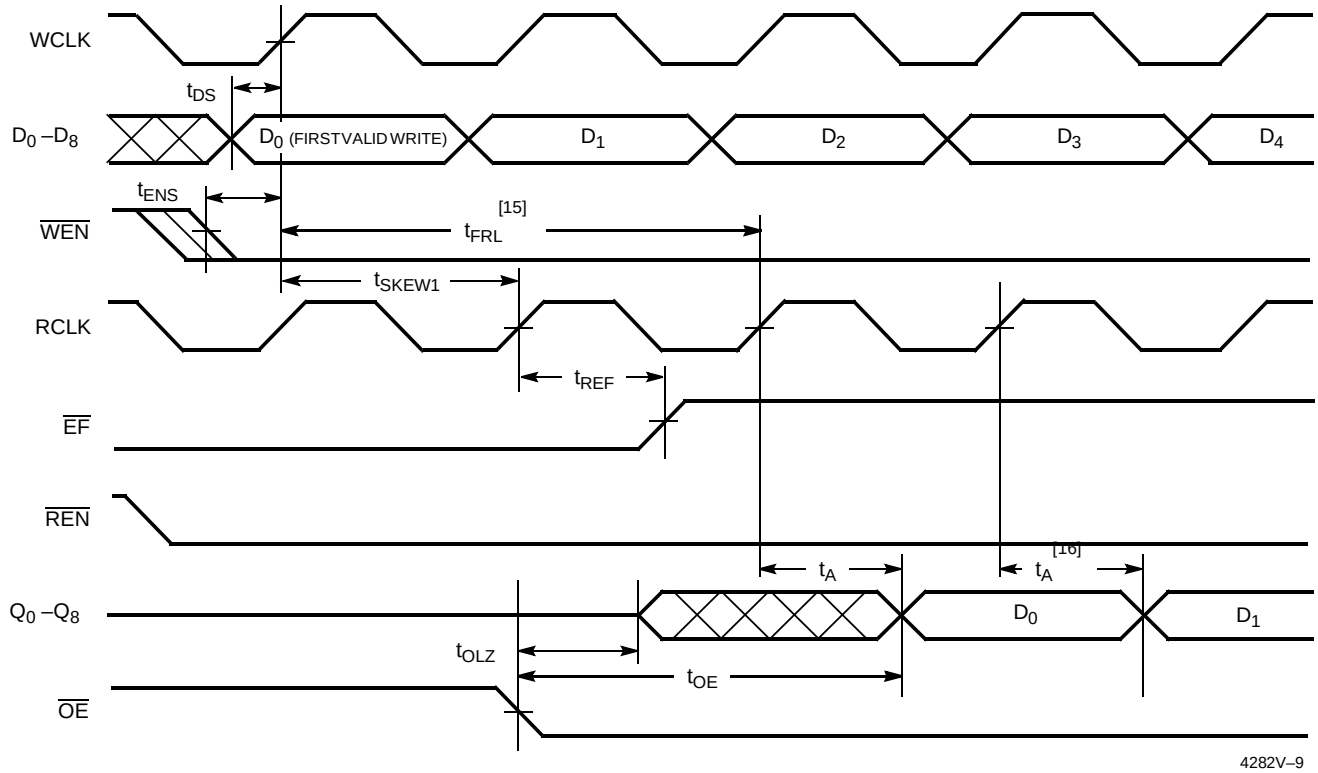
10. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
11. t_{SKEW1} is also the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing [12]



First Data Word Latency after Reset with Simultaneous Read and Write

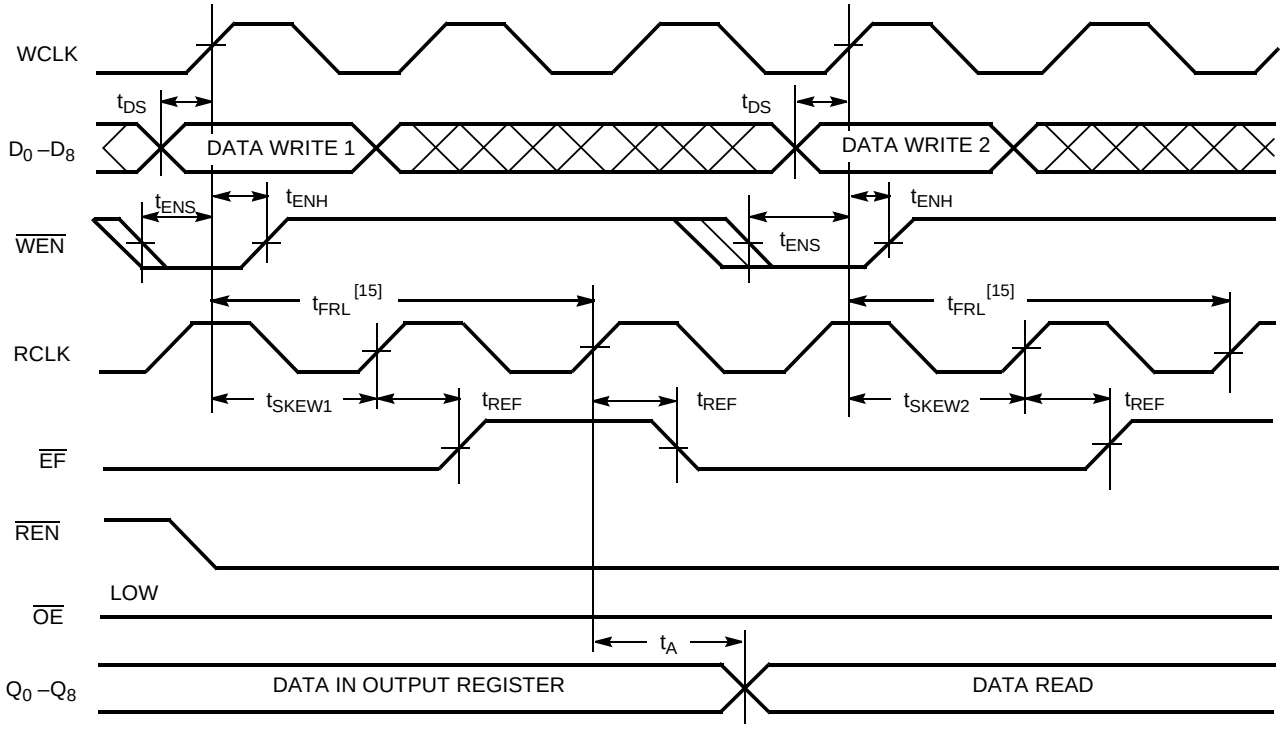


Notes:

12. The clocks (RCLK, WCLK) can be free-running during reset.
13. For standalone or width expansion configuration only.
14. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$=1.
15. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
16. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

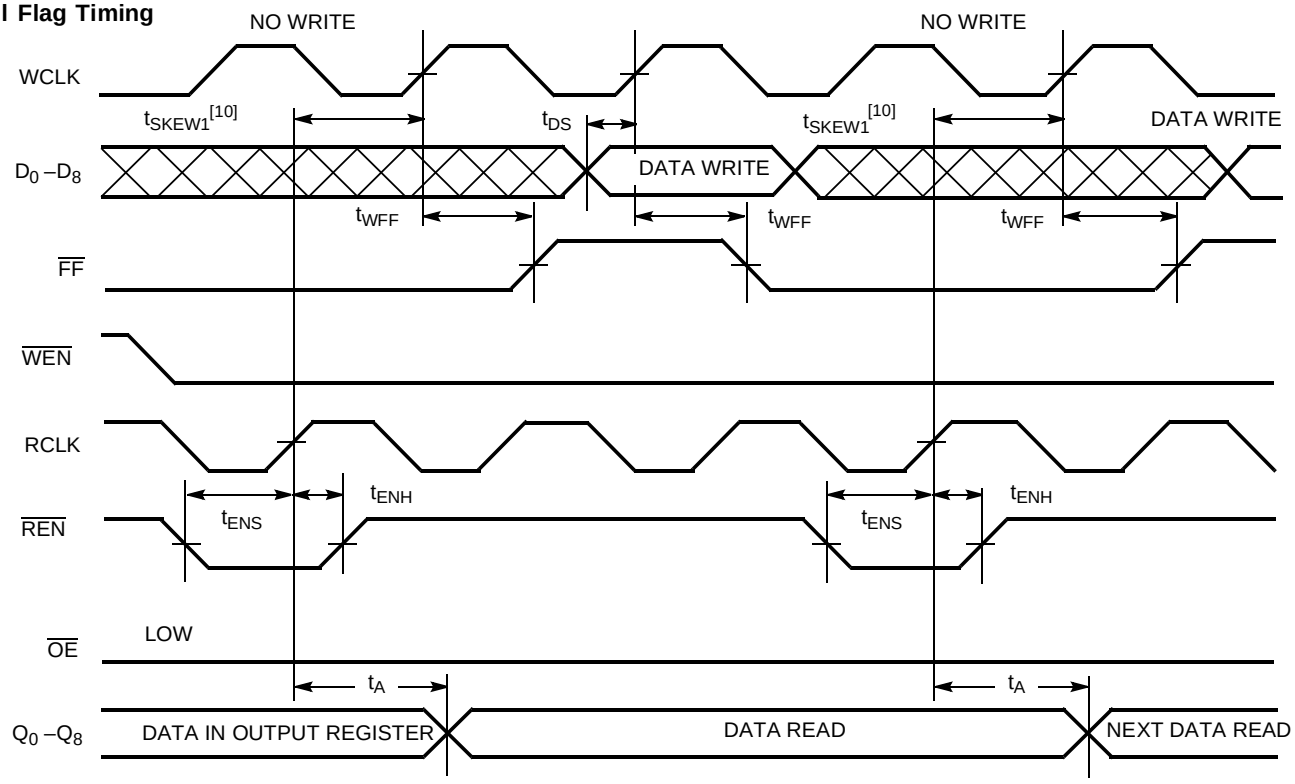
Switching Waveforms (continued)

Empty Flag Timing



4282V–10

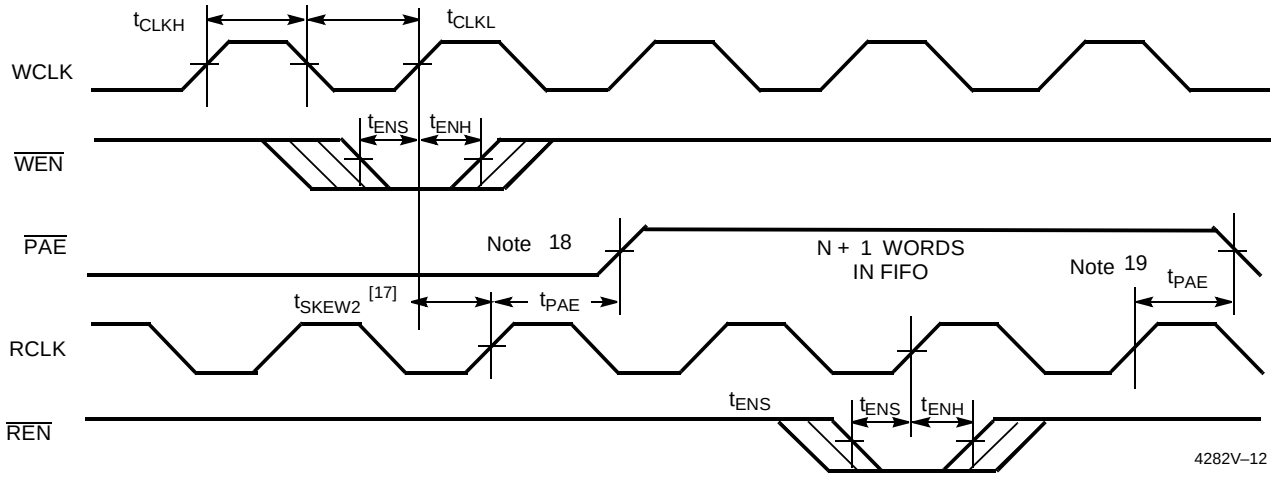
Full Flag Timing



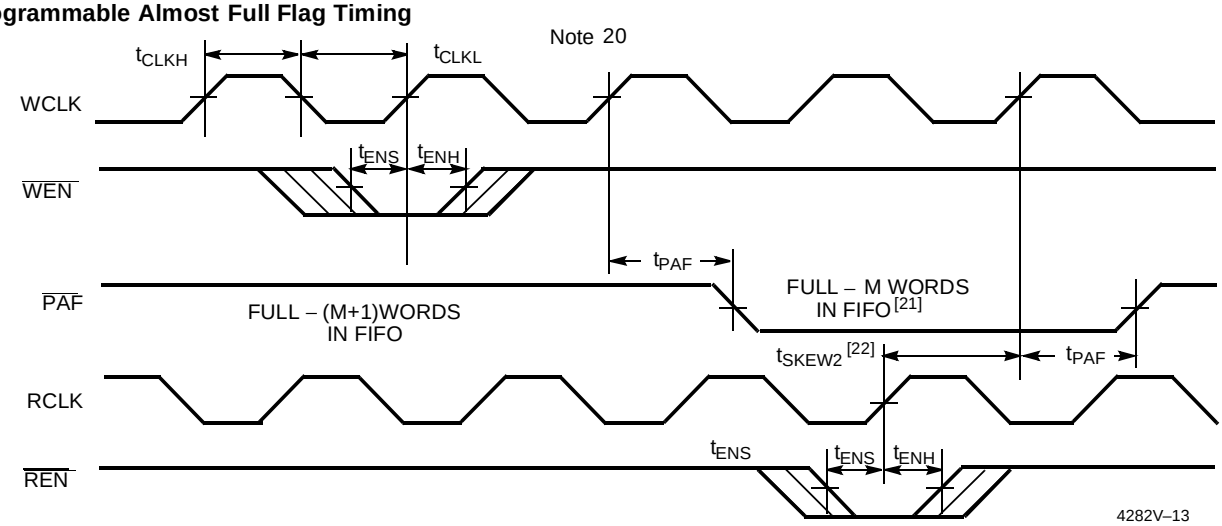
4282V–11

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Full Flag Timing

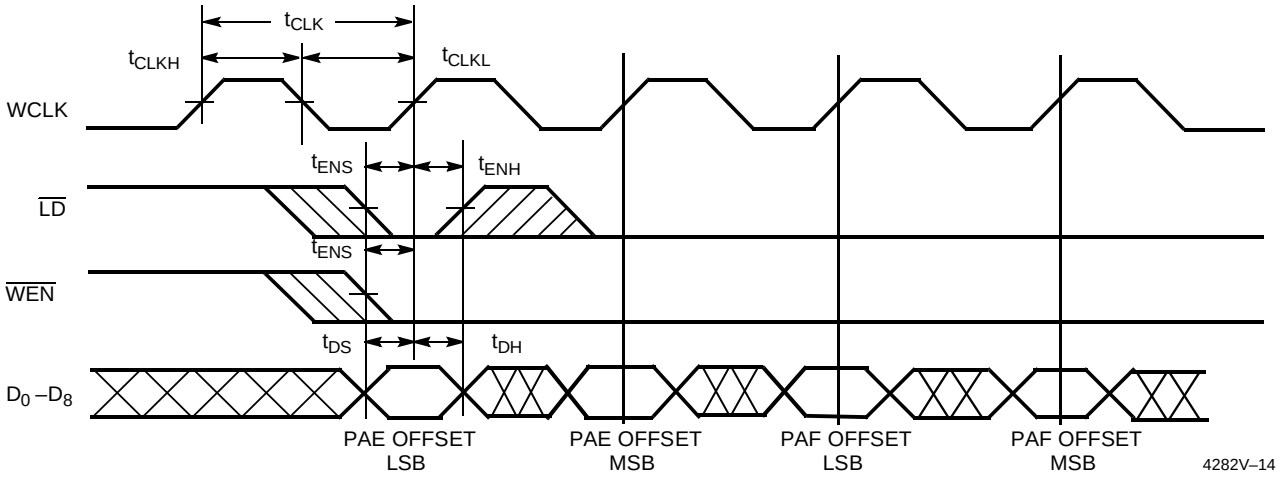


Notes:

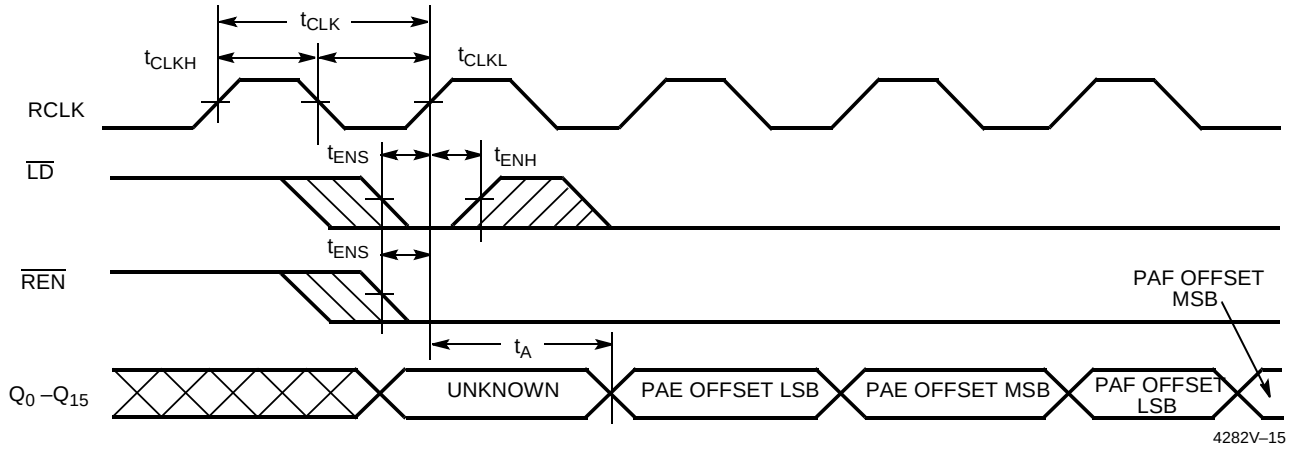
17. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
18. PAE offset= n.
19. If a read is performed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW
20. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
21. 64K – m words for CY7C4282V, 128K – m words for CY4292V.
22. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

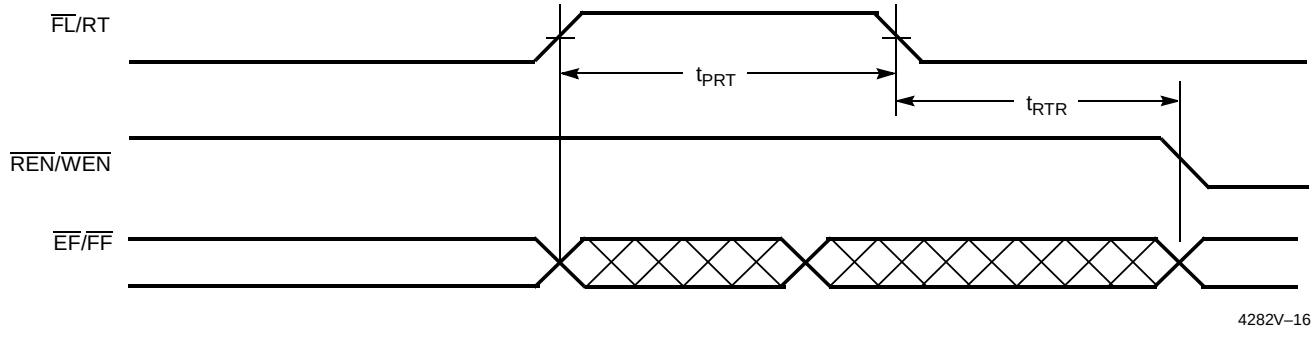
Write Programmable Registers



Read Programmable Registers



Retransmit Timing [23, 24, 25]



Notes:

23. Clocks are free-running in this case.
24. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
25. For the synchronous PAE and PAF flags an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Architecture

The CY7C4282V/92V consists of an array of 64K to 128K words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

During reset of the FIFO, the state of the $\overline{XI}/\overline{LD}$ pin determines if depth expansion operation is used. For depth expansion operation, $\overline{XI}/\overline{LD}$ is tied to $\overline{XO}$ of the next device. See "Depth Expansion Configuration" and *Figure 3*. For standalone or width expansion configuration, the $\overline{XI}/\overline{LD}$ pin must be asserted LOW during reset.

There is a 0-ns hold time requirement for the $\overline{XI}/\overline{LD}$ configuration at the $\overline{RS}$ deassertion edge. This allows the user to tie $\overline{XI}/\overline{LD}$ to $\overline{RS}$ directly for applications that do not require access to the flag offset registers.

FIFO Operation

When the $\overline{WEN}$ is asserted LOW and $\overline{FF}$ is HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ is asserted LOW and $\overline{EF}$ is HIGH, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur t_{ENS} before WCLK for it to be a valid write function.

An Output Enable ($\overline{OE}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Programming

When $\overline{LD}$ is held LOW during Reset, this pin is the Load Enable ($\overline{LD}$) for flag offset programming. In this configuration, $\overline{LD}$ can be used to access the four 9-bit offset registers contained in the CY7C4282V/92V for writing or reading data to these registers.

When the device is configured for programmable flags and both $\overline{LD}$ and $\overline{WEN}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when $\overline{LD}$ and $\overline{WEN}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while $\overline{LD}$ and $\overline{WEN}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

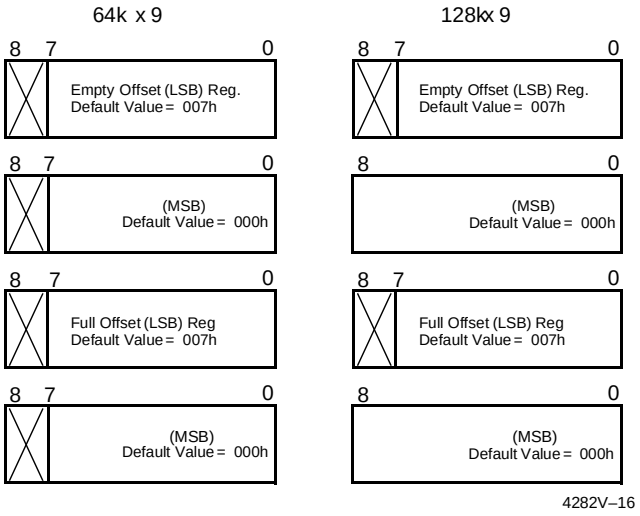


Figure 1. Offset Register Location and Default Values

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the $\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time $\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when $\overline{LD}$ is LOW and $\overline{REN}$ is LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable Almost Empty flag ($\overline{PAE}$) and programmable Almost Full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

LD	WEN	WCLK[26]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

Note:
26. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and a read is performed on the LOW-to-HIGH transition of RCLK.

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAF}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4282V (64K – m) and CY7C4292V (128K – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Flag Operation

The CY7C4282V/92V devices provide four flag pins to indicate the condition of the FIFO contents. All flags operate synchronously.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C4282V/92V features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 2* for a description of programmable flags.

Table 2. Status Flags

Number of Words in FIFO					
CY7C4282V	CY7C4292V	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	L	L
1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to (65536 – (m+1))	(n+1) to (131072 – (m+1))	H	H	H	H
(65536 – m)[28] to 65535	(131072 – m)[28] to 131071	H	L	H	H
65536	131072	L	L	H	H

Notes:
27. n = Empty Offset (n=7 default value).
28. m = Full Offset (m=7 default value).

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also. The full depth of the FIFO can be repeatedly retransmitted.

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C4282V/92V. Any word width can be attained by adding additional CY7C4282V/92V.

When the CY7C4282V/92V is in a Width Expansion Configuration, the Read Enable ($\overline{REN}$) control input can be grounded (see *Figure 2*). In this configuration, the Load ($\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

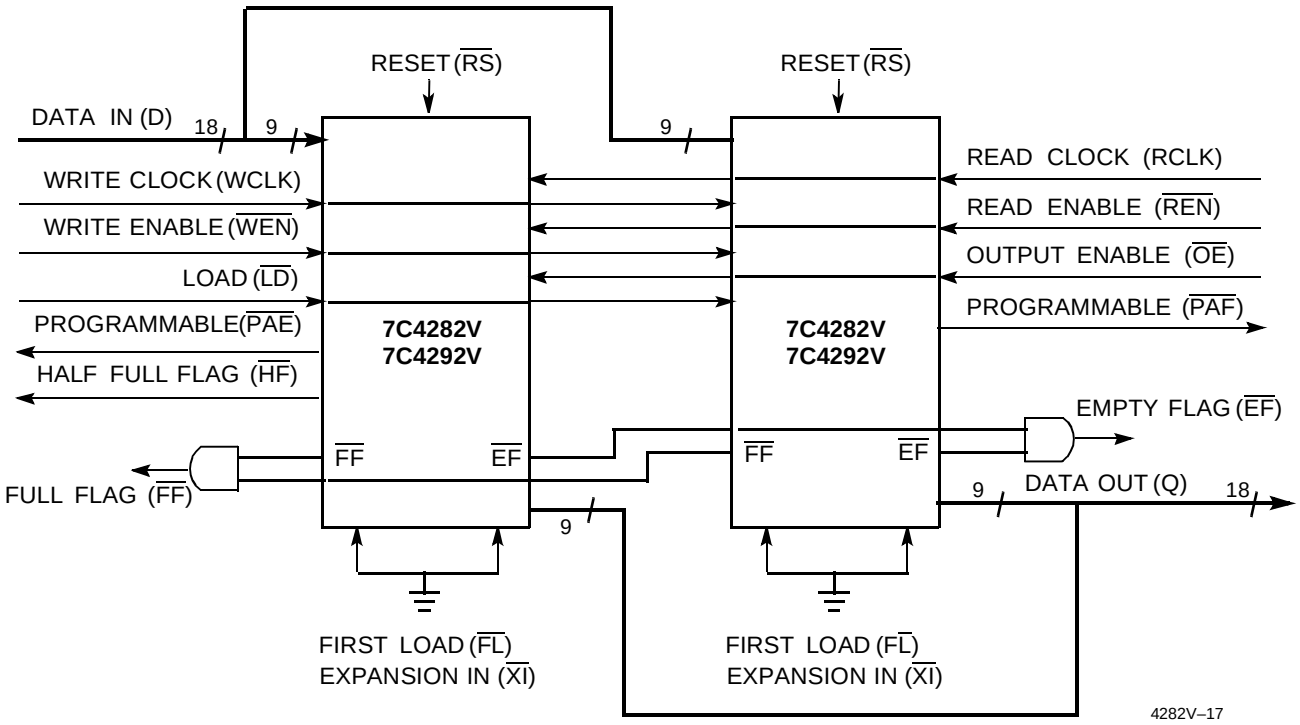


Figure 2. Block Diagram of 64Kx9/128Kx9 Low-Voltage Deep Sync FIFO Memory Used in a Width Expansion Configuration

Depth Expansion Configuration

The CY7C4282V/92V can easily be adapted to applications requiring more than 64K/128K words of buffering. *Figure 3* shows Depth Expansion using three CY7C4282V/92Vs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. $\overline{EF}$ and $\overline{FF}$ composite flags are created by ORing together each individual respective flag.

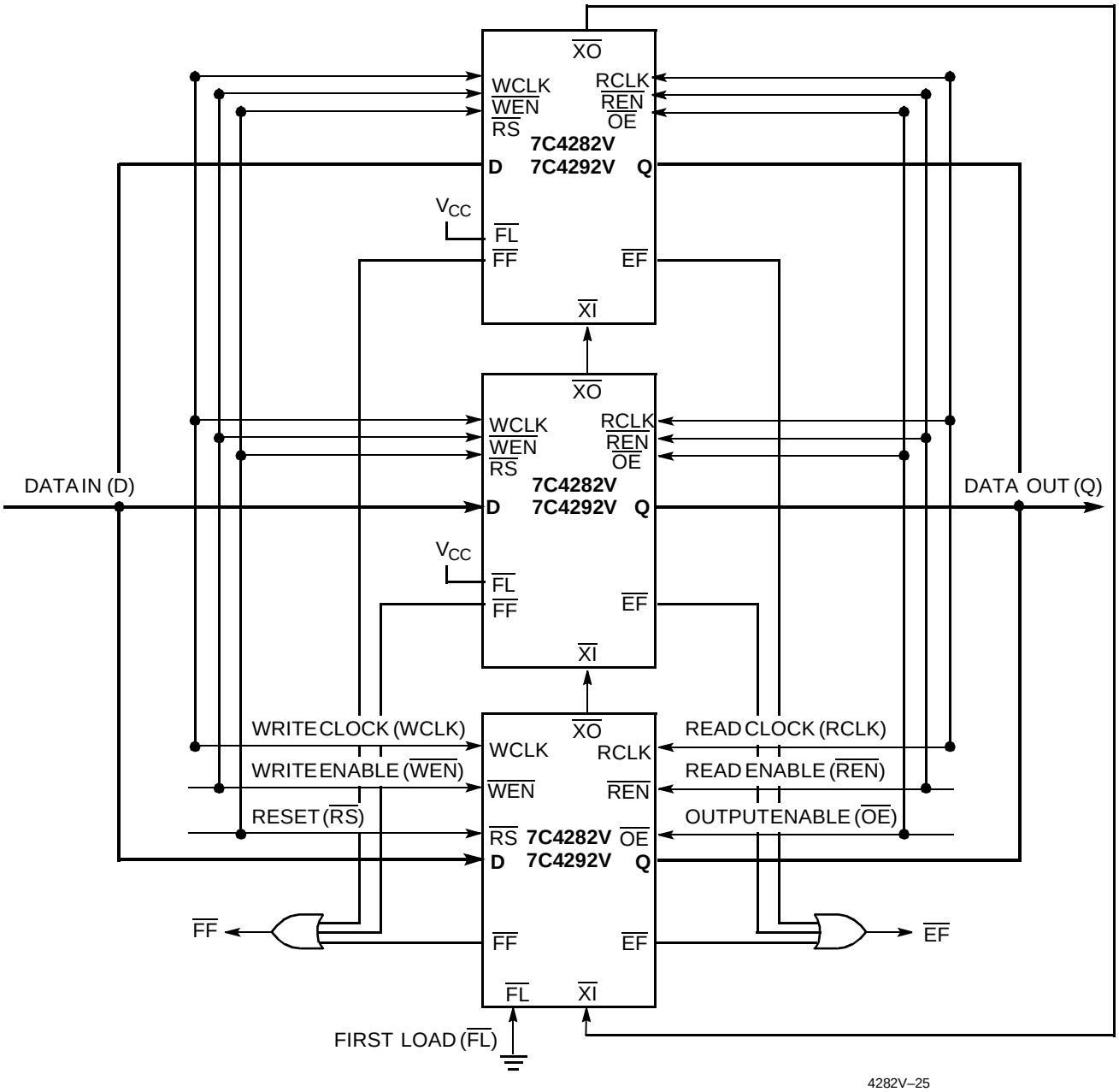


Figure 3. Block Diagram of 64Kx9/128Kx9 Low-Voltage Deep Sync FIFO Memory with Programmable Flags used in Depth Expansion Configuration

Ordering Information

64K x 9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4282V-10ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
15	CY7C4282V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4282V-15ASI	A64	64-Lead 10x10 Thin Quad Flatpack	Industrial
25	CY7C4282V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial

128K x 9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4292V-10ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
15	CY7C4292V-15ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial
	CY7C4292V-15ASI	A64	64-Lead 10x10 Thin Quad Flatpack	Industrial
25	CY7C4292V-25ASC	A64	64-Lead 10x10 Thin Quad Flatpack	Commercial

Document #: 38-00657-B

Package Diagram

64-Pin Thin Plastic Quad Flat Pack (10 x 10 x 1.4 mm) A64