

## 64K x 16 Static RAM

### Features

- 3.3V operation (3.0V–3.6V)
- High speed
  - $t_{AA} = 10/12/15$  ns
- CMOS for optimum speed/power
- Low Active Power (L version)
  - 576 mW (max.)
- Low CMOS Standby Power (L version)
  - 1.80 mW (max.)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 400-mil SOJ
- Available in a 48-Ball Mini BGA package

### Functional Description<sup>[1]</sup>

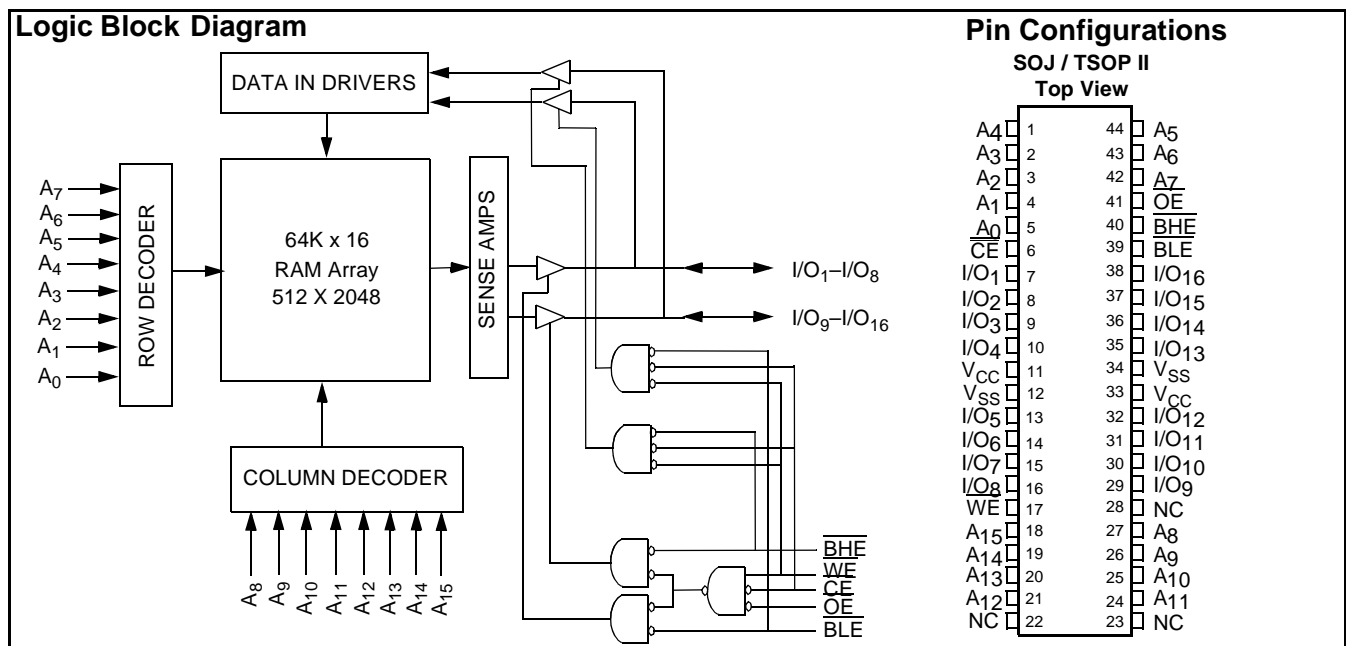
The CY7C1021BV is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1021BV is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and 48-ball mini BGA packages.



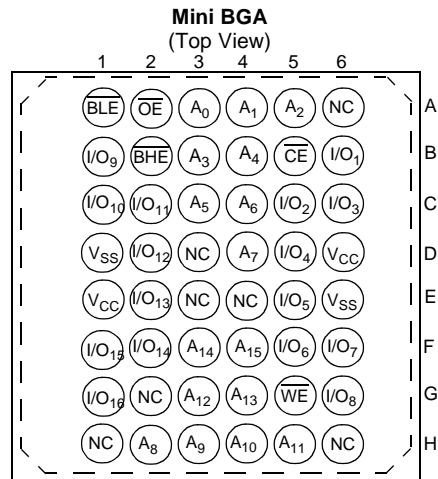
### Selection Guide

		7C1021BV-8	7C1021BV-10	7C1021BV-12	7C1021BV-15
Maximum Access Time (ns)		8	10	12	15
Maximum Operating Current (mA)	Commercial	170	160	150	140
	Industrial	190	180	170	160
Maximum CMOS Standby Current (mA)	Commercial	5	5	5	5
	L	0.500	0.500	0.500	0.500

Shaded areas contain advance information.

**Note:**

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Pin Configurations**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

DC Input Voltage<sup>[2]</sup>..... -0.5V to V<sub>CC</sub>+0.5V

**Note:**

2. Minimum voltage is -2.0V for pulse durations of less than 20 ns.

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1021BV-8		7C1021BV-10		7C1021BV-12		7C1021BV-15		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> +0.3V	2.2	V <sub>CC</sub> +0.3V	2.2	V <sub>CC</sub> +0.3V	2.2	V <sub>CC</sub> +0.3V	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	-1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	-1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com		170		160		150		140	mA
			Ind		190		120		170		160	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40		40		40	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	L	5		5		5		5	mA	
				500		500		500		500	μA	

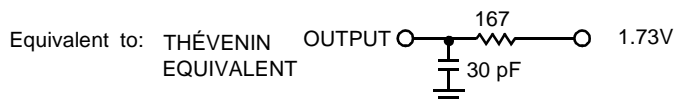
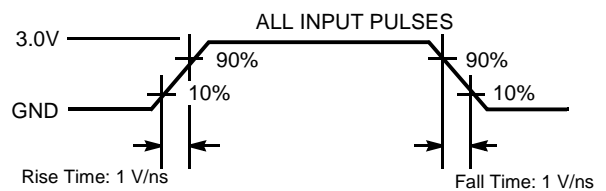
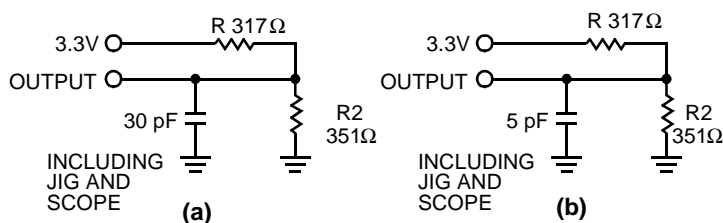
Shaded areas contain advance information.

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	7C1021BV-8		7C1021BV-10		7C1021BV-12		7C1021BV-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
t <sub>RC</sub>	Read Cycle Time	8		10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		8		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		4		4		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		4		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		4		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		12		12		15	ns
t <sub>DBE</sub>	Byte Enable to Data Valid	4		5		6		7		ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		4		5		6		7	ns
<b>WRITE CYCLE<sup>[7]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	8		10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	6		7		8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	6		8		8		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	4		6		6		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		4		5		6		7	ns
t <sub>BW</sub>	Byte Enable to End of Write	8		8		8		9		ns

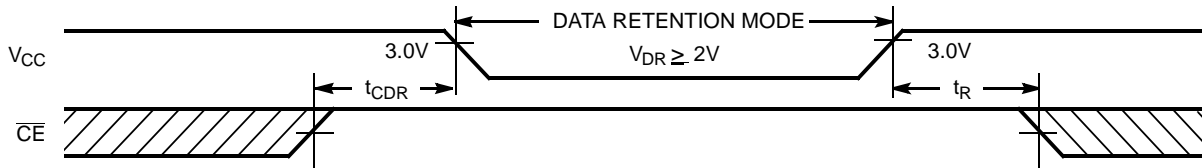
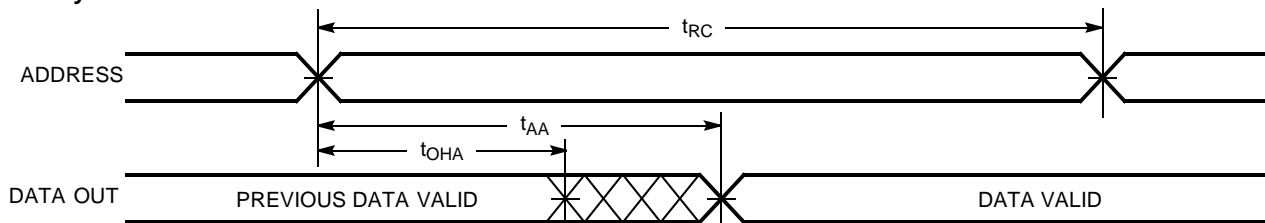
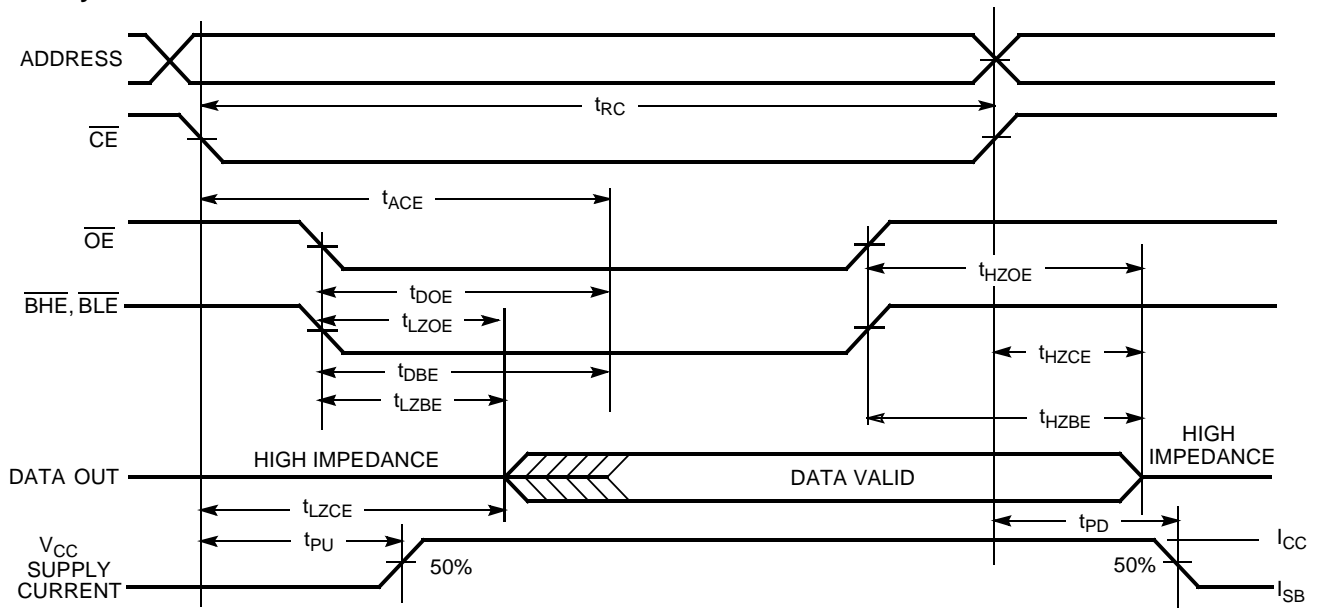
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**Data Retention Characteristics Over the Operating Range (L version only)**

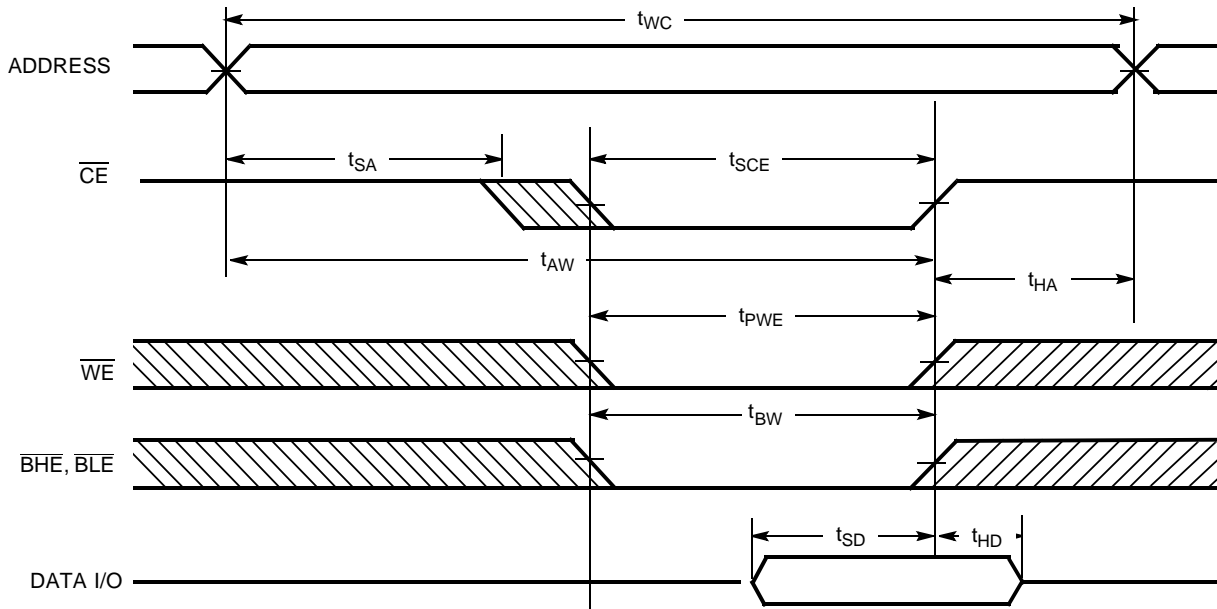
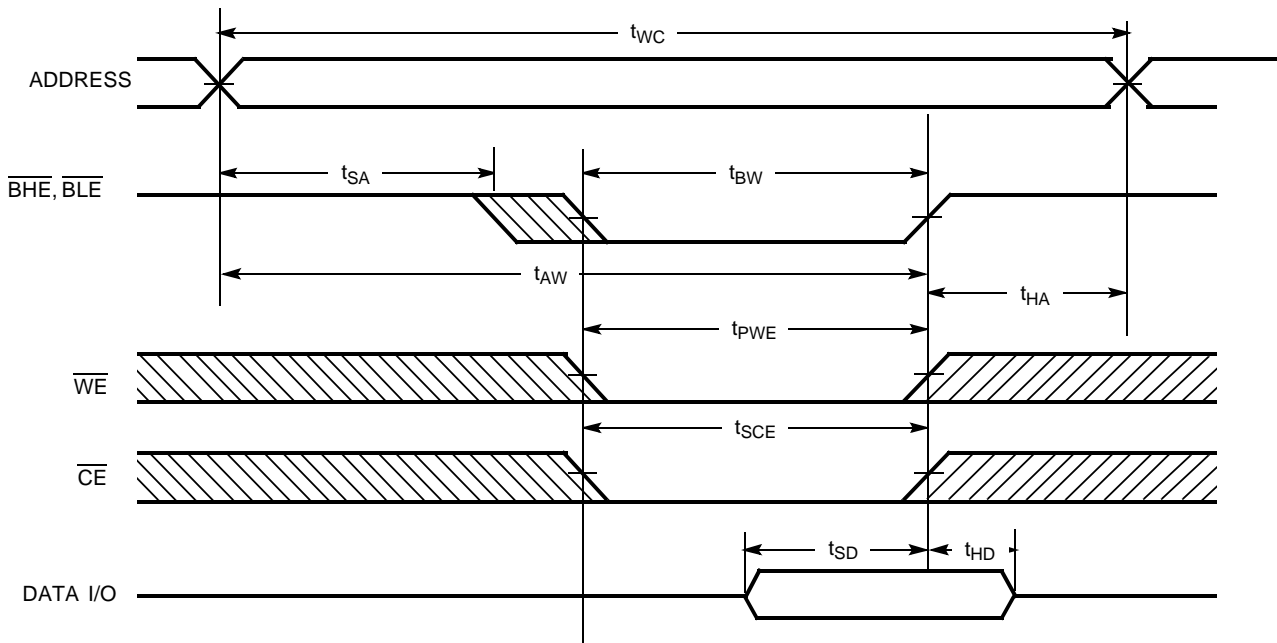
Parameter	Description		Conditions <sup>[8]</sup>	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			2.0		V
I <sub>CCDR</sub>	Data Retention Current	Com'l	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		100	μA
t <sub>CDR</sub> <sup>[9]</sup>	Chip Deselect to Data Retention Time			0		ns
t <sub>R</sub> <sup>[10]</sup>	Operation Recovery Time			t <sub>RC</sub>		ns

**Notes:**

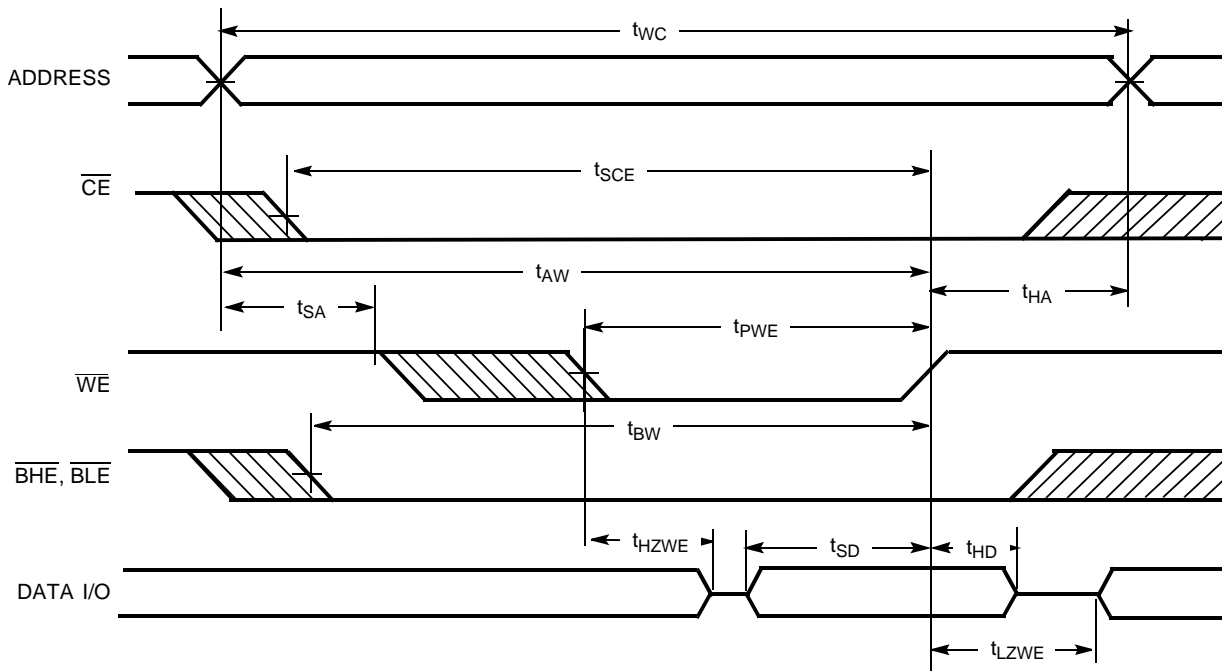
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW, WE LOW and BHE / BLE LOW. CE, WE and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- No input may exceed V<sub>CC</sub> + 0.5V.
- Tested initially and after any design or process changes that may affect these parameters.
- t<sub>r</sub> ≤ 3 ns for the -12 and -15 speeds. t<sub>r</sub> ≤ 5 ns for the -20 and slower speeds.

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1** <sup>[11, 12]</sup>

**Read Cycle No. 2 (OE Controlled)** <sup>[12, 13]</sup>

**Notes:**

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** <sup>[14, 15]</sup>

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

14. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled, LOW)**

**Truth Table**

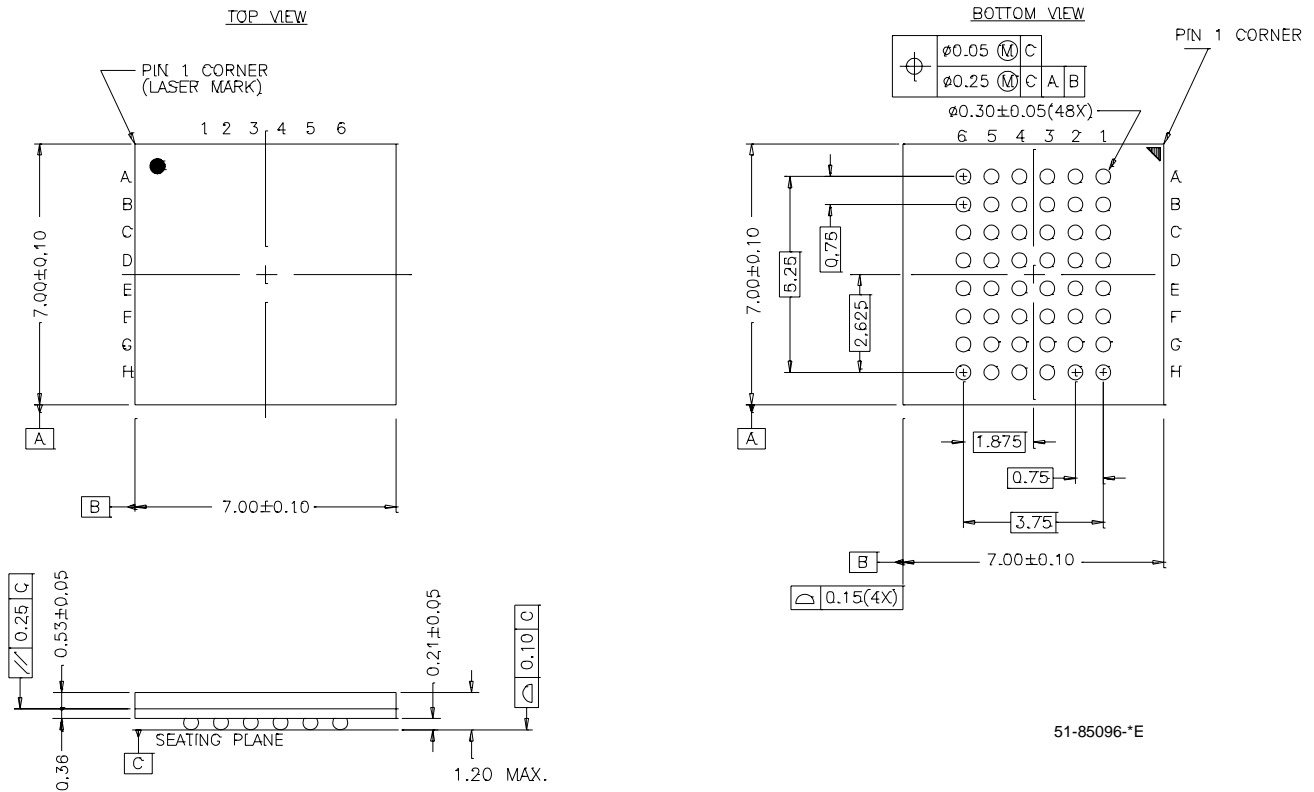
CE	OE	WE	BLE	BHE	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

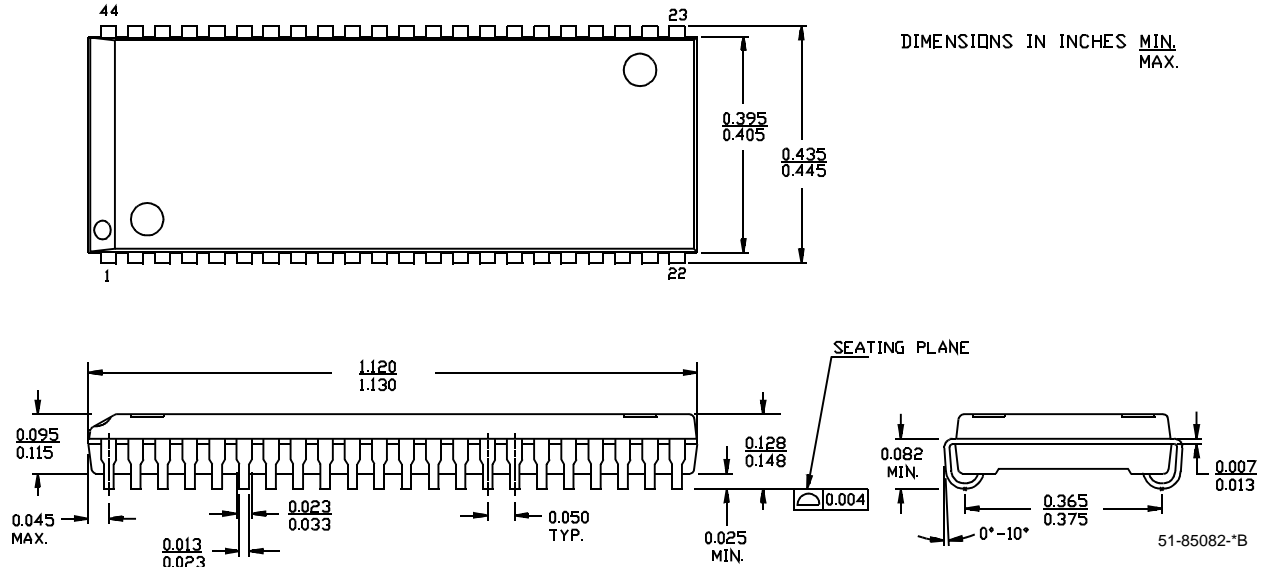
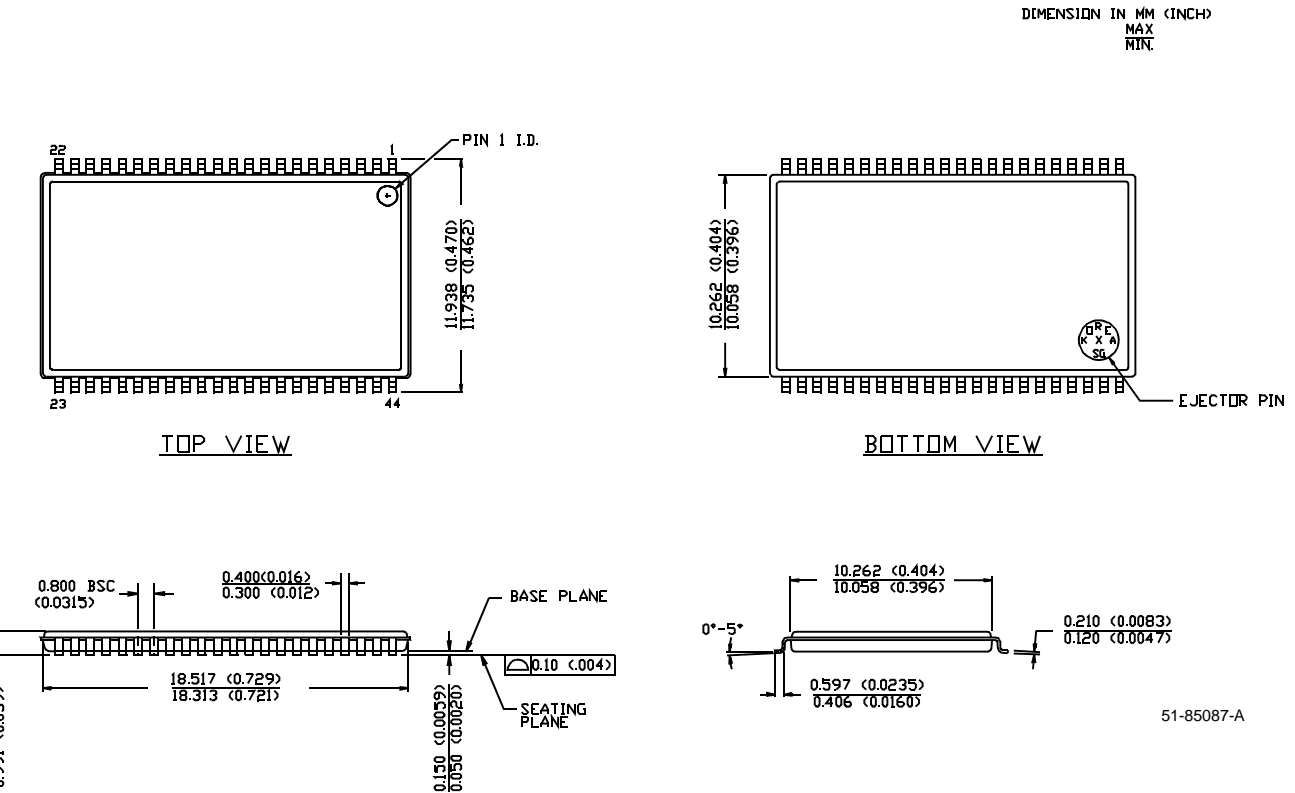
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1021BV33-8BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-8VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-8VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-8ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-8ZC	Z44	44-Lead TSOP Type II	
10	CY7C1021BV33-10BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-10ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-10ZC	Z44	44-Lead TSOP Type II	
12	CY7C1021BV33-12BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33-12BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021BV33-12VI	V34	44-Lead (400-Mil) Molded SOJ	
15	CY7C1021BV33-15BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021BV33L-15BAC	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021BV33-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33-15ZC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33L-15VC	Z44	44-Lead TSOP Type II	
	CY7C1021BV33-15BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021BV33L-15BAI	BA48A	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021BV33-15VI	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021BV33L-15ZI	Z44	44-Lead TSOP Type II	

Shaded areas contain advance information.



**Package Diagrams**
**48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A**


51-85096\*E

**Package Diagrams (continued)**
**44-Lead (400-Mil) Molded SOJ V34**

**44-Pin TSOP II Z44**


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**Document History Page**

<b>Document Title: CY7C1021BV33 64K x 16 Static RAM</b> <b>Document Number: 38-05148</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109892	09/22/01	SZV	Change from Spec number: 38-00954 to 38-05148
*A	116474	09/16/02	CEA	Add applications foot note to data sheet, page 1.