

## 256K x 4 Static RAM

### Features

- **High speed**  
—  $t_{AA} = 12 \text{ ns}$
- **CMOS for optimum speed/power**
- **Low active power**  
— 910 mW
- **Low standby power**  
— 275 mW
- **2.0V data retention (optional)**  
— 100  $\mu\text{W}$
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

### Functional Description

The CY7C106 and CY7C1006 are high-performance CMOS static RAMs organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{\text{CE}}$ ),

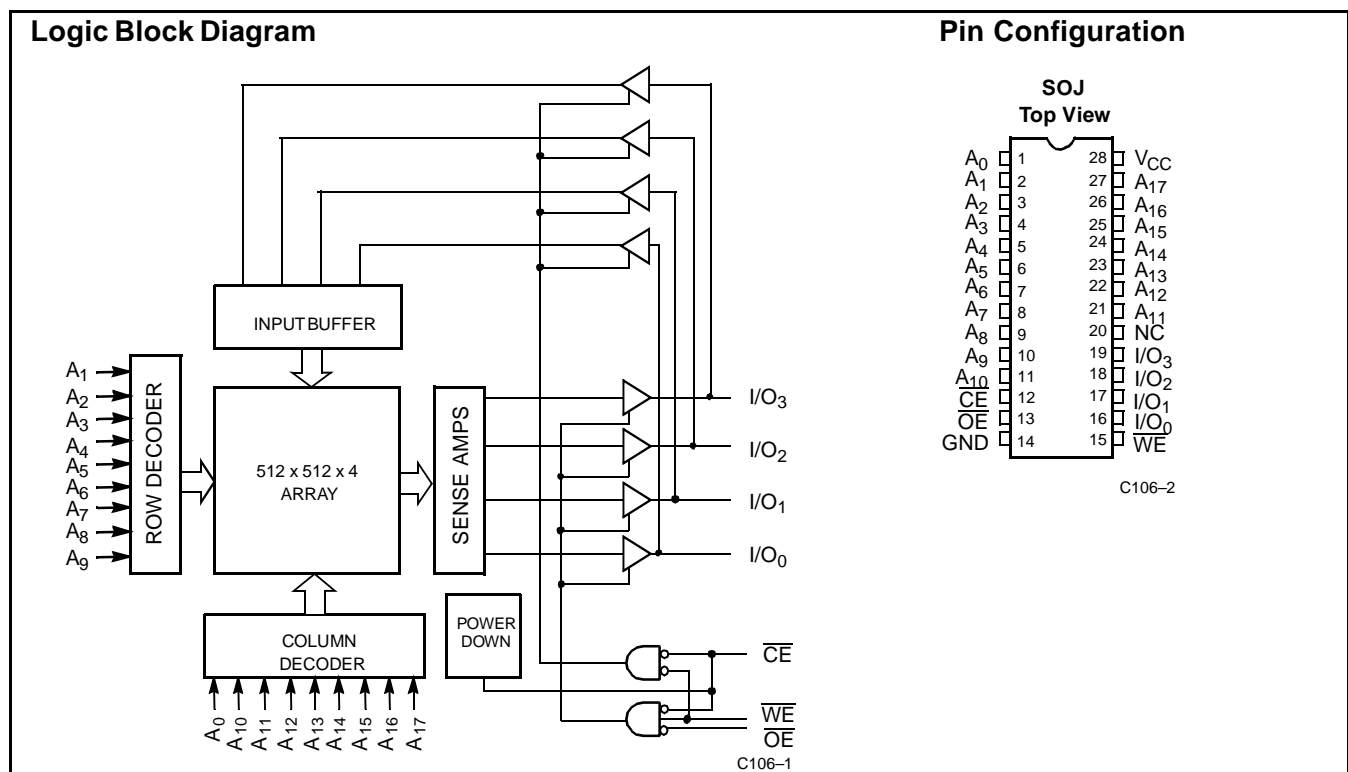
and three-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when the devices are deselected.

Writing to the devices is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and write enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the four I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the devices is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and output enable ( $\overline{\text{OE}}$ ) LOW while forcing write enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) are placed in a high-impedance state when the devices are deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  LOW).

The CY7C106 is available in a standard 400-mil-wide SOJ; the CY7C1006 is available in a standard 300-mil-wide SOJ.



### Selection Guide

	7C106-12 7C1006-12	7C106-15 7C1006-15	7C106-20 7C1006-20	7C106-25 7C1006-25	7C106-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	165	155	145	130	125
Maximum Standby Current (mA)	50	30	30	30	25

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> Relative to GND<sup>[1]</sup> ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C106-12 7C1006-12		7C106-15 7C1006-15		7C106-20 7C1006-20		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300	mA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		165		155		140	mA	
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		50		30		30	mA	
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f=0	Com'l		10		10		10	mA
			L		2		2		2	

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C106-25 7C1006-25		7C106-35		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		130		125	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		25	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f=0	Com'I	10		10	mA
			L	2		2	

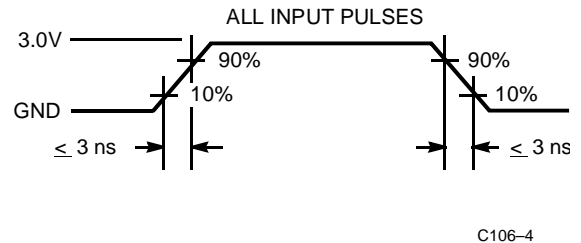
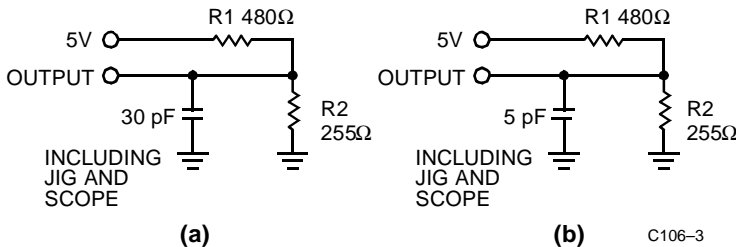
**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	7	pF
C <sub>IN</sub> : Controls			10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

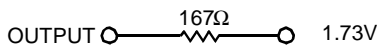
**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

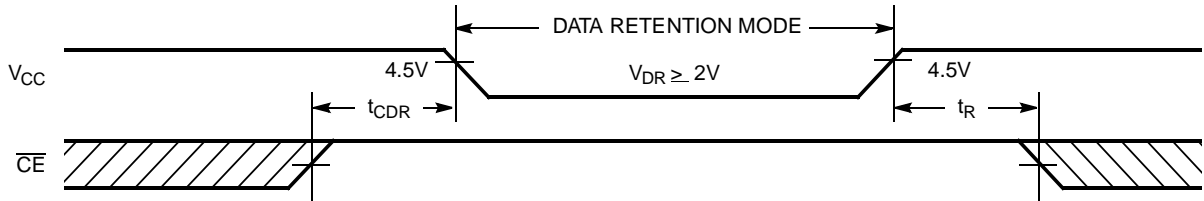
Parameter	Description	7C106-12 7C1006-12		7C106-15 7C1006-15		7C106-20 7C1006-20		7C106-25 7C1006-25		7C106-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6,7]</sup>		6		7		8		10		10	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6,7]</sup>		6		7		8		10		10	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
<b>WRITE CYCLE<sup>[8,9]</sup></b>												
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		35		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t <sub>AW</sub>	Address Set-Up to Write End	10		12		15		20		25		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t <sub>SD</sub>	Data Set-Up to Write End	7		8		10		15		20		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	2		3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6,7]</sup>		6		7		8		10		10	ns

**Notes:**

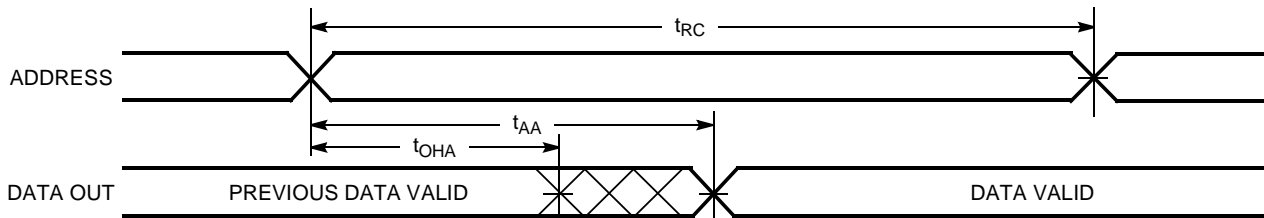
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Data Retention Characteristics** Over the Operating Range (L Version Only)

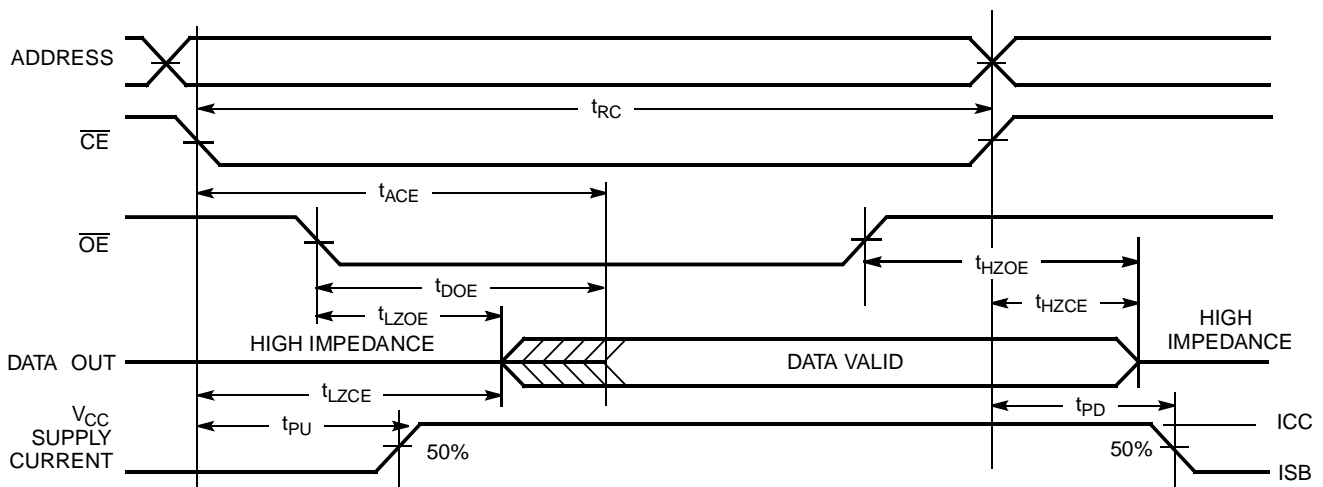
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ ,		50	$\mu A$
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[4]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**


C106-5

**Switching Waveforms**
**Read Cycle No.1<sup>[11, 12]</sup>**


C106-6

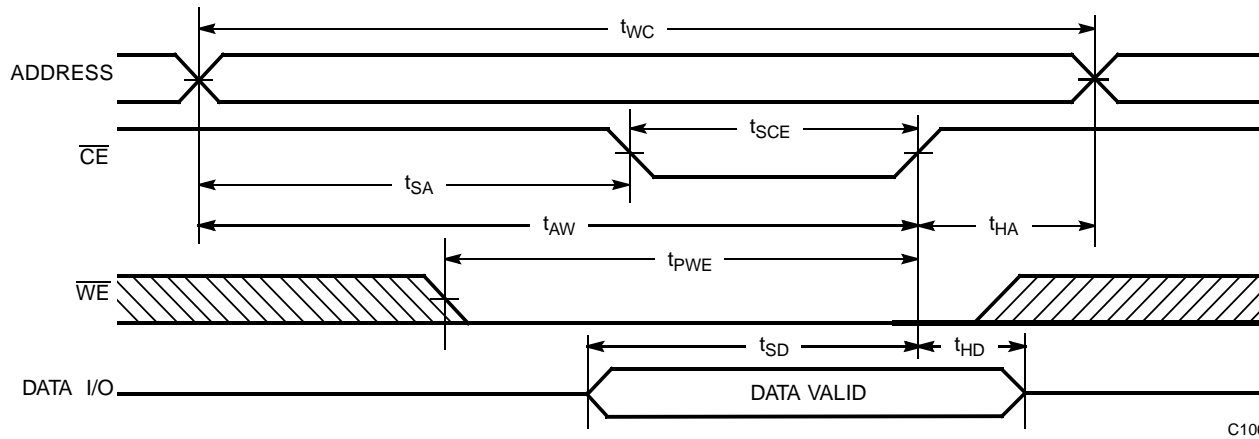
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>**


C106-7

**Notes:**

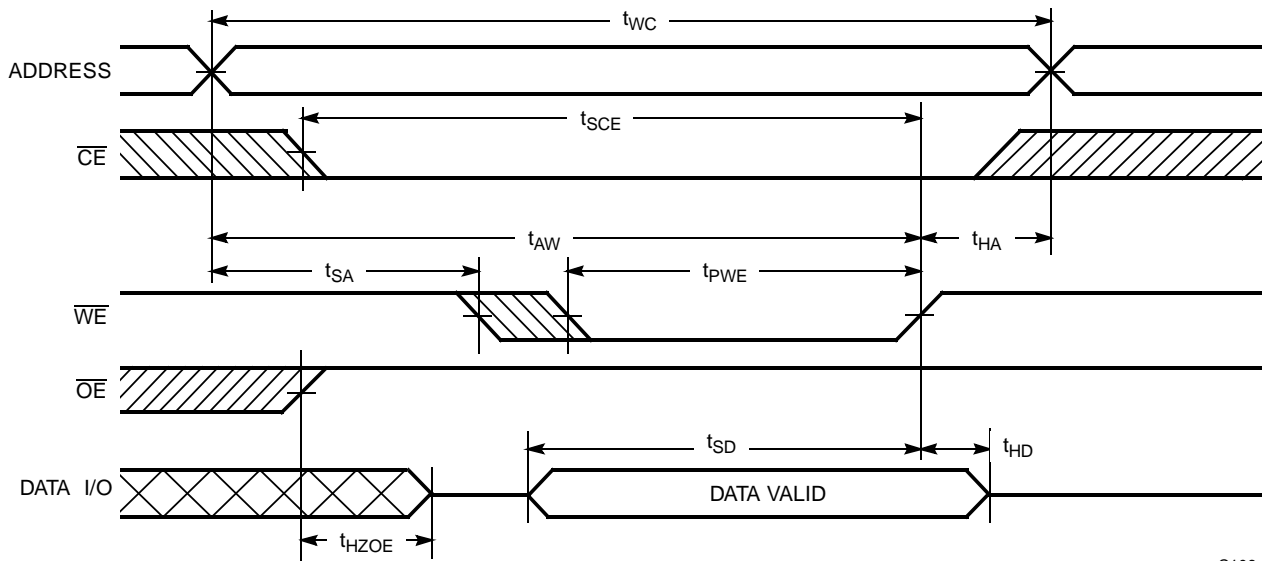
10. No input may exceed  $V_{CC} + 0.5V$ .
11. Device is continuously selected,  $\overline{OE}$  and  $\overline{CE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**  
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[14, 15]</sup>**



C106A-8

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[14, 15]</sup>**



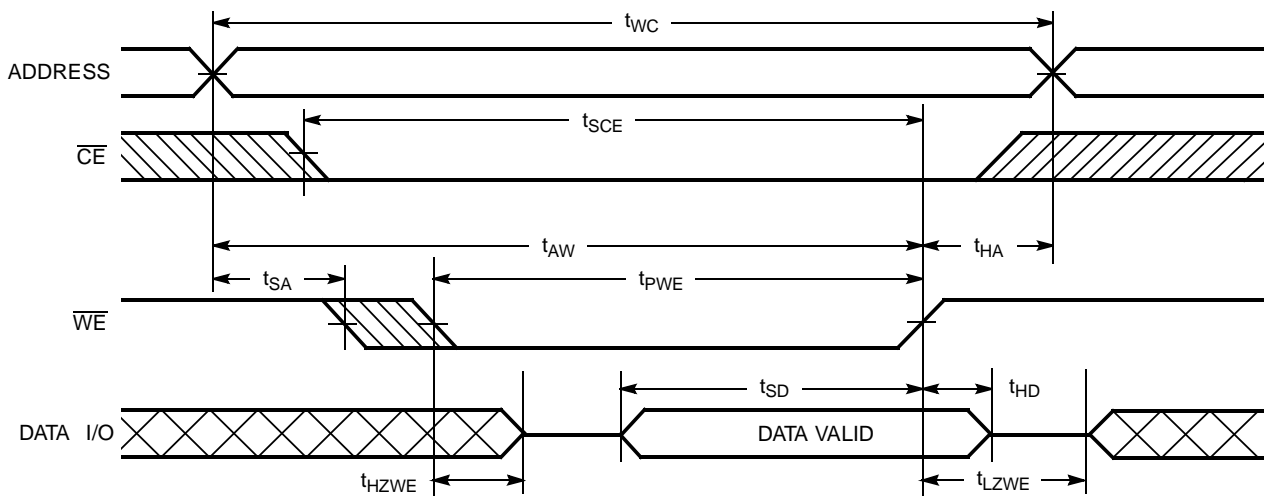
C106-9

**Notes:**

14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

**Switching Waveforms** (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[9, 15]</sup>



C106-10

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C106-12VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006-12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C106-15VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006-15VC	V21	28-Lead (300-Mil) Molded SOJ	
20	CY7C106-20VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006-20VC	V21	28-Lead (300-Mil) Molded SOJ	
25	CY7C106-25VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006-25VC	V21	28-Lead (300-Mil) Molded SOJ	
35	CY7C106-35VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial

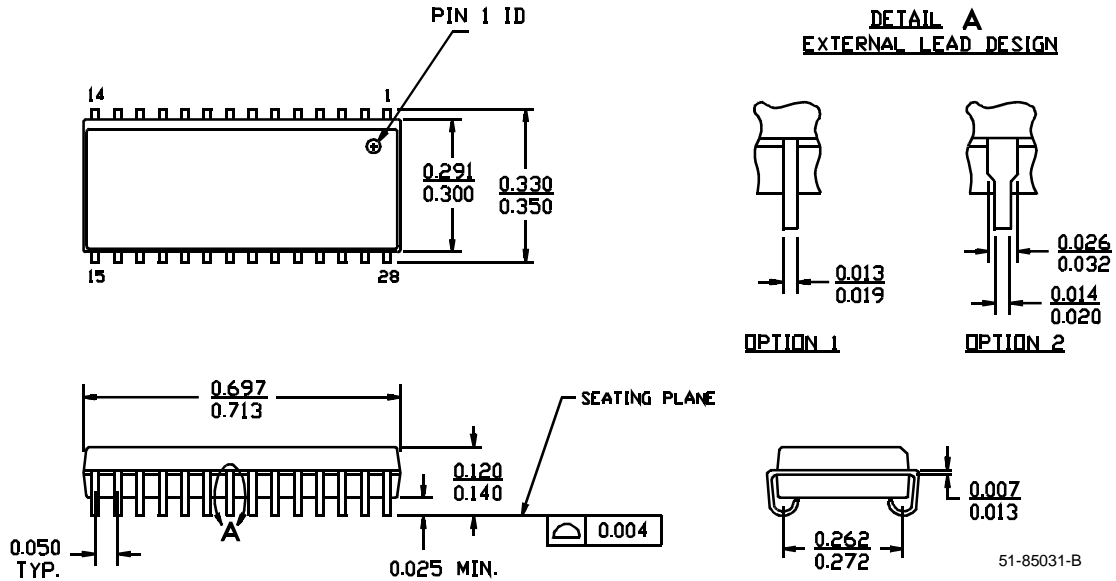
Contact factory for "L" version availability.

Document #: 38-00230-C

Package Diagrams

28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN.  
MAX.



28-Lead (400-Mil) Molded SOJ V28

DIMENSIONS IN INCHES MIN.  
MAX.

