

512K x 8 MoBL Static RAM

Features

- **High Speed**
 - 55 ns and 70 ns availability
- **Low voltage range:**
 - CY62148CV25: 2.2V–2.7V
 - CY62148CV30: 2.7V–3.3V
 - CY62148CV33: 3.0V–3.6V
- **Pin compatible with CY62148V**
- **Ultra low active power**
 - Typical active current: 1.5 mA @ f = 1MHz
 - Typical active current: 5.5 mA @ f = f_{max} (70 ns speed)
- **Low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The CY62148CV25/30/33 are high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can be put into standby mode when deselected ($\overline{\text{CE}}$ HIGH).

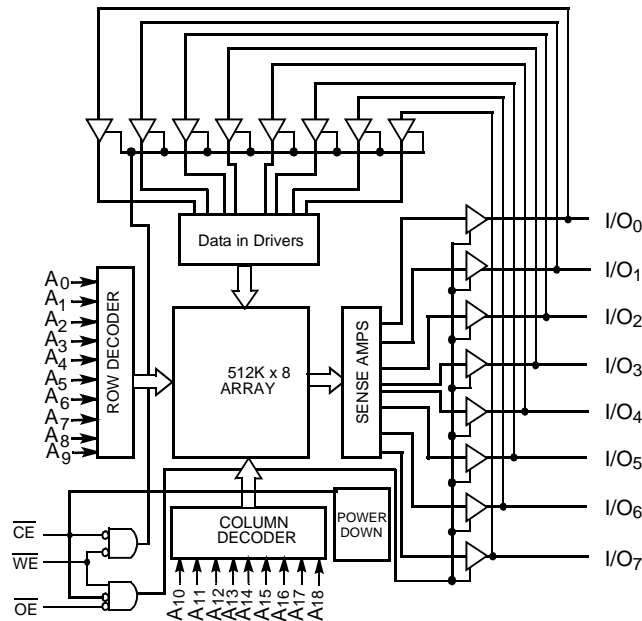
Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

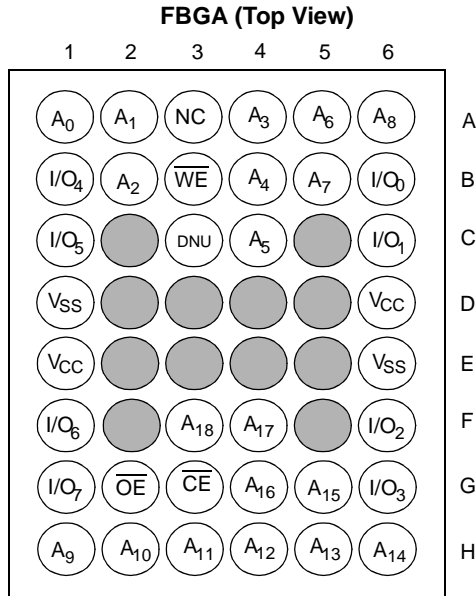
Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

The CY62148CV25/30/33 are available in a 36-ball FBGA package.

Logic Block Diagram



Pin Configurations^[1,2]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature-65°C to +150°C
 Ambient Temperature with Power Applied.....-55°C to +125°C
 Supply Voltage to Ground Potential.....-0.5V to V_{CCmax} + 0.5V

DC Voltage Applied to Outputs

in High Z State^[3]-0.5V to V_{CC} + 0.3V
 DC Input Voltage^[3]-0.5V to V_{CC} + 0.3V
 Output Current into Outputs (LOW).....20 mA
 Static Discharge Voltage.....>2001V
 MIL-STD-883, Method 3015)
 Latch-Up Current >.....>200 mA

Operating Range

Product	Range	Ambient Temperature	V _{CC}
CY62148CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62148CV30			2.7V to 3.3V
CY62148CV33			3.0V to 3.6V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I _{CC})				Standby (I _{SB2})	
	Min.	Typ. ^[4]	Max.		f = 1 MHz		f = f _{max}		Typ. ^[4]	Max.
					Typ. ^[4]	Max.	Typ. ^[4]	Max.		
CY62148CV25	2.2V	2.5V	2.7V	55 ns	1.5 mA	3 mA	7 mA	15 mA	5 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62148CV30	2.7V	3.0V	3.3V	55 ns	1.5 mA	3 mA	7 mA	15 mA	7 μA	15 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		
CY62148CV33	3.0V	3.3V	3.6V	55 ns	1.5 mA	3 mA	7 mA	15 mA	8 μA	20 μA
				70 ns	1.5 mA	3 mA	5.5 mA	12 mA		

Notes:

- NC pins are not connected to the die.
- C3 (DNU) can be left as NC or V_{SS} to ensure proper application.
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62148CV25-55			CY62148CV25-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = Min.	2.0			2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = MinV			0.4			0.4	V
V _{IH}	Input HIGH Voltage			1.8		V _{CC} +0.3V	1.8		V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage			-0.3		0.6	-0.3		0.6	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6V		7	15		5.5	12	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I _{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			5	15		5	15	μA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, V _{CC} = 3.6V								

Parameter	Description	Test Conditions		CY62148CV30-55			CY62148CV30-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = Min.	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = MinV			0.4			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} +0.5V	2.2		V _{CC} +0.5V	V
V _{IL}	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6V		12	25		7	15	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I _{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			7	15		7	15	μA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, V _{CC} = 3.6V								

Parameter	Description	Test Conditions		CY62148CV33-55			CY62148CV33-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = 3.0V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 3.0V			0.4			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} +0.5V	2.2		V _{CC} +0.5V	V
V _{IL}	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6V		7	15		5.5	12	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS Levels		1.5	3		1.5	3	mA
I _{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = f_{max}$ (Address and Data Only), $f = 0$ (OE, WE)			8	20		8	20	μA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, V _{CC} = 3.6V								

Capacitance⁵

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	6	pF
C _{OUT}	Output Capacitance		8	pF

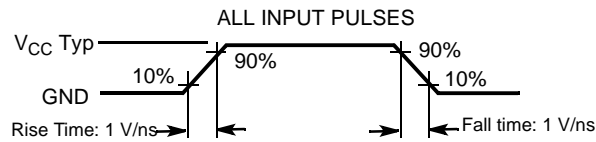
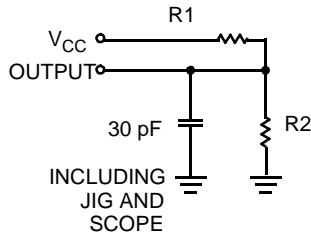
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance ^[5] (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance ^[5] (Junction to Case)		Θ _{JC}	16	°C/W

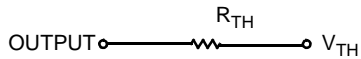
Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

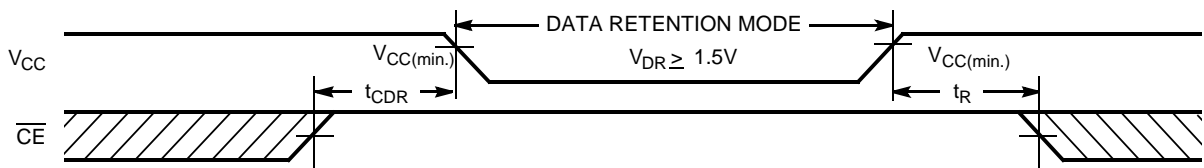


Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.216	K Ohms
R2	15.4	1.550	1.374	K Ohms
R _{TH}	8.0	0.645	0.645	K Ohms
V _{TH}	1.20	1.75	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		V _{CCmax}	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		3	10	μA
t _{CDR} ^[5]	Chip Deselect to Data Retention Time		0			ns
t _R ^[6]	Operation Recovery Time		t _{RC}			ns

Data Retention Waveform



Note:

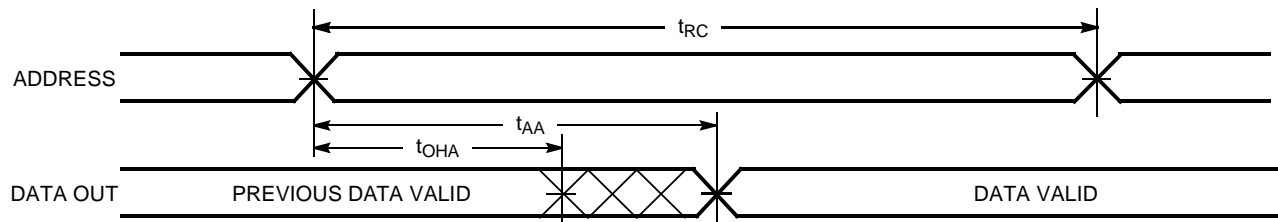
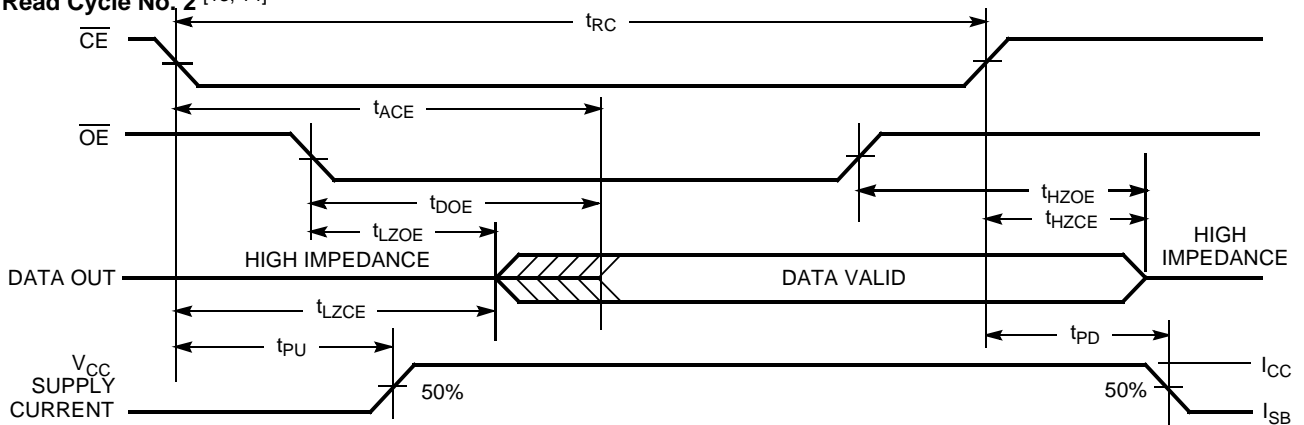
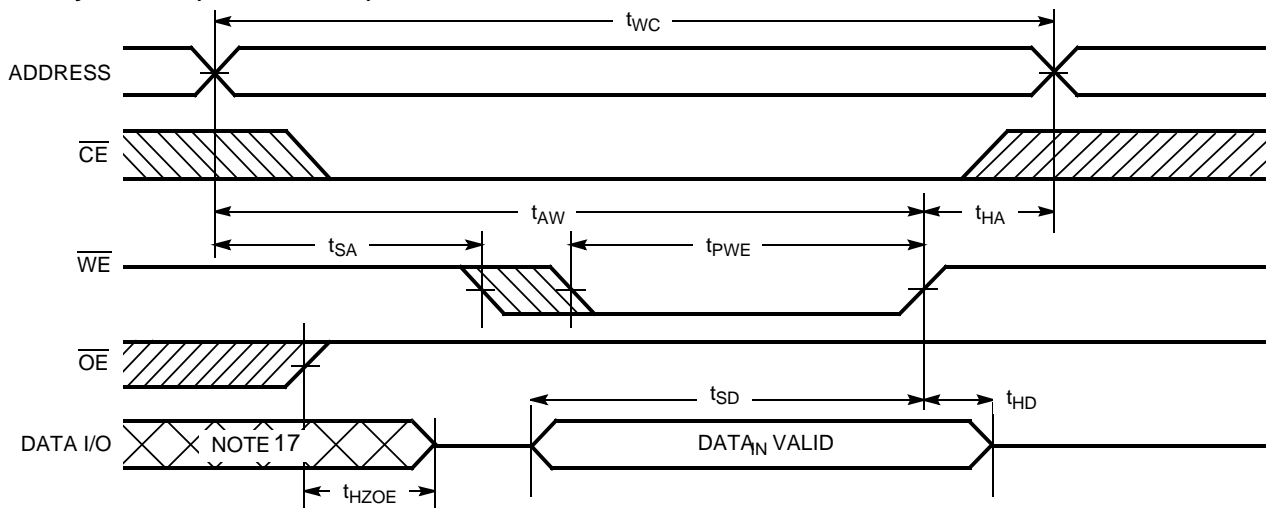
- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 50 μs or stable at V_{CC(min.)} ≥ 50 μs.

Switching Characteristics Over the Operating Range^[7]

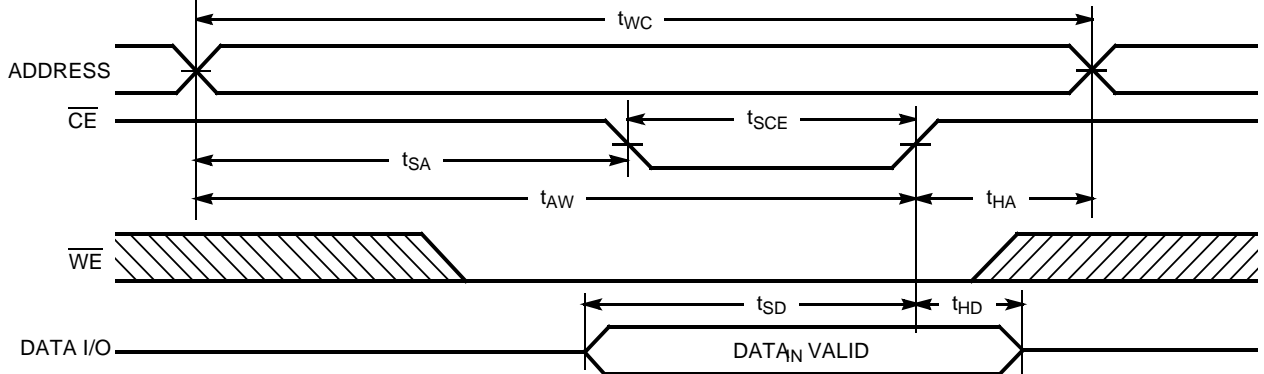
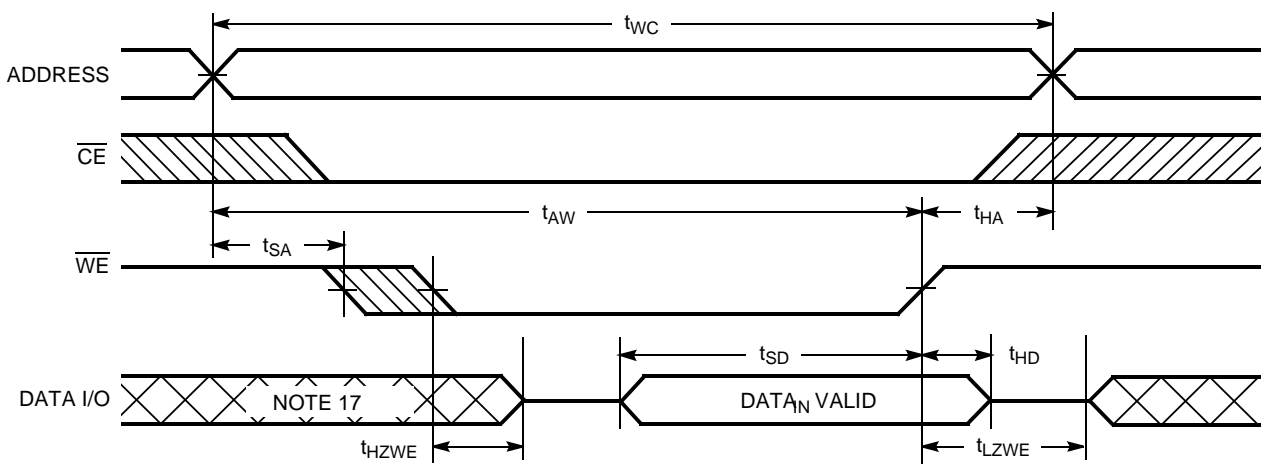
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		55		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[8]	5		5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[9]		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	10		10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[8, 9]		20		25	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		55		70	ns
WRITE CYCLE^[10, 11]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	\overline{CE} LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	30		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[8, 9]		20		25	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	5		10		ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC(typ.)}, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms
Read Cycle No. 1 [12, 13]

Read Cycle No. 2 [13, 14]

Write Cycle No. 1 (WE Controlled) [10, 15, 16]

Notes:

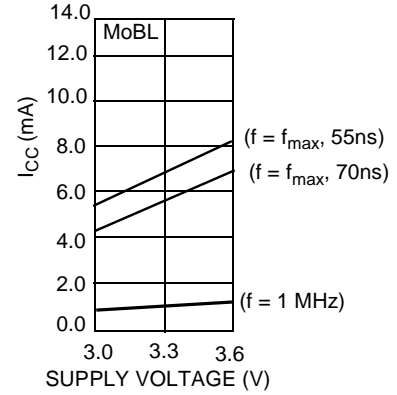
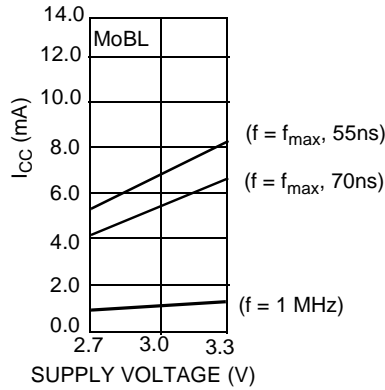
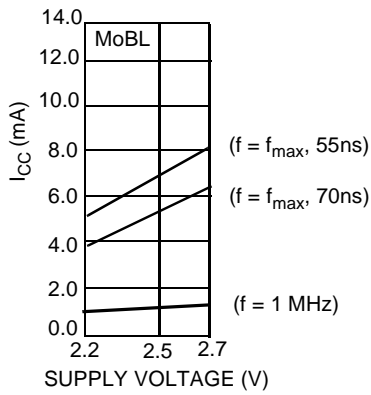
12. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE} transition LOW.
15. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [10, 15, 16]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [11, 16]


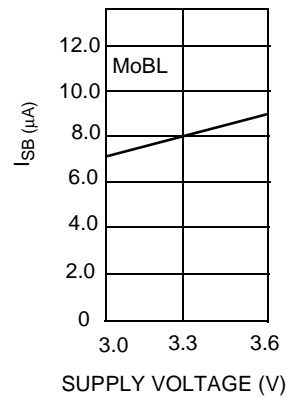
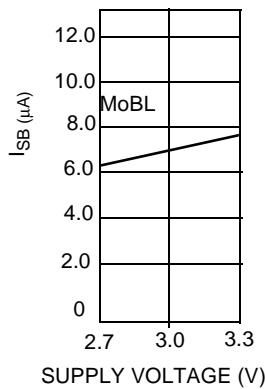
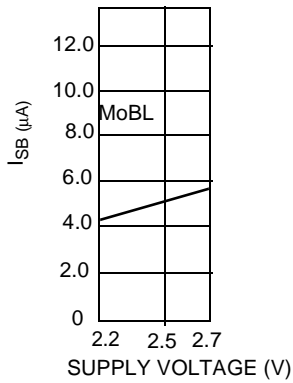
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.)

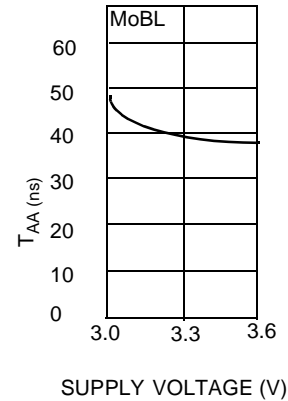
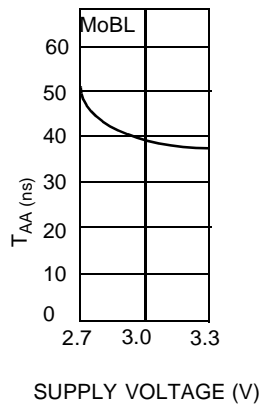
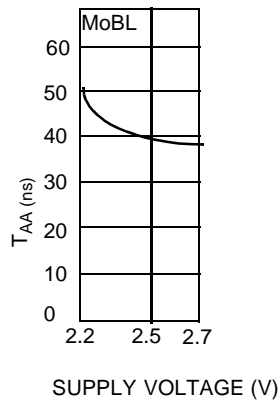
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

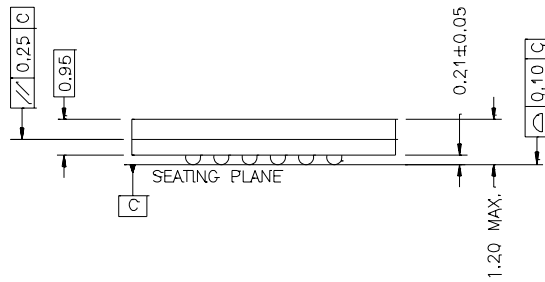
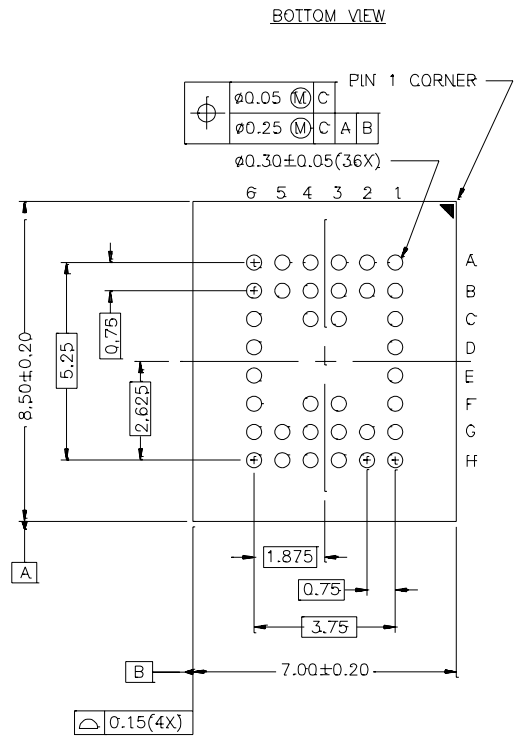
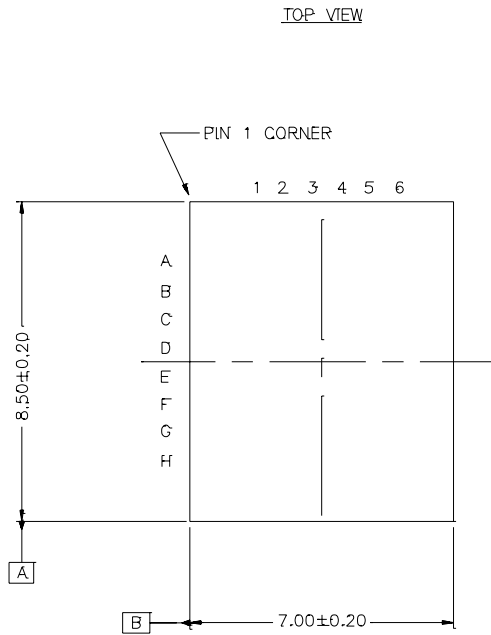
CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (I_{CC})

Ordering Information

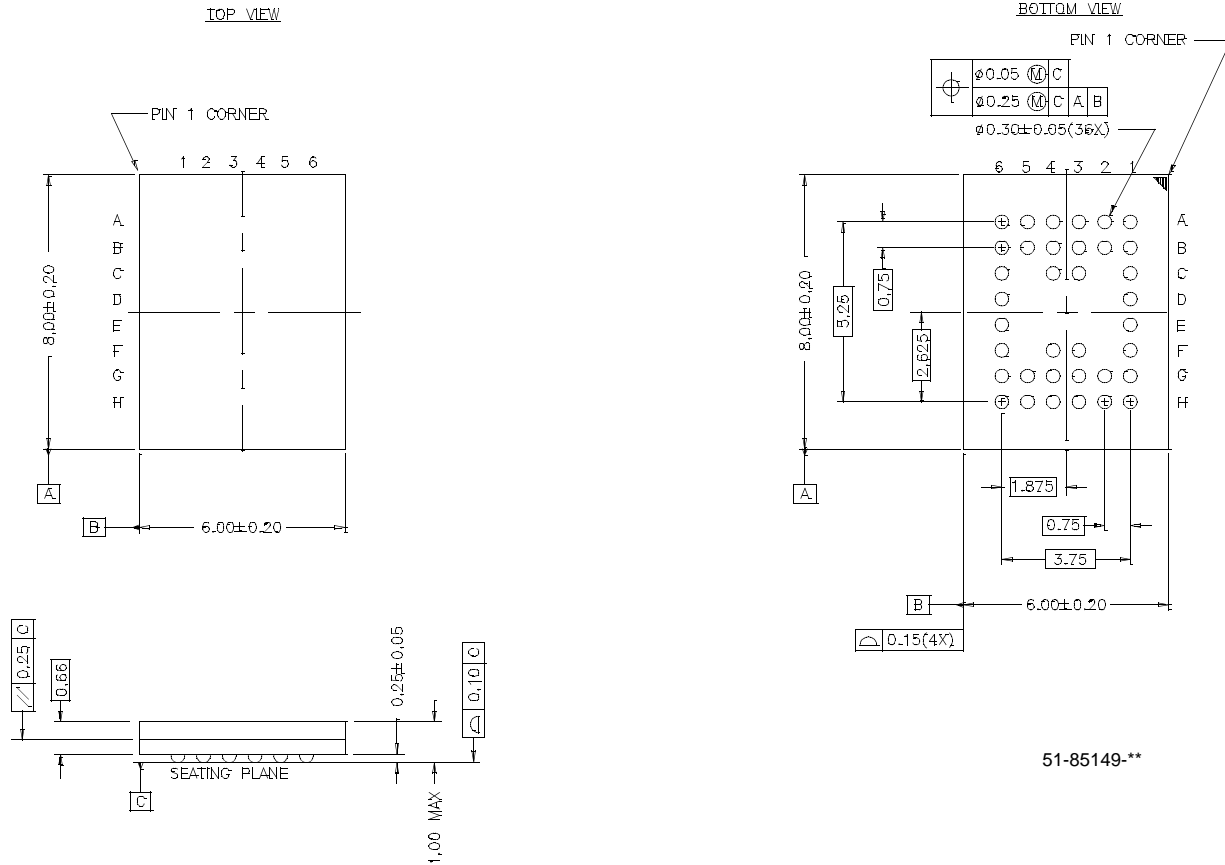
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148CV25LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62148CV25LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV30LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV30LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV33LL-70BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV33LL-70BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62148CV25LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV25LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV30LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV30LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62148CV33LL-55BAI	BA36B	36-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62148CV33LL-55BVI	BV36A	36-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams

36-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA36B



51-85105-°C

Package Diagrams (continued)
36-Lead VFBGA (6 x 8 x 1 mm) BV36A


51-85149-**

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Document Title: CY62148CV25/30/33 MoBL™ 512K x 8 MoBL Static RAM Document Number: 38-05035				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109951	12/02/01	SZV	Change from Spec number: 38-01126 to 38-05035
*A	110643	05/01/02	MGN	Advance to Final, Improved Typical and Max Icc values, added BV package