CDMA 3 V Receiver IF Subsystem with Integrated Voltage Regulator

AD6121

FEATURES

Fully Compliant with IS98A and PCS Specifications
CDMA, W-CDMA, AMPS, and TACS Operation
Linear IF Amplifier
5.9 dB Noise Figure
–47.5 dB to +47 dB Linear-in-dB Gain Control
Quadrature Demodulator
Demodulates IFs from 50 MHz to 350 MHz
Integral Low Dropout Regulator
200 mV Voltage Drop
Accepts 2.9 V to 4.2 V Input from Battery
Low Power
10 mA at Midgain
<1 μA Sleep Mode Operation
Companion Transmitter IF Chip Available (AD6122)

APPLICATIONS

CDMA, W-CDMA, AMPS, and TACS Operation
QPSK Receivers

GENERAL DESCRIPTION

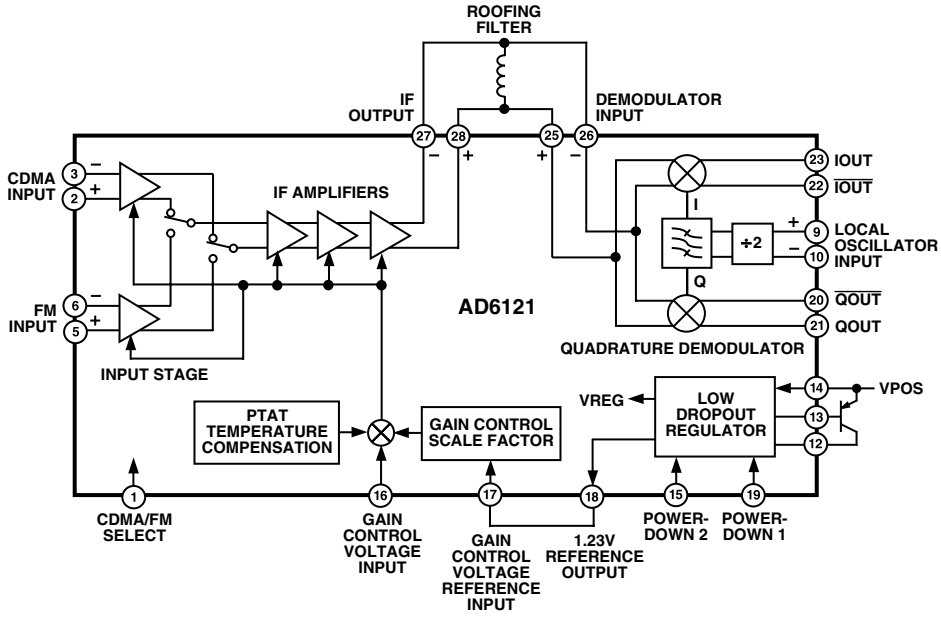
The AD6121 is a low power receiver IF subsystem specifically designed for CDMA applications. It consists of high dynamic range IF amplifiers with voltage controlled gain, a divide-by-two quadrature generator, an I and Q demodulator, and a power-down control input. An integral low dropout regulator allows operation from battery voltages from 2.9 V to 4.2 V.

The gain control input accepts an external gain control voltage input from a DAC. It provides 94.5 dB of gain control with a nominal 52.5 dB/V scale factor when using an internal voltage reference. The gain control interface reference input can be connected to either the internal reference or an external reference.

The I and Q demodulator provides differential quadrature baseband outputs to interface with CDMA baseband converters. A divide-by-two quadrature generator followed by dual polyphase filters ensures maximum ±2.5° quadrature accuracy.

The AD6121 IF Subsystem is fabricated using a 25 GHz f_t BiCMOS silicon process and is packaged in a 28-lead SSOP and a 32-leadless LPCC chip scale package (5 mm × 5 mm).

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD6121–SPECIFICATIONS

(T_A = +25°C, V_{CC} = 3.0 V, LO = 2 × IF, REFIN = 1.23 V, LDO Enabled, unless otherwise noted) Note: All power measurements in dBm are referred to 1 kΩ unless Z_{IN} is noted.

Specification	Conditions	Min	Typ	Max	Units
TOTAL GAIN					
Maximum Gain	IF Amplifiers and Demodulator Powered Up		+47		dB
	IF Amplifiers Powered Up and Demodulator Powered Down		+41.4		dB
Minimum Gain	IF Amplifier and Demodulator Powered Up		–47.5		dB
IF AMPLIFIER					
CDMA and FM Input	IF = 85.38 MHz				
Noise Figure	Maximum Gain		5.9		dB
Input Third-Order Intercept	Maximum Gain		–42.8		dBm
Input 1 dB Compression Point	Maximum Gain		–51.6		dBm
Gain Flatness	IF ±630 kHz, CDMA Mode		±0.25		dB
CDMA Input Capacitance	Differential		2.8		pF
CDMA Input Resistance	Differential		850		Ω
FM Input Capacitance	Differential		2.3		pF
FM Input Resistance	Differential		670		Ω
Output Capacitance	Differential		1.35		pF
Output Resistance	Differential		1.1		kΩ
GAIN CONTROL INTERFACE					
Gain Scaling	Using Internal Reference		52.5		dB/V
Gain Scaling Accuracy	Within a Gain Control Range of 90 dB		±3		dB/V
Gain Control Response Time	Minimum Gain to Maximum Gain		695		ns
Input Resistance at REFIN			10		MΩ
Input Resistance at VGAIN			100		kΩ
DEMODULATOR	LO = 172.76 MHz , –15 dBm Referred to 50 Ω, Baseband Frequency = 1 MHz				
Differential Input Impedance			1		kΩ
Differential Input Capacitance at Demodulator Input			2.9		pF
Input Third Order Intercept			–6.1		dBm
Demodulation Gain			5.6		dB
I/Q Output					
Differential Output Voltage	10 kΩ, 2 pF Differential Parallel Load Impedance		700		mV p-p
Bandwidth	–3 dB		16		MHz
Resistance	Single-Ended		630		Ω
Quadrature Accuracy				±2.5	Degree
Amplitude Balance			±0.1	±0.35	dB
LO Input Impedance	Differential		1.5		kΩ
LO Input Capacitance	Differential		4.16		pF
CONTROL INTERFACES					
Logic Threshold High			1.34		V
Logic Threshold Low			1.30		V
Input Current for Logic High			0.1		µA
Mode Control Response Time	CDMA/FM Pin High Selects CDMA, Low Selects FM		430		ns
Turn-On Response Time	PD1 and PD2 Pins Low Select IC ON, High Selects IC OFF		2.8		µs
Turn-Off Response Time	To 200 µA Supply Current		6.8		µs
LOW DROPOUT REGULATOR	External PNP Pass Transistor, VCE_{SAT} = –0.4 V Max h_{FE} = 100/300 Min/Max				
Input Range		2.9	4.2		V
Nominal Output			2.70		V
Voltage Drop			200		mV
Reference Output			1.23		V
POWER SUPPLY					
Supply Range Using Internal LDO	Supply Input at Pin LDOE		2.9–5.0		V
Supply Range Bypassing Internal LDO	Supply Input at Pins DVCC, IFVCC, LDOC		2.7–3.6		V
Supply Current	VGAIN = 1.5 V		10		mA
Standby Current			0.78		µA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}		–40		+85	°C

Specifications subject to change without notice.

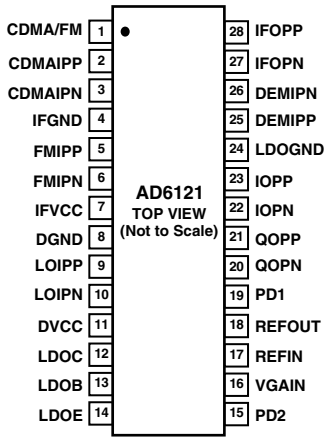
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPS1, VPS2 to COM1, COM2 . . . . . +5 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

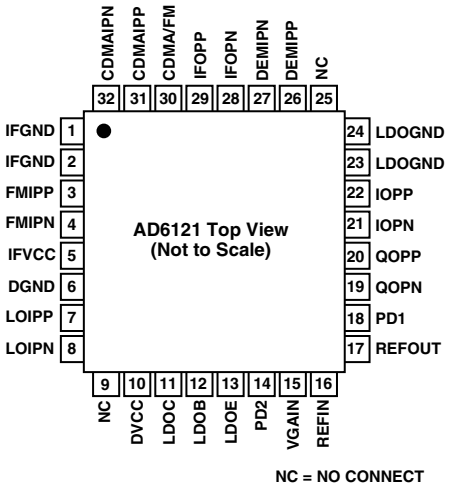
NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics: 28-lead SSOP Package: θ_{JA} = 115.25°C/W.

PIN CONFIGURATION

SSOP Package



LPCC Package



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6121ARS	–40°C to +85°C	Shrink Small Outline Package (SSOP)	RS-28
AD6121ARSRL	–40°C to +85°C	28-Lead SSOP on Tape and Reel	
AD6121ACP	–40°C to +85°C	Chip Scale Package (LPCC)	CP-32
AD6121ACPRL	–40°C to +85°C	32-Leadless LPCC on Tape and Reel	

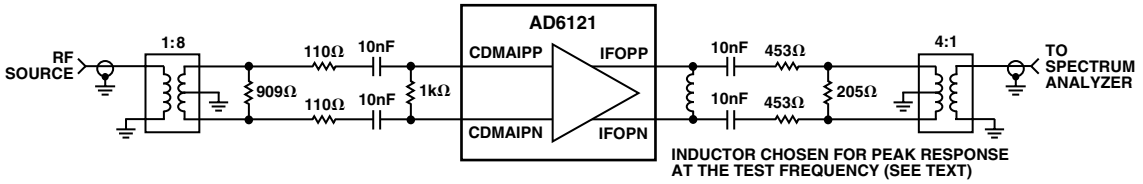
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6121 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

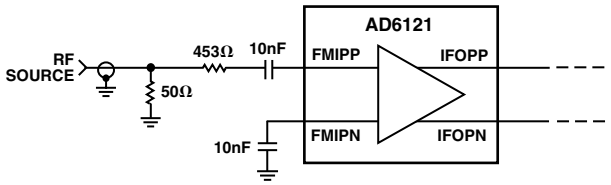
PIN FUNCTION DESCRIPTIONS

SSOP Pin Number	LPCC Pin Number	Pin Label	Description	Function
1	30	CDMA/FM	Selects CDMA or FM Input	CMOS-compatible; HIGH = CDMA, LOW = FM.
2	31	CDMAIPP	CDMA "Positive" Input	AC-coupled, IF input from CDMA SAW filter.
3	32	CDMAIPN	CDMA "Negative" Input	AC-coupled, IF input from CDMA SAW filter.
4	1, 2	IFGND	IF Ground	Ground.
5	3	FMIPP	FM "Positive" Input	AC-coupled, IF input from FM SAW filter.
6	4	FMIPN	FM "Negative" Input	AC-coupled, IF input from FM SAW filter.
7	5	IFVCC	IF VCC	VCC for IF AGC amplifiers.
8	6	DGND	Digital Ground	Ground.
9	7	LOIPP	Local Oscillator "Positive" Input	AC-coupled, Differential Local Oscillator Input.
10	8	LOIPN	Local Oscillator "Negative" Input	AC-coupled, Differential Local Oscillator Input.
	9, 25	NC	No Connect	
11	10	DVCC	Digital VCC	VCC for control logic.
12	11	LDOC	Low Dropout Regulator Pass Transistor Collector Connection	Connects to collector of external PNP pass transistor.
13	12	LDOB	Low Dropout Regulator Pass Transistor Base Connection	Connects to base of external PNP pass transistor.
14	13	LDOE	Low Dropout Regulator Pass Transistor Emitter Connection	Connects to emitter of external PNP pass transistor and DVCC, IFVCC.
15	14	PD2	Demodulator Power-Down Control Input	Demodulator Power-Down Control Input CMOS-compatible; HIGH = Modulator Off, LOW = Modulator On.
16	15	VGAIN	Gain Control Voltage Input	Accepts gain control input voltage from external DAC. Max Gain = 2.5 V. Min Gain = 0.5 V.
17	16	REFIN	Gain Control Reference Input	Accepts 1.23 V reference input from REFOUT (Pin 17) or external reference.
18	17	REFOUT	Reference Output	Provides 1.23 V reference output to REFIN (Pin 18) and CDMA baseband IC reference input so that gain control DAC and AD6121 use same reference.
19	18	PD1	IF Amplifier Power-Down Control Input	IF Amplifier Power-Down Control Input, CMOS compatible; HIGH = Entire IC Powers Down, LOW = IF Amplifier On.
20	19	QOPN	Q Output "Negative"	Connects to Q "Negative" Input of baseband IC.
21	20	QOPP	Q Output "Positive"	Connects to Q "Positive" Input of baseband IC.
22	21	IOPN	I Output "Negative"	Connects to I "Negative" Input of baseband IC.
23	22	IOPP	I Output "Positive"	Connects to I "Positive" Input of baseband IC.
24	23, 24	LDOGND	Ground	Ground.
25	26	DEMIPP	Demodulator "Positive" IF Input	Demodulator input from roofing filter.
26	27	DEMIPN	Demodulator "Negative" IF Input	Demodulator input from roofing filter.
27	28	IFOPN	IF Amplifier "Negative" IF Output	IF output to roofing filter.
28	29	IFOPP	IF Amplifier "Positive" IF Output	IF output to roofing filter.

Test Figures



a. CDMA Input Port Characterization Impedance Match



b. FM Input Port Characterization Impedance Match

Figure 1. Quadrature Modulator Characterization Input and Output Impedance Matches

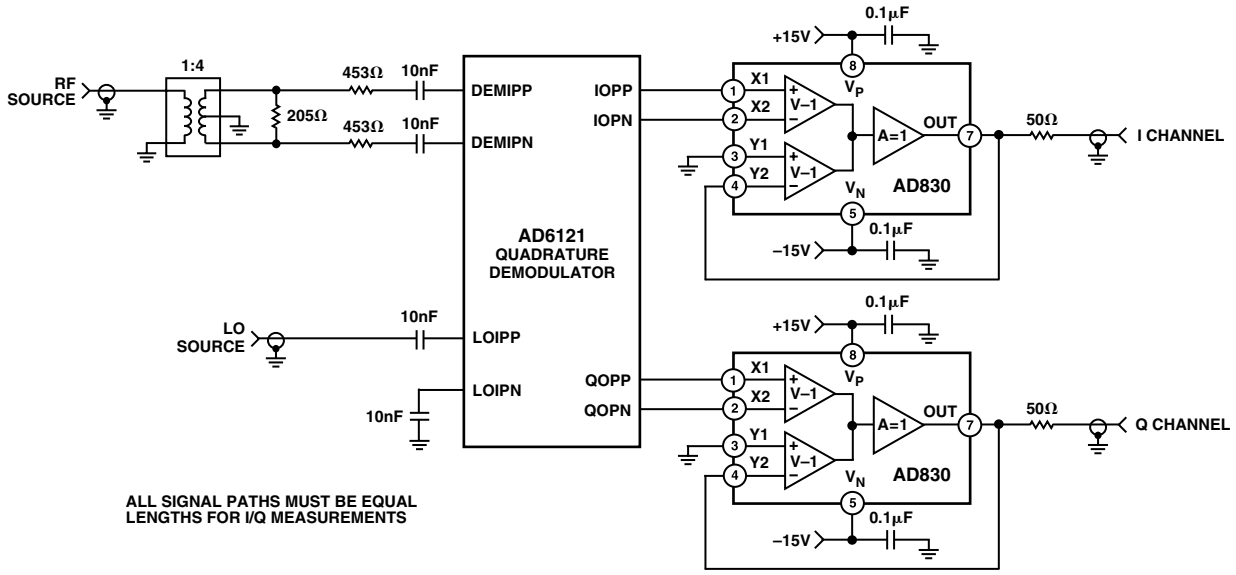


Figure 2. IF Amplifier Characterization Input and Output Impedance Matches

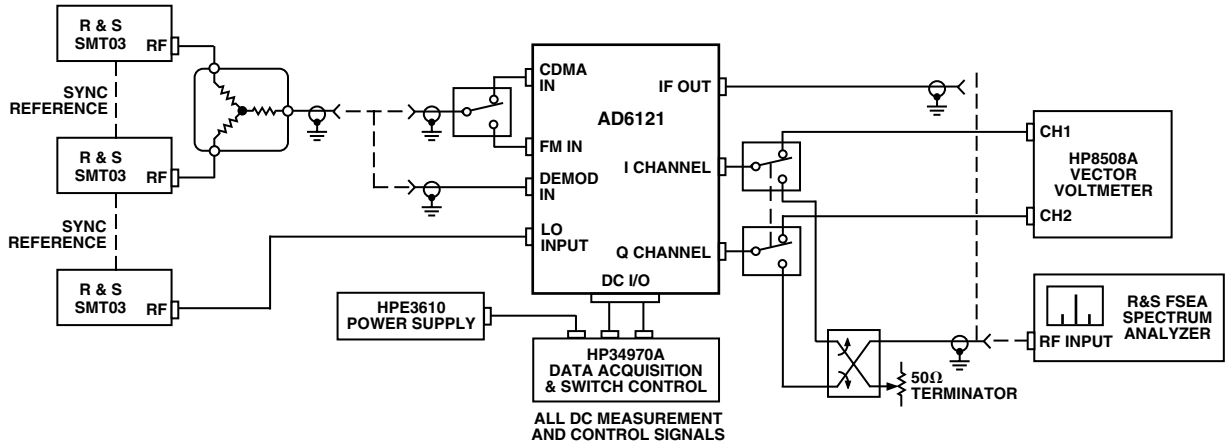


Figure 3. General Test Set

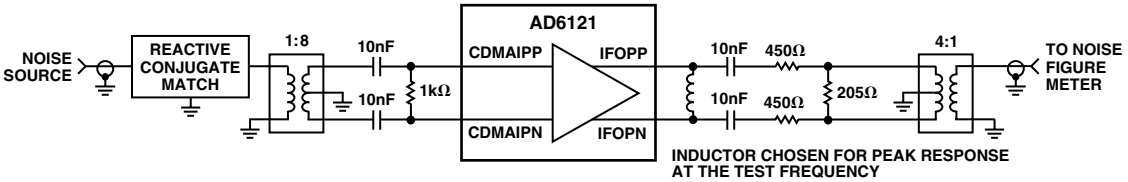
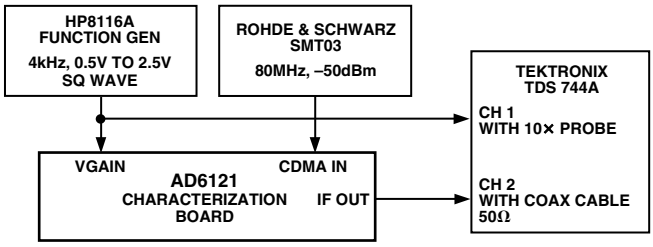
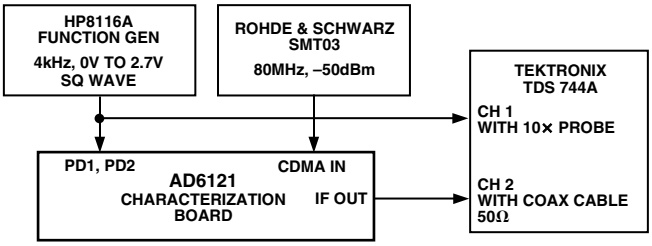


Figure 4. IF Amplifier Noise Figure Test Set



a. Response Time From Gain Control to IF Output



b. Response Time From PD1 and PD2 Control to IF Output

Figure 5. Response Time Setup

Typical Performance Characteristics

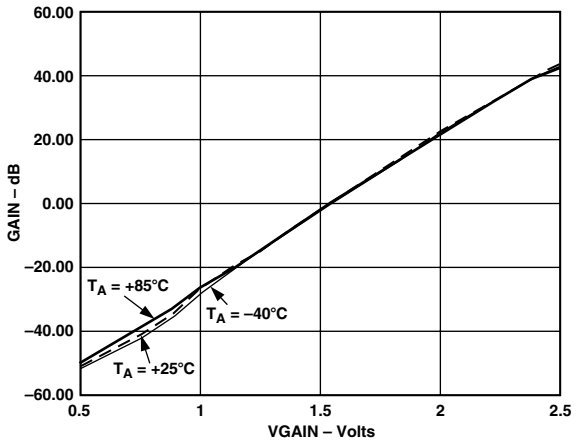


Figure 6. IF Amplifier's Gain vs. VGAIN, IF = 70 MHz, T_A = –40°C, +25°C and +85°C

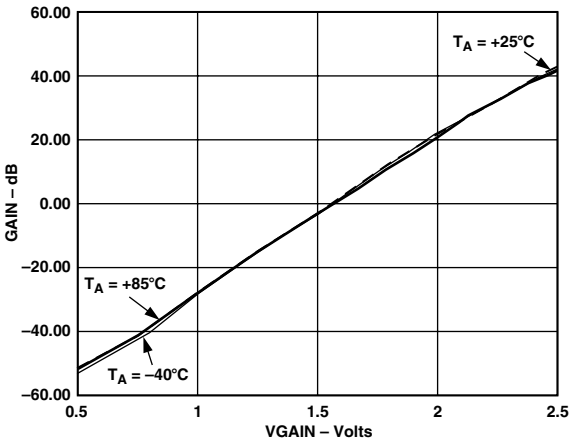


Figure 7. IF Amplifier's Gain vs. VGAIN, IF = 85 MHz, T_A = –40°C, +25°C and +85°C

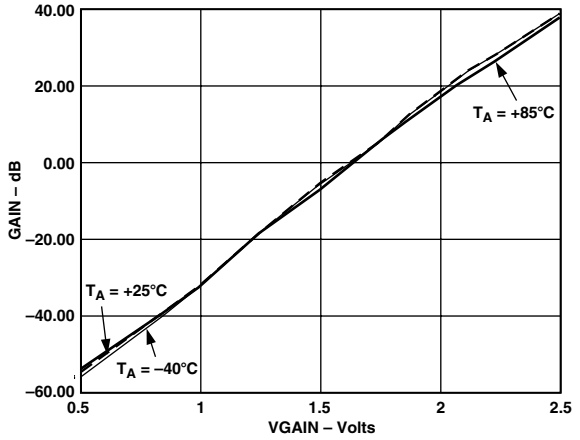


Figure 8. IF Amplifier's Gain vs. VGAIN, IF = 210 MHz, T_A = –40°C, +25°C and +85°C

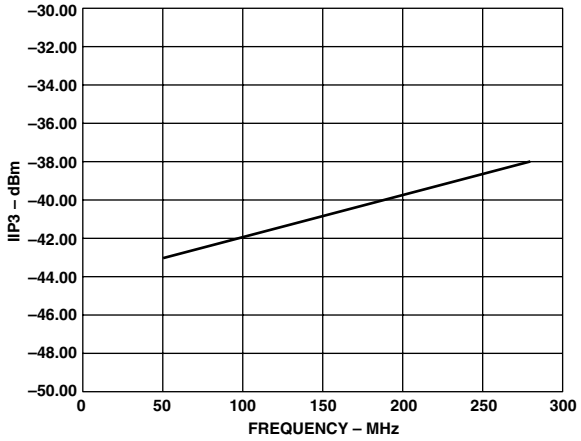


Figure 11. IF Amplifier's Input IP3 vs. Frequency, VGAIN = +2.5 V, T_A = +25°C

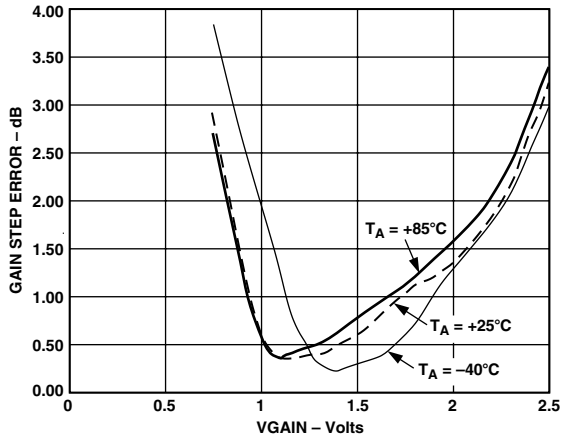


Figure 9. IF Amplifier's Gain Error vs. VGAIN, T_A = –40°C, +25°C and +85°C

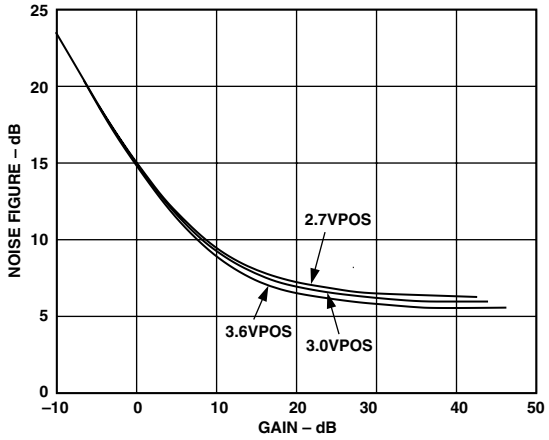


Figure 12. IF Amplifier Noise Figure vs. GAIN, IF= 85 MHz, T_A = +25°C

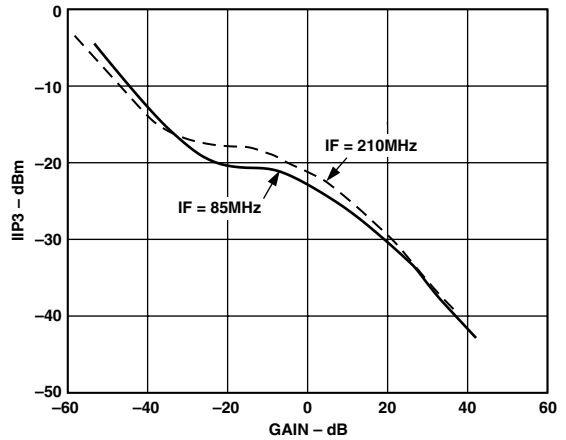


Figure 10. IF Amplifier's Input IP3 vs. Gain, IF = 85 MHz, 210 MHz, T_A = +25°C

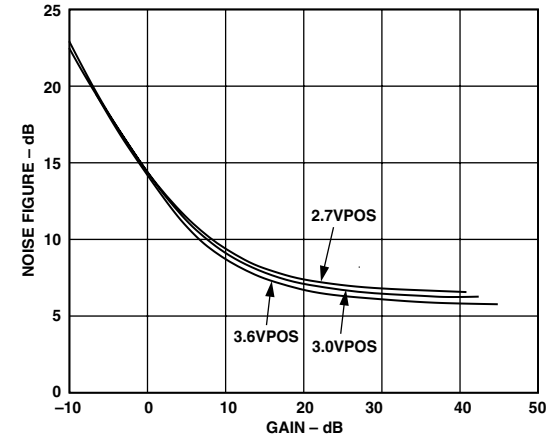


Figure 13. IF Amplifier Noise Figure vs. GAIN, IF= 210 MHz, T_A = +25°C

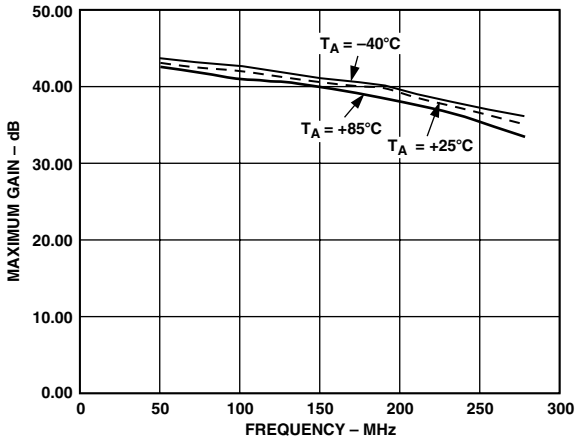


Figure 14. IF Amplifier Maximum Gain vs. Frequency, T_A = –40°C, +25°C and +85°C

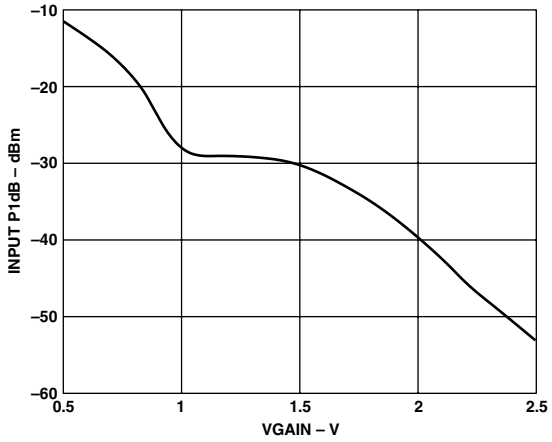


Figure 17. IF Amplifier Input 1 dB Compression Point vs. VGAIN, IF = 85.38 MHz

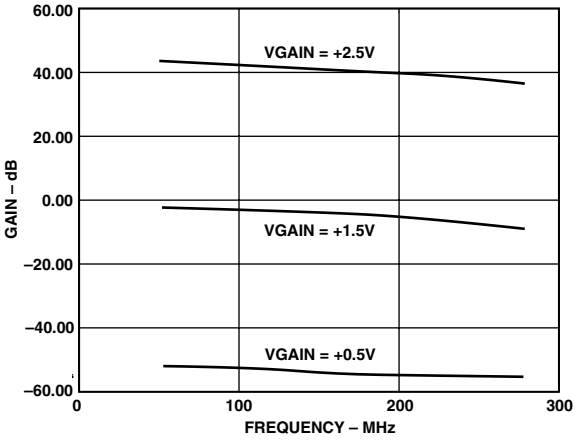


Figure 15. IF Amplifier Gain vs. Frequency, VGAIN = +0.5 V, +1.5 V and = +2.5 V

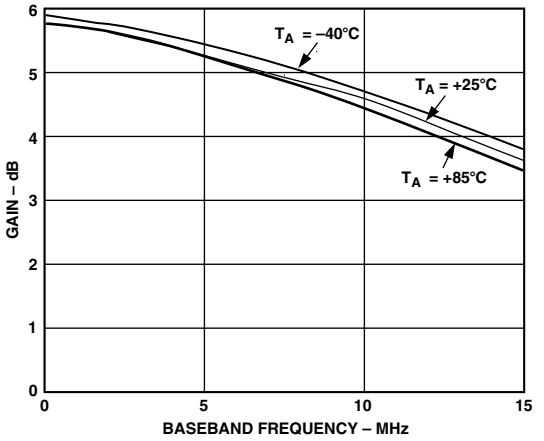


Figure 18. Demodulator I Channel Gain vs. Baseband Frequency, IF = 85 MHz

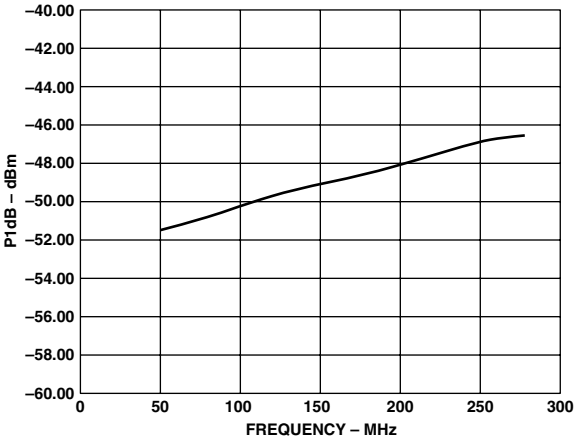


Figure 16. IF Amplifier 1 dB Compression Point vs. Frequency, VGAIN = +2.5 V

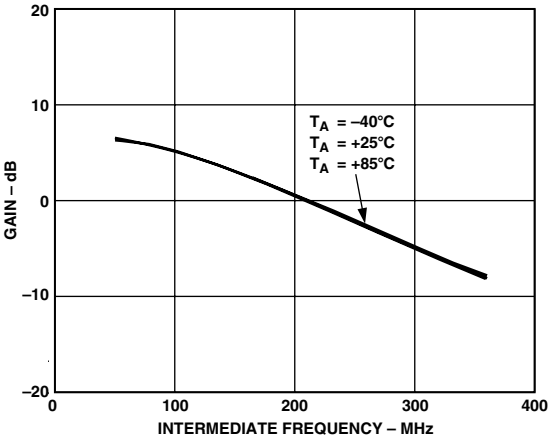


Figure 19. Demodulator I Channel Gain vs. IF, Baseband Frequency = 1 MHz, T_A = –40°C, +25°C and +85°C

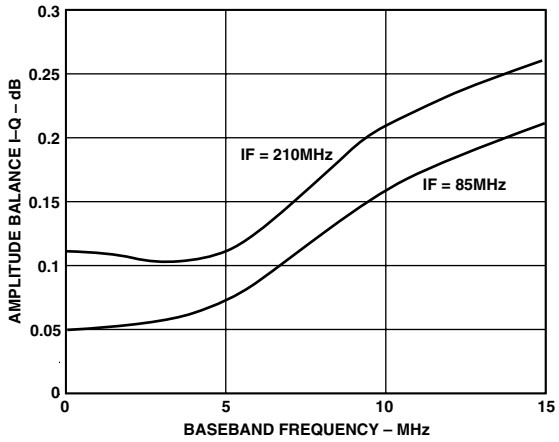


Figure 20. Demodulator I and Q Amplitude Balance vs. Baseband Frequency, IF = 85 MHz and 210 MHz

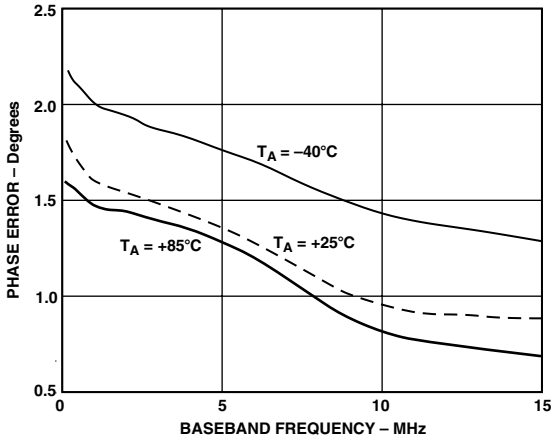


Figure 23. Demodulator Phase Error vs. Baseband Frequency, IF = 85 MHz, T_A = –40°C, +25°C and +85°C

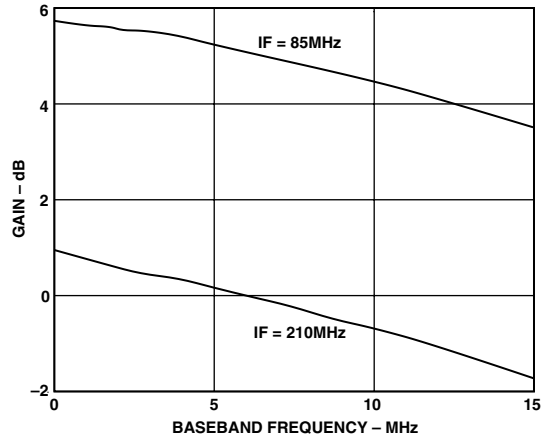


Figure 21. Demodulator I Channel Gain vs. Baseband Frequency, IF = 85 MHz and 210 MHz

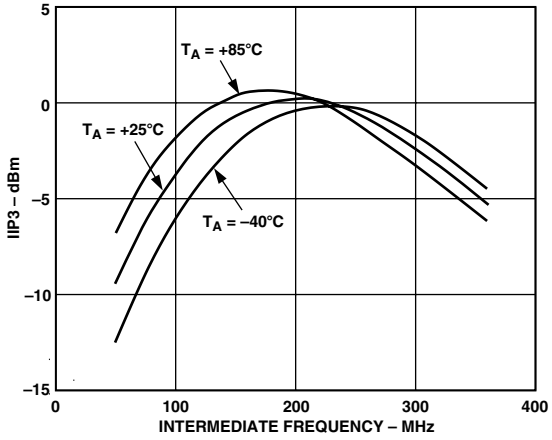


Figure 24. Demodulator Input IP3 vs. IF, Baseband Frequency = 1 MHz, T_A = –40°C, +25°C and +85°C

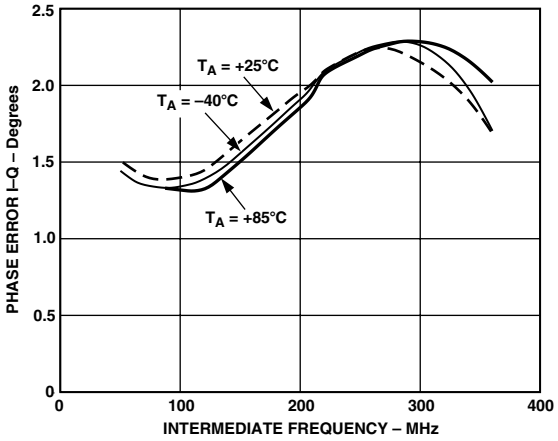


Figure 22. Demodulator Phase Error vs. IF, Baseband Frequency = 1 MHz, T_A = –40°C, +25°C and +85°C

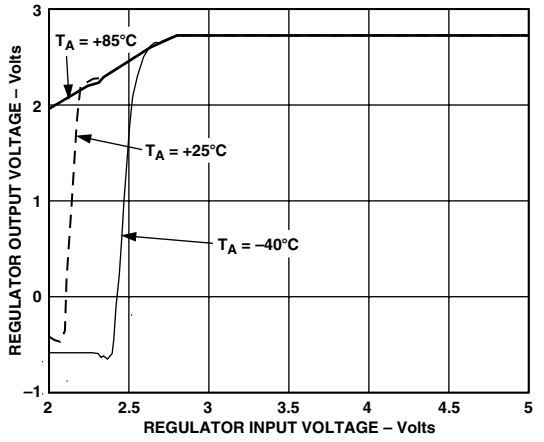


Figure 25. LDO Regulator Output Voltage vs. Input Voltage, T_A = –40°C, +25°C and +85°C

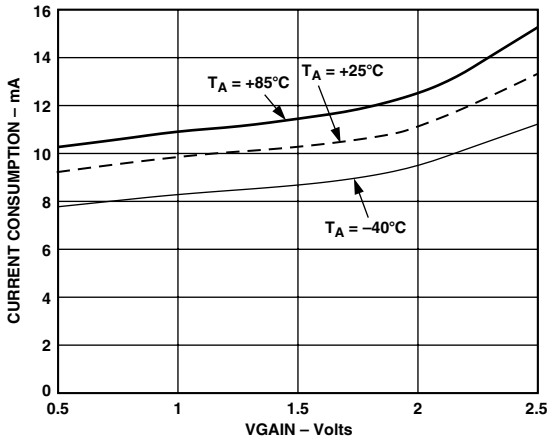


Figure 26. Current Consumption vs. VGAIN, T_A = –40°C, +25°C and +85°C

THEORY OF OPERATION

The AD6121 consists of high dynamic range IF amplifiers with voltage controlled gain, a divide-by-two quadrature generator, an I and Q demodulator, a low dropout regulator and power-down control inputs (Figure 27).

The AD6121 accommodates both the desired CDMA signal and an interferer 42 dB larger—approximately 6 mV p-p for the desired signal and 700 mV p-p for the interferer—as specified in the CDMA system.

IF Amplifiers and Gain Control

The IF gain is provided by two sections: a CDMA or FM input stage followed by three cascaded IF amplifiers. The CDMA and FM input stages use differential, continuously-variable attenuators based on Analog Devices' patented X-AMP™ topology. These low noise attenuators consist of a differential R-2R ladder network, linear interpolator, and a fixed gain amplifier. The bulk of the IF gain is provided by three cascaded, wideband amplifiers. The gain and input bandwidth of the AD6121 are identical for both the FM and CDMA operating modes. When the CDMA/FM pin is high, CDMA mode is enabled. When the pin is low, FM mode is enabled.

The IF amplifiers operate in two different configurations, one with the I and Q demodulator powered up and another with the I and Q demodulator powered down. The I and Q demodulator power setting is configured with pin PD2. The power-down control is further discussed in the section of this data sheet entitled Power-Down Control.

When the demodulator is powered up, the outputs of the IF amplifiers are internally dc-biased and there is no need for external pull-up inductors. A roofing filter is required (see section entitled Roofing Filter in this data sheet) when using the IF amplifiers with the I and Q demodulator powered up. Under these conditions, the IF amplifiers and the low noise attenuator input stage has +41.4 dB of gain.

When the I and Q demodulator is powered down, the IF amplifiers have open collector outputs resulting in the need for pull-up inductors. Under this configuration, and with the output of the IF amplifiers loaded with 1 kΩ, the gain of the IF amplifiers and low noise attenuator input stage is +47 dB. The pull-up inductors should be chosen so that the parasitic capacitance seen at the output of the IF amplifiers is resonated at the frequency of interest. Figure 28 shows how to configure the pull-up inductors at the output of the IF amplifiers. The 10 nF capacitors are used for ac coupling.

In order to resonate the parasitic capacitors, rearrange Equation 1 to solve for L.

$$f_0 = \frac{1}{2\pi\sqrt{LC_{PAR}}} \quad (1)$$

where f_0 is the IF frequency in Hertz, C_{PAR} is the total parasitic capacitance in Farads, and L is the total shunt inductor value in henrys.

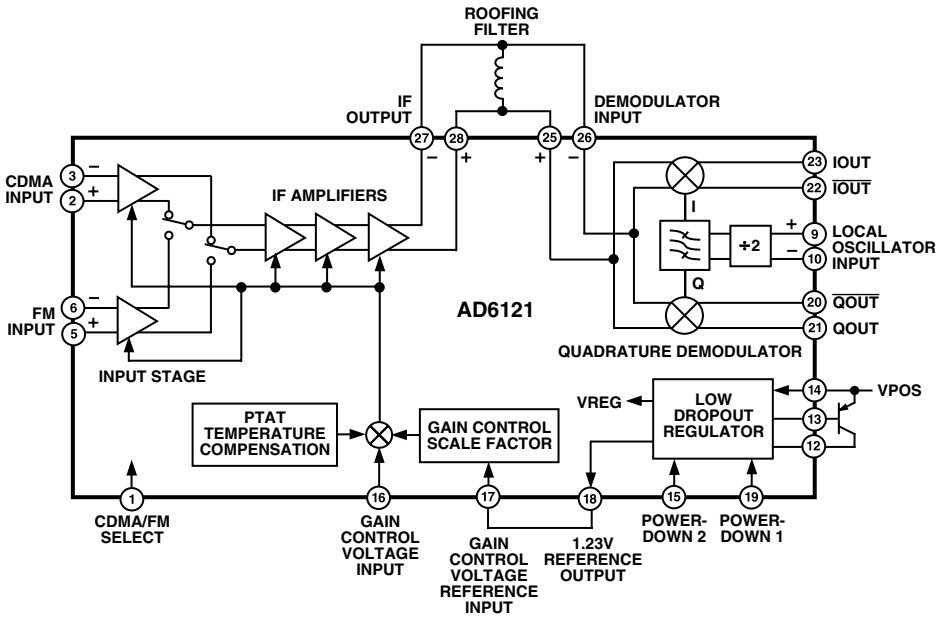


Figure 27. Functional Block Diagram

X-AMP is a trademark of Analog Devices, Inc.

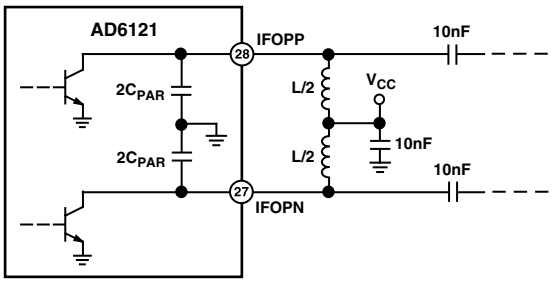


Figure 28. IF Amplifiers' Output Configuration When I and Q Demodulator Is Powered Down

In order to confirm whether the pull-up inductors have been properly designed, sweep the IF frequency and view the output of the IF amplifiers on a spectrum analyzer. If the inductor value is correct, the signal should peak at the IF frequency.

The gain of the two amplifier sections (input stage followed by amplifiers) changes sequentially for optimum signal-to-noise ratio. For example, in CDMA mode, the gain of the CDMA input amplifier first increases to maximum and then the gain of the cascaded IF amplifiers increases to maximum. Likewise, when decreasing gain, the gain of the cascaded amplifiers decreases to minimum before the gain of the CDMA input amplifier.

The gain control circuits contain both temperature compensation circuitry and a choice of internal or external reference for adjusting the gain scale factor. The gain control input accepts an external gain control voltage from a DAC. It provides 94.5 dB of gain control range with a nominal 52.5 dB/V scale factor. Either an internal or external reference may be used to set the gain control scale factor.

The external gain control input signal should be free of noise. In a typical wireless application, it is recommended to filter this signal in order to reduce the noise that results from the DAC that generates it. A simple RC filter can be employed, but care should be taken with its design. If too big a resistor is used, a large voltage drop may occur across the resistor resulting in lower gain than expected (as a result of a lower voltage reaching the AD6121). An RC filter with a 1 kHz bandwidth, employing a 1 kΩ resistor is appropriate. This results in a 150 nF capacitor. The resulting circuit is shown in Figure 29.

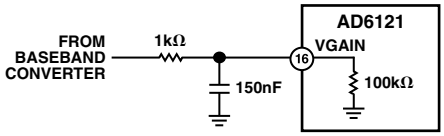


Figure 29. Gain Voltage Filtering

The AD6121's overall gain, expressed in decibels, is linear in dB with respect to the automatic gain control (AGC) voltage, VGAIN. Either REFOUT, or an external reference voltage connected to REFIN, may be used to set the voltage range for VGAIN. When the internal 1.23 V reference, REFOUT, is connected to REFIN, VGAIN will control the AGC range when it is typically set between 0.5 V and 2.5 V. Minimum gain occurs at minimum voltage on VGAIN and maximum gain occurs at maximum voltage on VGAIN. The maximum and minimum gain will not change with a change in voltage at REFIN. Rather, the slope of the gain curve will change as a result of a change in the required range for VGAIN. Figure 30 shows the piecewise linear approximation of the gain curve for the AD6121.

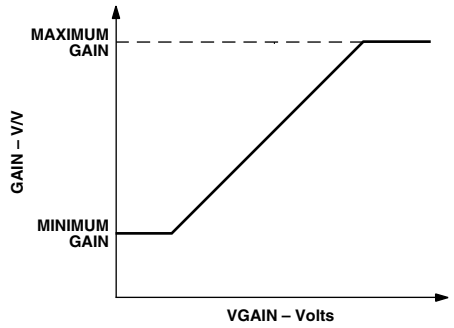


Figure 30. Piecewise Linear Approximation for the AD6121 Gain Curve

Because the minimum and maximum gains for the AD6121 are constant, we can approximate the VGAIN range for a given REFIN voltage by using Equation 2.

$$VGAIN = \frac{(GAIN - MinGain) \times 1.6\ REFIN}{MaxGain - MinGain} + 0.4\ REFIN \quad (2)$$

Where *MaxGain* is the maximum gain (+47 dB) in dB, *MinGain* is the minimum gain (–47.5 dB) in dB, *REFIN* is the reference input voltage, in volts, *VGAIN* is the gain control voltage input, in volts, and GAIN is the particular gain, in dB, we would have for a given REFIN and VGAIN. Consequently, for any REFIN we choose, we can calculate the VGAIN range by solving Equation 2 for VGAIN. For example, in order to determine the VGAIN value for the maximum gain condition, given a 1.23 V REFIN, we can solve Equation 2 for VGAIN by substituting 47 dB for GAIN and MaxGain, –47.5 dB for MinGain and 1.23 V for REFIN. VGAIN can then be calculated to be 2.46 V, or approximately 2.5 V. For the minimum gain condition, we can determine the VGAIN value by substituting 47 dB for MaxGain, –47.5 dB for Gain and MinGain and 1.23 V for REFIN. VGAIN can then be calculated to be 0.492 V or approximately 0.5 V.

I and Q Demodulator

The I and Q demodulator provides differential quadrature baseband outputs to CDMA baseband converters. The demodulator provides 5.6 dB of voltage gain in addition to the gain provided by the IF amplifier stage. The outputs of the I and Q demodulator are filtered with a low-pass filter, which typically has a 16 MHz bandwidth. A divide-by-two quadrature generator followed by dual polyphase filters ensures a typical ±1° quadrature accuracy (Figure 31).

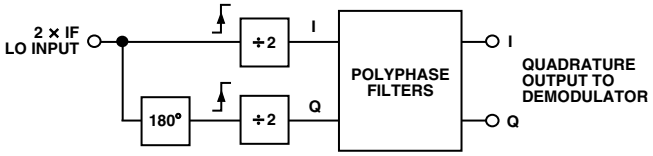


Figure 31. Simplified Quadrature Generator Circuit

Power-Down Control

The AD6121 can operate with the IF amplifier and I and Q demodulator stages both powered up, the IF amplifiers powered up alone or both the IF amplifiers and demodulator powered down. The AD6121 cannot operate with the demodulator powered up and the IF amplifiers powered down. The control for these different modes is performed via the PD1 and PD2 pins. Table I shows the decoding of the logic inputs.

Table I. AD6121 Operating Modes

PD1	PD2	IF Amplifiers	Demodulator
0	0	ON	ON
0	1	ON	OFF
1	0	INVALID STATE	INVALID STATE
1	1	OFF	OFF

Low Dropout Regulator

The AD6121 incorporates an integrated low dropout regulator. The regulator accepts inputs from 2.9 V to 4.2 V and supplies 2.7 V at LDOC. The 2.7 V signal can be used to provide the dc voltages required for the DVCC and IFVCC dc supplies. In order to configure the low dropout regulator, an external pass transistor is required. A pnp transistor with a minimum h_{FE} of 100 and a maximum h_{FE} of 300 and a V_{CE}(Sat.) of –0.4 V is required. In order to use the low dropout regulator, configure the transistor as shown in Figure 32. The 10 nF capacitor in Figure 32 is used for decoupling the 2.7 V dc signal.

In addition to the low dropout regulator, there is a bandgap voltage reference which produces a 1.23 V reference voltage at pin REFOUT. This reference voltage will be present whenever a voltage is applied to IFVCC and DVCC. This 1.23 V reference voltage can then be used to provide the gain reference voltage for the receive ADCs in the baseband converter.

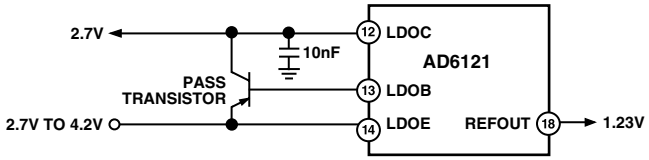


Figure 32. Configuring the Low Dropout Regulator

It is possible to bypass the low dropout regulator on the AD6121 and use an external regulator instead. In order to bypass the integrated low dropout regulator, connect pins LDOE, LDOB and LDOC together and then connect them all to the external regulator voltage. This configuration is shown in Figure 33. Even when the low dropout regulator is bypassed, the 1.23 V reference voltage at pin REFOUT is still present.

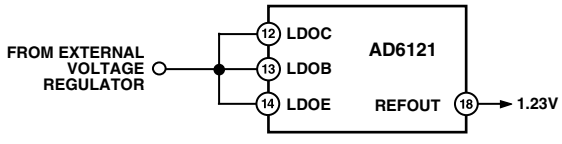


Figure 33. Configuration for Bypassing the Low Dropout Regulator

ROOFING FILTER

When the IF amplifiers and I and Q demodulator of the AD6121 are both powered up, the parasitic impedances seen at the output of the IF amplifiers and inputs of the I and Q demodulator are high enough to create a low-pass filter, which may attenuate the IF signal. Consequently, the parasitic capacitance must be cancelled by using an external inductor to form a parallel resonant circuit. The external inductor that is required and the internal parasitic capacitors form what is known as the roofing filter, with the resonant frequency given by Equation 1 (see IF Amplifiers and Gain Control section of this data sheet).

The roofing filter may be composed of a shunt inductor between the IF amplifiers differential output pins. Because the demodulator is powered up when the output of the IF amplifiers are fed into the I and Q demodulator, the output of the IF amplifiers are not open collector. As a result, pull up inductors are not required. This configuration is shown in Figure 34. The 10 nF capacitors are used for ac coupling.

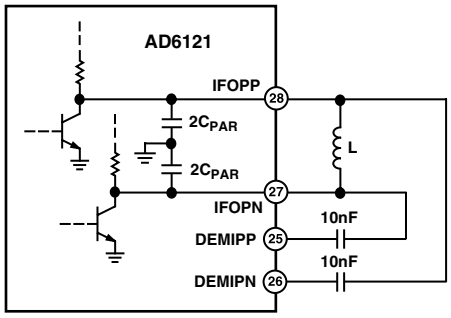


Figure 34. Roofing Filter Configuration

In order to confirm whether the roofing filter has been correctly designed, sweep the IF frequency and view the output of the I and Q demodulator on a spectrum analyzer. The output level of the I or Q signal should be approximately flat from dc to 16 MHz, after which the low-pass filters at the I and Q output will attenuate the signal. With the correct roofing filter inductor, the I and Q output signal will be higher than for any other roofing filter inductor value.

It should be noted that the roofing filter is only required when cascading the output from the IF amplifiers to the input of the I and Q demodulator. If we are looking at the output of the IF amplifiers, no roofing filter is required. Because the IF amplifiers' outputs are open collector when the I and Q demodulator is powered down, pull-up inductors will be required in order to set the dc voltage (see the section of this data sheet entitled IF Amplifiers and Gain Control) and to resonate the parasitic capacitors that are present under these conditions.

LEVEL DIAGRAM

Figure 35 is provided in order to better understand the different voltage and power levels you can expect to see at different points on the AD6121. It represents the levels that would be seen on Rev. B of the AD6121 Customer Evaluation Board. When trying to make these measurements, a high impedance (10 MΩ) active FET probe (for example, the TEK P6204 from Tektronix) should be used to minimize the effects of loading the circuits with the probe.

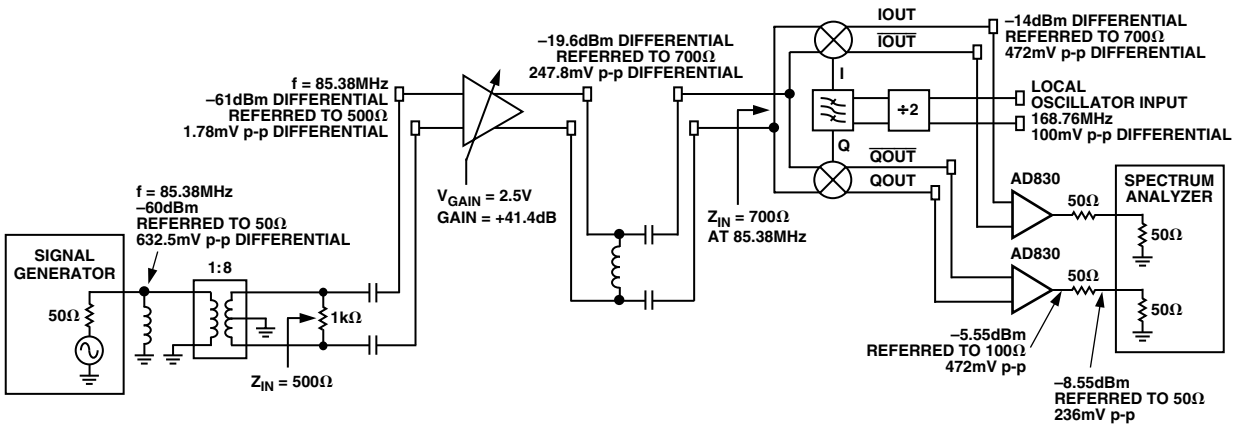


Figure 35. AD6121 Signal Level Diagram for AD6121 Customer Sample Board, Rev. B

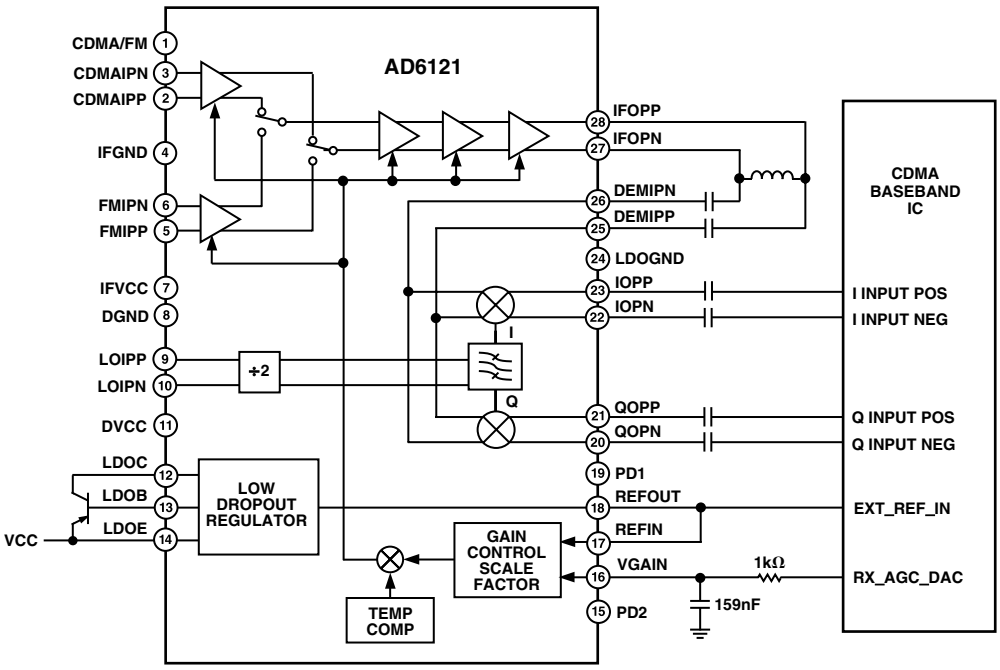


Figure 36. Typical Application Showing Interface to Baseband IC with SSOP Package

OUTPUT INTERFACES

The AD6121 interfaces to CDMA baseband converters requiring either IF or baseband inputs. The baseband output is provided by direct connection of the AD6121's baseband output to the baseband input of the baseband converter (Figure 36). The output interfaces are controlled by the AD6121's power-down modes.

AD6121 CUSTOMER EVALUATION BOARD

The AD6121 customer evaluation board consists of an AD6121, I/O connectors, 3 two-pin headers, a 20-pin dual header and two AD830 High Speed Video Difference Amplifiers. It allows the user to evaluate the AD6121's I and Q demodulator and IF amplifiers operating together or separately. The board is identical for both the SSOP and LPCC packages. Because the AD6121 can operate at any IF frequency from 50 MHz to 350 MHz, pads are provided on the LOIPP, IFIP, CDMAIP and DMOD IN inputs as well as the IF OUT output ports to allow the user to add matching networks. The board is configured for an IF frequency of 85.38 MHz when shipped.

The AD830s are used to provide differential to single ended conversion for analysis of the differential I and Q outputs. As a result, the output can be displayed on a spectrum analyzer or other test equipment requiring a single ended input.

Prior to applying a CDMA or FM input signal, the appropriate mode must be selected. FM mode will be selected by shorting the two pins of the two pin header labeled FM/CDMA. Open circuiting these two pins will select CDMA mode.

In order to test the power-down modes of the AD6121, locate the bank of 3 two-pin headers on the evaluation board. In order to have both the IF amplifiers and the I and Q demodulator powered up, short circuit each of the two pins on the two pin headers labeled PD1 and PD2. In order to power down the demodulator and keep the IF amplifiers powered up, short circuit the 2 pins on the header labeled PD1 and open circuit

the header labeled PD2. As described in Table I of this data sheet, it is invalid to have PD1 open circuited and PD2 short circuited. In order to power down the IF amplifiers and demodulator, open circuit both PD1 and PD2.

As shipped, the board is configured as follows:

1. J1 is open circuited and J2 is short circuited. This enables the LDO regulator. In order to bypass the LDO regulator, short circuit J1 and open circuit J2.
2. X18, X26, X25 and X23 are short circuited resulting in the IF amplifiers' output being connected to the I and Q demodulator's input.
3. L4, the roofing filter inductor is optimized for an IF frequency of 85.38 MHz.
4. L2 and L3 are open circuited, although the components are soldered on one pad of each set of solder pads.

In order to evaluate the IF amplifiers and I and Q demodulator independent of each other, the roofing filter will have to be removed from the circuit and the pull up inductors will have to be added at the output of the IF amplifiers. When evaluating the IF amplifiers alone, the I and Q demodulator should be powered down as described earlier in this section. The 470 nH pull up inductors required for the 85.38 MHz IF frequency are provided with the board, however, they will need to be soldered down to pads L2 and L3. The roofing filter should be disconnected from the circuit and the output ports for the IF amplifiers as well as the input ports for the I and Q demodulator should be connected. This is accomplished by open circuiting X18, X25, X26 and X33 and short circuiting X19, X21, X27 and X29.

Table II describes the high frequency signal connectors on the AD6121 customer sample board.

Table II. Evaluation Board SMA Signal Connector Descriptions

Connector	Description
LOIPP	Local oscillator positive input at 2 × IF frequency
FMIP	FM signal input port. The differential to single ended conversion performed on board by a balun. Impedance matched to 50 Ω for a 85.38 MHz IF frequency.
CDMAIP	CDMA signal input port. The differential to single ended conversion performed on board by a balun. Impedance matched to 50 Ω for a 85.38 MHz IF frequency.
IF OUT	IF Amplifier output port. The differential to single ended conversion performed on board by a balun. Impedance matched to 50 Ω for a 85.38 MHz IF frequency.
DMOD IN	Demodulator input port. The differential to single ended conversion performed on board by a balun. Impedance matched to 50 Ω for a 85.38 MHz IF frequency.
I CH	I channel output port for the I and Q demodulator.
Q CH	Q channel output port for the I and Q demodulator

Table III lists the connections for the 20-pin power supply connector.

Table III. 20-Pin Power Supply Connection Information

Pin Number	Function
1	VPOS for AD6121. 2.9 V–4.2 V using the LDO Regulator. 2.7 V–4.2 V bypassing the LDO Regulator.
2	VPOS for AD6121. 2.9 V–4.2 V using the LDO Regulator. 2.7 V–4.2 V bypassing the LDO Regulator.
3	Ground.
4	Ground.
5	Ground.
6	Ground.
7	Ground.
8	PD1. Connects to 2-pin header labeled PD1.
9	Ground.
10	PD2. Connects to 2-pin header labeled PD2.
11	Ground.
12	FM/CDMA. Selects FM or CDMA mode. Connected to 2-pin header labeled FM/CDMA.
13	Ground.
14	REFOUT. 1.23 V output reference voltage from Pin 18 on AD6121.
15	Ground.
16	VGAIN. Gain control voltage input. Connected to Pin 16 on AD6121.
17	Ground.
18	V_{REGOUT}. The 2.7 V output of the LDO regulator when it is enabled. Connects to Pin 12 on AD6121.
19	–15 V for AD830 Amplifier.
20	+15 V for AD830 Amplifier.

A schematic diagram of the evaluation board is shown in Figure 37.

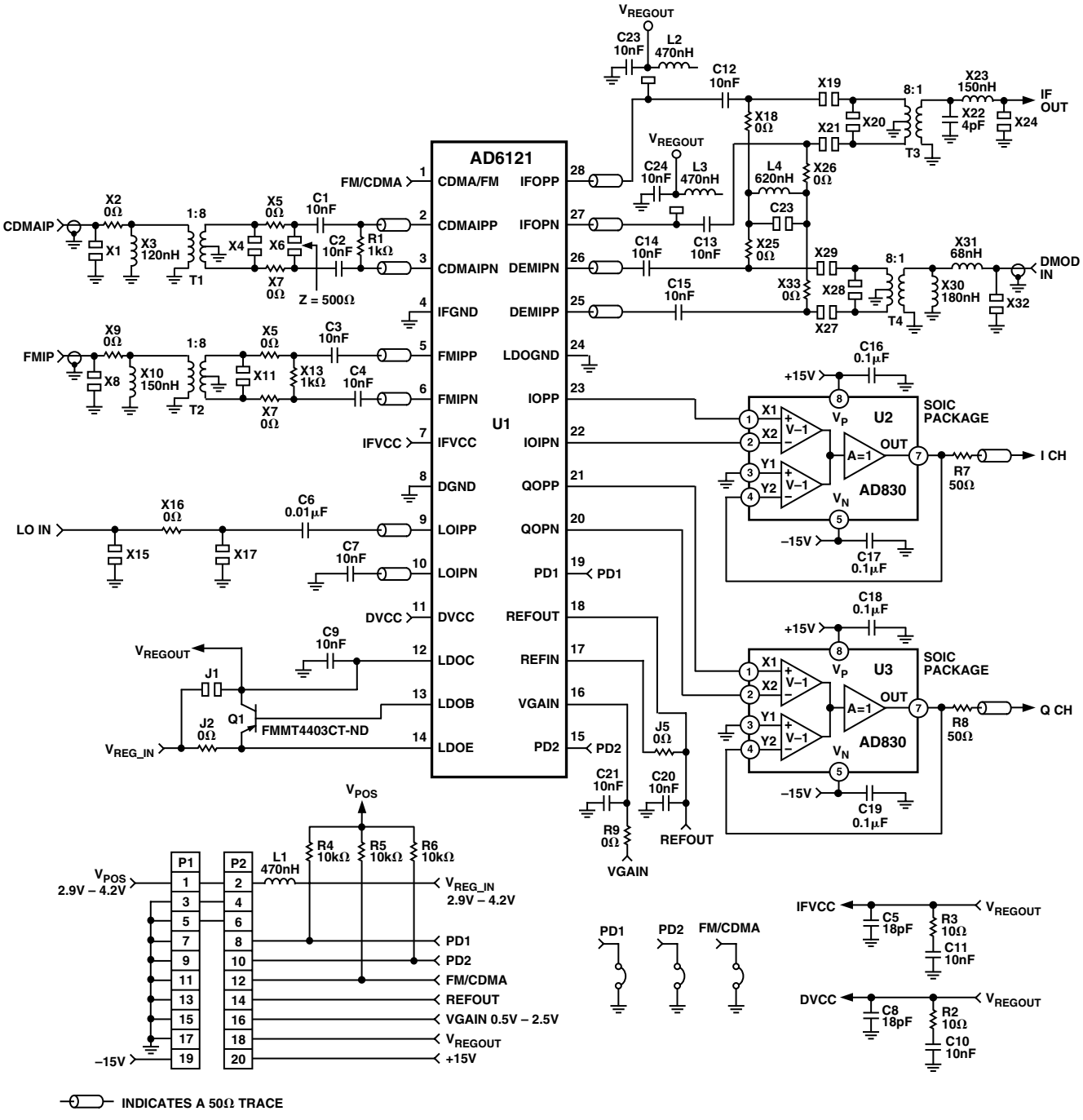
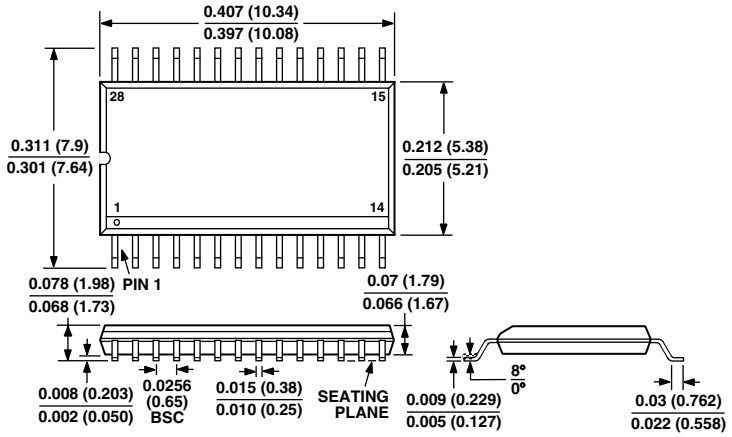


Figure 37. Schematic Diagram of AD6121 Evaluation Board

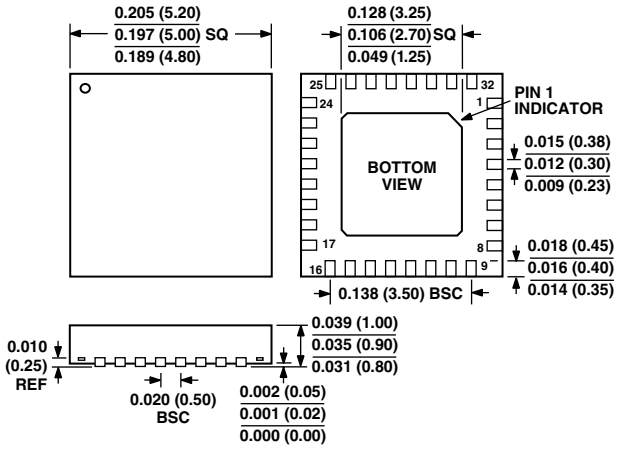
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



32-Leadless Chip Scale Package (LPCC)
(CP-32)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS MEET JEDEC MO-220-VHHD-2

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