Z9974

3.3V, 125-MHz, Multi-Output Zero Delay Buffer

Features

- **Output Frequency up to 125 MHz**
- **Supports PowerPC®, and Pentium® processors**
- **15 Clock outputs: frequency configurable**
- **Two Reference clock inputs for dynamic toggling**
- **Output Three-State control**
- **Spread spectrum compatible**
- **3.3V power supply**
- **Pin compatible with MPC974**
- **Industrial temperature range: –40°C to +85°C**
- **52-pin TQFP package**

Description

The Z9974 is a low-cost 3.3V zero delay clock driver for high-speed signal buffering and redistribution.

The designer can select various Input/Output Frequency by setting fsela, fselb, fselc, fselFB(0:1), and VCO_Sel.

The Z9974 integrates PLL technology for zero delay propagation from input to output. The PLL feedback is externally available for propagation delay tuning and divide ratio alternatives as per *Table 1*.

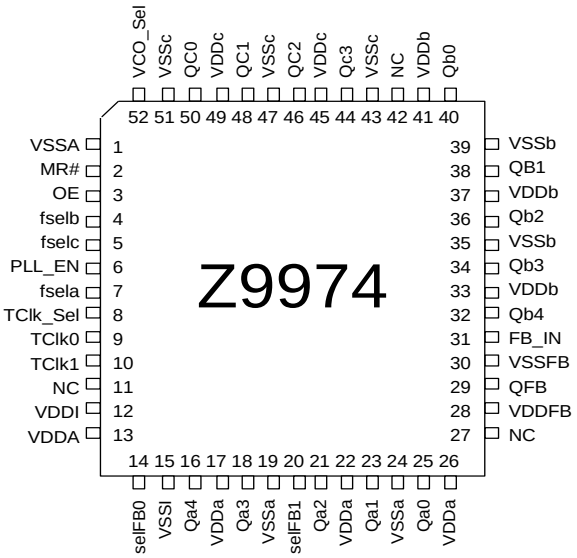
The Z9974 has three banks of outputs with independent divider stages. These dividers allow the banks to have different frequencies as per *Table 2*.

TCLK0 and TCLK1 are selectable input reference clocks and may be toggled dynamically during operation to provide modulation and phase shifting designs.

This device includes a Master Reset signal, which disables the outputs (Hi-Z) mode, and reset all internal digital circuitry (excluding the PLL).

An Output Enable, OE, input pin is available for disabling the Qa(0:4), Qb(0:4), and Qc(0:3) outputs and forcing them to LOW state. All outputs are held LOW with input clock turned off.

Pin Configuration



Block Diagram

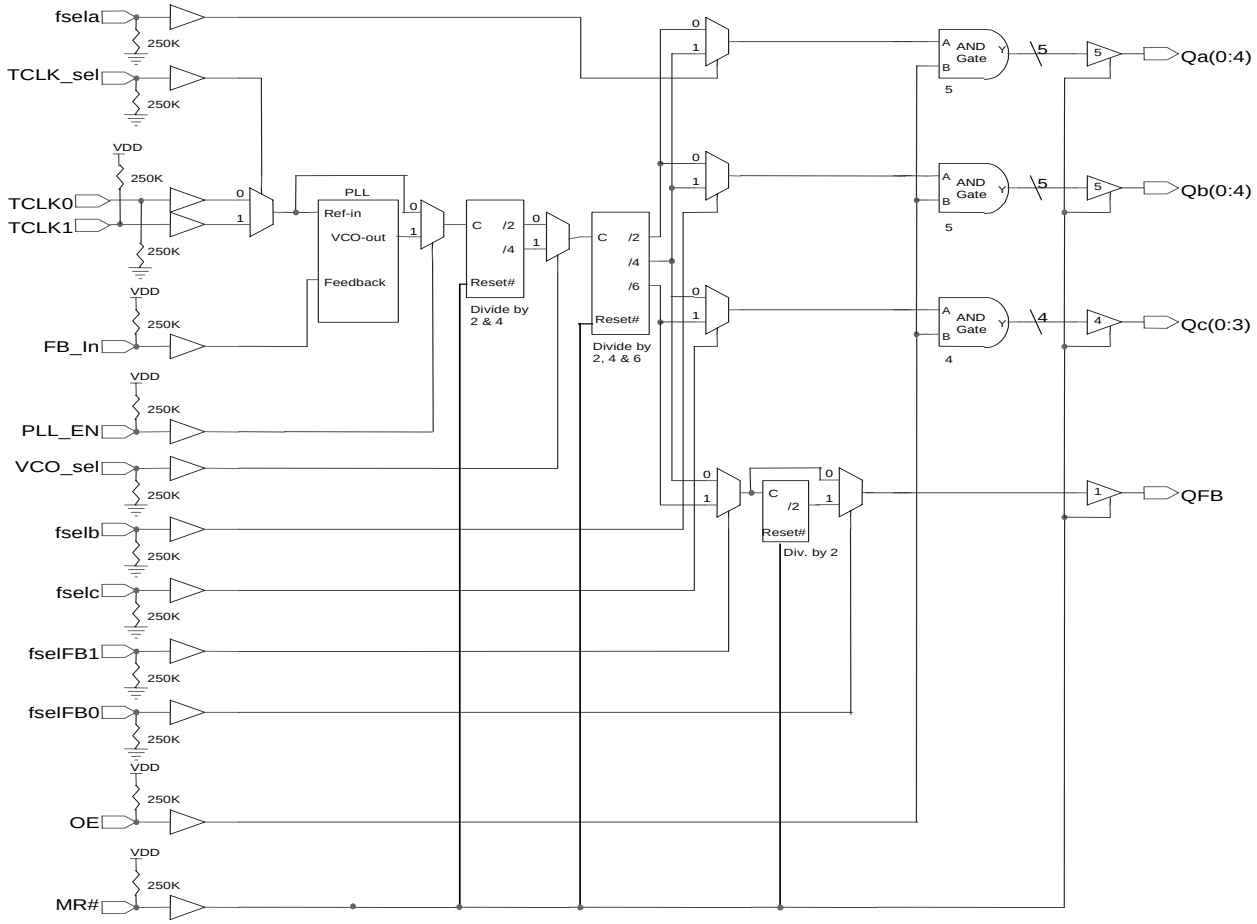


Table 1. Feedback Divider Selection

Inputs			Output
VCO_Sel	fselFB0	fselFB1	QFB
0	0	0	VCO/8
0	0	1	VCO/12
0	1	0	VCO/16
0	1	1	VCO/24
1	0	0	VCO/16
1	0	1	VCO/24
1	1	0	VCO/32
1	1	1	VCO/48

Table 2. Output Divider Selection

VCO_Sel	fsela	Qa	fselb	Qb	fselC	Qc
0	0	VCO/4	0	VCO/4	0	VCO/8
0	1	VCO/8	1	VCO/8	1	VCO/12
1	0	VCO/8	0	VCO/8	0	VCO/16
1	1	VCO/16	1	VCO/16	1	VCO/24

Pin Description[1]

Pin	Name	PWR	I/O	Description
2	MR#		I	**Master Reset pin**. Active LOW. It has a 250-KΩ internal pull-up. When forced LOW, all outputs are three-stated (high impedance) and internal dividers are reset.
3	OE		I	**Output Enable pin**. Active LOW. It has a 250-KΩ internal pull-up. When forced LOW, Qa(0:4), Qb(0:4), and Qc(0:3) outputs are stopped in a LOW state. QFB is not affected by this control signal.
7, 5, 4	fsel(a,b, c)		I	**Input select pins** for setting the output dividers of Qa(0:4), Qb(0:4), and Qc(0:3) respectively. Each pin has an internal 250-KΩ pull-down. See *Table 2* for output divide ratios.
6	PLL_EN		I	**Input pin for bypassing the PLL**. It has an internal 250-KΩ pull-up. When forced LOW, the input reference clock (applied at TCLK0, or TCLK1) bypasses the PLL and drives the dividers, typically for device testing.
8	TCLK_sel		I	**Input pin for selecting TCLK0 or TCLK1 as input reference**. When TCLK_sel = 0, TCLK0 is selected, when TCLK_sel = 1, TCLK1 is selected. This pin has a 250-kΩ internal pull-down.
9,10	TCLK(0:1)		I	**Input pins for applying a reference clock to the PLL**. The active input is selected by TCLK_sel, pin# 8. TCLK0 has a 250-KΩ internal pull-down. TCLK1 has a 250-KΩ internal pull-up.
14,20	fselFB(0:1)		I	**Input select pins for setting the Feedback divide ratio at QFB output**, pin #29. See *Table 1*. Each of these pins has a 250-KΩ internal pull-down.
16,18,21,23, 25	Qa(0:4)	VDDa	O	**High-drive, low-voltage CMOS, output clock buffers, Bank Qa**. Their divide ratio is programmed by fsela, pin #7.
29	QFB	VDDFB	O	**Low-voltage CMOS output feedback clock to the internal PLL**. The divide ratio for this output is set by fselFB(0:1). A delay capacitor or trace may be applied to this pin in order to control the Input Reference/Output Banks phase relationship.
31	FB_In		I	**Feedback input pin**. Typically connects to the QFB output for accessing the feedback to the PLL. It has a 250-kΩ internal pull-up.
32,34,36,48, 40	Qb(0:4)	VDDb	O	**High-drive, low-voltage CMOS, output clock buffers, Bank Qb**. Their divide ratio is programmed by fselb, pin #4.
44,46,48,50	Qc(0:3)	VDDc	O	**High-drive, low-voltage CMOS, output clock buffers, Bank Qc**. Their divide ratio is programmed by fselc, pin #5.
52	VCO_Sel		I	**Input select pin for setting the divider of the VCO output**. It has a 250-kΩ internal pull-down. If VCO_sel = 0, then the PLL VCO output is divided by 2. If VCO_sel = 1, then the PLL VCO output is divided by 4. See *Table 1* and *Table 2*.
11,27,42	n/c		-	**These pins are not connected internally**. They may be attached to a ground plane.
12	VDDI		P	**Power for input logic circuitry**.
15	VSSI		P	**Ground for input logic circuitry**.
13	VDDA		P	**Power and Ground supply pins for internal analog circuitry**.
17,22,26	VDDa		P	**3.3V supply for Qa(0:4) output bank, and fselFB1 input**.
19,24	VSSa		P	**Common ground for Qa(0:4) output bank, and fselFB1 input**.
28	VDDFB		P	**Power supply pin for QFB output and FB_In input pins and digital circuitry**.
30	VSSFB		P	**Ground supply pin for QFB output and FB_In input pins and digital circuitry**.
33,37,41	VDDb		P	**3.3V supply for Qb(0:4) output bank**.

Note:

1. A bypass capacitor (0.1 µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristic will be cancelled by the lead inductances of the traces.

Pin Description[1] (continued)

Pin	Name	PWR	I/O	Description
35,39	VSSb		P	**Common ground for Qb(0:4) output bank**.
45,49	VDDc		P	**3.3V supply for Qc(0:3) output bank and VCO_sel pin**.
43,47,51	VSSc		P	**Common ground for Qc(0:3) output bank and VCO_sel pin**.
1	VSSA		P	**Analog Ground**

Glitch-Free Output Frequency Transitions

Customarily when zero delay buffers have their internal counters change “on the fly” their output clock periods will:

1. Contain short or “runt” clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency that is being transitioned to.
2. Contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency that is being transitioned to.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed “on the fly” while it is operating: Fsela, Fselb, Fselc, and VCO_Sel

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: ..... –65°C to + 150°C

Operating Temperature: ..... –40°C to +85°C

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current				–100	µA
I_{IH}	Input High Current				100	µA
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = –20 mA	2.4			V
I_{DDQ}	Quiescent Supply Current			20		mA
Cin	Input Capacitance	per input			8	pF

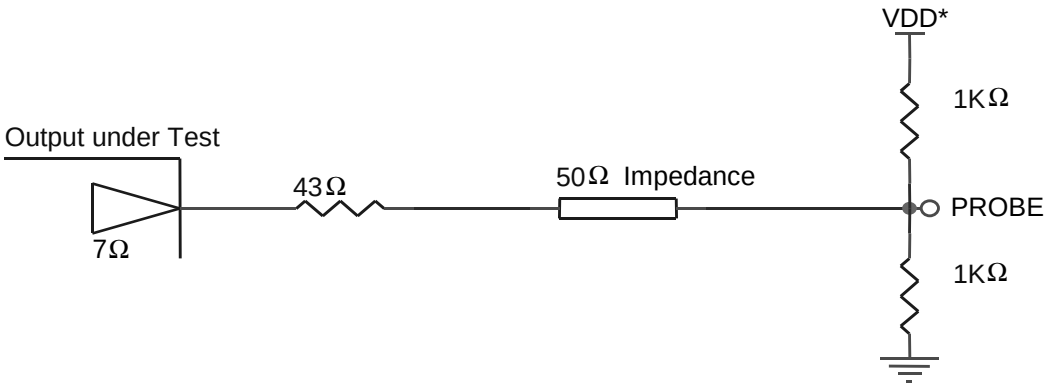
AC Parameters[3] V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{LOCK}	Maximum PLL Lock Time	Stable power supply & valid clocks presented on TCLK(0:1) pins			10	ms
F_{VCO}	VCO Lock Range	FselFB(0:1)=/4 to /12	200		500	MHz
T_{inr},T_{inf}	TCLK(0:1) Input Rise/Fall Time				3	ns
F_{REF}	Input Reference Frequency		*Note 4*		*Note 4*	MHz
F_{REFpw}	Input Reference Duty Cycle		*Note 4*		*Note 4*	%
T_{pw}	Output Duty Cycle	Measured at V_{DD}/2	Tcycle/2 – 800	Tcycle/2 ± 500	Tcycle/2 + 800	ps
T_r,T_f	Rise Time/Fall Time	Measured between 0.8V and 2.0V	0.15		1.5	ns
Z_o	Output Impedance			7	10	Ω
T_s	Output to Output Skew	All outputs equally loaded			250	ps
T_{pd}	Propagation Delay, TCLK(0:1) to FBIN	Measured at 50 MHz, V_{DD}/2	–250		100	ps
T_j	Cycle to Cycle Jitter	Measured at 50 MHz, V_{DD}/2		±100		ps
T_{PLZ}, T_{PHZ}	Output Disable Time	After MR# goes LOW	2		10	ns
T_{PZL}	Output Enable Time	After MR# goes HIGH	2		10	ns
F_{out}	Maximum Output Frequency	Q (/2)			125	MHz
		Q (/4)			62	
		Q (/6)			41	

Notes:

2. The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs. Z9974 outputs can drive series or parallel terminator 50Ω (or 50Ω to V_{DD}/2).
4. Input Reference Frequency is limited by the divider selection and the VCO lock range.

Test Circuit Diagram



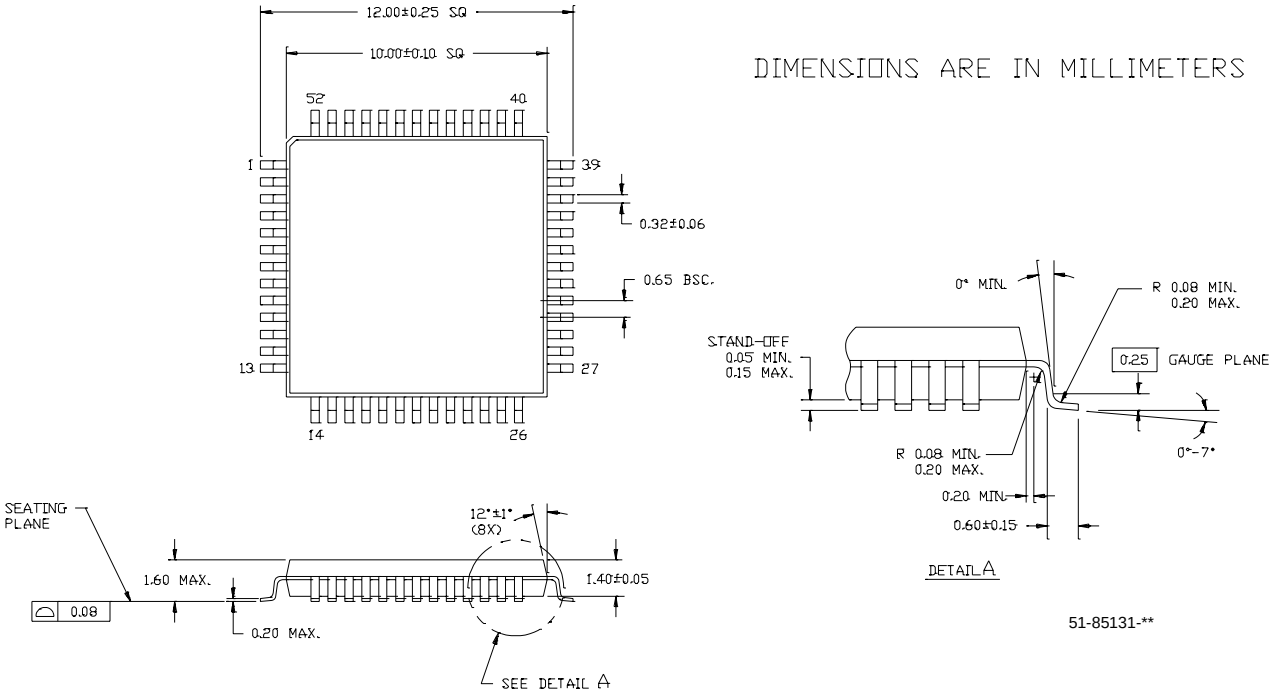
Note: All buffer outputs are tied to a common 3.3-Volt V_{DD} (V_{DD}*) for testing purposes

Ordering Information

Part Number	Package Type	Production Flow
IMIZ9974CA	52-pin TQFP	Industrial, –40°C to +85°C
IMIZ9974CAT	52-pin TQFP–Tape and Reel	Industrial, –40°C to +85°C

Package Drawing and Dimensions

52-Lead Thin Plastic Quad Flat Pack (10x10x1.4 mm) A52



Document Title: Z9974 3.3V, 125-MHz, Multi-Output Zero Delay Buffer Document #: 38-07090				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107126	06/05/01	IKA	Converted to IMI Cypress Spec
*A	108068	07/03/01	NDP	Changed Commercial to Industrial
*B	116195	08/14/02	ITH	Converted from Word to Framemaker Corrected TCLK0 & TCLK1 on schematic to match the Pull-up/down in the pin description Corrected PLL_EN in the pin description. Corrected the package drawing and dimension
*C	122775	12/21/02	RBI	Add power up requirements to maximum ratings information.