ST70235A

ASCOT™ DMT TRANSCEIVER

PRELIMINARY DATA

- DMT MODEM FOR CPE ADSL, COMPATIBLE WITH THE FOLLOWING STANDARDS:
  - ANSI T1.413 ISSUE 2
  - ITU-T G.992.1 (G.DMT)
  - ITU-T G.992.2 (G.LITE)
- SUPPORTS EITHER ATM (UTOPIA LEVEL 1 & 2) OR BITSTREAM INTERFACE
- 16 BIT MULTIPLEXED MICROPROCESSOR INTERFACE (LITTLE AND BIG ENDIAN COMPATIBILITY)
- ANALOG FRONT END MANAGEMENT
- DUAL LATENCY PATHS: FAST AND INTERLEAVED
- ATM'S PHY LAYER: CELL PROCESSING (CELL DELINEATION, CELL INSERTION, HEC)
- ADSL'S OVERHEAD MANAGEMENT
- REED SOLOMON ENCODE/DECODE
- TRELLIS ENCODE/DECODE (VITERBI)
- DMT MAPPING / DEMAPPING OVER 256 CARRIERS
- FINE (2PPM) TIMING RECOVER USING ROTOR AND ADAPTATIVE FREQUENCY DOMAIN EQUALIZING
- TIME DOMAIN EQUALIZATION
- FRONT END DIGITAL FILTERS
- 0.25µm HCMOS7 TECHNOLOGY
- 144 PIN TQFP
- POWER CONSUMPTION: 0.4 WATT

APPLICATIONS

Routers at SOHO, stand-alone modems, PC modems.

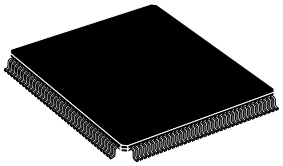
GENERAL DESCRIPTION

The ST70235A is the DMT modem and ATM framer of the STMicroelectronics ASCOT™ chipset. When coupled with ST70134 analog front-end and an external controller running dedicated firmware, the product fulfills ANSI T1.413 "Issue 2" DMT ADSL specification. The chip supports UTOPIA level 1 and UTOPIA level 2 interface.

The ST70235A can be split up into two different sections. The physical one performs the DMT modulation, demodulation, Reed-Solomon encoding, bit interleaving and 4D trellis coding.

The ATM section embodies framing functions for the generic and ATM Transmission Convergence (TC) layers. The generic TC consists of data scrambling and Reed Solomon error corrections, with and without interleaving.

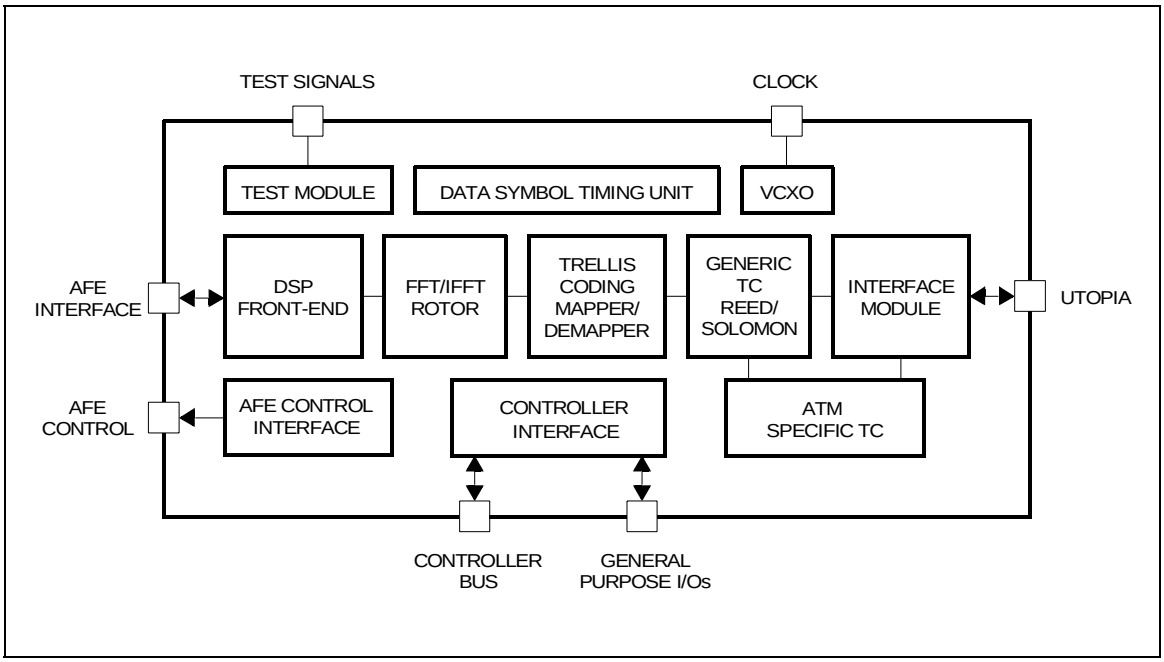
The ST70235A is controlled and programmed by an external controller (ADSL Transceiver Controller, ATC) that sets the programmable coefficients. The firmware controls the initialization phase and carries out the consequent adaptation operations.



TQFP144 Full Plastic
(20 x 20 x 1.40 mm)

ORDER CODE: ST70235A

Figure 1 : Block Diagram



Transient Energy Capabilities

ESD (Electronic Discharged) tests have been performed for the Human Body Model (HBM) and for the Charged Device Model (CDM).

The pins of the device are to be able to withstand minimum 2000V for the HBM and minimum 250V for CDM.

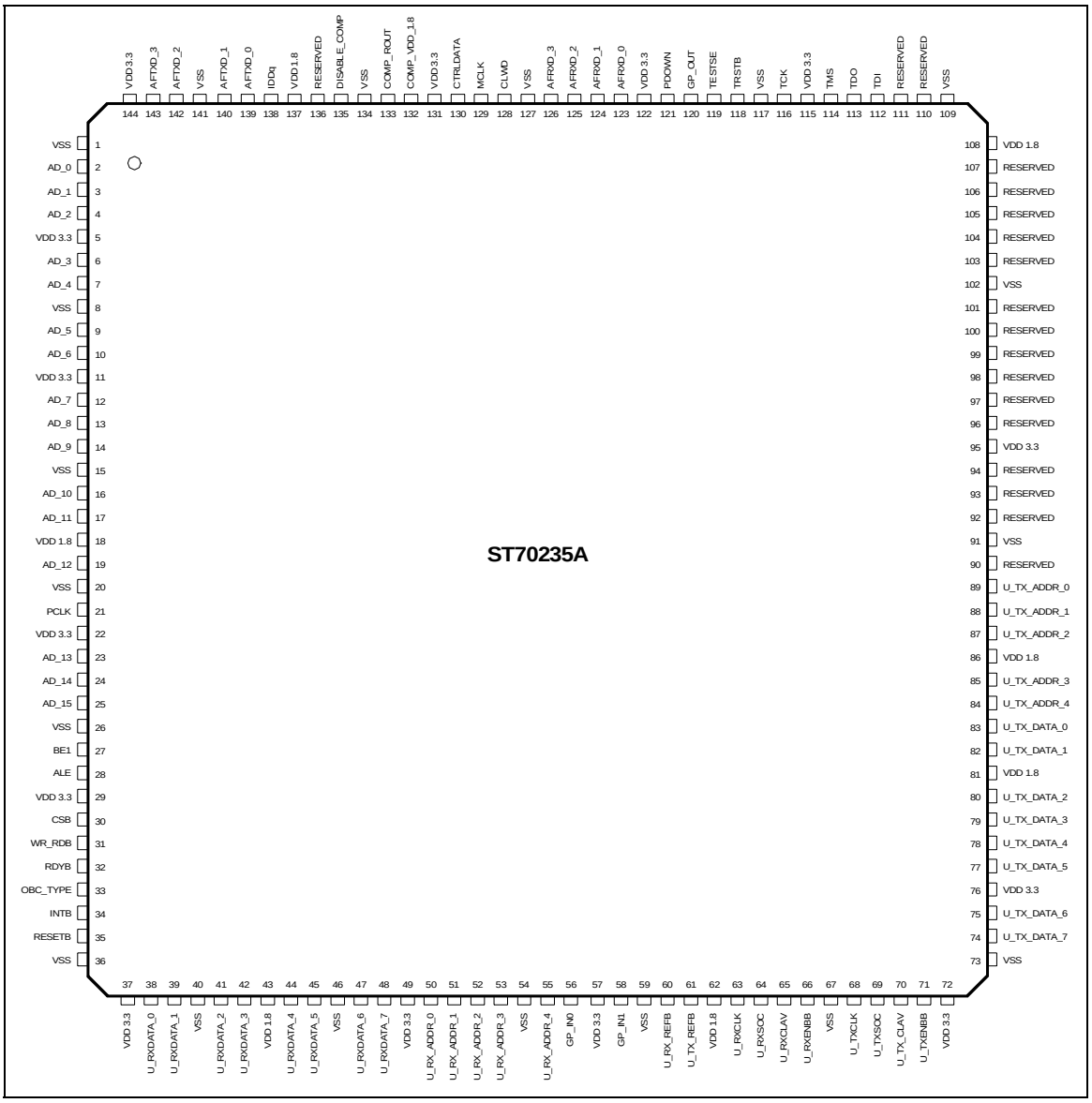
Latch-up

The maximum sink or source current from any pin is limited to 200mA to prevent latch-up.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD} 3.3	Supply Voltage	3.0	3.3	3.6	V
V_{DD} 1.8	Supply Voltage	1.62	1.8	1.98	V
P_{tot}	Total Power Dissipation		300	400	mW
T_{amb}	Ambient Temperature 1m/s airflow	0		70	°C
R_{th} J/A	Thermal Resistivity		38		°C/W
$I_{3.3}$	Current Consumption			14	mA
$I_{1.8}$	Current Consumption			135	mA

Figure 2 : Pin Connection



PIN FUNCTIONS

Pin	Name	Type	PAD Type HCMOS7	BS	Function
1	VSS				0V Ground
2	AD_0	B	BD8STARP	B	Data 0
3	AD_1	B	BD8STARP	B	Data 1
4	AD_2	B	BD8STARP	B	Address / Data 2
5	VDD 3.3				(VSS + 3.3V) Power Supply
6	AD_3	B	BD8STARP	B	Address / Data 3
7	AD_4	B	BD8STARP	B	Address / Data 4
8	VSS				0V Ground
9	AD_5	B	BD8STARP	B	Address / Data 5
10	AD_6	B	BD8STARP	B	Address / Data 6
11	VDD 3.3				(VSS + 3.3V) Power Supply
12	AD_7	B	BD8STARP	B	Address / Data 7
13	AD_8	B	BD8STARP	B	Address / Data 8
14	AD_9	B	BD8STARP	B	Address / Data 9
15	VSS				0V Ground
16	AD_10	B	BD8STARP	B	Address / Data 10
17	AD_11	B	BD8STARP	B	Address / Data 11
18	VDD 1.8				(VSS + 1.8V) Power Supply
19	AD_12	B	BD8STARP	B	Address / Data 12
20	VSS				0V Ground
21	PCLK	I	TLCHT	I	Processor clock
22	VDD 3.3				(VSS + 3.3V) Power Supply
23	AD_13	B	BD8STARP	B	Address / Data 13
24	AD_14	B	BD8STARP	B	Address / Data 14
25	AD_15	B	BD8STARP	B	Address / Data 15
26	VSS				0V Ground
27	BE1	I	TLCHT	I	Address 1
28	ALE	I	TLCHT	C	Address Latch
29	VDD 3.3				(VSS + 3.3V) Power Supply
30	CSB	I	TLCHT	I	Chip Select
31	WR_RDB	I	TLCHT	I	Specifies the direction of the access cycle
32	RDYB	OZ	BD4STARP	O	Controls the ATC bus cycle termination
33	OBC_TYPE	I-PD	TLCHTDQ	I	ATC Mode Selection (0 = i960; 1 = generic)
34	INTB	O	BD4STARP	O	Requests ATC interrupt service
35	RESETB	I	TLCHT	I	Hard reset
36	VSS				0V Ground
37	VDD 3.3				(VSS + 3.3V) Power Supply
38	U_RxData_0	OZ	BD8STARP	B	Utopia RX Data 0
39	U_RxData_1	OZ	BD8STARP	B	Utopia RX Data 1
40	VSS				0V Ground

PIN FUNCTIONS (continued)

Pin	Name	Type	PAD Type HCMOS7	BS	Function
41	U_RxData_2	OZ	BD8STARP	B	Utopia RX Data 2
42	U_RxData_3	OZ	BD8STARP	B	Utopia RX Data 3
43	VDD 1.8				(VSS + 1.8V) Power Supply
44	U_RxData_4	OZ	BD8STARP	B	Utopia RX Data 4
45	U_RxData_5	OZ	BD8STARP	B	Utopia RX Data 5
46	VSS				0V Ground
47	U_RxData_6	OZ	BD8STARP	B	Utopia RX Data 6
48	U_RxData_7	OZ	BD8STARP	B	Utopia RX Data 7
49	VDD 3.3				(VSS + 3.3V) Power Supply
50	U_RxADDR_0	I	TLCHT	I	Utopia RX Address 0
51	U_RxADDR_1	I	TLCHT	I	Utopia RX Address 1
52	U_RxADDR_2	I	TLCHT	I	Utopia RX Address 2
53	U_RxADDR_3	I	TLCHT	I	Utopia RX Address 3
54	VSS				0V Ground
55	U_RxADDR_4	I	TLCHT	I	Utopia RX Address 4
56	GP_IN_0	I-PD	TLCHTDQ	I	General purpose input 0
57	VDD 3.3				(VSS + 3.3V) Power Supply
58	GP_IN_1	I-PD	TLCHTDQ	I	General purpose input 1
59	VSS				0V Ground
60	U_RxRefB	O	BD4STARP	O	8kHz clock to ATM device
61	U_TxRefB	I	TLCHT	I	8kHz clock from ATM device
62	VDD 1.8				(VSS + 1.8V) Power Supply
63	U_Rx_CLK	I	TLCHT		Utopia RX Clock
64	U_Rx_SOC	OZ	BD8STARP		Utopia RX Start of Cell
65	U_RxCLAV	OZ	BD8STARP		Utopia RX Cell Available
66	U_RxENBB	I	TLCHT		Utopia RX Enable
67	VSS				0V Ground
68	U_Tx_CLK	I	TLCHT		Utopia TX Clock
69	U_Tx_SOC	I	TLCHT		Utopia TX Start of Cell
70	U_TxCLAV	OZ	BD8SCR		Utopia TX Cell Available
71	U_TxENBB	I	TLCHT		Utopia TX Enable
72	VDD 3.3				(VSS + 3.3V) Power Supply
73	VSS				0V Ground
74	U_TxData_7	I	TLCHT	I	Utopia TX Data 7
75	U_TxData_6	I	TLCHT	I	Utopia TX Data 6
76	VDD 3.3				(VSS + 3.3V) Power Supply
77	U_TxData_5	I	TLCHT	I	Utopia TX Data 5
78	U_TxData_4	I	TLCHT	I	Utopia TX Data 4
79	U_TxData_3	I	TLCHT	I	Utopia TX Data 3
80	U_TxData_2	I	TLCHT	I	Utopia TX Data 2

PIN FUNCTIONS (continued)

Pin	Name	Type	PAD Type HCMOS7	BS	Function
81	VDD 1.8				(VSS + 1.8V) Power Supply
82	U_TxData_1	I	TLCHT	I	Utopia TX Data 1
83	U_TxData_0	I	TLCHT	I	Utopia TX Data 0
84	U_TxADDR_4	I	TLCHT	I	Utopia TX Address 4
85	U_TxADDR_3	I	TLCHT	I	Utopia TX Address 3
86	VDD 1.8				(VSS + 1.8V) Power Supply
87	U_TxADDR_2	I	TLCHT	I	Utopia TX Address 2
88	U_TxADDR_1	I	TLCHT	I	Utopia TX Address 1
89	U_TxADDR_0	I	TLCHT	I	Utopia TX Address 0
90	RESERVED		BD4STARP		Reserved 0
91	VSS				0V Ground
92	RESERVED		BD4STARP		Reserved 1
93	RESERVED		BD4STARP		Reserved 2
94	RESERVED		BD4STARP		Reserved 3
95	VDD 3.3				(VSS + 3.3V) Power Supply
96	RESERVED		BD4STARP		Reserved 4
97	RESERVED		BD4STARP		Reserved 5
98	RESERVED		BD4STARP		Reserved 6
99	RESERVED		BD4STARP		Reserved 7
100	RESERVED		BD4STARP		Reserved 8
101	RESERVED		BD4STARP		Reserved 9
102	VSS				0V Ground
103	RESERVED		TLCHTDQ		Reserved 10
104	RESERVED		TLCHTDQ		Reserved 11
105	RESERVED		TLCHTDQ		Reserved 12
106	RESERVED		TLCHTDQ		Reserved 13
107	RESERVED		BD4STARP		Reserved 14
108	VDD 1.8				(VSS + 1.8V) Power Supply
109	VSS				0V Ground
110	RESERVED		BD4STARP		Reserved 15
111	RESERVED		BD4STARP		Reserved 16
112	TDI	I-PU	TLCHTUQ		JTAG I/P
113	TDO	OZ	BD4STARP		JTAG O/P
114	TMS	I-PU	TLCHTUQ		JTAG Made Select
115	VDD 3.3				(VSS + 3.3V) Power Supply
116	TCK	I-PD	TLCHTDQ		JTAG Clock
117	VSS				0V Ground
118	TRSTB	I-PD	TLCHTDQ		JTAG Reset
119	TESTSE	I	TLCHTDQ	none	Enables scan test mode
120	GP_OUT	O	BD8STARP	O	General purpose output

PIN FUNCTIONS (continued)

Pin	Name	Type	PAD Type HCMOS7	BS	Function
121	PDOWN	O	BD4STARP	O	Power down analog front end (Reset)
122	VDD 3.3				(VSS + 3.3V) Power Supply
123	AFRXD_0	I	TLCHT	I	Receive data nibble
124	AFRXD_1	I	TLCHT	I	Receive data nibble
125	AFRXD_2	I	TLCHT	I	Receive data nibble
126	AFRXD_3	I	TLCHT	I	Receive data nibble
127	VSS				0V Ground
128	CLWD	I	TLCHT	I	Start of word indication
129	MCLK	I	TLCHT	C	Master clock
130	CTRLDATA	O	BD4STARP	O	Serial data Transmit channel
131	VDD 3.3				(VSS + 3.3V) Power Supply
132	COMP_VDD_1.8		COMP_1V60		Compensation Cell VDD 1.8V (see note 1)
133	COMP_ROUT	O	COMP_1V60	none	Compensation Cell Resistor (see note 1)
134	VSS		COMP_1V60		0V Ground
135	DISABLE_COMP	I	TLCHTDQ		Disable Compensation Cell (see note 1)
136	RESERVED				Reserved
137	VDD 1.8				(VSS + 1.8V) Power Supply
138	IDDq	I	TLCHT	none	Test pin, active high
139	AFTXD_0	O	BD8STARP	O	Transmit data nibble
140	AFTXD_1	O	BD8STARP	O	Transmit data nibble
141	VSS				0V Ground
142	AFTXD_2	O	BD8STARP	O	Transmit data nibble
143	AFTXD_3	O	BD8STARP	O	Transmit data nibble
144	VDD 3.3				(VSS + 3.3V) Power Supply

Note: Compensation cell - The COMP_OUT pin must be connected at GND by a 100KΩ resistor on board.
Specifications of the resistor have to meet the following requirements:
± 5% allowed on the value, ±1% is preferred.
Advice is given to place the resistor so that there will be the shortest path between it and the pin.
Using the DISABLE_COMP signal is possible to disable the slew rate control of IOs, in this mode the IOs are however still functional, but dynamic performances are affected.
An internal pull-down on DISABLE_COMP pin enables the slew rate control of IOs, an external pull-up resistor (connected at 3.3V) must be inserted in order to disable the slew rate control.

Table 1 : I/O Driver Function

Driver	Function
BD4STARP	TTL Three Volt capable Schmitt Trigger Bidirectional Pad Buffer, 4mA, with Test pins, with Active Slew Rate Control
BD8STARP	TTL Three Volt capable Schmitt Trigger Bidirectional Pad Buffer, 8mA, with Test pins, with Active Slew Rate Control
TLCHTDQ	TTL Three Volt capable Input Buffer with Active Pull-Down and Test pin
TLCHTUQ	TTL Three Volt capable Input Buffer with Active Pull-Up and Test pin
TLCHT	TLL Three Volt capable Input Pad Buffer

PIN SUMMARY

Mnemonic	Type	BS Type	Number of Signals	Function
Power Supply				
VDD 3.3 VDD 1.8				(VSS + 3.3V) Power supply (VSS + 1.8V) Power supply
VSS				0V Ground
ATC INTERFACE				
ALE	I	C	1	Used to latch the address of the internal register to be accessed
PCLK	I	I	1	Processor clock
CSB	I	I	1	Chip selected to respond to bus cycle
BE1	I	I	1	Address 1 (not multiplexed)
WR_RDB	I	I	1	Specifies the direction of the access cycle
RDYB	OZ	O	1	Controls the ATC bus cycle termination
INTB	O	O	1	Requests ATC interrupt service
AD	IO	B	16	Multiplexed Address/Data bus
OBC_TYPE	I-PD	I	1	Select between i960 (0) or generic (1) controller interface
TEST ACCESS PART INTERFACE				
TDI	I-PU		1	Refer to section
TDO	OZ		1	
TCK	I-PD		1	
TMS	I-PU		1	
TRSTB	I-PD		1	
ANALOG FRONT END INTERFACE				
AFRXD	I	I	4	Receive data nibble
AFTXD	O	O	4	Transmit data nibble
CLWD	I	I	1	Start of word indication
PDOWN	O	O	1	Power down analog front end
CTRLDATA	O	O	1	Serial data transmit channel
MCLK	I	C	1	Master cloc
ATM UTOPIA INTERFACE				
U_RxData	OZ	B	8	Receive interface Data
U_TxData	I	I	8	Transmit interface Data
U_RxADDR	I	I	5	Receive interface Address
U_TxADDR	I	I	5	Transmit interface Address
U_RxCLAV	OZ	O	1	Receive interface Cell Available
U_TxCLAV	OZ	O	1	Transmit interface Cell Available
U_RxENBB	I-TTL	I	1	Receive interface Enable
U_TxENBB	I-TTL	I	1	Transmit interface Enable
U_RxSOC	OZ	O	1	Receive interface Start of Cell
U_TxSOC	I-TTL	I	1	Transmit interface Start of Cell
U_RxCLK	I-TTL	C	1	Receive interface Utopia Clock
U_TxCLK	I-TTL	C	1	Transmit interface Utopia Clock
U_RxRefB	O	O	1	8kHz reference clock to ATM device
U_TxRefB	I-TTL	I	1	8kHz reference clock from ATM device

PIN SUMMARY (continued)

Mnemonic	Type	BS Type	Number of Signals	Function
MISCELLANEOUS				
GP_IN	I-PD	I	2	General purpose input
GP_OUT	O	O	1	General purpose output
RESETB	I	I	I	Hard reset
TESTSE	I	none	none	Enable scan test mode
IDDq	I	none	none	Test pin, active high
COMP_ROUT	O	none	1	Compensation cell resistor
DISABLE_COMP	I-PD	I	1	Disable compensation cell

I = Input, CMOS levels
I-PU = Input with pull-up resistance, TTL levels
I-PD = Input with pull-down resistance, TTL levels
I-TTL = Input TTL levels
O = Push-pull output
OZ = Push-pull output with high-impedance state
IO = Input / Tristate Push-pull output
BS cell = Boundary-Scan cell
I = Input cell
O = Output cell
B = Bidirectional cell
C = Clock

Main Block Description

The following drawings describe the sequence of functions performed by the chip.

DSP Front-End

The DSP Front-End contains 4 parts in the receive direction: the Input Selector, the Analog Front-End Interface, the Decimator and the Time Equalizer.

The input selector is used internally to enable test loopbacks inside the chip. The Analog Front-End Interface transfers 16-bit words, multiplexed on 4 input/output signals. Word transfer is carried out in 4 clock cycles.

The Decimator receives 16-bit samples at 8.8MHz (as sent by the Analog Front-End chip: ST70134) and reduces this rate to 2.2MHz.

The Time Equalizer (TEQ) module is a FIR filter with programmable coefficients. Its main purpose is to reduce the effect of Inter-Symbol Interferences (ISI) by shortening the channel impulse response.

Both the Decimator and TEQ can be bypassed. In the transmit direction, the DSP Front-End includes: sidelobe filtering, clipping, delay equalization and interpolation. The sidelobe filtering and delay equalization are implemented by IIR Filters, reducing the effect of echo in FDM systems.

Clipping is a statistical process limiting the amplitude of the output signal, optimizing the dynamic range of the AFE. The interpolator receives data at 2.2MHz and generates samples at a rate of 8.8MHz.

DMT Modem

This module is a programmable DSP unit. Its instruction set enables the basic functions of the DMT algorithm like FFT, IFFT, Scaling, Rotor and Frequency Equalization (FEQ) in compliance with ANSI T1.413 specifications.

In the RX path, the 512-point FFT transforms the time-domain DMT symbol into a frequency domain representation which can be further decoded by the subsequent demapping stages.

In other words, the Fast Fourier Transform process is used to transform from time domain to frequency domain (receive path). 1024 time samples are processed. After the first stage time domain equalization and FFT block an ICI (InterCarrier Interference) free information stream turns out.

Figure 3 : DSP Front-End Receive

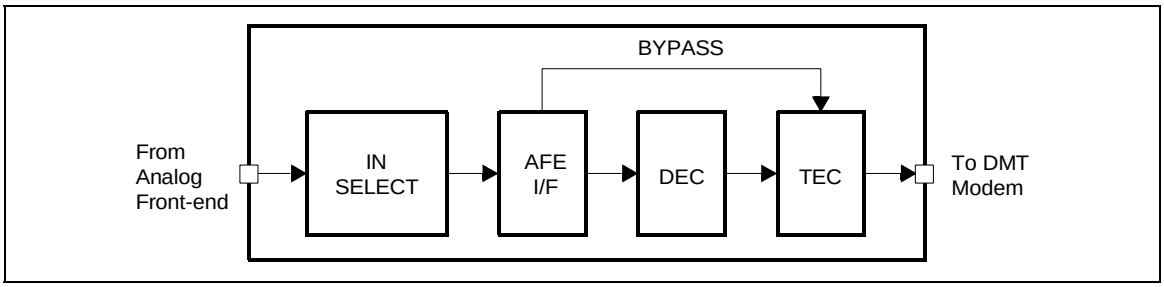


Figure 4 : DSP Front-End Transmit

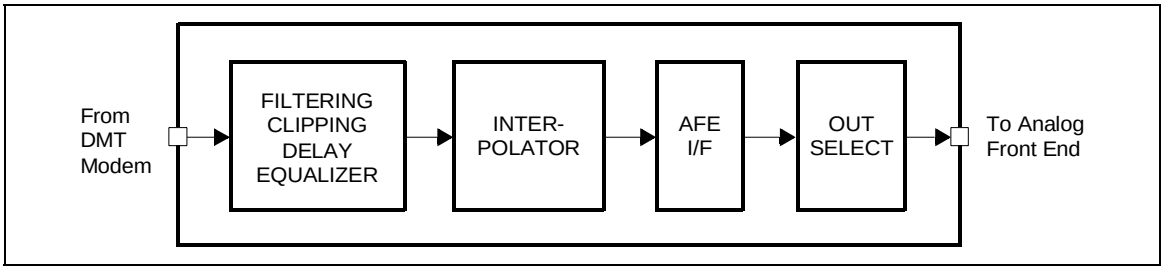
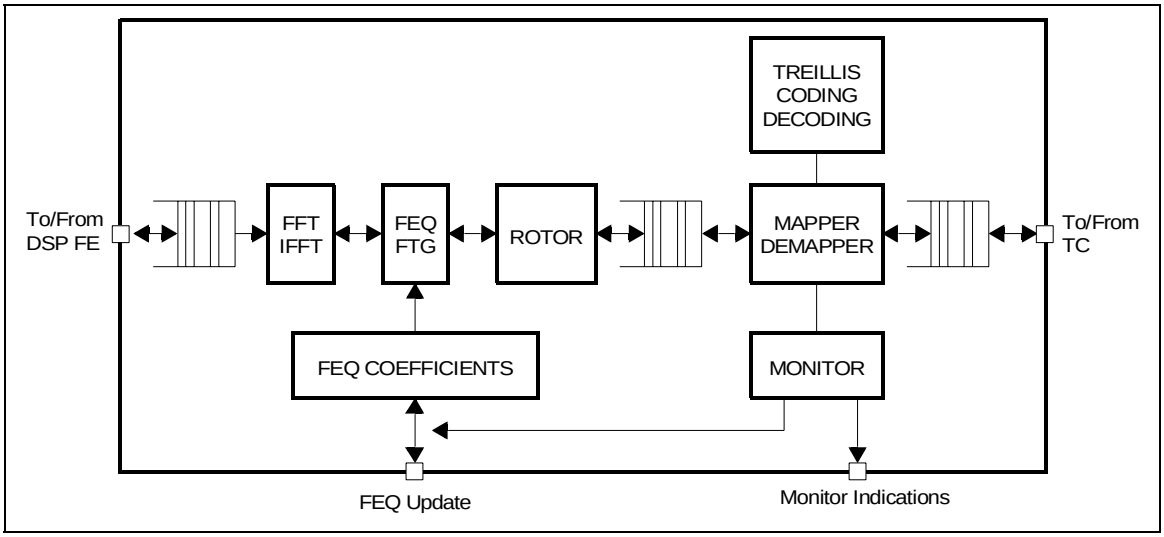


Figure 5 : DMT Modem (Rx & Tx)



This stream is still affected by carrier specific channel distortion resulting in an attenuation of the signal amplitude and a rotation of the signal phase. To compensate, a Frequency domain equalizer (FEQ) and a Rotor (phase shifter) are implemented. The frequency domain equalization performs an operation on the received vector in order to match it with the associated point in the constellation. The coefficient used to perform the equalization are floating point, and may be updated by hardware or software, using a mechanism of active and inactive table to avoid DMT synchro problems.In the transmit path, the IFFT reverses the DMT symbol from frequency domain to time domain.

The IFFT block is preceded by Fine Tune Gain (FTG) and Rotor stages, allowing for a compensation of the possible frequency mismatch between the master clock frequency and the transmitter clock frequency (which may be locked to another reference).

The Inverse Fast Fourier Transform process is used to transform from frequency domain to time domain (transmit path). 256 positive frequencies are processed, giving 512 samples in the time domain.

The FFT module is a slave DSP engine controlled by the firmware running on an external controller. It works off line and communicates with other blocks through buffers controlled by the "Data Symbol Timing Unit". The DSP executes a program stored in a RAM area, which constitutes a flexible element that allows for future system enhancements.

DPLL

The Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at the ends (transmitter and receiver) do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. Various processes can use this estimate to deal with the frequency mismatch.

In particular, small accumulated phase error can be compensated in the frequency domain by a rotation of the received code constellation (Rotor). Larger errors are compensated in the time domain by inserting or deleting clock cycles in the sample input sequence.

Eventually that leads to achieve less than 2ppm between the two ends.

Mapper/Demapper, Monitor, Trellis Coding, FEQ Update

The Demapper converts the constellation points computed by the FFT to a block of bits. This means to identify a point in a 2D QAM constellation plane. The Demapper supports Trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the Trellis is active, the Demapper receives an indication for the most likely constellation subset to be used.

In the transmit direction, the mapper receives a bit stream from the Trellis encoder and modulates the bit stream on a set of carriers (up to 256). It generates coordinates for 2n QAM constellation, where n < 15 for all carriers.

The Mapper performs the inverse operation, mapping a block of bits into one constellation point (in a complex x+jy representation) which is passed to the IFFT block. The Trellis Encoder generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme.

This feature can be disabled.The Monitor computes error parameters for carriers specified in the Demapper process. Those parameters can be used for updates of adaptive filters coefficients, clock phase adjustments, error detection, etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame, etc.

Generic TC Layer Functions

These functions relate to byte oriented data streams. They are completely described in ANSI T 1.4 13. Additions described in the Issue 2 of this specification are also supported.

The data received from the demapper may be split into two paths, one dedicated to an interleaved data flow the other one for a fast data flow. No external RAM is needed for the interleaved path.

The interleaving/deinterleaving is used to increase the error correcting capability of block codes for error bursts.

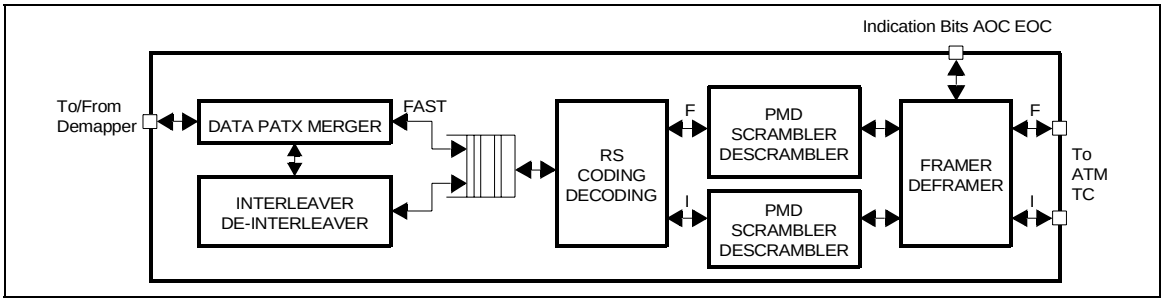
After deinterleaving (if applicable), the data flow enters a Reed-Solomon error correcting code decoder, able to correct a number of bytes containing bit errors.

The decoder also uses the information of previous receiving stages that may have detected the error bytes and have labelled them with an "erasure indication". Each time the RS decoder detects and corrects errors in a RS codeword, an RS correction event is generated.

The occurrence of such events can be signalled to the management layer.After the RS decoder, the corrected byte stream is descrambled in the PMD (Physical Medium Dependent) descramblers. Two descramblers are used, for interleaved and non-interleaved data flows. These are defined in ANSI T1.413. After descrambling, the data flows enter the Deframer that extracts and processes bytes to support Physical layer related functions according to ANSI T1.413. The ADSL frames indeed contain physical layer-related information in addition to the data passed to the higher layers. In particular, the deframer extracts the EOC (Embedded Operations Channel), the AOC (ADSL Overhead Control) and the indicators bits and passes them to the appropriate processing unit (e.g. the transceiver controller). The deframer also performs a CRC check (Cyclic Redundancy Check) on the received frame and generates events in case of error detection.Event counters can be read by management processes.

The outputs of the deframer are an interleaved and a fast data streams. These data streams can either carry ATM cells or another type of traffic. In the latter case, the ATM specific TC layer functional block, described hereafter, is bypassed and the data stream is directly presented at the input of the interface module.

Figure 6 : Generic TC Layer Functions



ATM Specific TC Layer Functions

The 2 bytes streams (fast and slow) are received from the byte-based processing unit. When ATM cells are transported, this block provides basic cell functions such as cell synchronization, cell payload descrambling, idle/unassigned cell filter, cell Header Error Correction (HEC) and detection.

The cell processing happens according to ITU-T I.163 standard. Provision is also made for BER measurements at this ATM cell level. When non cell oriented byte streams are transported, the cell processing unit is not active. The interface module collects cells (from the cell-based function module). Cells are stored in FIFO's (424 bytes or 8 cell wide, transmit buffers have the same size), from which they are extracted by 2 interface submodules, one providing a Utopia level 1 interface and the other a Utopia level 2 interface.

Figure 7 : ATM Specific TC Layer Functions

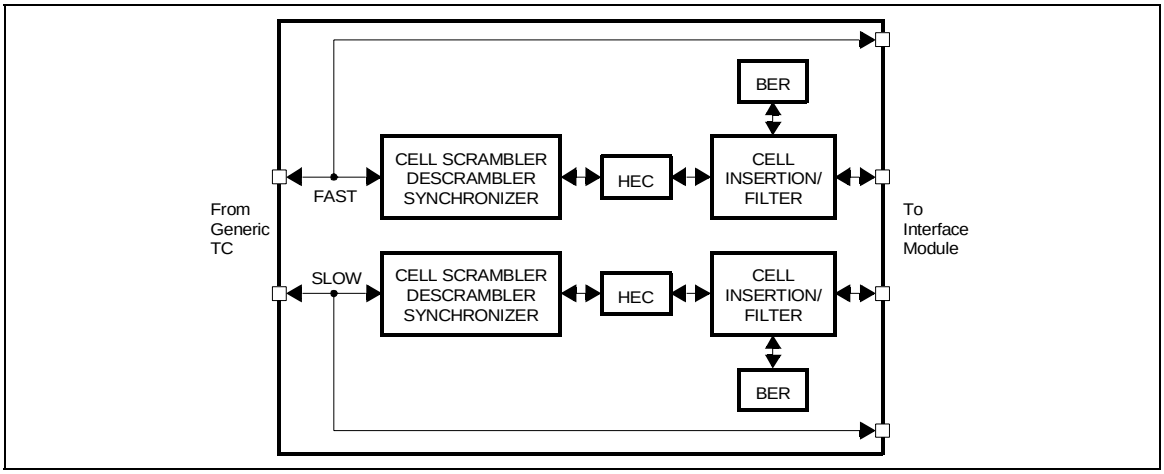
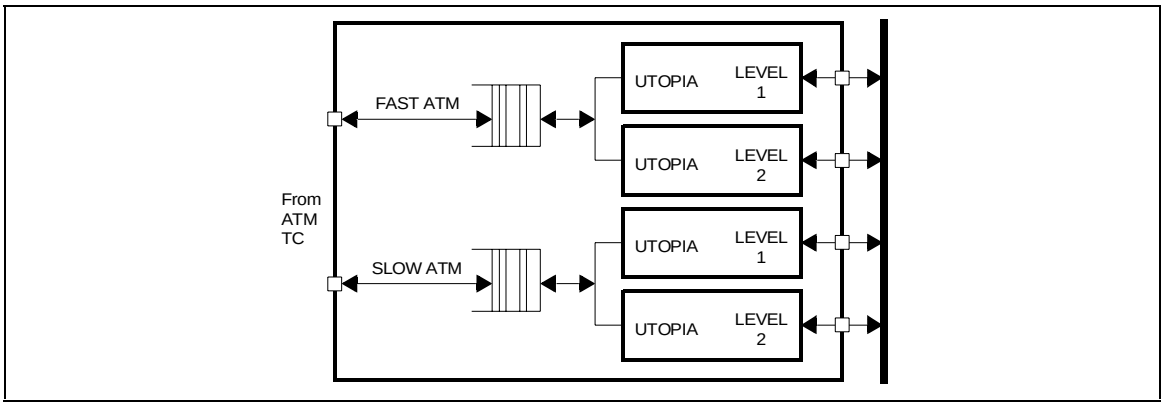


Figure 8 : Interface Module



DMT Symbol Timing Unit (DSTU)

The DSTU interfaces with various modules, like DSP FrontEnd, FFT/IFFT, Mapper/Demapper, RS, Monitor and Transceiver Controller. It consists of a real time and a scheduler modules.

The real time unit generates a timebase for the DMT symbols (sample counter), superframes (symbol counter) and hyper-frames (sync counter). The timebases can be modified by various control features. They are continuously fine-tuned by the DPLL module.

The DSTU schedulers execute a program, controlled by program opcodes and a set of variables, the most important of which are real time counters.

The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can be updated in real time.

ST70235A interfaces

Overview

See Figure 9.

Processor Interface (ATC)

The ST70235A is controlled and configured by an external processor across the processor interface. All programmable coefficients and parameters are loaded through this path.

Data and addresses are multiplexed

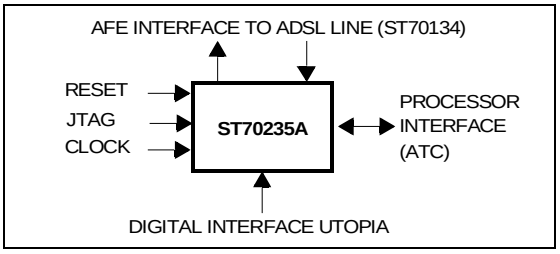
ST70235A works in 16 bits data access, so address bit 0 is not used. Address bit 1 is not multiplexed with data. It has its own pin : BE1.

Byte access are not supported. Access cycle read or write are always in 16 bits data wide, ie bit address A0 is always zero value.

The interrupt request pin to the processor is INTB, and is an Open Drain output.

The ST70235A supports both little and big endian. The default feature is big endian.

Figure 9 : ST70235A Interfaces



Generic Interface

This interface is suitable for a number of processors using a multiplexed Address/data bus. In this case, synchronization of the input signals with PCLK pin is not necessary.

Figure 10 : Generic Processor Interface Write Timing Cycle

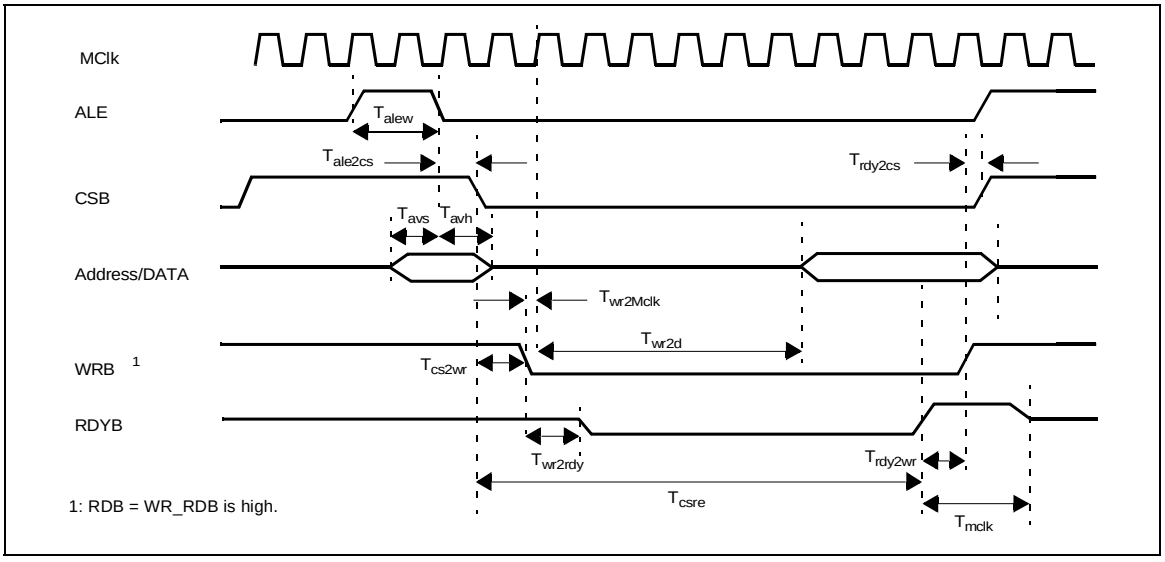
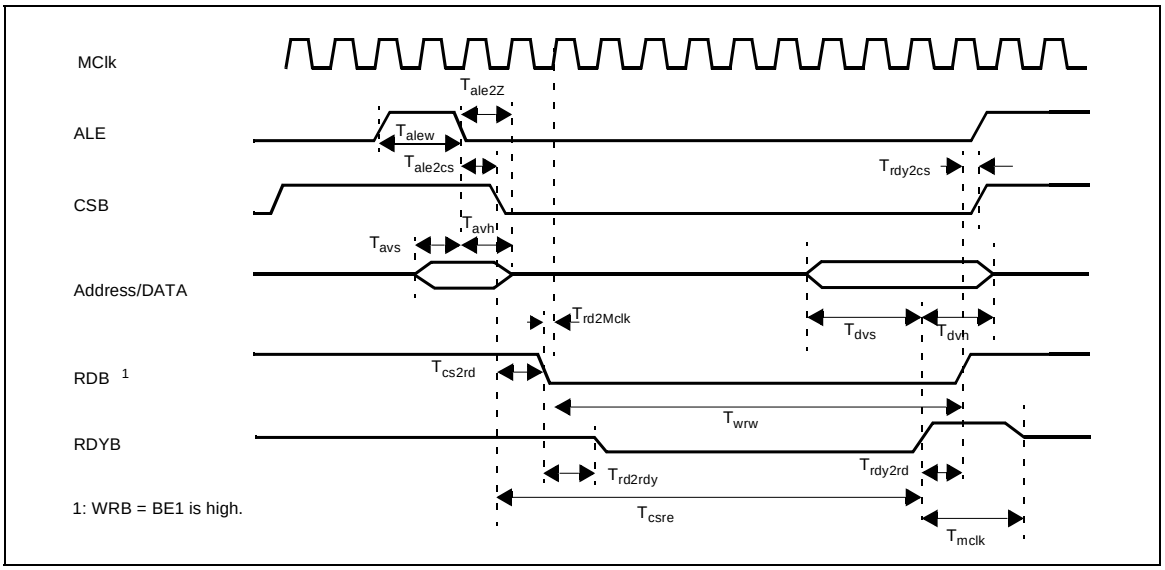


Figure 11 : Generic Processor Interface Read Timing Cycle



Generic processor interface Cycle Timing

All AC characteristics are indicated for a 100pF capacitive load.Cycle timing for generic interface.

Table 2 : Cycle timing

Symbol	Parameters	Minimum	Maximum	Unit
Tcsre	Access Time		900	µs
Talew	Ale pulse width	12		ns
Tavs	Address valid setup time	10		ns
Tavh	Address valid hold time	10		ns
Tale2cs	ALE to CSB	0		ns
Tale2Z	ALE to high Z state of bus		50	ns
Tcs2wr	CSB to WRB	0		ns
Tcs2rd	CSB to RDB	0		ns
Twr2d	WR to data		15	ns
Twr2rdy	WR to Dy asserted		60	ns
Trd2rdy	RD to Rdy asserted		60	ns
Trdy2wr	Rdyb to WRB	0		ns
Trdy2rd	Rdyb to RDB	0		ns
Tdvs	Data valid setup time	10		ns
Tdvh	Data valid hold time	1/2 Tmclk	Tmclk	ns
Trdy2cs	RdyB to CSB	0		ns
Tmclk	master clock timing : cf specifications			
Twr2Mclk	Setup time according to the master clock	10		ns
Trd2Mclk	Setup time according to the master clock	10		ns

The timing are generally presented with the write signal, but as shown on the read diagram, they are also valid for the read signal, so for example the Trdy2wr timing is the same as what can be Trdy2rd.

Generic Processor Interface Pins and Functional Description

Name	Type	Function
AD[0..15]	I/O	Multiplexed address / data bus
ALE	I	Address Latch Enable
RDB	I	Read cycle indication
WRB	I	Write cycle indication
CSB	I	Chip Select
RDYB	OZ	Bus cycle ready indication
INTB	O	Interrupt

Digital interface ATM or serial

Digital Interface for data to the loop before modulation and from the loop after demodulation.

This interface collects cells (from the cell based function module) or a byte stream (from the deframer).

Cells are stored in a fifo, 2 interfaces submodules can extract data from the fifo.

2 kinds of interface are allowed:

– Utopia Level 1

– Utopia Level 2

The interface selection is programmed by writing the Utopia PHY address register.

Only one interface can be enabled in a ST70235A configuration.

Utopia Level 1 supports only one PHY device. Utopia Level 2 supports multi-PHY devices (See Utopia Level 2 specifications).

Each buffer provides storage for 8 ATM cells (both directions for Fast and Interleaved channel).

The Utopia Level 2 supports point to multipoint configurations by introducing an addressing capability and by making distinction between polling and selecting a device.

Figure 12 : Receive Interface

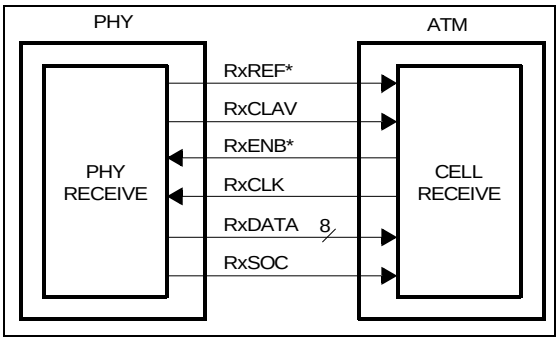
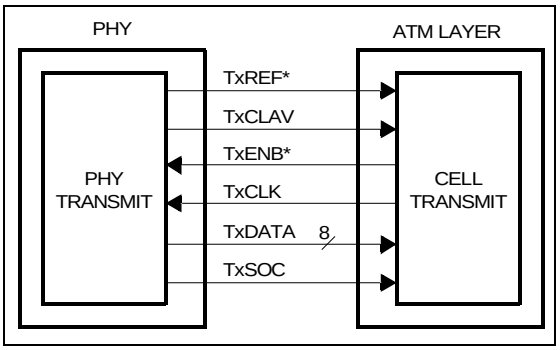


Figure 13 : Transmit Interface



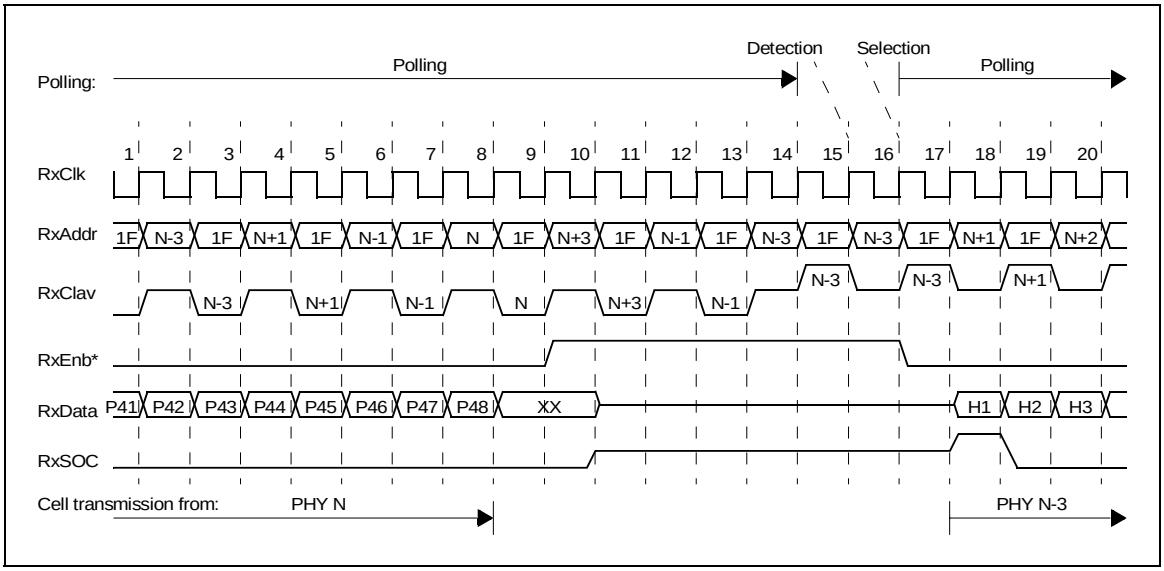
Utopia Level 1 Interface

The ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction. The direction from physical layer to ATM is the Receive direction.

Figures 12 & 13 show the interconnection between ATM and PHY layer devices, the optional signals are not supported and not shown. The Utopia interface transfers one byte in a single clock cycle, as a result cells are transformed in 53 clock cycles.

Both transmit and receive are synchronized on clocks generated by the ATM layer chip, and no specific relationship between receive and transmit clocks is required. In this mode, the ST70235A can only support one data flow : either interleaved or fast.

Figure 14 : Timing (Utopia 2 Receive Interface)



Pin Description

Name	Type	Meaning	Usage	Remark
RxClav	O	Receive Cell available	Signals to the ATM chip that the ST70235A has a cell ready for transfer	Remains active for the entire cell transfer
RxEnb [1]	I	Receive Enable	Signals to the ST70235A that the ATM chip will sample and accept data during next clock cycle	RxData and RxSOC could be tri-state when RxEnb* is inactive (high). Active low signal
RxClk	I	Receive Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
RxData	O	Receive Data (8bits)	ATM cell data, from ST70235A chip to ATM chip, byte wide. Rx Data [7] is the MSB.	
RxSOC	O	Receive Start Cell	Identifies the cell boundary on RxData	Indicate to the ATM layer chip that RxData contains the first valid byte of a cell
RxRef [1]	O	Reference Clock	8 kHz clock transported over the network	Active low signal

Note 1. Active low signal

When RxEnb is asserted, the ST70235A reads data from its internal fifo and presents it on RxData and RxSOC on each low-to-high transition of RxClk, ie the ATM layer chip samples all RxData and RxSOC on the rising edge of RxSOC on the rising edge of RxClk.

Pin Description

Name	Type	Meaning	Usage	Remark
TxClav	O	Transmit Cell available	Signals to the ATM chip that the physical layer chip is ready to accept a complete cell	Remains active for the entire cell transfer
TxEnb [1]	I	Transmit Enable	Signals to the ST70235A that TxData and TxSOC are valid	
TxClk	I	Transmit Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
TxData	I	Transmit Data (8bits)	ATM cell data, from ATM layer chip to ST70235A, byte wide. TxData [7] is the MSB.	
TxSOC	I	Transmit Start of Cell	Identifies the cell boundary on TxData	TxData contains the first valid byte of the cell.
TxRef [1]	I	Reference Clock	8kHz clock from the ATM layer chip	

Note 1. Active low signal

The ST70235A samples TxData and TxSOC signals on the rising edge of TxClk, if TxEnb is asserted.

TxClk, RxClk, AC Electrical Characteristics

Symbol	Parameters	Minimum	Maximum	Unit
F	Clock frequency	1.5	25	MHz
Tc	Clock duty cycle	40	60	%
Tj	Clock peak to peak jitter		5	%
Trf	Clock rise fall time		4	ns
L	Load		100	pF

TxData, TxSOC, TxAddr, TxEnb, AC Electrical Characteristics

Symbol	Parameters	Minimum	Maximum	Unit
T5	Input set-up time to TxClk	10		ns
T6	Hold time to TxClk	1		ns
L	Load		100	pF

Note: Tx data hold time is 1.2ns. All the UTOPIA hold time are guarantee by design.

RxData, RxSOC, RxClav, TxClav, AC Electrical Characteristics

Symbol	Parameters	Minimum	Maximum	Unit
T7	Input set-up time to TxClk	10		ns
T8	Hold time to Tx Clk	1		ns
T9	Signal going low impedance to RxClk	10		ns
T10	Signal going High impedance to RxClk	0		ns
T11	Signal going low impedance to RxClk	1		ns
T12	Signal going High impedance to RxClk	1		ns
L	Load		100	pF

RxAddr, RxEnb, AC Electrical Characteristics

Symbol	Parameters	Minimum	Maximum	Unit
T5	Input setup time to RxClk	10		ns
T6	Hold time to RxClk	1		ns
L	Load		100	pF

Figure 15 : Timing (Utopia 2 Transmit Interface)

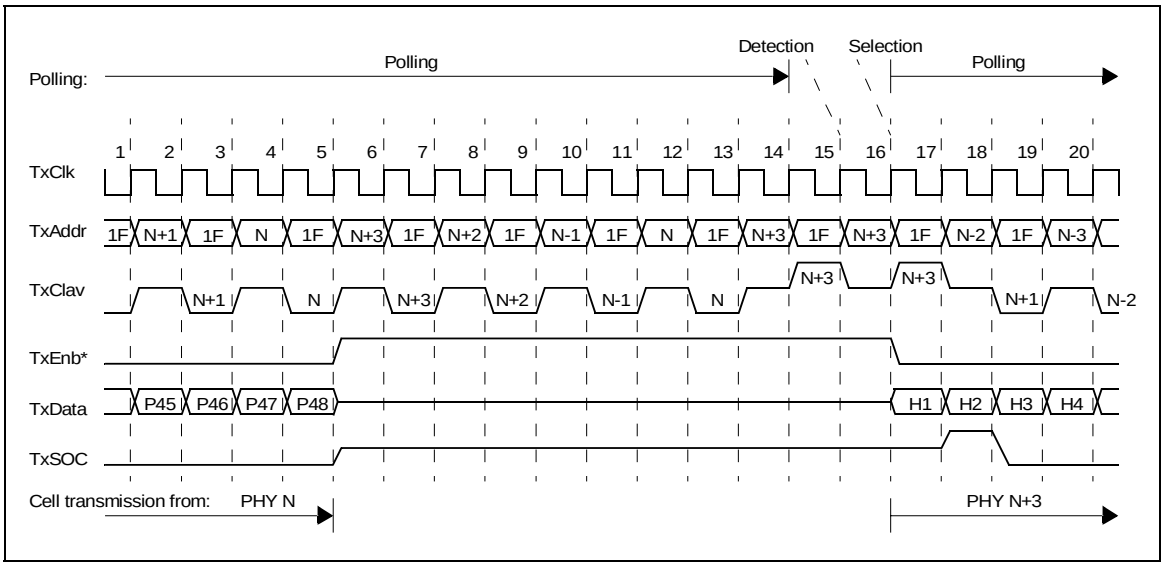
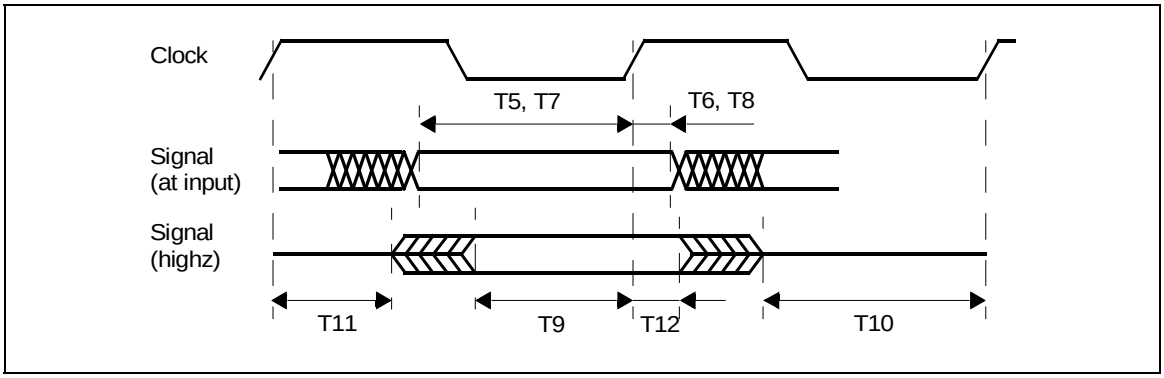


Figure 16 : Timing Specification (Utopia 2)



DIGITAL INTERFACE

Utopia Level 2 Interface

The ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction. The direction from physical layer to ATM is the Receive direction. Figure 17 shows the interconnection between ATM and PHY layer devices, the optional signals are not supported and not shown.

The UTOPIA interface transfers one byte in a single clock cycle, as a result cells are transferred in 53 clock cycles.Both transmit and receive interfaces are synchronized on clocks generated by the ATM layer chip, and no specific relationship between Receive and Transmit clock is assumed, they must be regarded as mutually asynchronous clocks. Flow control signals are available to match the bandwidth constraints of the physical layer and the ATM layer. The UTOPIA level 2 supports point to multipoint configurations by introducing on addressing capability and by making a distinction between polling and selecting a device:

– The ATM chip polls a specific physical layer chip by putting its address on the address bus when the Enb* line is asserted. The addressed physical layer answers the next cycle via the Clav line reflecting its status at that time.

– The ATM chip selects a specific physical layer by putting its address on the address bus when the Enb* line is deasserted and asserting the Enb* line on the next cycle. The addressed physical layer chip will be the target or source of the next cell transfer (see Figure 17).

Utopia Level 2 Signals

The physical chip sends cell data towards the ATM layer chip. The ATM layer chip polls the status of the fifo of the physical layer chip. The cell exchange proceeds like:

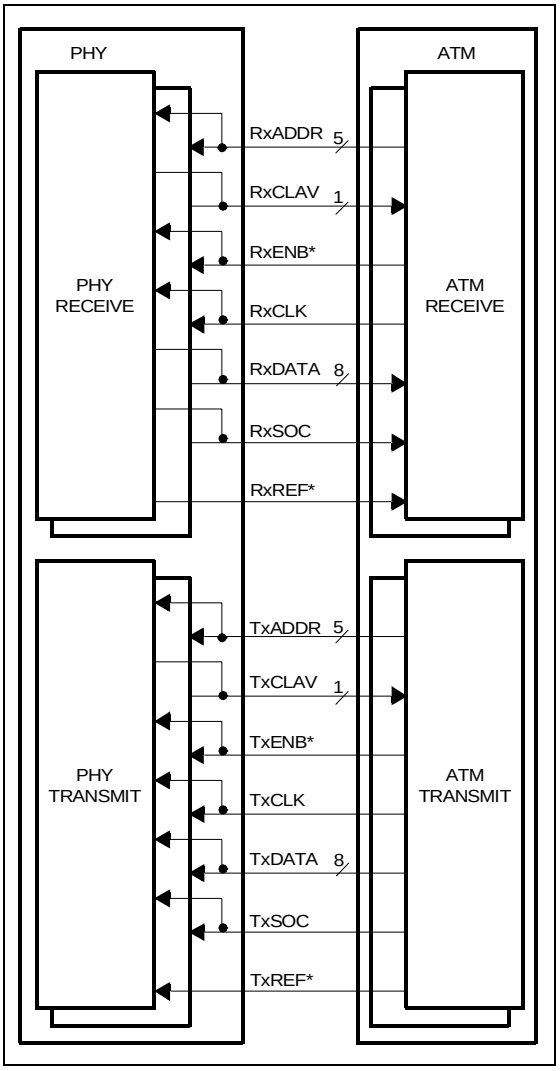
a) The physical layer chip signals the availability of a cell by asserting RxClav when polled by the ATM chip.

b) The ATM chips selects a physical layer chip, then starts the transfer by asserting RxEnb*.

c) If the physical layer chip has data to send, it puts them on the RxData line the cycle after it sampled RxEnb* active. It also advances the offset in the cell. If the data transferred is the first byte of a cell, RxSOC is 1b at the time of the data transfer, 0b otherwise.

d) The ATM chip accepts the data when they are available. If RxSOC was 1b during the transfer, it resets its internal offset pointer to the value 1, otherwise it advances the offset in the cell.

Figure 17 : Signal at Utopia Level 2 Interface



ST70235A Utopia Level 2 MPHY Operation

Utopia level 2 MPHY operation can be done by various interface schemes. The ST70235A supports only the required mode, this mode is referred to as "Operation with 1 TxClav and 1 RxClav".

PHY Device Identification

The ST70235A holds 2 PHY layer Utopia ports, one is dedicated to the fast data channel, the other one to the interleaved data channel. The associated PHY address is specified by the PHY_ADDR_x fields in the Utopia PHY address register.

Beware that an incorrect address configuration may lead to bus conflicts. A feature is defined to disable (tri-state) all outputs of the Utopia interface. It is enabled by the TRI_STATE_EN bit in the Rx_interface control register.

Pin Description Utopia 2 (Receive Interface)

Name	Type	Meaning	Usage	Remark
RxClav	O	Receive Cell available	Signals to the ATM chip that the STLC60135 has a cell ready for transfer	Remains active for the entire cell transfer
RxEnb*	I	Receive Enable	Signals to the physical layer that the ATM chip will sample and accept data during next clock cycle	RxData and RxSOC could be tri-state when RxEnb* is inactive (high)
RxClk	I	Receive Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
RxData	O	Receive Data (8 bits)	ATM cell data, from physical layer chip to ATM chip, byte wide.	
RxSOC	O	Receive Start Cell	Identifies the cell boundary on RxData	Indicate to the ATM layer chip that RxData contains the first valid byte of a cell.
RxAddr	I	Receive Address (5 bits)	Use to select the port that will be active or polled	
RxRef *	O	Reference Clock	8kHz clock transported over the network	

Note **Active low signal*

Pin Description Utopia 2 (Transmit interface)

Name	Type	Meaning	Usage	Remark
TxClav	O	Transmit Cell available	Signals to the ATM chip that the physical layer chip is ready to accept a cell	Remains active for the entire cell transfer
TxEnb*	I	Transmit Enable	Signals to the physical layer that TxData and TxSOC are valid	
TxClk	I	Transmit Byte Clock	Gives the timing signal for the transfer, generated by ATM layer chip.	
TxData	I	Transmit Data (8 bits)	ATM cell data, to physical layer chip to ATM chip, byte wide.	
TxSOC	I	Transmit Start of Cell	Identifies the cell boundary on TxData	
TxAddr	I	Transmit Address (5 bits)	Use to select the port that will be active or polled	
TxRef *	I	Reference Clock	8kHz clock from the ATM layer chip	

Note **Active low signal*

Analog Front End Control Interface

The Analog Front End Interface is designed to be connected to the ST70134 Analog Front End component.

Transmit Interface

The 16 bit words are multiplexed on 4 AFTXD output signals. As a result 4 cycles are needed to transfer 1 word. Refer to table 1 for the bit/pin allocation for the 4 cycles.

The first of 4 cycles is identified by the CLWD signal. Refer to Figure 18.

The ST70235A fetches the 16 bit word to be multiplexed on AFTXD from the Tx Digital Front-End module.

Receive Interface

The 16 bit receive word is multiplexed on 4 AFRXD input signals. As a result 4 cycles are needed to transfer 1 word.

Refer to Table 2 for the bit / pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD must repeat after 4 MCLK cycles.

Figure 18 : Transmit Word Timing Diagram

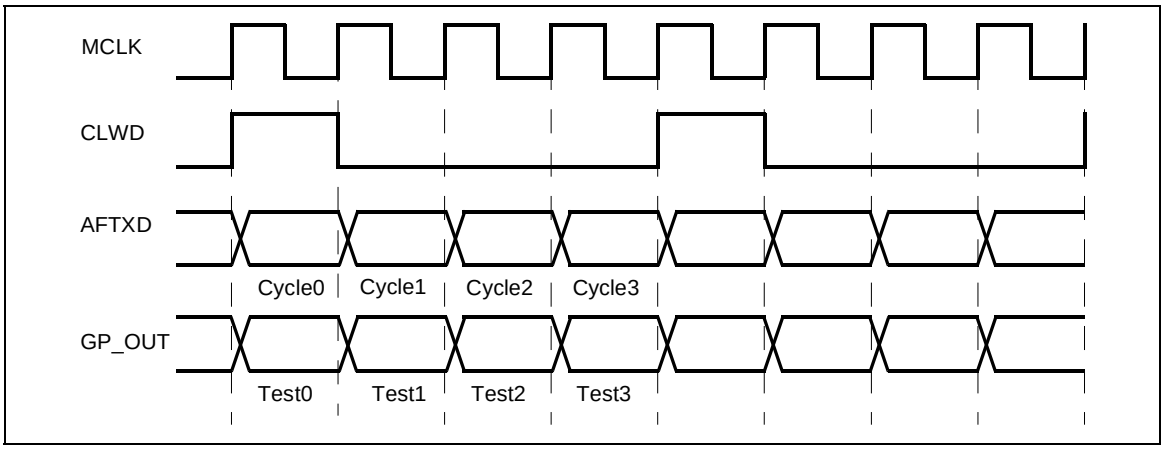


Figure 19 : Receive Word Timing Diagram

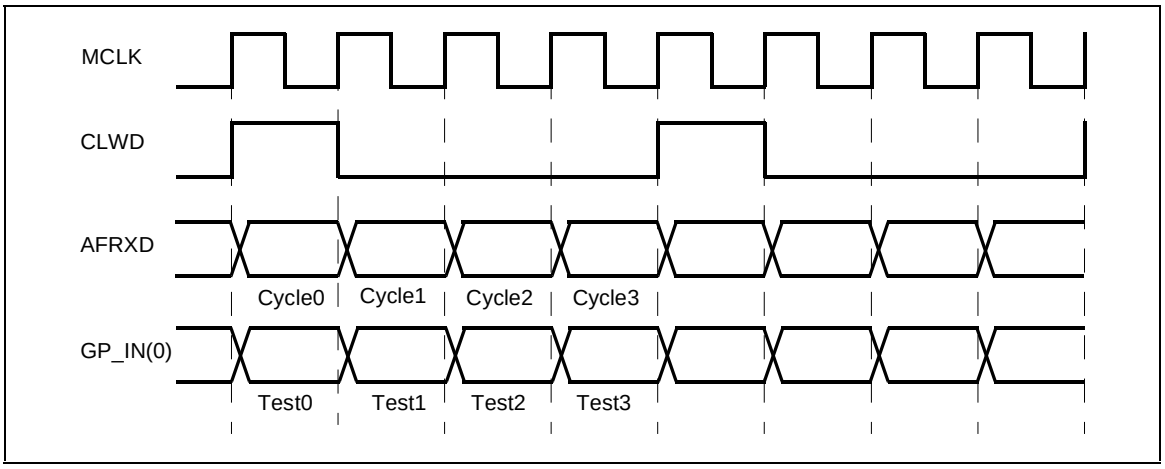


Figure 20 : Transmit Interface

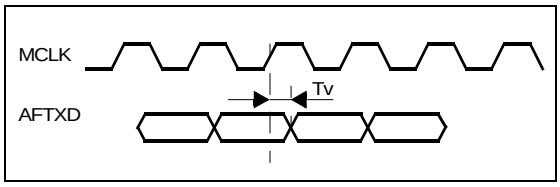


Figure 21 : Receive Interface

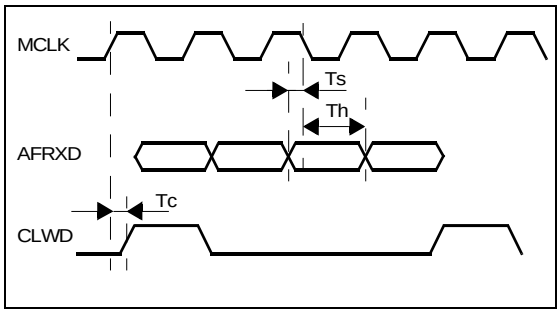


Table 3 : Transmitted Bits Assigned to Signal / Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFTXD[0]	b0	b4	b8	b12
AFTXD[1]	b1	b5	b9	b13
AFTXD[2]	b2	b6	b10	b14
AFTXD[3]	b3	b7	b11	b15

Table 4 : Transmitted Bits Assigned to Signal / Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFRXD[0]	b0	b4	b8	b12
AFRXD[1]	b1	b5	b9	b13
AFRXD[2]	b2	b6	b10	b14
AFRXD[3]	b3	b7	b11	b15

Table 5 : Master Clock (MCLK) AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F	Clock Frequency		35.328		MHz
Tper	Clock Period		28.3		ns
Th	Clock Duty Cycle	40		60	%

Table 6 : AFTXD, AFTXED, CLWD AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Tv	Data Valid Time	0		13	ns
Tc	Data Valid Time	0		10	ns

Table 7 : AFRXD AC Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Ts	Data setup Time	5			ns
Th	Data hold Time	5			ns

Tests, Clock, JTAG Interface

– Mclk: Master Clock (35.328MHz) generated by VCXO

– ATM receive interface, asynchronous clock generated by Utopia Master

– ATM transmit interface, asynchronous clock generated by Utopia Master

– ATC clock (Pclk): external asynchronous clock (synchronous with ATC in case of i960 specific interface)

JTAG TP interface: Standard Test Access Port, Used with the boundary scan for chip and board testing. This JTAG TAP interface consists in 5 signals:

TDI, TDO, TCK & TMS.

TSRTB: Test Reset, reset the TAP controller. TRSTB is an active low signal.

Table 8 : Boundary Scan Chain Sequence

Signal Name	Sequence Number	BS Type
Ad[0]	IO2	B
Ad[1]	IO3	B
Ad[2]	IO4	B
Ad[3]	IO6	B
Ad[4]	IO7	B
Ad[5]	IO9	B
Ad[6]	IO10	B
Ad[7]	IO12	B
Ad[8]	IO13	B
Ad[9]	IO14	B
Ad[10]	IO16	B
Ad[11]	IO17	B
Ad[12]	IO19	B
Pclk	IO21	C
Ad[13]	IO23	B
Ad[14]	IO24	B
Ad[15]	IO25	B
Be1	IO27	I
Ale	IO28	C

Table 8 : Boundary Scan Chain Sequence

Signal Name	Sequence Number	BS Type
Csb	IO30	I
Wr_Rdb	IO31	I
Rdyb	IO32	B
Obc_Type	IO33	I
Intb	IO34	O
Resetb	IO35	I
U_Rxdata[0]	IO38	B
U_Rxdata[1]	IO39	B
U_Rxdata[2]	IO41	B
U_Rxdata[3]	IO42	B
U_Rxdata[4]	IO44	B
U_Rxdata[5]	IO45	B
U_Rxdata[6]	IO47	B
U_Rxdata[7]	IO48	B
U_Rxaddr[0]	IO50	I
U_Rxaddr[1]	IO51	I
U_Rxaddr[2]	IO52	I
U_Rxaddr[3]	IO53	I
U_Rxaddr[4]	IO55	I
Gp_In[0]	IO56	I
Gp_In[1]	IO58	I
U_Rxrefb	IO60	O
U_Txrefb	IO61	I
U_Rxclk	IO63	C
U_Rxsoc	IO64	I
U_Rxclav	IO65	O
U_Rxenb	IO66	I
U_Txclk	IO68	C
U_Txsoc	IO69	I
U_Txclav	IO70	O
U_Txenb	IO71	I
U_Txdata[7]	IO74	I
U_Txdata[6]	IO75	I

Table 8 : Boundary Scan Chain Sequence

Signal Name	Sequence Number	BS Type
U_Txdata[5]	IO77	I
U_Txdata[4]	IO78	I
U_Txdata[3]	IO79	I
U_Txdata[2]	IO80	I
U_Txdata[1]	IO82	I
U_Txdata[0]	IO83	I
U_Txaddr[4]	IO84	I
U_Txaddr[3]	IO85	I
U_Txaddr[2]	IO87	I
U_Txaddr[1]	IO88	I
U_Txaddr[0]	IO89	I
Reserved 0	IO90	O
Reserved 1	IO92	O
Reserved 2	IO93	O
Reserved 3	IO94	O
Reserved 4	IO96	O
Reserved 5	IO97	O
Reserved 6	IO98	O
Reserved 7	IO99	O
Reserved 8	IO100	NONE
Reserved 9	IO101	O
Reserved 10	IO103	I
Reserved 11	IO104	I
Reserved 12	IO105	I
Reserved 13	IO106	I
Reserved 14	IO107	O
Reserved 15	IO110	O
Reserved 16	IO111	O
TDI	IO112	NONE
TDO	IO113	NONE
TMS	IO114	NONE
TCK	IO116	NONE
TRSTB	IO118	NONE
Testse	IO119	C
GP_Out	IO120	O

Table 8 : Boundary Scan Chain Sequence

Signal Name	Sequence Number	BS Type
Pdown	IO121	O
Afrxd[0]	IO123	I
Afrxd[1]	IO124	I
Afrxd[2]	IO125	I
Afrxd[3]	IO126	I
Clwd	IO128	I
Mclk	IO129	C
Ctrldata	IO130	O
Disable_Comp	IO135	I
Iddq	IO138	C
AFTXD[0]	IO139	NONE
AFTXD[1]	IO140	NONE
AFTXD[2]	IO142	NONE
AFTXD[3]	IO143	NONE

General purpose I/O register (0x40)

Field	Type	Position Bits	Length	Function
GP_IN	R	[0,1]	2	Sampled level on pins GP_IN
GP_OUT	RW	[2]	1	Output level on pins GP_OUT

Bits from 3 to 15 are reserved

Reset Initialization

The ST70235A supports two reset modes:

– A 'hardware' reset is activated by the RESETB pin (active low). A hard reset occurs when a low input value is detected at the RESETB input. The low level must be applied for at least 1ms to guarantee a correct reset operation. All clocks and power supplies must be stable for 200ns prior to the rising edge of the RESETB signal.

– 'Soft' reset activated by the controller write access to a soft reset configuration bit. The reset process takes less than 10000 MCLK clock cycles.

ELECTRICAL SPECIFICATIONS

Generic DC Electrical Characteristics

The values presented in the following table apply for all inputs and/or outputs unless otherwise specified. All voltages are referenced to V_{SS}, unless otherwise specified, positive current is towards the device.

IO Buffers Generic DC Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
I_{IN}	Input Leakage Current	$V_{IN} = V_{SS}$, V_{DD} no pull up /pull down	-4		4	µA
I_{OZ}	Tristate Leakage Current	$V_{IN} = V_{SS}$, V_{DD} no pull up /pull down	-4		4	µA
I_{PU}	Pull up Current	$V_{IN} = V_{SS}$	-15	-66	-125	µA
I_{PD}	Pull Down Current	$V_{IN} = V_{DD}$	15	66	125	µA
R_{PU}	Pull up Resistance	$V_{IN} = V_{SS}$		50		KΩ
R_{PD}	Pull Down Resistance	$V_{IN} = V_{DD}$		50		KΩ

Input/ Output TTL Generic Characteristics

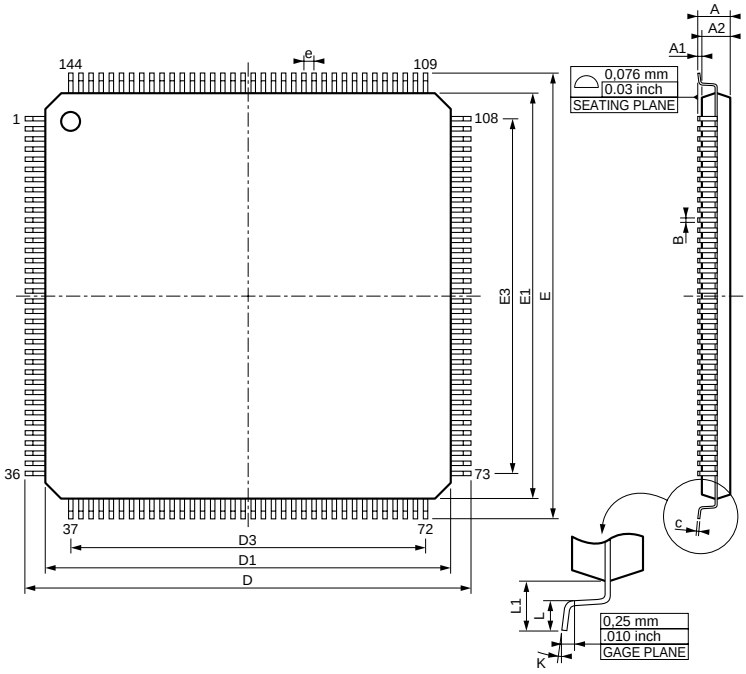
The values presented in the following table apply for all TTL inputs and/or outputs unless otherwise specified.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{HY}	Schmitt Trigger Hysteresis	Slow edge < 1V/µs	0.4		0.7	V
V_{OL}	Low Level Output Voltage	I_{OUT} = XmA*			0.4	V
V_{OH}	High Level Output Voltage	I_{OUT} = XmA*	2.4			V

** The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are 4 and 8mA.*

TQFP144 PACKAGE MECHANICAL DATA

Figure 22 : Package Outline TQFP144



Dimension	Millimeter			Inch		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0067	0.0087	0.011
C	0.09		0.20	0.0035		0.008
D		22.00			0.866	
D1		20.00			0.787	
D3		17.50			0.689	
e		0.50			0.020	
E		22.00			0.866	
E1		20.00			0.787	
E3		17.50			0.689	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (minimum), 7° (maximum)					

ST70235A.REF