

# ***EICEDRIVER™***

1ED020I12-F

Single IGBT Driver IC

**Power Management & Drives**



Never stop thinking.

## Power Management & Drives

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Page	Subjects (major changes since last revision)
6	2.2.3 Watchdog Timer
14	4.4.6 Dynamic Characteristics

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### Single IGBT Driver IC

#### Product Highlights

- Coreless transformer isolated driver
- Galvanic Insulation
- Integrated protection features
- Suitable for operation at high ambient temperature
- Cost effective technology
- Approvals: DIN EN 60747-5-2, UL1577



#### Features

- Single channel isolated IGBT Driver
- For 600V/1200V IGBTs
- 2A rail-to-rail output
- Vcesat-detection
- Active Miller Clamp

#### Typical Application

- AC-Drives
- UPS-Systems
- Welding

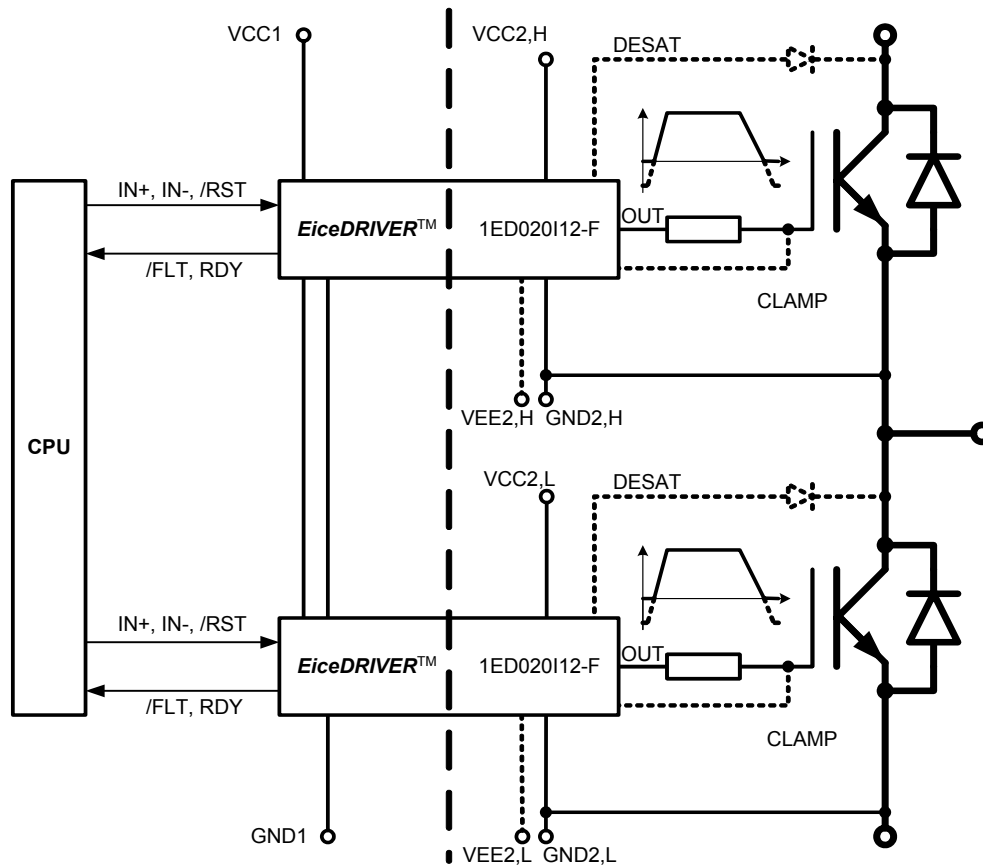


Figure 1: Typical Application

Type	Gate drive current	Package
1ED020I12-F	+/- 2A	PG-DSO-16-15

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# 1 Blockdiagram and Application

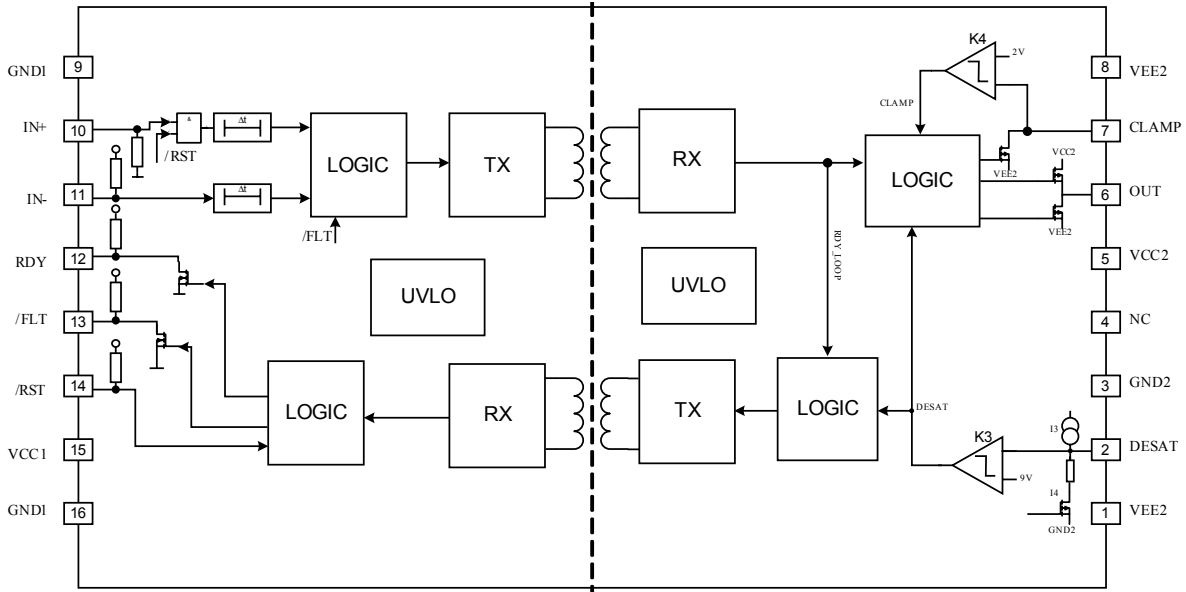


Figure 2: Blockdiagram 1ED020I12-F

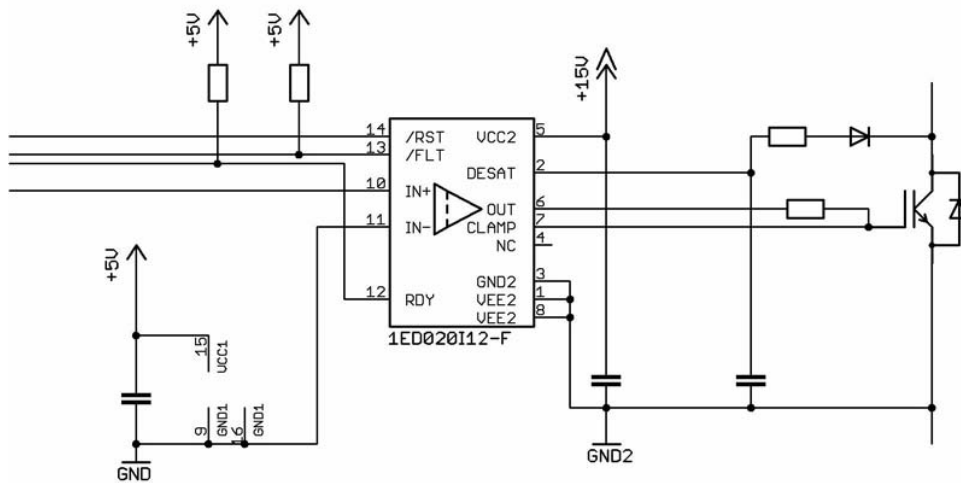


Figure 3: Application example

## 2 Functional Description

### 2.1 Introduction

The 1ED020I12-F is an advanced IGBT gate driver that can be also used for driving power MOS devices. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

An effective active Miller clamp function avoids the need of negative gate driving in most applications and allows the use of a simple bootstrap supply for the high side driver.

A rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes an IGBT desaturation protection with a FAULT status output.

A READY status output reports if the device is supplied and operates correctly.

### 2.2 Internal Protection Features

#### 2.2.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips.

If the power supply voltage  $V_{VCC1}$  of the input chip drops below  $V_{UVLO1}$  a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored as long as  $V_{VCC1}$  reaches the power-up voltage  $V_{UVLOH1}$ .

If the power supply voltage  $V_{VCC2}$  of the output chip goes down below  $V_{UVLO2}$  the IGBT is switched off and signals from the input chip are ignored as long as  $V_{VCC2}$  reaches the power-up voltage  $V_{UVLOH2}$ .

#### 2.2.2 READY status output

The READY output shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission

It is not necessary to reset the READY signal since its state only depends on the status of the former protection signals.

#### 2.2.3 Watchdog Timer

The 1ED020I12-F incorporates two level of signal transmission security implemented through two independent watchdog timers. First level ensures the short term signal integrity by resending the (turn on/off) signals with a watchdog period of typical 500ns. The second level monitors during normal operation the internal signal transmission. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

#### 2.2.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply.

### 2.3 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high. A minimum input pulse width is defined to filter occasional glitches.

### 2.4 Driver Output

The output driver section uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

## **2.5 External Protection Features**

### **2.5.1 Desaturation Protection**

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches 9V, the output is driven low. Further, the /FAULT output is activated. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

### **2.5.2 Active Miller Clamping**

A Miller clamp allows sinking the Miller current during a high dV/dt situation. Therefore, the use of a negative supply voltage can be avoided in many applications. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2).

### **2.5.3 Short Circuit Clamping**

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10us may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

## **2.6 RESET**

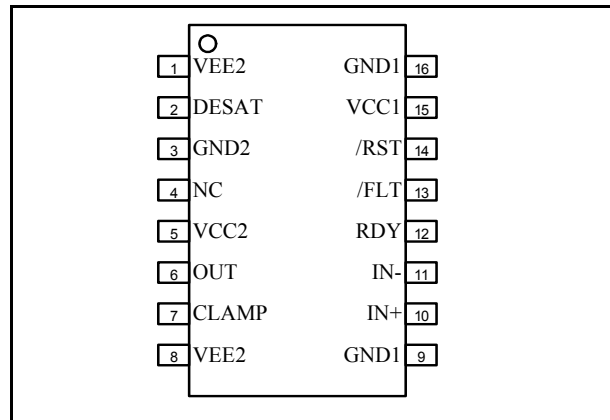
The reset input has two functions.

Firstly, /RST is in charge of setting back the FAULT output. If /RST is low longer than a given time, /FLT will be reseted at the rising edge of /RST; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic.

### 3 Pin Configuration and Functionality

#### 3.1 Pin Configuration

Pin	Symbol	Function
1	VEE2	Negative power supply output side
2	DESAT	Desaturation protection
3	GND2	Signal ground output side
4	NC	Not connected
5	VCC2	Positive power supply output side
6	OUT	Driver output
7	CLAMP	Miller clamping
8	VEE2	Negative power supply output side
9	GND1	Signal ground input side
10	IN+	Non inverted driver input
11	IN-	Inverted driver input
12	RDY	Ready output
13	$\overline{\text{FLT}}$	Fault output
14	$\overline{\text{RST}}$	Reset input
15	VCC1	Positive power supply input side
16	GND1	Signal ground input side



**Figure 4: PG-DSO-16-15**

#### 3.2 Pin Functionality

##### GND1

Ground connection of the input side.

##### IN+ Non-inverting driver input

IN+ control signal for the driver output if IN- is set to low. (The IGBT is on if IN+ = high and IN- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

##### IN- Inverting driver input

IN- control signal for driver output if IN+ is set to high. (IGBT is on if IN- = low and IN+ = high)

A minimum pulse width is defined to make the IC robust against glitches at IN-. An internal Pull-Up-Resistor ensures IGBT Off-State.

##### /RST (Reset) input

**Function 1:** Enable/shutdown of the input chip. (The IGBT is off if /RST = low). A minimum pulse width is defined to make the IC robust against glitches at IN-.

**Function 2:** Resets the DESAT-FAULT-state of the chip if /RST is low for a time  $T_{\text{RST}}$ . An internal Pull-Up-Resistor is used to ensure FLT status output.

##### /FLT (Fault output)

Open-drain with internal pull up resistor output to report a desaturation error of the IGBT (/FLT is low if desaturation occurs)

##### RDY (Ready status)

Open-drain with internal pull up resistor output to report the correct operation of the device. (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless)

##### VCC1

5V power supply of the input chip

##### VEE2

Negative power supply pins of the output chip. If no negative supply voltage is available, both pins have to be connected to GND2.

##### DESAT (Desaturation)

Monitoring of the IGBT saturation voltage ( $V_{\text{CE}}$ ) to detect desaturation caused by short circuits. If OUT is high,  $V_{\text{CE}}$  is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an



external capacitor.

**CLAMP (Clamping)**

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2).

**GND2**

Reference ground of the output chip.

**OUT (Driver output)**

Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode Vout is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) Vout is set to VEE2 independent of the input control signals.

**VCC2**

Positive power supply pin of the output side.

## 4 Electrical Parameters

### 4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	$V_{VCC2}$	-0.3	20	V	1)
Negative power supply output side	$V_{VEE2}$	-12	0.3	V	1)
Maximum power supply voltage output side ( $V_{VCC2}-V_{VEE2}$ )	$V_{max2}$	—	28	V	
Gate driver output	$V_{OUT}$	$V_{VEE2}-0.3$	$V_{max2}+0.3$	V	
Gate driver high output maximum current	$I_{OUT}$	—	2.4	A	$t = 2\mu s$
Gate driver low output maximum current	$I_{OUT}$	—	2.4	A	$t = 2\mu s$
Maximum short circuit clamping time	$t_{CLP}$	—	10	us	$I_{CLAMP/OUT} = 500mA$
Positive power supply input side	$V_{VCC1}$	-0.3	6.5	V	
Logic input voltages ( $IN+, IN-, \overline{RST}$ )	$V_{LogicIN}$	-0.3	6.5	V	
Opendrain Logic output voltage ( $\overline{FLT}$ )	$V_{\overline{FLT}}$	-0.3	6.5	V	
Opendrain Logic output voltage (RDY)	$V_{RDY}$	-0.3	6.5	V	
Opendrain Logic output current ( $\overline{FAULT}$ )	$I_{\overline{FLT}}$	—	10	mA	
Opendrain Logic output current (RDY)	$I_{RDY}$	—	10	mA	
Pin DESAT voltage	$V_{DESAT}$	-0.3	$V_{VCC2}+0.3$	V	1) $V_{VEE2} = -8V$
Pin CLAMP voltage	$V_{CLAMP}$	$V_{VEE2}-0.3$	$V_{VCC2}+0.3$	V	2)
Junction temperature	$T_J$	-40	150	°C	
Storage temperature	$T_S$	-55	150	°C	
Power dissipation, Input chip	$P_{D, IN}$	—	100	mW	3) @ $T_A = 25^\circ$
Power dissipation, Output chip	$P_{D, OUT}$	—	700	mW	3) @ $T_A = 25^\circ$
Thermal resistance (Input chip active)	$R_{THJA, IN}$	—	160	K/W	@ $T_A = 25^\circ C$
Thermal resistance (Output chip active)	$R_{THJA, OUT}$	—	125	K/W	@ $T_A = 25^\circ C$
ESD Capability	$V_{ESD}$	—	1	kV	Human Body Model <sup>4)</sup>

1) With respect to GND2.

2) may be exceeded during short circuit clamping

3) Output IC power dissipation is derated linearly at 10 mW/°C above 62°C. Input IC power dissipation does not require derating. See section 8.1 for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

4) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor).

## 4.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	$V_{VCC2}$	13	20	V	<sup>1)</sup>
Negative power supply output side	$V_{VEE2}$	-12	0	V	<sup>1)</sup>
Maximum power supply voltage output side ( $V_{VCC2}-V_{VEE2}$ )	$V_{max2}$	—	28	V	
Positive power supply input side	$V_{VCC1}$	4.5	5.5	V	
Logic input voltages ( $IN+$ , $IN-$ , $\overline{RST}$ )	$V_{LogicIN}$	-0.3	5.5	V	
Pin CLAMP voltage	$V_{CLAMP}$	$V_{VEE2}-0.3$	$V_{VCC2}$ <sup>2)</sup>	V	
Pin DESAT voltage	$V_{DESAT}$	-0.3	$V_{VCC2}$	V	<sup>1)</sup>
Ambient temperature	$T_A$	-40	105	°C	
Common mode transient immunity <sup>3)</sup>	$ \Delta V_{ISO}/dt $	—	50	kV/ $\mu$ s	@ 500V

1) With respect to GND2.

2) may be exceeded during short circuit clamping

3) The parameter is not subject to production test - verified by design/characterization

## 4.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Values	Unit	Remarks
Positive power supply output side	$V_{VCC2}$	15	V	<sup>1)</sup>
Negative power supply output side	$V_{VEE2}$	-8	V	<sup>1)</sup>
Positive power supply input side	$V_{VCC1}$	5	V	

1) With respect to GND2.

#### 4.4 Electrical Characteristics

Note: The electrical characteristics involve the spread of values for the supply voltages, load and junction temperatures given below. Typical values represent the median values, which are related to production processes at  $T = 25^{\circ}\text{C}$ . Unless otherwise noted all voltages are given with respect to GND.

##### 4.4.1 Voltage Supply.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
UVLO Threshold Input Chip	$V_{UVLOH1}$	—	4.1	4.3	V	
	$V_{UVLOL1}$	3.5	3.8	—	V	
UVLO Hysteresis Input Chip ( $V_{UVLOH1} - V_{UVLOL1}$ )	$V_{HYS1}$	0.15	—	—	V	
UVLO Threshold Output Chip	$V_{UVLOH2}$	—	12.0	12.6	V	
	$V_{UVLOL2}$	10.4	11.0	—	V	
UVLO Hysteresis Output Chip ( $V_{UVLOH1} - V_{UVLOL1}$ )	$V_{HYS2}$	0.7	0.9	—	V	
Quiescent Current Input Chip	$I_{Q1}$	—	7	9	mA	$V_{VCC1} = 5\text{V}$ IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	$I_{Q2}$	—	4	6	mA	$V_{VCC2} = 15\text{V}$ $V_{VEE2} = -8\text{V}$ IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

##### 4.4.2 Logic Input and Output

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
IN+, IN-, $\overline{\text{RST}}$ Low Input Voltage	$V_{IN+L}, V_{IN-L}, V_{\overline{\text{RST}}L}$	—	—	1.5	V	
IN+, IN-, $\overline{\text{RST}}$ High Input Voltage	$V_{IN+H}, V_{IN-H}, V_{\overline{\text{RST}}H}$	3.5	—	—	V	
IN-, $\overline{\text{RST}}$ Input Current	$I_{IN-}, I_{\overline{\text{RST}}}$	—	100	400	uA	$V_{IN-} = \text{GND1}$ $V_{\overline{\text{RST}}} = \text{GND1}$
IN+ Input Current	$I_{IN+}$	—	100	400	uA	$V_{IN+} = \text{VCC1}$
RDY, /FLT Pull Up Current	$I_{\text{PRDY}}, I_{\overline{\text{FLT}}}$	—	100	400	uA	$V_{\text{RDY}} = \text{GND1}$ $V_{\overline{\text{FLT}}} = \text{GND1}$
Input Pulse Suppression IN+, IN-	$T_{\text{MININ}+}, T_{\text{MININ}-}$	30	40	—	ns	
Input Pulse Suppression $\overline{\text{RST}}$ for ENABLE/SHUTDOWN	$T_{\text{MINRST}}$	30	40	—	ns	
Pulse Width $\overline{\text{RST}}$ for Resetting $\overline{\text{FLT}}$	$T_{\text{RST}}$	800	—	—	ns	
/FLT Low Voltage	$V_{\overline{\text{FLT}}}$	—	—	300	mV	$I_{\text{SINK}(\overline{\text{FLT}})} = 5\text{mA}$
RDY Low Voltage	$V_{\text{RDYL}}$	—	—	300	mV	$I_{\text{SINK}(\text{RDY})} = 5\text{mA}$

**Electrical Parameters**
**4.4.3 Gate Driver**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High Level Output Voltage	V <sub>OUTH1</sub>	V <sub>VCC2</sub> -1.2	V <sub>VCC2</sub> -0.8	—	V	I <sub>OUTH</sub> = -20mA
	V <sub>OUTH2</sub>	V <sub>VCC2</sub> -2.5	V <sub>VCC2</sub> -2	—	V	I <sub>OUTH</sub> = -200mA
	V <sub>OUTH3</sub>	V <sub>VCC2</sub> -9	V <sub>VCC2</sub> -5	—	V	I <sub>OUTH</sub> = -1A
	V <sub>OUTH4</sub>		V <sub>VCC2</sub> -10	—	V	I <sub>OUTH</sub> = -2A
High Level Output Peak Current	I <sub>OUTH</sub>	-1.5	-2	—	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V <sub>OUTL1</sub>	—	V <sub>VEE2</sub> +0.04	V <sub>VEE2</sub> +0.09	V	I <sub>OUTL</sub> = 20mA
	V <sub>OUTL2</sub>	—	V <sub>VEE2</sub> +0.5	V <sub>VEE2</sub> +0.85	V	I <sub>OUTL</sub> = 200mA
	V <sub>OUTL3</sub>	—	V <sub>VEE2</sub> +2.5	V <sub>VEE2</sub> +5.0	V	I <sub>OUTL</sub> = 1A
	V <sub>OUTL4</sub>	—	V <sub>VEE2</sub> +7	—	V	I <sub>OUTL</sub> = 2A
Low Level Output Peak Current	I <sub>OUTL</sub>	1.5	2	—	A	IN+ = Low, IN- = Low; OUT = Low

**4.4.4 Active Miller Clamp**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Low Level Clamp Voltage	V <sub>CLAMPL1</sub>	—	V <sub>VEE2</sub> +0.03	V <sub>VEE2</sub> +0.08	V	I <sub>OUTL</sub> = 20mA
	V <sub>CLAMPL2</sub>	—	V <sub>VEE2</sub> +0.3	V <sub>VEE2</sub> +0.8	V	I <sub>OUTL</sub> = 200mA
	V <sub>CLAMPL3</sub>	—	V <sub>VEE2</sub> +1.9	V <sub>VEE2</sub> +4.8	V	I <sub>OUTL</sub> = 1A
Low Level Clamp Current	I <sub>CLAMPL</sub>	2	—	—	A	1)
Clamp Threshold Voltage	V <sub>CLAMP</sub>	1.6	2.1	2.4	V	Related to VEE2

1) The parameter is not subject to production test - verified by design/characterization

#### 4.4.5 Short Circuit Clamping

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Clamping voltage (OUT) ( $V_{OUT}-V_{VCC2}$ )	$V_{CLPout}$	—	0.8	1.3	V	IN+=High, IN-=Low, OUT=High $I_{OUT} = 500mA$ (pulse test, $t_{CLPmax} = 10\mu s$ )
Clamping voltage (CLAMP) ( $V_{VCLAMP}-V_{VCC2}$ )	$V_{CLPclamp}$	—	1.3	—	V	IN+=High, IN-=Low, OUT=High $I_{CLAMP} = 500mA$ (pulse test, $t_{CLPmax} = 10\mu s$ )
Clamping voltage (CLAMP)	$V_{CLPclamp}$	—	0.7	1.1	V	IN+=High, IN-=Low, OUT=High $I_{CLAMP} = 20mA$

#### 4.4.6 Dynamic Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Input to output propagation delay ON	$T_{PDON}$	165	185	750 <sup>1)</sup>	ns	$V_{VCC1} = 5V,$ $V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 100pF$ $V_{IN+} = 50\%, V_{OUT} = 50\%$ @ 25°C
Input to output propagation delay OFF	$T_{PDOFF}$	150	170	190	ns	
Input to output propagation delay distortion	$T_{PDISTO}$	—	20	555 <sup>1)</sup>	ns	
Input to output propagation delay ON variation due to temp <sup>2)</sup>	$T_{PDONt}$	—	—	20	ns	$V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 100pF$ $V_{IN+} = 50\%, V_{OUT} = 50\%$
Input to output propagation delay OFF variation due to temp <sup>2)</sup>	$T_{PDOFFt}$	—	—	35	ns	
Input to output propagation delay distortion variation due to temp <sup>2)</sup>	$T_{PDISTOt}$	—	—	20	ns	
Rise Time	$T_{RISE}$	—	60	—	ns	$V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 1nF$ VL 10% , VH 90%
		—	400	—	ns	$V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 34nF$ VL 10% , VH 90%
Fall Time	$T_{FALL}$	—	60	—	ns	$V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 1nF$ VL 10% , VH 90%
		—	600	—	ns	$V_{VCC2} = 15V, V_{VEE2} = -8V$ $C_{LOAD} = 34nF$ VL 10% , VH 90%

1) The maximum value of input to output propagation delay ON occurs only in case of electromagnetic interferences, typically the input to output delay is 205ns at TA =25°C, one worst case watchdog clock cycle shorter (see chapter 2.2.3). The turn OFF-signal is prioritized/dominant and will not show up this behavior.

2) The parameter is not subject to production test - verified by design/characterization

**Electrical Parameters**
**4.4.7 Desaturation protection**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Blanking Capacitor Charge Current	$I_{DESATC}$	215	250	295	uA	$V_{VCC2}=15V, V_{VEE2}=-8V$ $V_{DESAT}=2V$
Blanking Capacitor Discharge Current	$I_{DESATD}$	1	2	—	mA	$V_{VCC2}=15V, V_{VEE2}=-8V$ $V_{DESAT}=6V$
Desaturation Reference Level	$V_{DESAT}$	8.3	9	9.5	V	$V_{VCC2}=15V, V_{VEE2}=-8V$
Desaturation Reference Level	$V_{DESAT}$	7.6	8.6	9.5	V	$V_{VCC2}=15V, V_{VEE2}=0V$
Desaturation Sense to OUT Low Delay	$T_{DESATOUT}$	—	100	150	ns	$V_{OUT}=90\%$ $C_{LOAD}=1nF$
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	—	—	2.25	us	$V_{FLT}=10\%; I_{FLT}=5mA$
Desaturation Low Voltage	$V_{DESATL}$	0.4	0.6	0.95	V	IN+=Low, IN-=Low, OUT=Low

**4.4.8 Active Shut Down**

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Active Shut Down Voltage	$V_{ACTSD}$ <sup>1)</sup>	—	—	4	V	$I_{OUT}=-200mA,$ $V_{CC2}$ open

1) With reference to VEE2

## 5 Insulation Characteristics

### 5.1 DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01. Basic Insulation

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$		I-IV I-III I-II	
Climatic Classification		55/105/21	
Pollution Degree (EN 60664-1)		2	
Minimum External Clearance	CLR	8.12	mm
Minimum External Creepage	CPG	8.24	mm
Minimum Comparative Tracking Index	CTI	175	
Maximum Repetitive Insulation Voltage	$V_{IORM}$	1420	$V_{PEAK}$
Input to Output Test Voltage, Method b <sup>1)</sup> $V_{IORM} * 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5pC$	$V_{PR}$	2663	$V_{PEAK}$
Input to Output Test Voltage, Method a <sup>1)</sup> $V_{IORM} * 1.6 = V_{PR}$ , Type and sample Test, $t_m = 60$ sec, Partial Discharge $< 5pC$	$V_{PR}$	2272	$V_{PEAK}$
Highest Allowable Overvoltage <sup>1)</sup>	$V_{IOTM}$	6000	$V_{PEAK}$
Maximum Surge Insulation Voltage	$V_{IOSM}$	6000	V
Insulation Resistance at $T_s$ , $V_{IO} = 500$ V	$R_{IO}$	$>10^9$	$\Omega$

1) Refer to VDE 0884 for a detailed description of Method a and Method b partial discharge test profiles.

\*Note 1: Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECC00802.

\*Note 2: This coupler is suitable for “basic insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 5.2 UL 1577

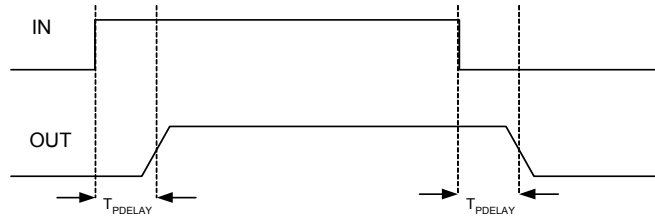
Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1min	$V_{ISO}$	3750	$V_{rms}$
Insulation Test Voltage / 1sec	$V_{ISO}$	4500	$V_{rms}$

### 5.3 Reliability

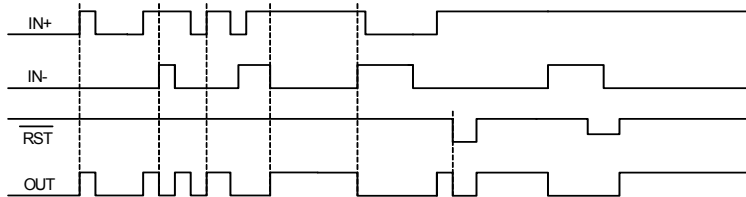
For Qualification Report please contact your local Infineon Technologies office.



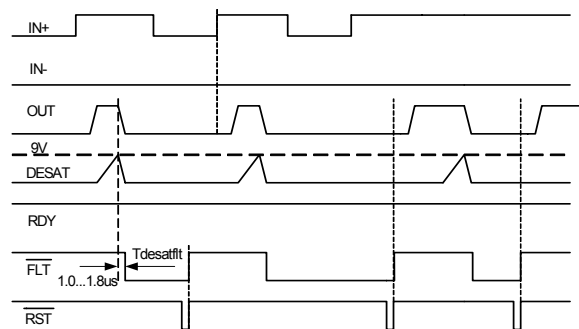
## 6 Timing Diagrams



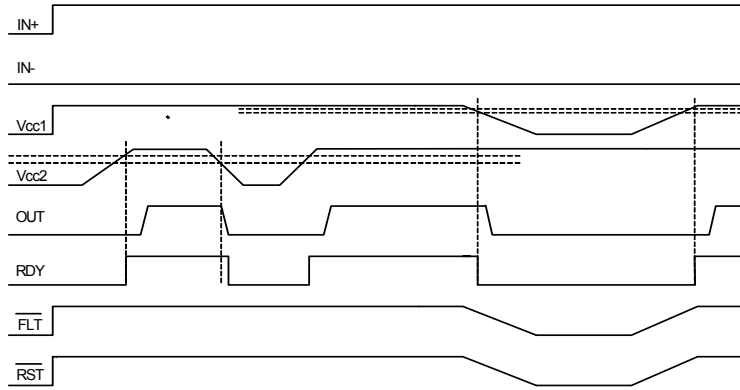
**Figure 5: Propagation Delay**



**Figure 6: Turn-on and Turn-off**



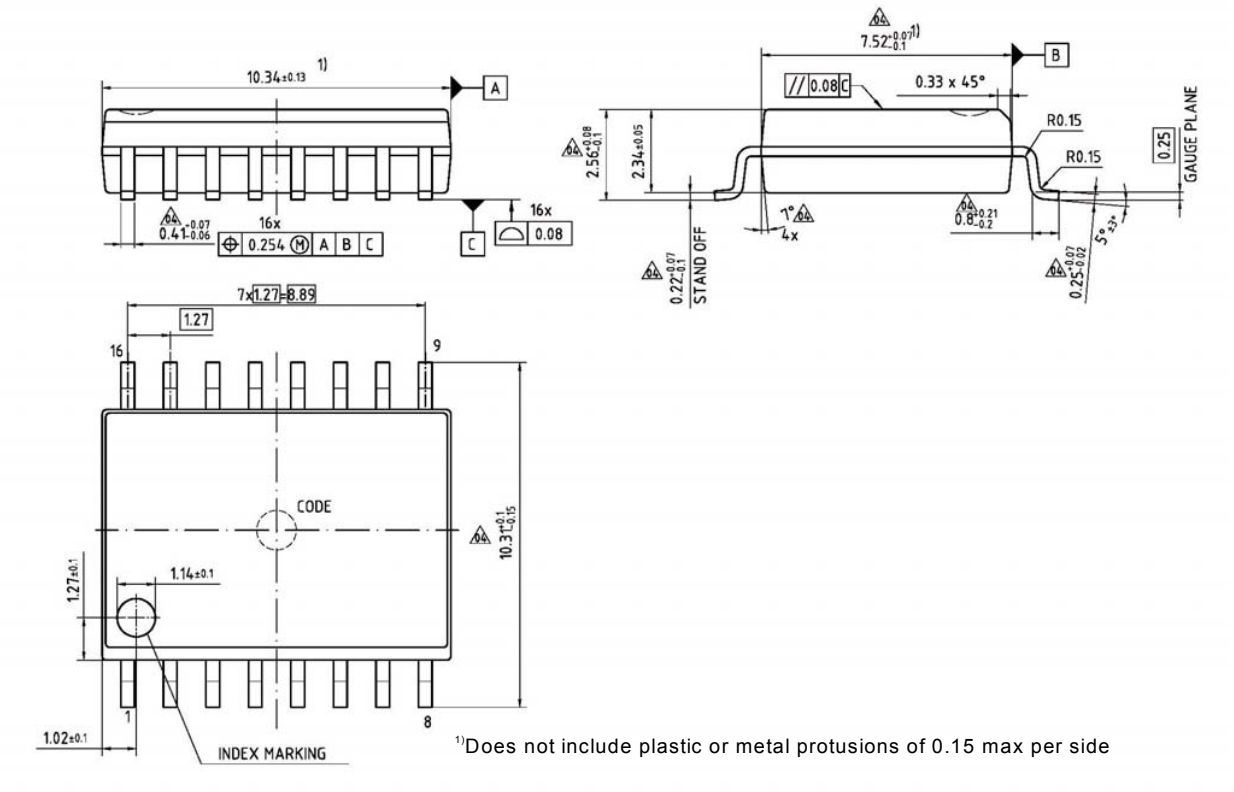
**Figure 7: Desaturation Fault**



**Figure 8: UVLO**

## 7 Package Outlines

### PG-DSO-16-15 (Plastic Dual Small)



**Figure 9: PG-DSO-16-15**

## 8 Application Notes

### 8.1 Reference Layout for Thermal Data

The PCB layout shown in figure 12 represents the reference layout used for the thermal characterisation. Pins 9 and 16 (GND1) and pins 1 and 8 (VEE2) require ground plane connections for achieving maximum power dissipation. The 1ED020I12-F is conceived to dissipate most of the heat generated through this pins.

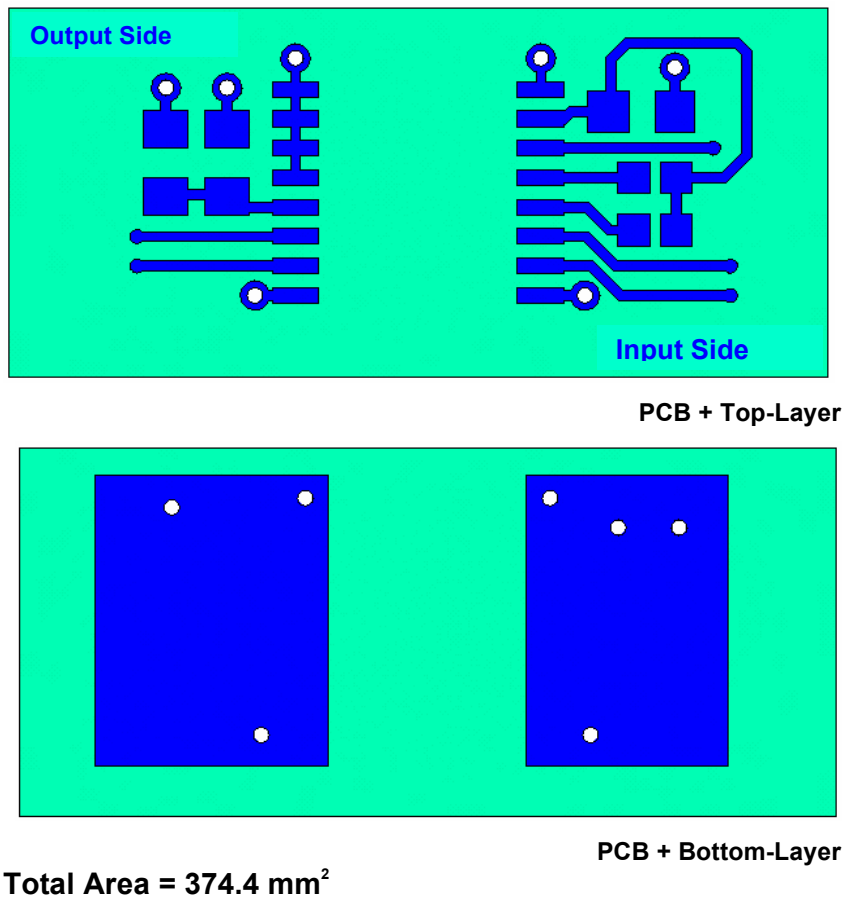


Figure 10: Reference layout for thermal data (Copper thickness 105µm)

### 8.2 Printed Circuit Board Guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.



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Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

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