MH89793

E1 Transceiver with Selectable Impedance

Preliminary Information

ISSUE 1 April 1995

Features

- Complete primary rate 2048kb/s CEPT line driver and receiver
- Onboard pulse transformers for transmit and receive
- Meets latest ETSI requirements [ETSI ETS 300 011 (NET 5)]
- Inductorless clock recovery
- Loss of signal ($\overline{\text{LOS}}$) indication
- Single +5V operation
- Compatible with MT9079 Framer
- Selectable termination impedance

Applications

- Primary rate ISDN network Interface
- Multiplexer equipment
- Private Network links
- Isochronous LANS/WANS

Ordering Information

MH89793 28 Pin DIL Package
Surface Mount Option is available by adding the suffix “S”

0°C to +70°C

Description

The Mitel MH89793 is a low cost E1 line driver/receiver with clock extraction requiring no external components.

The device is suitable for both 120R and 75R applications, by linking external pins.

By combining the MH89793 with Mitel’s E1 framer, the MT9079, a cost effective and efficient interface to E1 lines can be built.

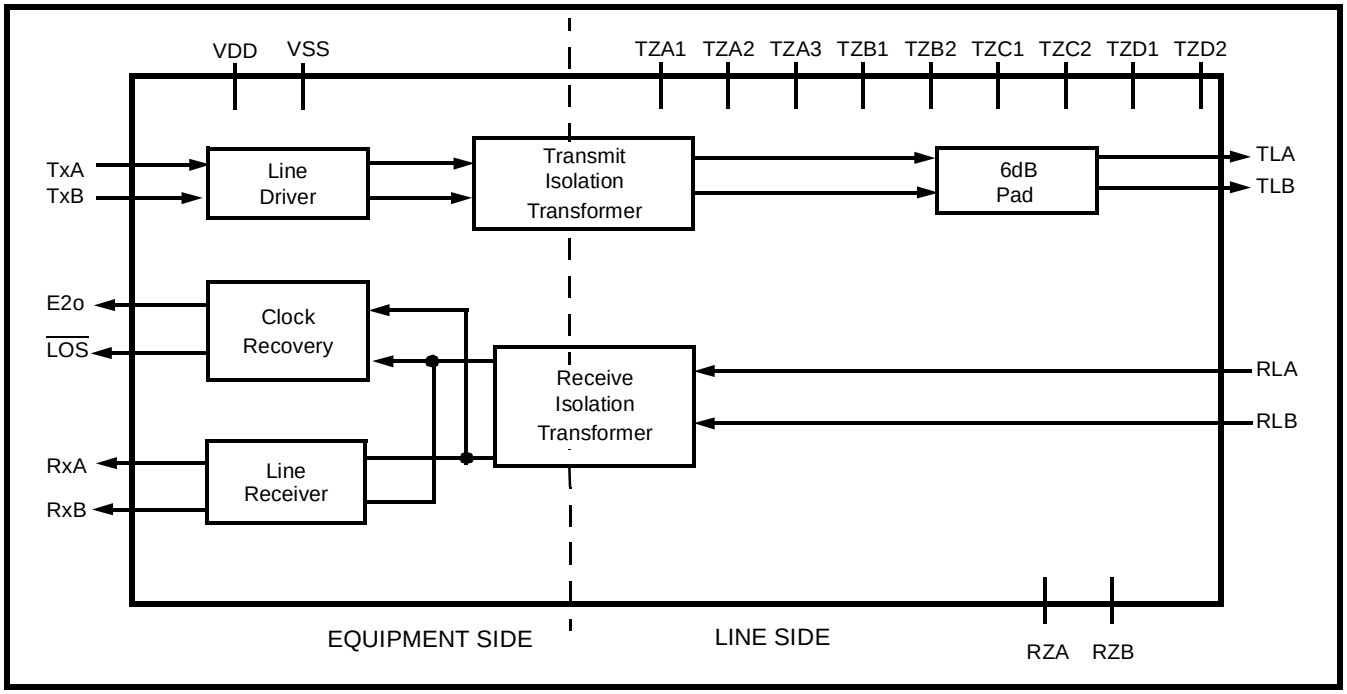

Figure 1 - Functional Block Diagram

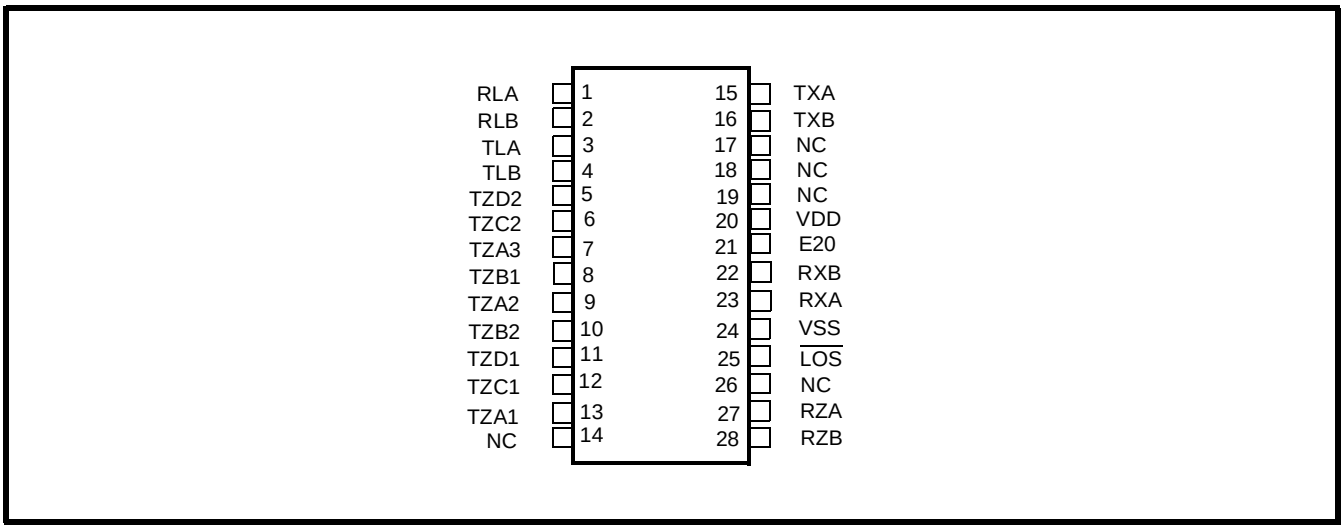

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	RLA	**Received Line A (Input)**. The A wire or Tip connection of the E1 receive line is connected to this pin.
2	RLB	**Received Line B (Input).** The B wire or Ring connection of the E1 receive line is connected to this pin.
3	TLA	**Transmit Line B (Output).** The A wire or Tip connection of the E1 receive line connected to this pin.
4	TLB	**Transmit Line B (Output)**. The B wire or Ring connection of the E1 receive line connected to this pin.
5	TZD2	**Transmit Impedance Select.** This pin is connected to pin 4 TLB to select 75Ω impedance. For 120Ω operation this pin is left open circuit.
6	TZC2	**Transmit Impedance Select.** This pin is connected to pin 3 TLA to select 75Ω impedance. For 120Ω operation this pin is left open circuit.
7	TZA3	**Transmit Impedance Select.** This pin is connected to pin 9 TZA2 to select 75Ω impedance. For 120Ω operation this pin is left open circuit.
8	TZA3	**Transmit Impedance Select.** This pin is connected to pin 10 TZB2 to select 120Ω impedance. For 75Ω operation this pin is left open circuit.
9	TZA2	**Transmit Impedance Select.** This pin is connected to pin 7 TZA3 to select 75Ω impedance. For 120Ω operation this pin is left open circuit.
10	TZB2	**Transmit Impedance Select.** This pin is connected to pin 8 TZB1 to select 120Ω impedance. For 75Ω operation this pin is left open circuit.
11	TZD1	**Transmit Impedance Select.** This pin is connected to pin 4 TLB to select 120Ω impedance. For 75Ω operation this pin is left open circuit.
12	TZC1	**Transmit Impedance Select.** This pin is connected to pin 3 TLA to select 120Ω impedance. For 75Ω operation this pin is left open circuit.
13	TZA1	**Transmit Impedance Select.** This pin is connected to pin 9 TZA2 to select 120Ω impedance. For 75Ω operation this pin is left open circuit.
14	NC	**No Connection**. This pin is used for internal connection.
15	TXA	**Transmit A (Input).** A unipolar signal from the framer device used in conjunction with TXB is used to generate the bipolar output signal.

Pin Description (Continued)

Pin #	Name	Description
16	TXB	**Transmit B (Input).** A unipolar signal from the framer device used in conjunction with TXA is used to generate the bipolar output signal.
17	NC	**No Connection.** This pin is used for internal connection.
18	NC	**No Connection.** This pin is used for internal connection.
19	NC	**No Connection.** This pin is used for internal connection.
20	VDD	**D.C. Power (Input).** +5V supply.
21	E2o	**2048kHz Extraction Clock (Output).** This clock is extracted by the device from the received signal. It is used internally to clock in data received from RLA and RLB.
22	RXB	**Receive B (Output).** This pin is connected to the negative receive pin of the framer and provides a signal of the same format as RXA.
23	RXA	**Receiver A (Output).** The bipolar CEPT signal received by the device at RLA and RLB input is converted to a unipolar format and output at this pin. This pin is connected to the positive receive pin of the framer.
24	VSS	**Ground (Input).** D.C. power return path.
25	$\overline{\text{LOS}}$	**Loss of Signal (Output).** This pin goes low when 128 contiguous zeros are received on the RLA and RLB inputs. $\overline{\text{LOS}}$ is reset when 64 ones are received in dual E1 frame periods.
26	NC	**No Connection.** This pin is used for internal connection.
27	RZA	**Receive Impedance Select.** This pin is connected to pin 17 RZB to select 75Ω input impedance. For 120Ω operation this pin is left open circuit.
28	RZB	**Receive Impedance Select.** This pin is connected to pin 16 RZA to select 75Ω input impedance. For 120Ω operation this pin is left open circuit.

Functional Description

The MH89793 is an E1 digital trunk interface which when used with an approved framer will conform to CCITT recommendation G.703 for PCM30 and I.431 for the ISDN. The functions provided include line driver and receiver circuitry, inductorless clock recovery, and loss of signal indication.

Bipolar Line Receiver

The MH89793 receiver interfaces to the transmission line through an internal pulse transformer which splits the received AMI lines signal into RxA and RxB. The line impedance is selected by linking appropriate option pins.

Attenuation of the transmission line shall not exceed 6dB (at 1024kHz) and attenuation characteristics shall be close to the “square root of f”.

$$Af\ (dB) = AF_{ref}\ (dB)^* \frac{\sqrt{f}}{f_{ref}}$$

Where:
AF - attenuation at frequency f in dB
AF_{ref} - attenuation at frequency f_{ref} in dB (in kHz)
f_{ref} - reference frequency (in this case 1024) kHz
f - frequency in kHz

Bipolar Line Transmitter

The MH89793 transmitter interfaces to the transmission line through an internal pulse transformer which combines the TxA and TxB data into an AMI line coded signal. This is then passed through the 6dB pad prior to being applied to the line.

Clock Extractor

The MH89793 contains a clock extraction circuit that generates the E2o clock from the received data without the use of external crystals or a tunable inductor.

The edge of the E2o extracted clock approximately aligns with the centre of the received data pulse.

Loss of Signal

The circuitry on board the hybrid is capable of detecting 128 continuous ZEROs received on RLA and RLB and indicating this condition as a logic low on pin 9, ($\overline{LOS}$). $\overline{LOS}$ will not reset until 64 ONEs are received in a two E1 frame period.

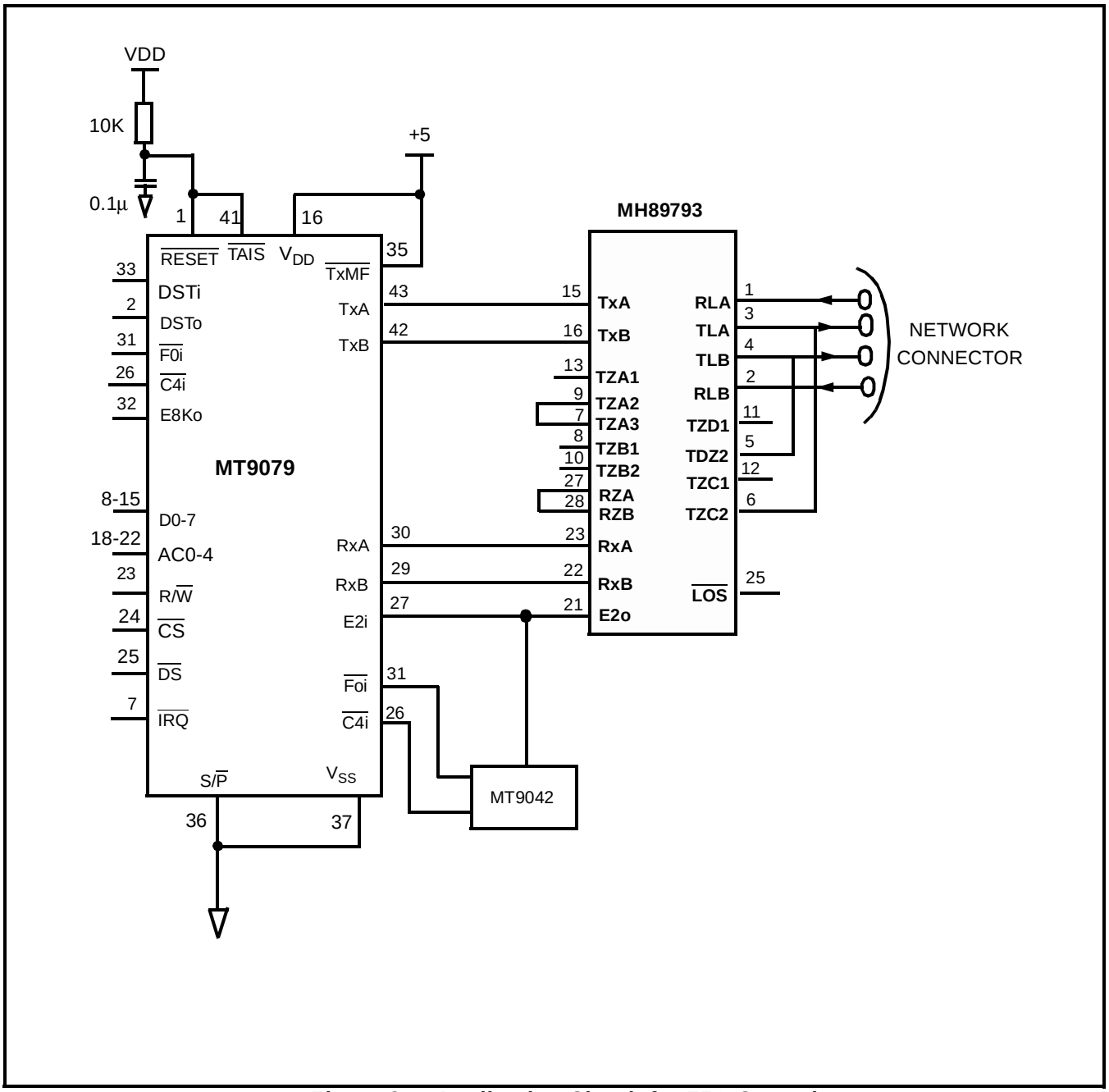

Figure 3a - Application Circuit for 75Ω Operation

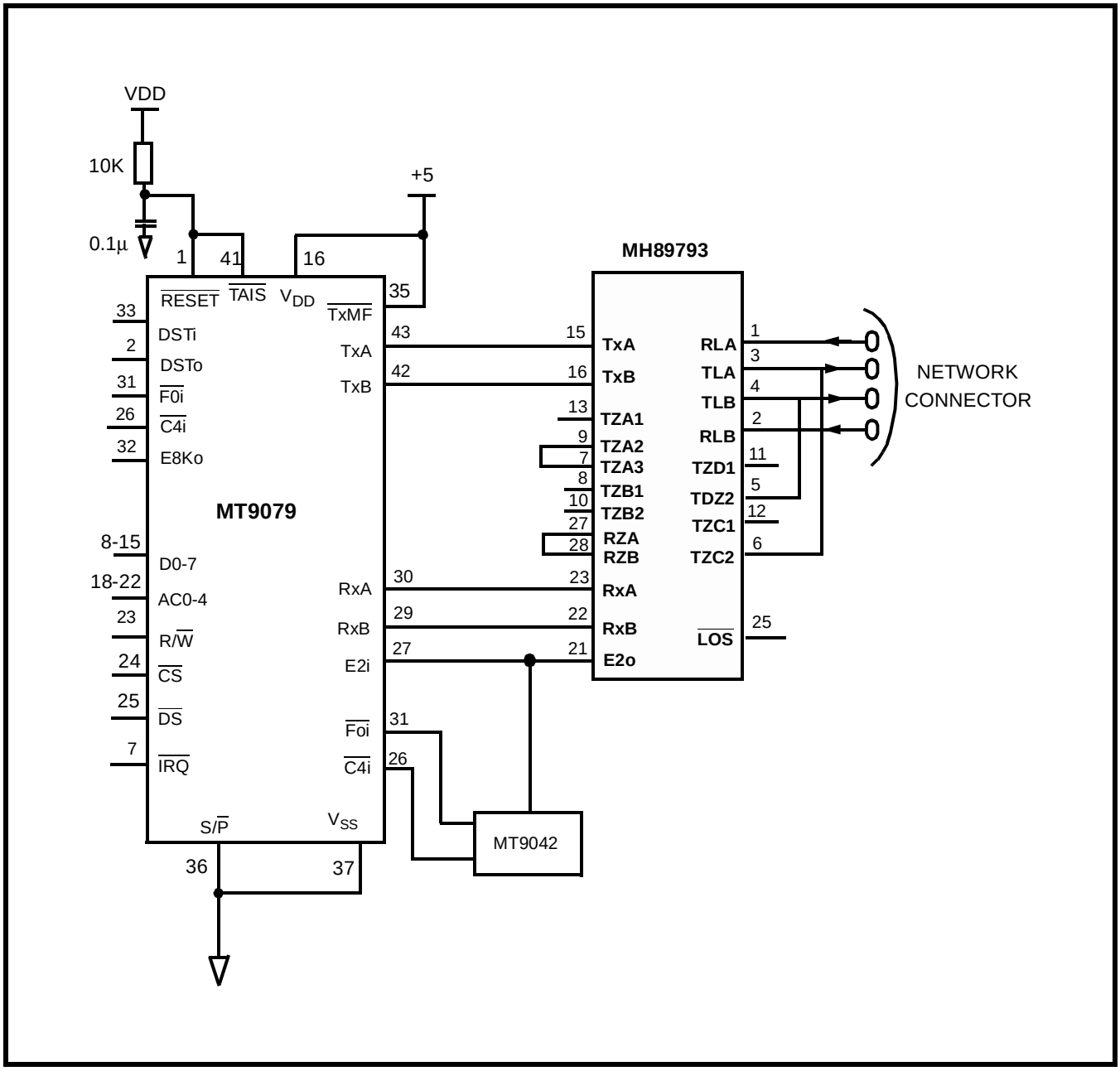

Figure 3b - Application Circuit for 120Ω Operation

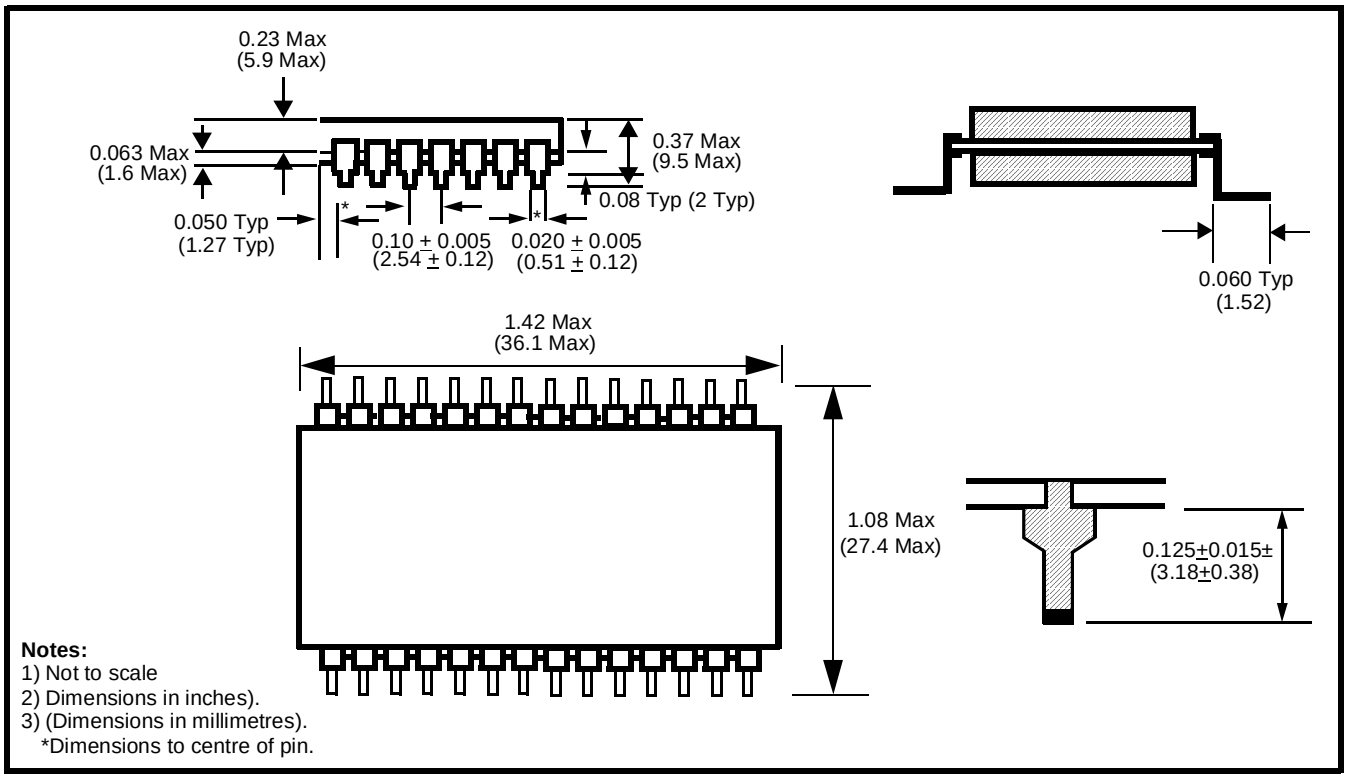

Figure 4 - Mechanical Data for 28 Pin Surface Mount Hybrid

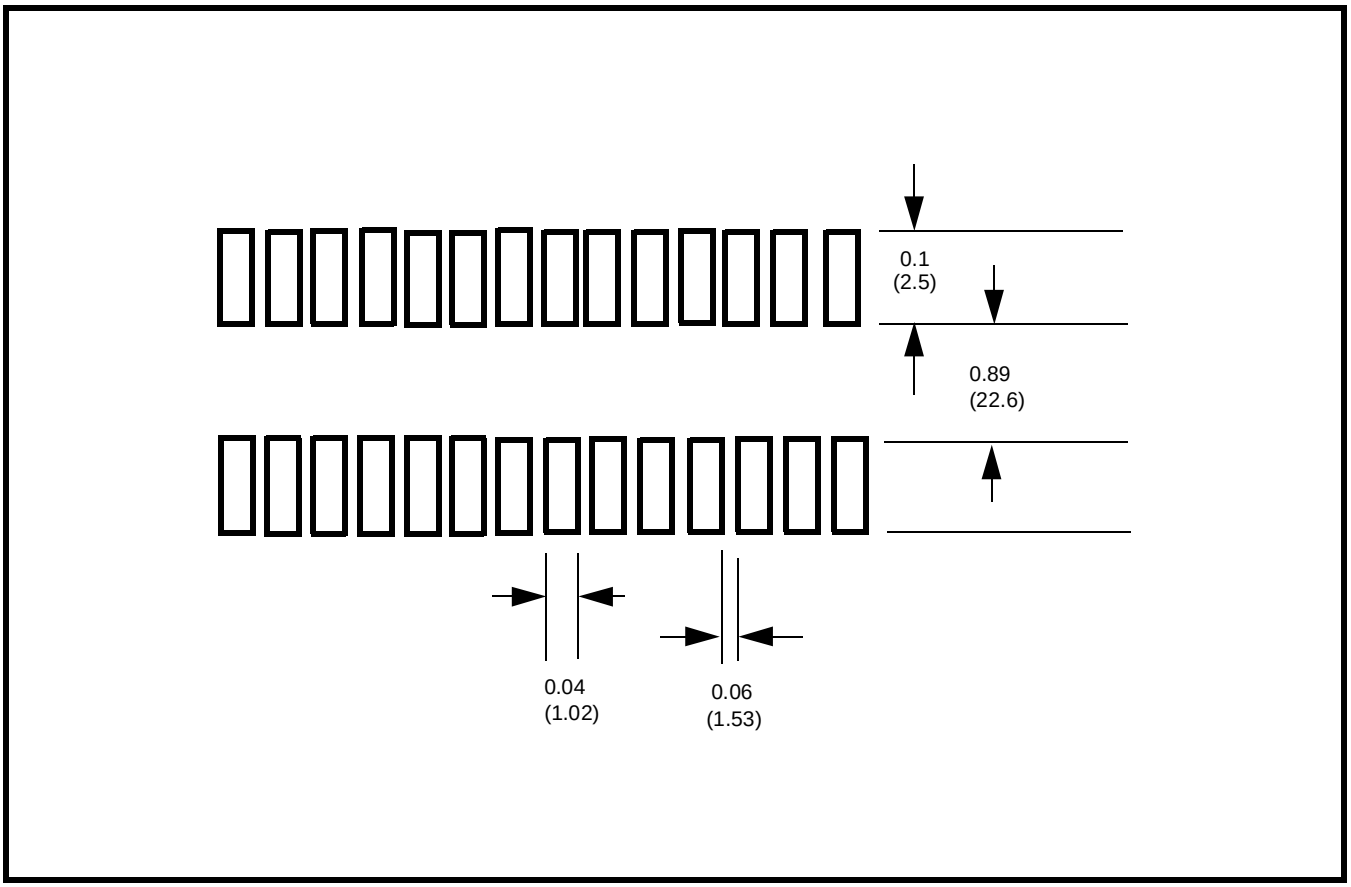

Figure 5 - Recommended Footprint for 28 Pin Surface Mount Hybrid

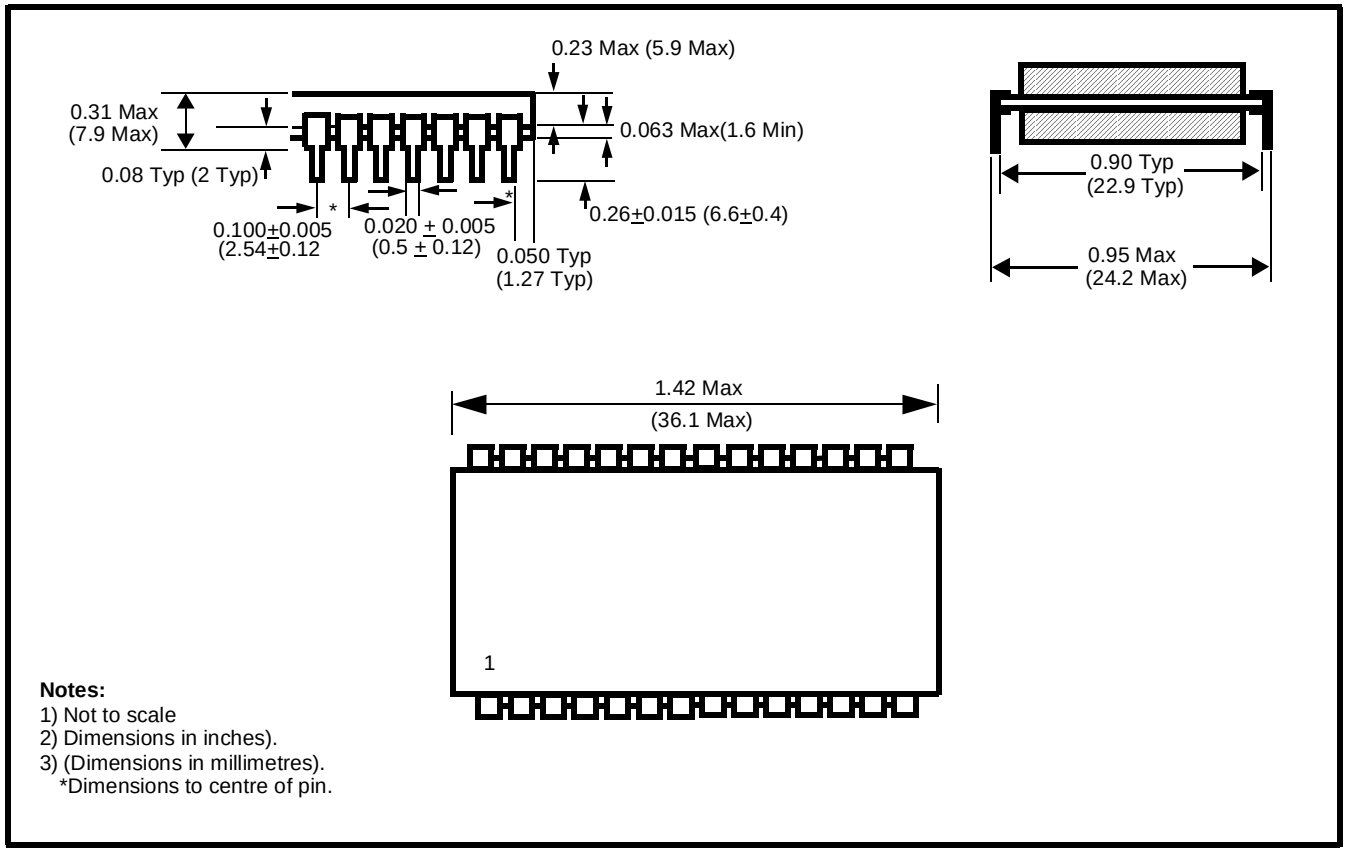

Figure 6 - Mechanical Data for 28 Pin DIL Hybrid

Notes: