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MOTOROLA

MC44144

Subcarrier Phase-Locked Loop

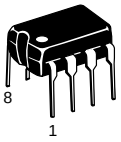
The MC44144 is a gated phase–locked loop intended for, but not restricted to, video applications. The integrated circuit contains a gated phase detector, voltage controlled crystal oscillator, divide–by–4 circuitry, and a video clamp. This device provides a 4X reference frequency output, and a 1X reference frequency output.

The MC44144 is manufactured using Motorola's high density, bipolar MOSAIC™ process.

- 8–Pin DIP or Surface Mount Package
- Gated–Phase Detector
- Single Pin Voltage Controlled Crystal Oscillator
- 1X and 4X Subcarrier Output
- Operates Off of a Standard 5.0 V Supply

SUBCARRIER PHASE–LOCKED LOOP

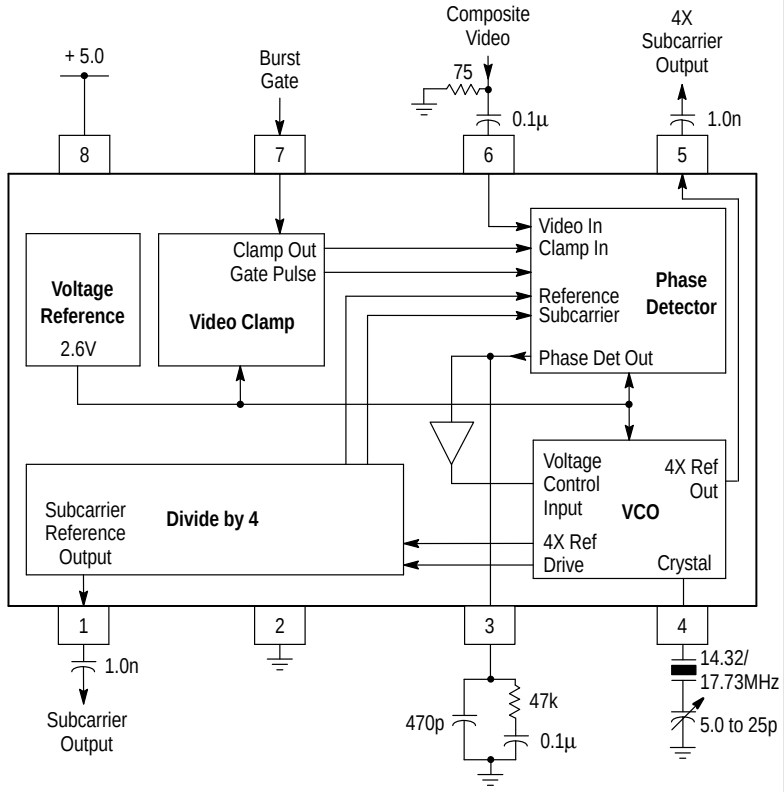
SEMICONDUCTOR TECHNICAL DATA



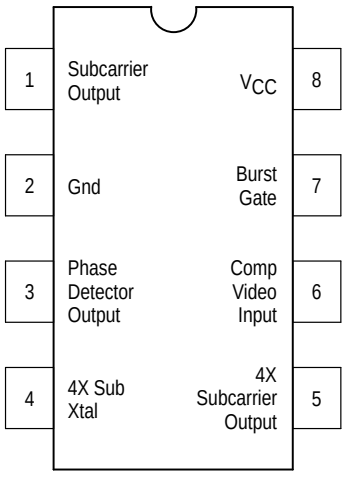
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44144D	T_A = 0° to +70°C	SO–8
MC44144P		Plastic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Ambient Temperature	T_A	0° to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage	8	V_{CC}	4.5	5.0	5.5	Vdc
Composite Video Input (Note 1) Burst Amplitude to Acquire Lock	6	–	50	300	1000	mVpp

NOTE: 1. Total peak–to–peak voltage of video should not exceed ground or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

Characteristic		Pin	Min	Typ	Max	Unit
Operating Current		8	8.0	10	12	mA
Burst Gate Threshold Voltage:	V_{IH}	7	3.0	–	–	Vdc
	V_{IL}		–	–	1.5	
Burst Gate Input Current:	I_{IH} (V_{in} = 5.0 V)		–	–	20	μA
	I_{IL} (V_{in} = 0 V)		–	–	–0.5	
4X Subcarrier		5				
Output Voltage: (14.32 MHz)			400	610	650	mVpp
(17.73 MHz)			–	450	–	
Output Impedance: (14.3 MHz and 17.73 MHz)			–	25	–	Ω
Subcarrier Output						
Output Voltage: (3.58 MHz and 4.43 MHz)			200	300	400	mVpp
Output Impedance: (3.58 MHz and 4.43 MHz)		1	–	200	–	Ω
Phase Angle (Note 1)			–	–60	–	deg
Phase Sensitivity (Notes 1 & 2)			–	3.0	–	Note 2
Static Phase Error (Note 2)		1, 2	–	3	–	deg/100 Hz
Phase–Locked Loop Pull–In Range			–	± 350	–	Hz
Phase–Locked Loop Hold–In Range			–	± 500	–	

NOTES: 1. Referenced to composite video input color burst.
2. See paragraph 1 of the Functional Description text.

Figure 1. Typical VCXO Gain

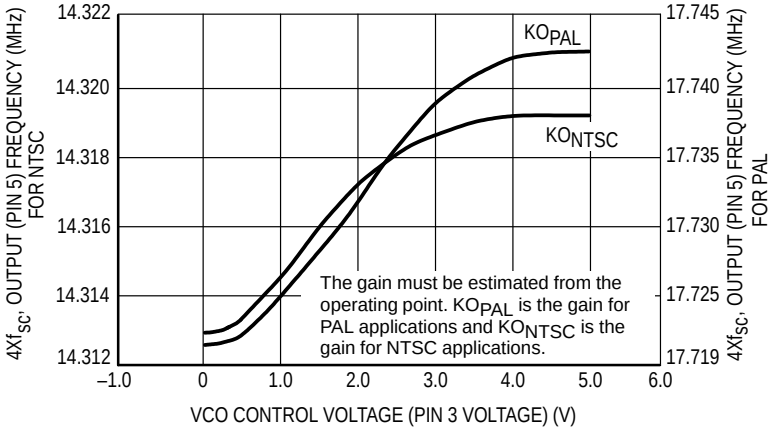
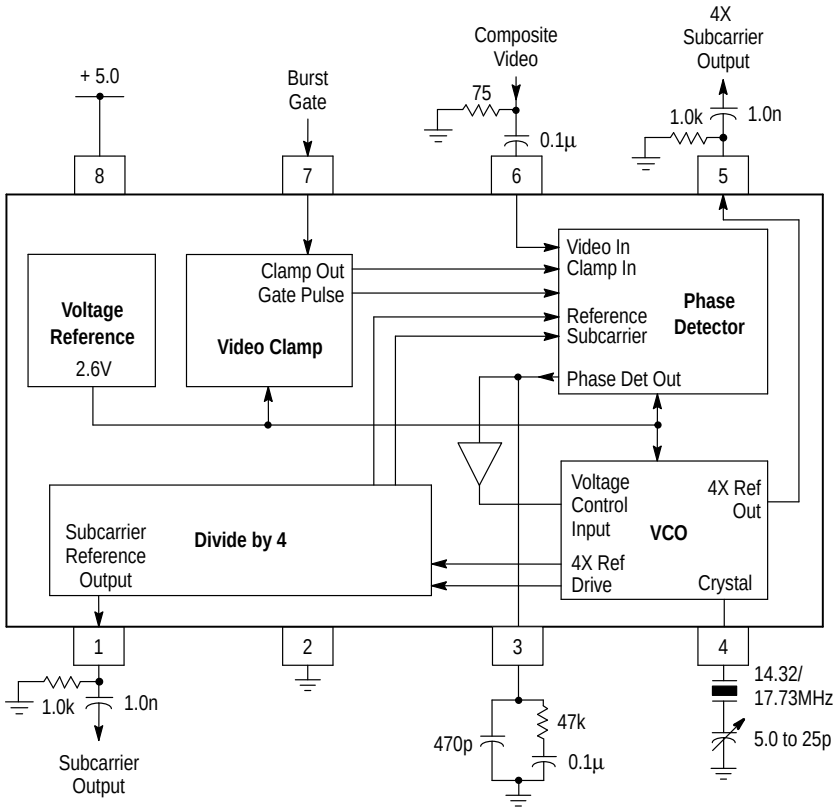


Table 1. Crystal Specifications

Frequency	14.31818 MHz (NTSC) 17.734475 MHz (PAL)
Mode	Fundamental
Frequency Tolerance @ 25°C df/dfo 0°C – 70°C	40 ppm
Load Capacitance	20 pF
ESR	50 Ω
C1 (Internal Series Capacitance)	15 mpF

Figure 2. Representative Schematic Diagram



FUNCTIONAL DESCRIPTION

The MC44144 is designed to implement the color sync function in a video system. When provided NTSC/PAL composite video or composite chroma and burst gate inputs, the IC will phase–lock a Voltage Controlled Crystal Oscillator (VCXO) to the color burst. Both 4X and 1X subcarrier frequency outputs are provided by the IC. The VCXO operates off of a 4X subcarrier crystal and The VCXO operates off a 4X subcarrier crystal and is capable of at least ± 600 Hz of pull–in. The tradeoff for such a wide pull–in range is a resultant "soft" lock, or a 3° phase shift per 100 Hz *change* in oscillator free–run or input reference frequency.

In addition to providing the gate pulse for the MC44144 phase detector, the Burst Gate input also initiates a clamp pulse that sets up the level of the composite video at the input to the Phase Detector. The start and duration of the Gate Pulse should be timed so that the pulse envelopes the color burst of the video signal, but not so wide as to gate sync or video into the Phase Detector.

The Phase Detector is enabled when the voltage at the Burst Gate input (Pin 7) is above the nominal 2.2 V threshold. While this makes possible the ability to lock to a color burst, it does not exclude the possibility of lock to a constant reference. If a constant source is to be the reference, the Phase Detector can be permanently enabled by holding the voltage on the Phase Detector input pin higher than the threshold voltage.

The phase detector gain must be specified in two ways, for a constant reference and for a burst–locked application. The gain in a constant reference application is specified by the maximum current output with the maximum phase error. For a maximum phase error of π/2 radians the maximum current available is approximately 200 µA. So the phase detector gain is defined as,

$$KPD = 200/(\pi/2)(\mu A/rad \bullet sec)$$

For a burst–locked application, the Phase Detector is active for only the duration of the color burst. Therefore the phase detector gain must be specified as an average gain over a line period. In this case the phase detector gain for NTSC and for PAL applications is,

$$KPD_{NTSC} = (8/(\pi/2))(\mu A/rad \bullet sec) \text{ and,}$$

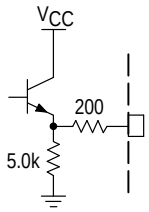
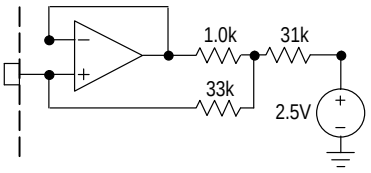
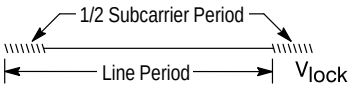
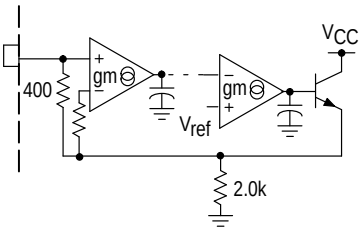
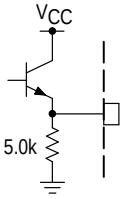
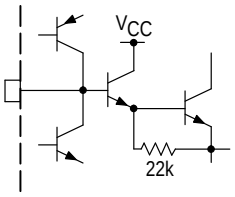
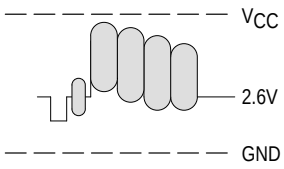
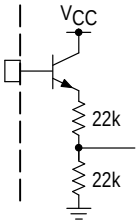
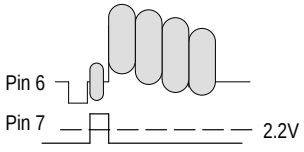
$$KPD_{PAL} = (7/(\pi/2))(\mu A/rad \bullet sec)$$

A suitable filter for both types of applications is shown in the test schematic Figure 2. This same filter also works for both NTSC and PAL applications.

The 4X subcarrier Voltage Controlled Crystal Oscillator (VCXO) uses a design that enables the use of series or parallel resonant types of crystals. Still, layout and crystal positioning are critical as the oscillator frequency is sensitive to shunt capacitance. Care should be taken to keep the crystal close to the IC and crystal switching should be avoided. A suitable parallel type crystal would meet the specifications in Table 1.

A plot showing the VCXO gain is shown in Figure 1. From this plot the gain must be estimated from the operating point. KO_{PAL} is the gain for PAL applications and KO_{NTSC} is the gain for NTSC applications.

PIN FUNCTION DESCRIPTION

Name	Pin	Representative Circuitry	Description	Expected Waveforms
Subcarrier Output	1		Subcarrier Output. A phase–locked reference of the PAL or NTSC color burst is output at this pin.	A 300 mVpp square wave is output. Some high frequency content is present.
Ground	2		Circuit Ground	
Phase Detector Output	3		The error current from the phase detector is output at this pin. A filter circuit should be connected at this pin.	A beat waveform, showing both horizontal period and half the subcarrier period, is present. 
4X Sub Xtal	4		Crystal Oscillator Pin. A 4X subcarrier parallel resonant crystal, in series with a 5.0 to 25 pF trimmer capacitor provides the resonant element for the Voltage Controlled Crystal Oscillator (VCXO).	Approximately 40 mVpp. A scope probe will disturb the frequency of oscillation.
4X Subcarrier Output (or Black Burst)	5		Buffered output from the 4X voltage controlled oscillator.	The sinusoidal 4Xf_{SC} oscillator output is available at this pin. The output is nominally: 525 mVpp for NTSC, 425 mVpp for PAL.
Composite Video Input (Black Burst, Continuous Wave, or Composite Chroma can also be applied)	6		Composite Video Input. Color burst from the video present at this pin is used as a reference to phase lock the VCXO. Positive or negative video may be used.	Composite video should be applied at this pin. The color burst amplitude of the input video should be at least 50 mV, but no more than 1000 mV. The waveform at this pin should not exceed ground or V_{CC}. 
Burst Gate Input	7		Input for the phase detector gate pulse. TTL compatible. The threshold is nominally 2.6V.	A positive going gate pulse should be applied at this pin. The Burst Gate input should envelope the color burst. 
V_{CC}	8		Power Supply Pin. 5.0 Vdc should be applied at this pin.	

Linear and TTL Output Buffers

The output buffers of the MC44144 are not designed to any specific logic family. If it is desired, Linear or TTL buffers can be added externally. Figure 3 shows an example of a Linear buffer using an MC3346 Transistor array; virtually any utility transistor can be used. Figure 4 shows a TTL type buffer using an MC74LS04 buffer.

Figure 3. Linear Buffer

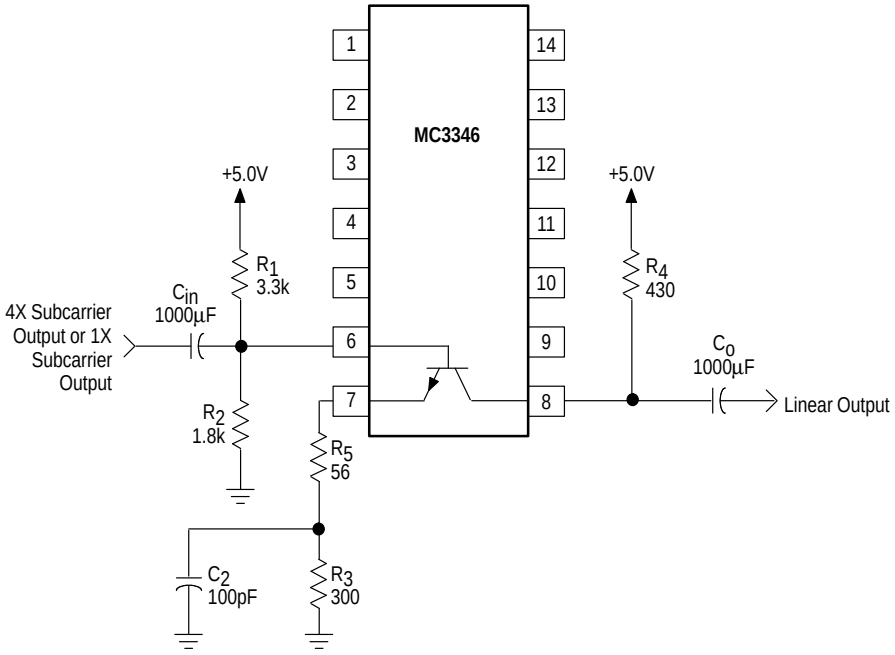
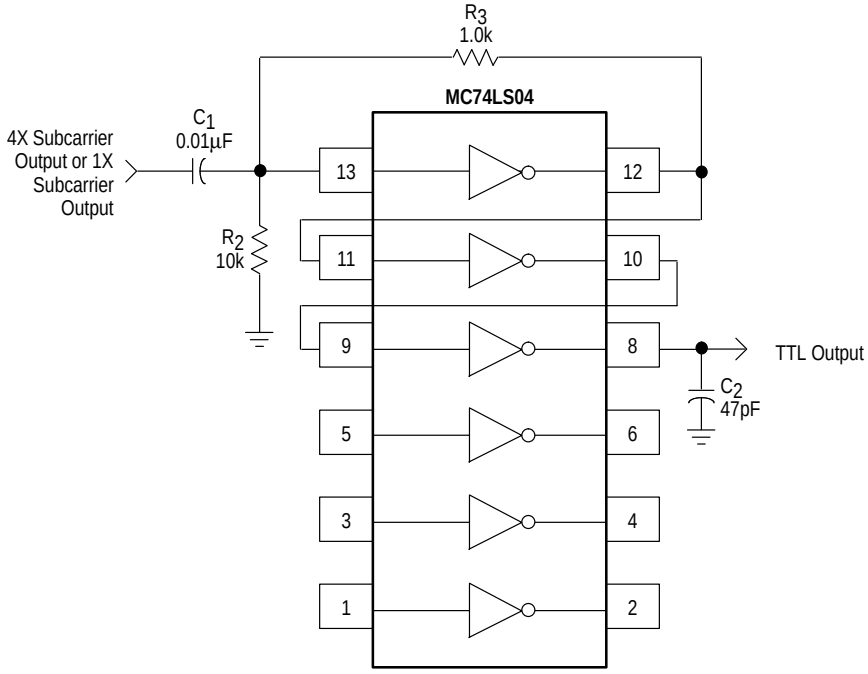
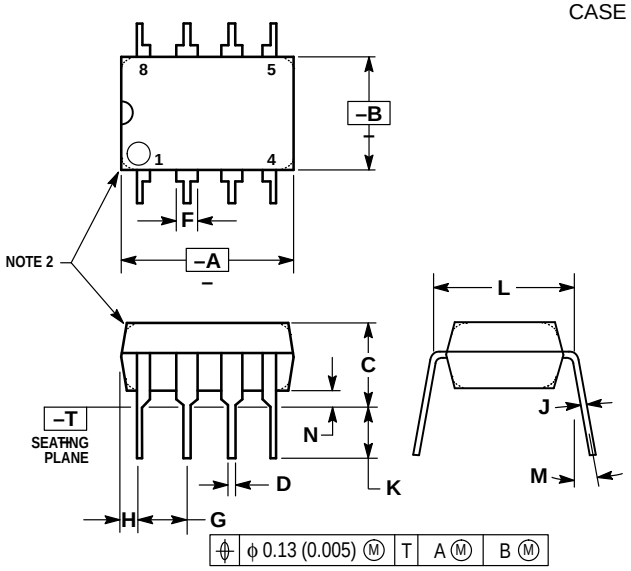


Figure 4. TTL Buffer



OUTLINE DIMENSIONS

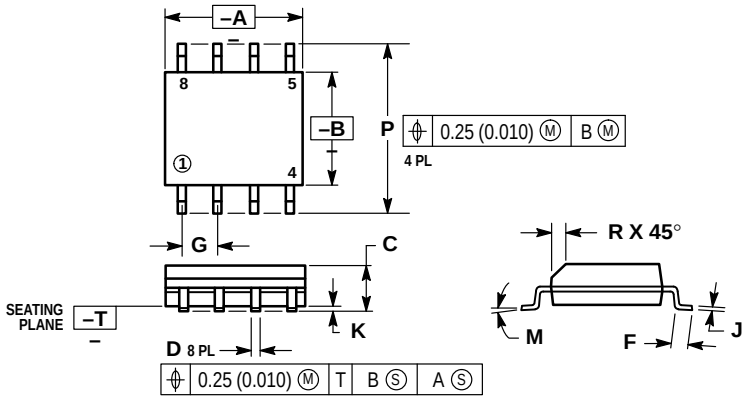
P SUFFIX
PLASTIC PACKAGE
CASE 626–05



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. 626–03 AND 626–04 OBSOLETE, NEW STANDARD 626–05.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–03
(SO–8)



NOTES:
1. DIMENSIONS “A” AND “B” ARE DATUMS AND “T” IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION “A” AND “B” DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751–01 AND –02 OBSOLETE, NEW STANDARD 751–03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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