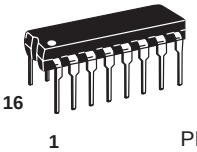
MC44140

Chroma Delay Line
HCMOS Technology

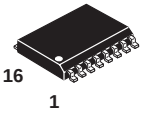
The MC44140 is a monolithic 64 µs delay line, intended for color TV applications. It may be used as a baseband chroma correction circuit (with PAL), or as a chroma delay line (with SECAM).

The device has been designed for use with the MC44000 as part of CHROMA 4, or with the MC44011, but may also be used as a general purpose delay line for other applications.

- Part of SYSTEM 4 Concept
- Works with Baseband Color Difference Signals
- PAL (4.43 MHz)/SECAM/NTSC Capability
- Uses 17.734475 MHz Clock with PAL/SECAM Signals
- 8–Bit Sampling at 1/6 Clock Frequency
- External Inputs (Satellite ....)
- Minimum Number of External Components
- Low Current (35 mA), + 5 V Supply



P SUFFIX
PLASTIC PACKAGE
CASE 648–08

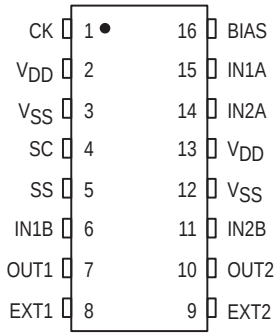


DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02

ORDERING INFORMATION

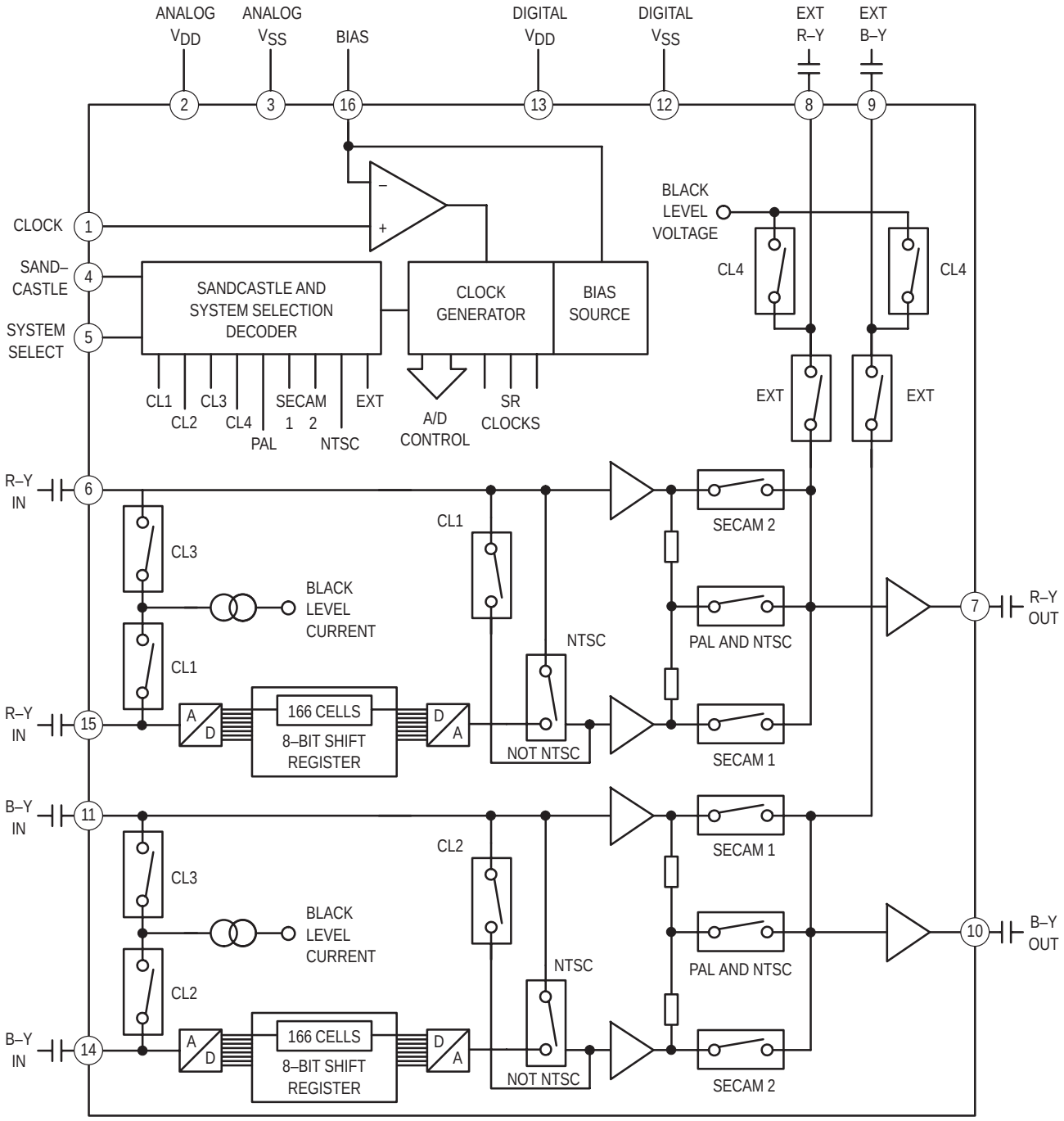
MC44140P	Plastic DIP
MC44140DW	SO–L

PIN ASSIGNMENT



MOTOROLA

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Symbol	Function
2	V_{DD}	Positive supply voltage.
3	V_{SS}	Supply ground.
1	CK	System clock. Supplied from MC440XX master clock. Either 17.734475 MHz (PAL and SECAM) or 14.31818 MHz (NTSC) sine wave.
5	SS	System selection. 4–level signal supplied by MC440XX to indicate whether color difference signals are PAL, NTSC, SECAM, or EXTERNAL.
4	SC	Sandcastle pulse. Periodic multi–level signal supplied by MC440XX. The pulse has 4 levels to indicate the timing of black level, ident. gate, and active signal, together with a level changing every other line. Used to control the clamps and for the timing of the SECAM switching.
15 14	IN1A IN2A	R–Y (IN1) and B–Y (IN2) inputs to the A/D converters. Baseband color difference (0 to 1.2 MHz) signals supplied by MC440XX via external coupling capacitors of a value greater than 560 nF; these may originate from PAL, NTSC, or SECAM systems.
6 11	IN1B IN2B	From same source as the “A” inputs but using separate 100 nf coupling capacitors to the direct (un–delayed) inputs.
8 9	EXT1 EXT2	External R–Y (EXT1) and B–Y (EXT2) inputs. These are baseband color difference signals which are ac coupled via 10 nF capacitors from an external source.
7 10	OUT1 OUT2	R–Y (OUT1) and B–Y (OUT2) outputs. The “corrected” baseband color difference signals are returned to MC440XX via external 10 nF capacitors.
16	BIAS	Bias current. A bias current is fed to this pin by means of an external pull–up resistor of 68 kΩ, in order to set the dc operating point of the operational amplifiers. An external decoupling capacitor to GND of 10 nF is required.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C
Package Power Dissipation	P_D	500	mW

GENERAL ELECTRICAL CHARACTERISTICS

Parameter	Pin	Min	Typ	Max	Unit
Supply Voltage (Maximum ripple 200 mVpk–pk at 50/100 Hz)	2, 13	4.75	5.0	5.5	V
Operating Current	2, 3	30	35	50	mA
Operating Power Dissipation (Ext. resistor: R BIAS = 68 kΩ)		143	175	275	mW

BIAS CURRENT (BIAS)

Parameter	Pin	Min	Typ	Max	Unit
Current (Ext. resistor; R BIAS = 68 kΩ)	16	—	60	—	µA

CLOCK INPUT (CK)

Parameter		Pin	Min	Typ	Max	Unit
Frequency	PAL/SECAM NTSC	1	— —	17.734475 14.318180	— —	MHz
Amplitude (Sinusoidal signal)		1	50	—	1000	mVpp

CLAMP

Parameter		Pin	Min	Typ	Max	Unit
Clamp Current (Absolute Value)	Sinked if V_{in} > Vclamp) Sourced if V_{in} < Vclamp	6, 11 14, 15	10 80	25 150	40 220	µA
Clamp Voltage (VCLAMP)		8, 9	1.3	1.4	1.5	V

DELAYED SIGNAL CHARACTERISTICS

Parameter		Min	Typ	Max	Unit
Sampling Frequency (Sixth of CK frequency)		—	2.95	—	MHz
Number of Samples (Per line period and per signal)		166	166	166	
Resolution		7	—	8	bit
Delay Value (Equal to sandcastle period for PAL/NTSC or to half this period for SECAM)		—	64	—	µs
Gain		– 0.9	0.0	0.9	dB
Gain Mismatch Between the Two Lines		—	—	2	%
Gain Mismatch Between Direct and Delayed Signals		—	—	2	%
Impedance	Input Output	10 k —	— 220	— —	Ω
Non–Linearity	Differential Integral	— —	— —	± 1 ± 2	LSB %

COLOR DIFFERENCE INPUT SIGNALS (IN1A, IN1B, IN2A, and IN2B)

Parameter		Pin	Min	Typ	Max	Unit
B–Y Voltage Range (peak to peak)		6, 15	—	—	1.8	V
R–Y Voltage Range (peak to peak)		11,14	—	—	1.8	V
DC Level (Relative to black level) (For SECAM only; when R–Y, B–Y absent)			– 0.3	—	+ 0.3	V
Bandwidth			0.0	—	1.2	MHz
Line Period	625–Line Systems 525–Line Systems		61.7 63.0	64.0 63.5	66.7 64.0	µs
Active Signal Duration	625–Line Systems 525–Line Systems		— —	52.0 51.6	— —	µs
Black Level Duration	PAL/NTSC 625–Line PAL/NTSC 525–Line SECAM		— — —	12.0 11.9 6.0	— — —	µs

SANDCASTLE TIMING CHARACTERISTICS (Pin 4)

Parameter		Min	Typ	Max	Unit
Signal Period	PAL/NTSC 625–Line PAL/NTSC 525–Line SECAM	— — —	64.0 63.5 128.0	— — —	µs
Level “0” Duration	PAL/NTSC 625–Line or SECAM 1 PAL/NTSC 525–Line	— —	54.0 53.5	— —	µs
Level “1” Duration (only for SECAM 2)		—	54.0	—	µs
Level “2” Duration		—	5.0	—	µs
Level “3” Duration		—	5.0	—	µs
Safety Margin Between Start/Finish of Active Signal and Start/Finish of Level “0” or Level “1”		0.0	1.0	2.0	µs

FUNCTIONAL DESCRIPTION

The MC44140 has been designed and is intended as a companion device to the MC440XX decoders. As such the MC44140 is used as a baseband chroma correction circuit with PAL, and as the one line delay for SECAM. The device is also compatible with NTSC color difference signals which do not require any correction, and has the facility for routing external R–Y and B–Y signals (e.g., from satellite or from field store feature systems).

The block diagram for the MC44140 appears at the beginning of this document. The baseband color difference signals are derived in the MC440XX by demodulation of the chrominance part of the video signal. They are then ac coupled into the MC44140 and black level clamped. Each of the channels has a direct path and a path containing a delay of one line (64 μs). The clamped signals from pins 14 and 15 are taken from the input and A/D converted to a 8–bit wide digital data stream; this then passes through shift registers containing 166 cells in order to realize the one line delay. After this, the data is converted back into analog signals by means of D/A converters. The clocks for the converters are derived by dividing by 6 the frequency obtained from the CHROMA 4 master oscillator, which consists of a crystal running at 17.734475 MHz for PAL and SECAM. Timing of the switches and clamps in the circuit is achieved by means of a special sandcastle pulse provided by the MC440XX. Mode selection is also undertaken by the MC440XX by means of a 4 voltage level output supplied to pin 5.

Color difference signals provided by the MC440XX may originate from any one of PAL, SECAM, or NTSC, so the treatment of these incoming signals is different according to the mode selected; as determined by the SYSTEM SELECT level emanating from the MC440XX. Referring to the block diagram, it is possible to follow the procedure adopted for each standard. The clamping action may be interpreted in each case from Figures 1 thru 4.

In the case of PAL signals, black level clamps CL1 and CL2 are in use every line. Considering only the R–Y channel, it will be seen that the signal is ac coupled into the circuit at pin 6 (direct) and pin 15 (delayed). CL1 clamps the input at pin 15 to the BLACK LEVEL VOLTAGE, this signal then passes through the delay line. The second CL1 clamp uses the dc level present after the delay line to clamp the black level of the direct path. The two signals are then buffered and averaged together, and the result is switched through to the output at pin 7.

For NTSC color difference signals, black level clamps CL1, 2 and 3 are all in use on every line. Again considering the R–Y channel, the inputs at pins 6 and 15 are both clamped to BLACK LEVEL VOLTAGE by CL1 and CL3. The delayed path is now switched out of circuit, however, as this is not required with NTSC. The direct path only is then routed to the output at pin 7.

The nature of the SECAM color difference signals is somewhat different from the other standards in that the signal is only present on every other line as is indicated in Figure 3. For the R–Y channel, the delayed path input is clamped to BLACK LEVEL VOLTAGE by CL1 at pin 15. The direct path signal is clamped by the other CL1 switch to the dc level of the delayed path (including any offsets) to ensure there is no difference in clamping level between the two paths. During the period “SECAM 1”, the B–Y signal is present and this is clamped to the delayed path dc level. Switch SECAM 1 is closed during this time and so the direct signal passes straight to the output. During the next line period (SECAM 2) there is no direct path signal; now switch SECAM 2 is closed and switch SECAM 1 is open. Therefore, the delayed path signal is now switched through to the output. For the R–Y channel the exact reverse process will occur as in this case the direct path signal is present during the “SECAM 2” lines.

When EXT R–Y and B–Y signals are used, these are assumed to be always “corrected” from whichever source they originate. These signals are ac coupled into the circuit at pins 8 and 9 and are switched straight through to the outputs, using clamps CL4 to set the black level voltage of the two channels line by line.

SIGNALS SUPPLIED BY MC440XX DECODERS

Sandcastle Pulse

This is a multi–level line repetitive timing pulse input to pin 4 of the IC. The signal provides timing commands to the clamp circuits CL1, CL2, CL3, and CL4 and is also necessary for the clock generator to indicate the beginning of active signal storage. The pulse train contains a level changing at half line rate which is used to control the switches SECAM 1 and SECAM 2 when the circuit is operating in the SECAM mode. Tables 1 and 2 explain the meaning of the different levels as used with the sandcastle pulse. It should be noted that “level 1” of the pulse is only used for line by line switching in SECAM mode.

System Selection Signal

This input may have any one of four different dc voltage levels and is used to command the functioning of the NTSC, PAL and NTSC, SECAM 1, SECAM 2 and EXT switches of the block diagram for the four possible modes of operation. For the SECAM mode this signal together with the sandcastle pulse command switches SECAM 1 and SECAM 2. The significance of the different levels is given in Table 3.

Input Color Difference Signals

The general appearance of the baseband inputs as derived from the MC440XX with a color bars input, is shown in Figures 1 thru 4. Each of the color difference signals has two ac coupled inputs to the MC44140. The line period is 64 μs for 625 line systems and 63.5 μs for 525 line systems. Whichever line standard is in use, only about 52 μs of active signal time needs to be stored and delayed for one line period for processing.

The PAL and NTSC inputs are both present at the same time on every line and black level is provided during the whole of the line blanking period (sandcastle periods 2 and 3) to serve as a reference for the active signal. With SECAM only one color difference signal is provided on any given line by the MC440XX, while the other is replaced by a dc level for the duration of that line period. On the following line the sequence is then reversed. For the signal provided, black level is supplied during blanking time minus the ident. gate period (i.e., sandcastle period 3 only).

Output Color Difference Signals

Whatever the origin of the input signals, the two outputs supplied at pins 7 and 10 are always corrected signals which are then ac coupled back to the MC440XX. Black level is pro-

vided during the whole line blanking period to allow the MC440XX to clamp the signals on the other end of the external output coupling capacitors.

Differential Clock Input

Pins 1 and 16 form a differential clock input of high sensitivity and good noise rejection. Pin 16 is an ac ground of the differential input and must be decoupled to ground.

APPLICATION CIRCUIT

A schematic diagram of the MC44140 application circuit is shown in Figure 5. All of the inputs/outputs shown on the left of the diagram have the MC44000 as their destination. The 17.7 MHz and 14.3 MHz crystals shown in fact form part of the MC44000 circuit; this device controls the crystal selection and applies the drive to it. The majority of the rest of the circuit consists of coupling capacitors for the signal inputs and outputs, whose function for black level clamping has already been described. A pull–up resistor is connected to pin 16 for the purpose of providing a bias current, which the IC uses to set the dc operating point of internal operational amplifiers.

Separate power supply pins (V_{DD} and V_{SS}) are provided to each of the analog section and the digital section of the chip. Both of the + 5 V supply pins are filtered using a series resistor and small ceramic and electrolytic capacitors mounted close by each supply pin and its adjacent ground pin. The supplies, especially the analog pin, should be very well bypassed in order to avoid noise interfering with the clock input (pin 1), whose input level is only some 50 mVp–p.

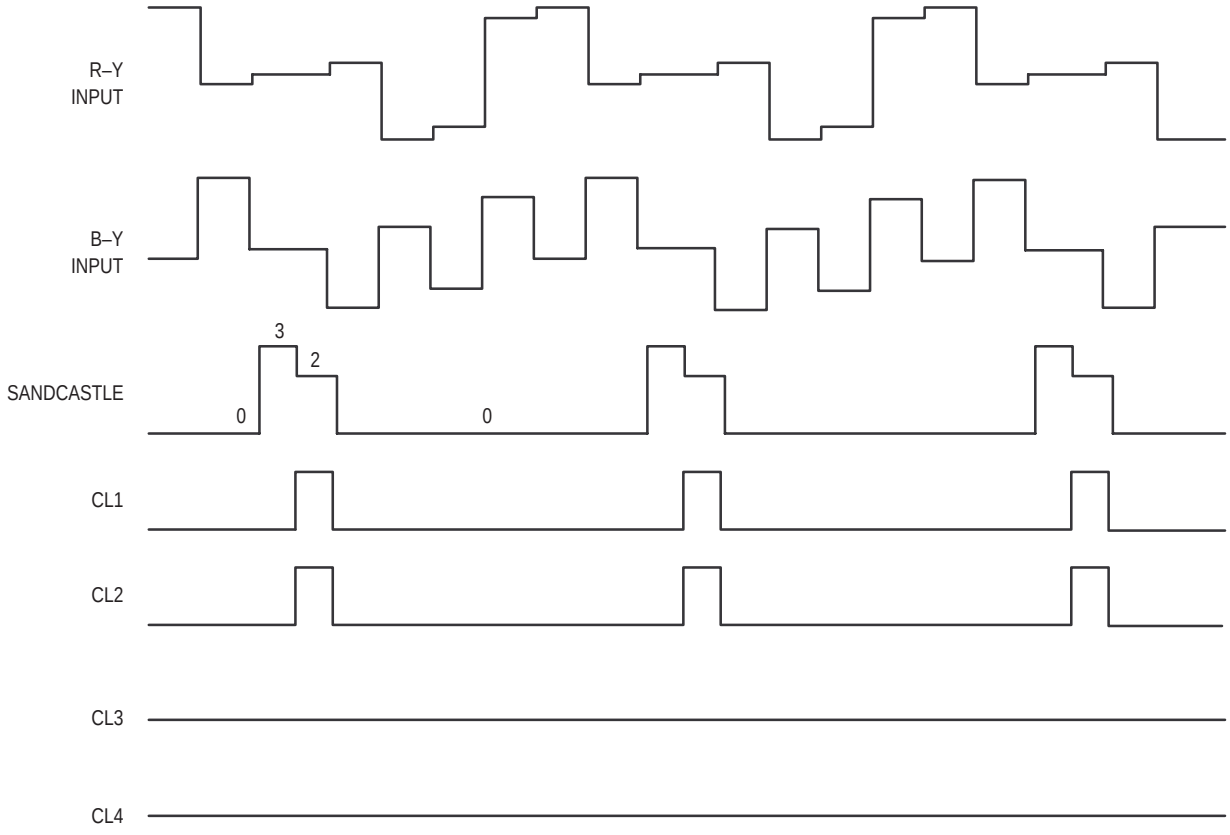


Figure 1. PAL

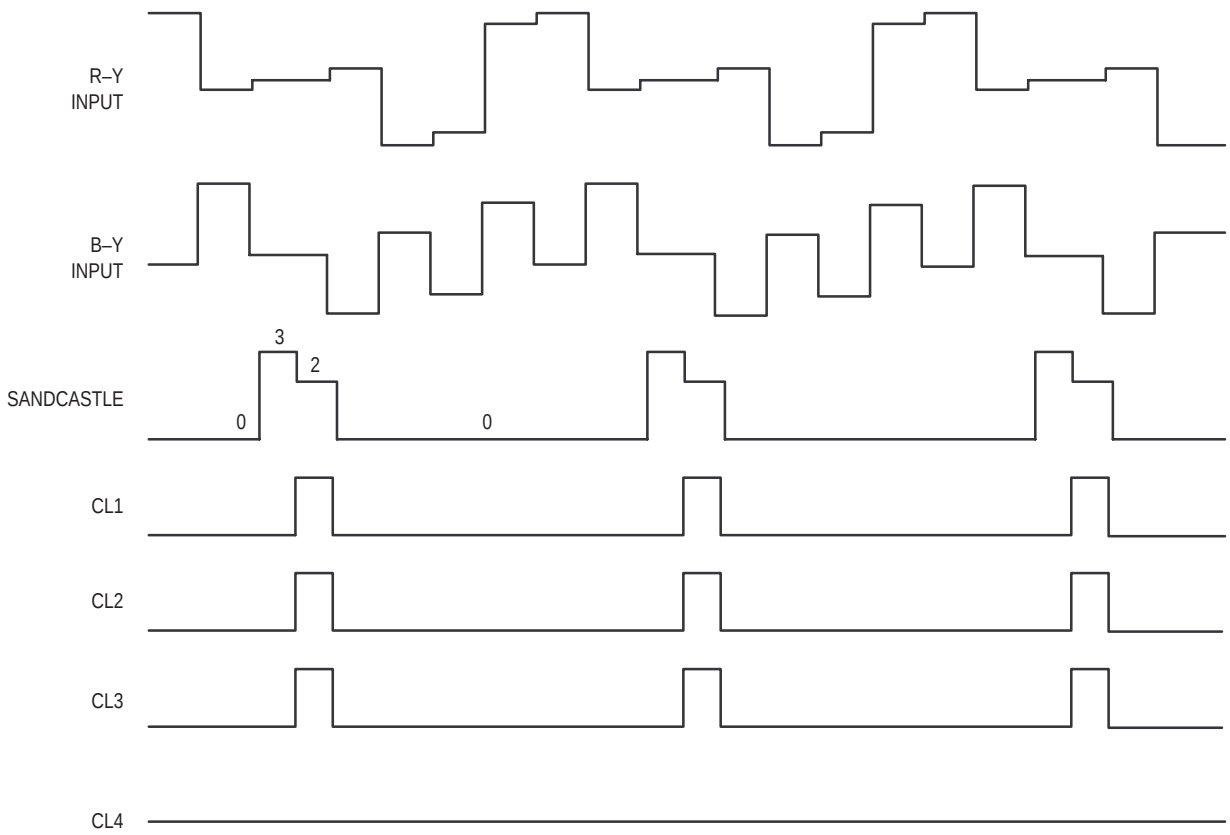


Figure 2. NTSC

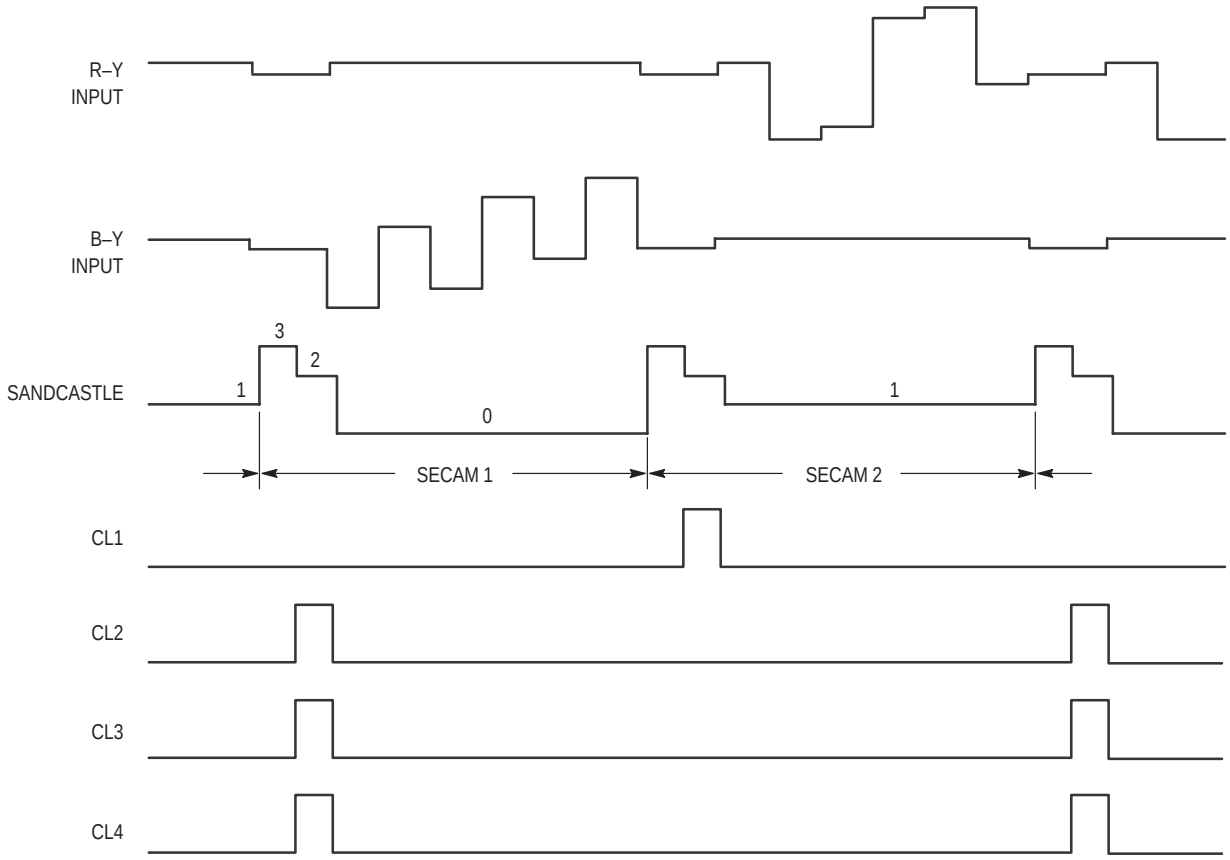


Figure 3. SECAM

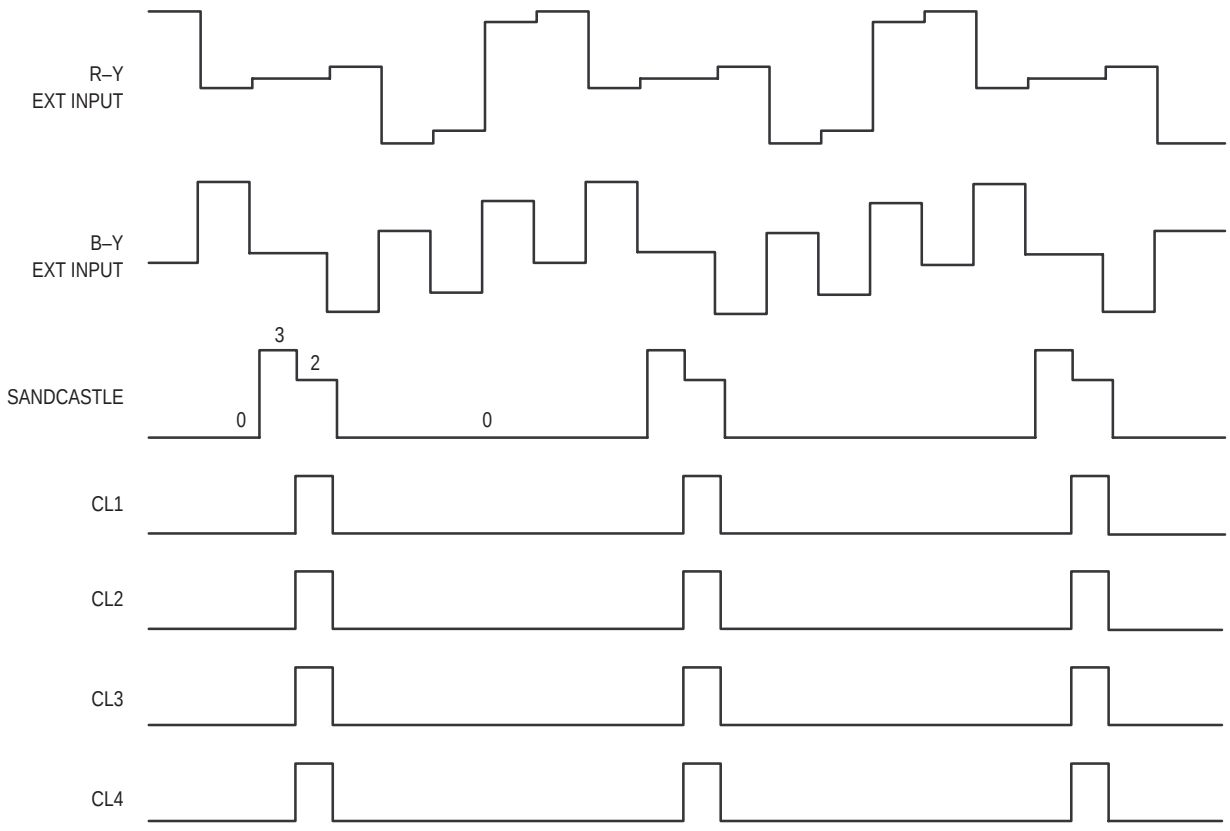


Figure 4. EXT

Table 1. Sandcastle Ident. Pulse for PAL/NTSC

Level	Meaning	Typical Duration µs	Range (V_{DD} = 5.00 V)	
			Lower Limit	Upper Limit
3	Black Level	5.0	3.67 V	5.00 V
2	Black Level	5.0	2.34 V	3.27 V
0	Active Signal PAL NTSC	54.0 53.5	0.00 V —	0.50 V —

Table 2. Sandcastle Ident. Pulse for SECAM

Level in Chrono–logical Order	Typical Duration µs	Meaning		Line Period	Range (V_{DD} = 5.00 V)	
		B–Y Input	R–Y Input		Lower Limit	Upper Limit
3	5.0	Black Level	DC Level		3.67 V	5.00 V
2	5.0	Ident. Gate	DC Level		2.34 V	3.27 V
0	54.0	Active Signal	DC Level	SECAM 1	0.00 V	0.50 V
3	5.0	DC Level	Black Level		3.67 V	5.00 V
2	5.0	DC Level	Ident. Gate		2.34 V	3.27 V
1	54.0	DC Level	Active Signal	SECAM 2	0.90 V	1.94 V

Table 3. System Selection

Level	Meaning	Typical Voltage	Range (V_{DD} = 5.00 V)	
			Lower Limit	Upper Limit
0	PAL	0.00 V	0.00 V	0.50 V
1	NTSC	1.40 V	0.90 V	1.94 V
2	SECAM	2.50 V	2.34 V	3.27 V
3	EXTERNAL	5.00 V	3.67 V	5.00 V

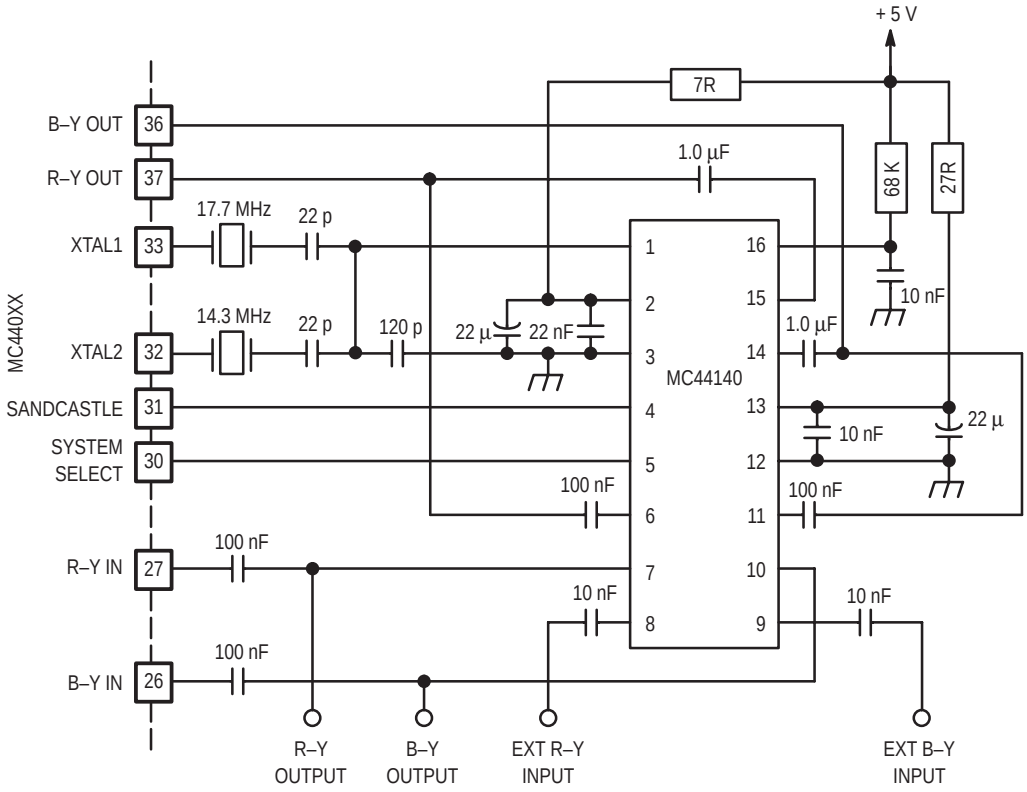
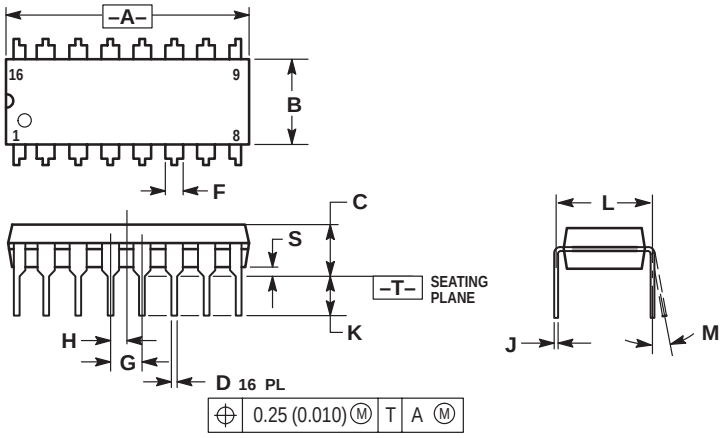


Figure 5. Application Circuit

PACKAGE DIMENSIONS

P SUFFIX
PLASTIC
CASE 648–08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

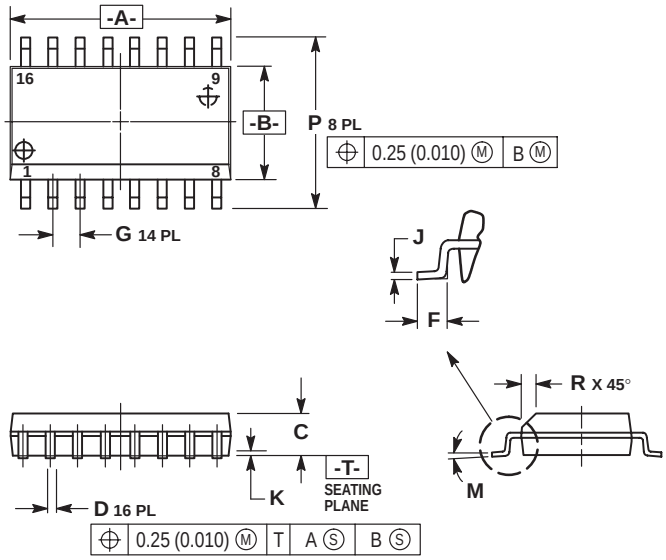
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

PACKAGE DIMENSIONS

DW SUFFIX
SO–L
CASE 751G–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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