MC10H350

PECL* to TTL Translator

(+5 Vdc Power Supply Only)

ON Semiconductor®

http://onsemi.com

Description

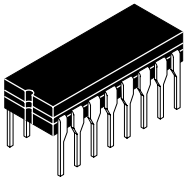
The MC10H350 is a member of the 10H family of high performance ECL logic. It consists of 4 translators with differential inputs and TTL outputs. The 3−state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

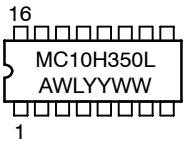
The MC10H350 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the MC10H350 to be used as an inverting or noninverting translator, or a differential line receiver. The MC10H350 can also drive CMOS with the addition of a pullup resistor.

Features

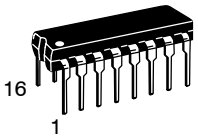
- Propagation Delay, 3.5 ns Typical
- MECL 10K™ Compatible
- Pb−Free Packages are Available*

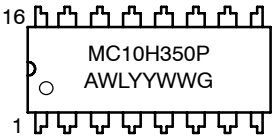
MARKING DIAGRAMS*



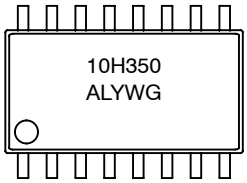


CDIP−16
L SUFFIX
CASE 620A

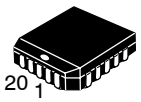


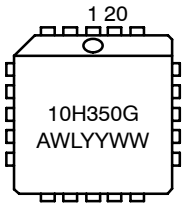


PDIP−16
P SUFFIX
CASE 648



SOEIAJ−16
CASE 966





PLLC−20
FN SUFFIX
CASE 775

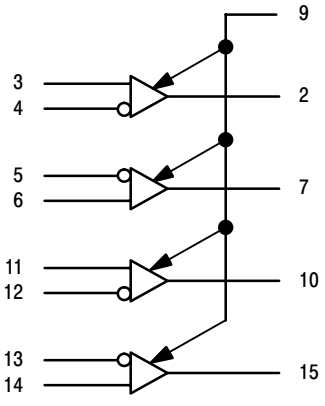
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

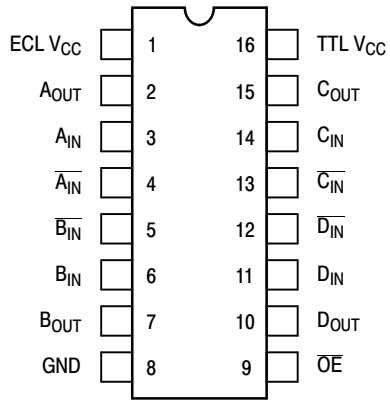
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.



V_{CC} (+5.0 VDC) = PINS 1 AND 16
GND = PIN 8

Figure 1. Logic Diagram



Pin assignment is for Dual−in−Line Package.

Figure 2. Dip Pin Assignment

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply (V_{EE} = GND)	7.0	Vdc
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range − Plastic − Ceramic	−55 to +150 −55 to +165	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 2. ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%) (Note 1)

Symbol	Characteristic		T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
I_{CC}	Power Supply Current	TTL ECL	– –	20 12	mA
I_{IH} I_{INH}	Input Current High	Pin 9 Others	– –	20 50	μA
I_{IL} I_{INL}	Input Current Low	Pin 9 Others	– –	–0.6 50	mA μA
V_{IH}	Input Voltage High	Pin 9	2.0	–	Vdc
V_{IL}	Input Voltage Low	Pin 9	–	0.8	Vdc
V_{DIFF}	Differential Input Voltage (Note 1) Pins 3–6, 11–14 (1)		350	–	mV
V_{CM}	Voltage Common Mode Pins 3–6, 11–14		2.8	V_{CC}	Vdc
V_{OH}	Output Voltage High I_{OH} = 3.0 mA		2.7	–	Vdc
V_{OL}	Output Voltage Low I_{OL} = 20 mA		–	0.5	Vdc
I_{OS}	Short Circuit Current V_{OUT} = 0 V		–60	–150	mA
I_{OZH}	Output Disable Current High V_{OUT} = 2.7 V		–	50	μA
I_{OZL}	Output Disable Current Low V_{OUT} = 0.5 V		–	–50	μA

*Positive Emitter Coupled Logic

1. Common mode input voltage to pins 3–4, 5–6, 11–12, 13–14 must be between the values of 2.8 V and 5.0 V. This common mode input voltage range includes the differential input swing.
2. For single–ended use, apply 3.75 V (V_{BB}) to either input depending on output polarity required. Signal level range to other input is 3.3 V to 4.2 V.
3. Any unused gates should have the inverting inputs tied to V_{CC} and the noninverting inputs tied to ground to prevent output glitching.

Table 3. AC PARAMETERS (C_L = 50 pF) (V_{CC} = 5.0 ± 5%) (T_A = 0°C to 75°C)

Symbol	Characteristic	T_A = 0°C to 75°C Min	T_A = 0°C to 75°C Max	Unit
t_{pd}	Propagation Delay Data (50% to 1.5 V)	1.5	5.0	ns
t_r	Rise Time (Note 4)	0.3	1.6	ns
t_f	Fall Time (Note 4)	0.3	1.6	ns
t_{pdLZ} t_{pdHZ}	Output Disable Time	2.0 2.0	6.0 6.0	ns
t_{pdZL} t_{pdZH}	Output Enable Time	2.0 2.0	8.0 8.0	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. 1.0 V to 2.0 V w/50 pF into 500 Ω.

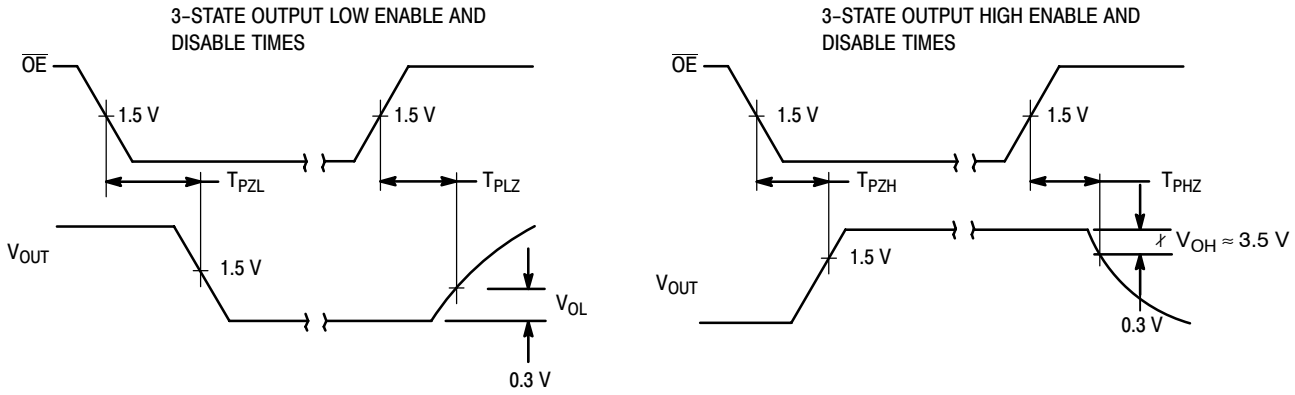
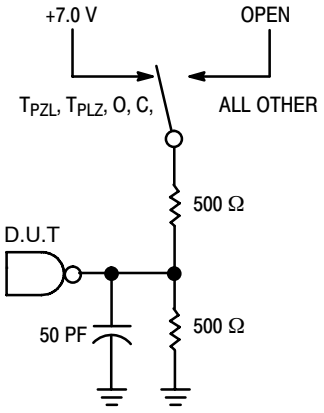


Figure 3. 3−State Switching Waveforms



*INCLUDES JIG AND PROBE CAPACITANCE

Application Note: Pin 9 is an $\overline{OE}$ and the MC10H350 is disabled when $\overline{OE}$ is at V_{IH} or higher.

Figure 4. Test Load

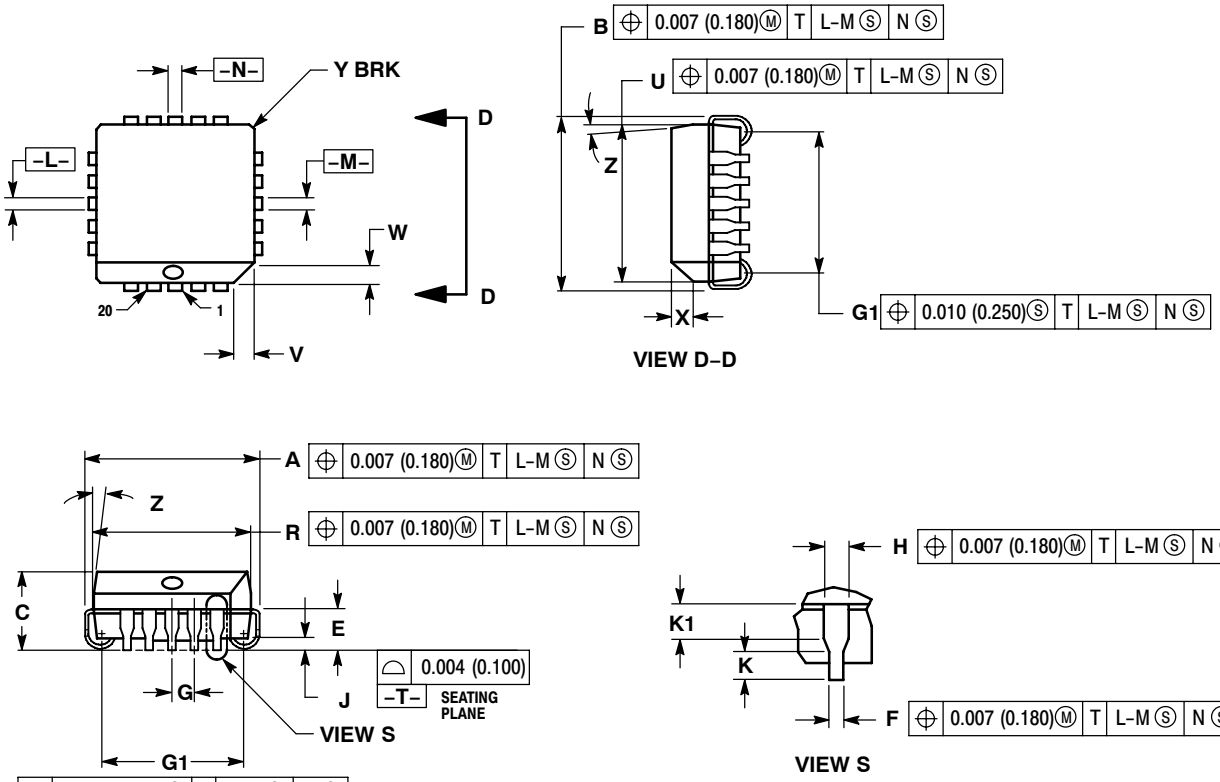
ORDERING INFORMATION

Device	Package	Shipping†
MC10H350FN	PLLC−20	46 Units / Rail
MC10H350FNG	PLLC−20 (Pb−Free)	46 Units / Rail
MC10H350FNR2	PLLC−20	500 / Tape & Reel
MC10H350FNR2G	PLLC−20 (Pb−Free)	500 / Tape & Reel
MC10H350L	CDIP−16	25 Unit / Rail
MC10H350M	SOEIAJ−16	50 Unit / Rail
MC10H350MG	SOEIAJ−16 (Pb−Free)	50 Unit / Rail
MC10H350MEL	SOEIAJ−16	2000 / Tape & Reel
MC10H350MELG	SOEIAJ−16 (Pb−Free)	2000 / Tape & Reel
MC10H350P	PDIP−16	25 Unit / Rail
MC10H350PG	PDIP−16 (Pb−Free)	25 Unit / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

20 LEAD PLLC
CASE 775−02
ISSUE E

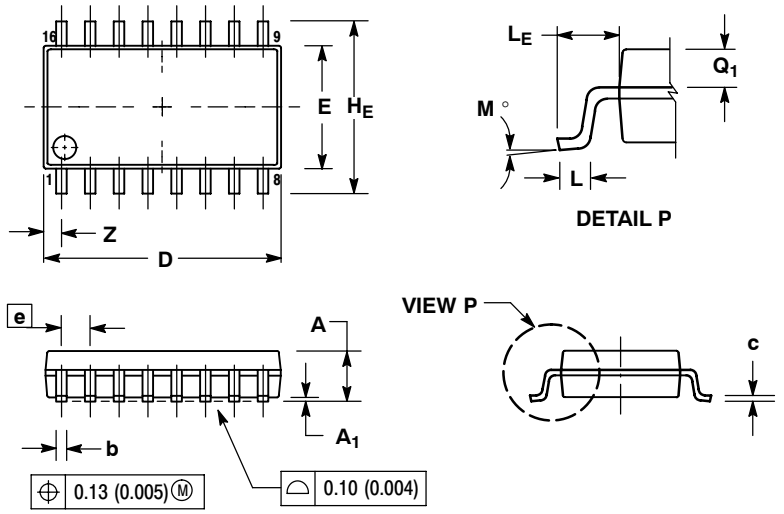


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

PACKAGE DIMENSIONS

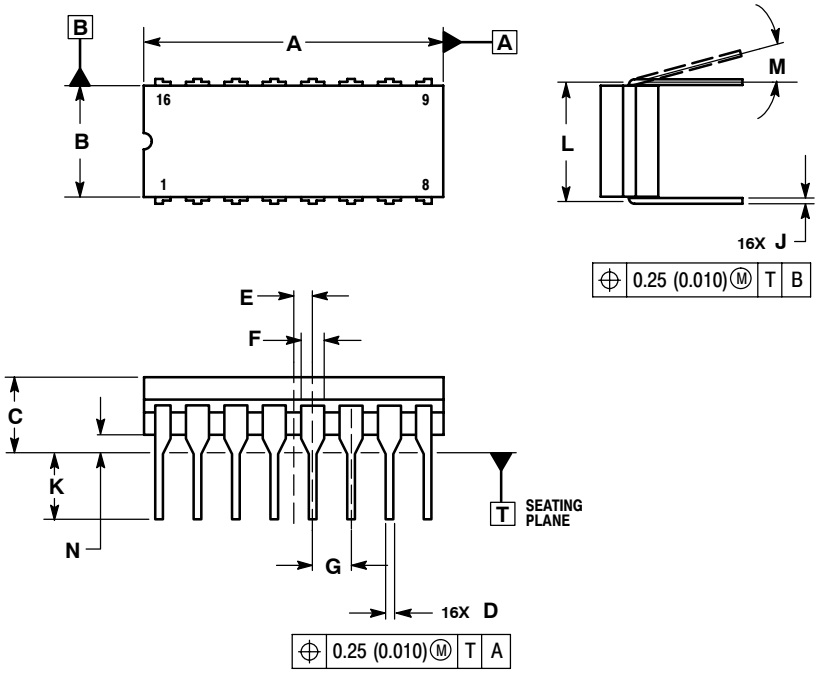
SOEIAJ−16
CASE 966−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

CDIP−16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620A−01
ISSUE O

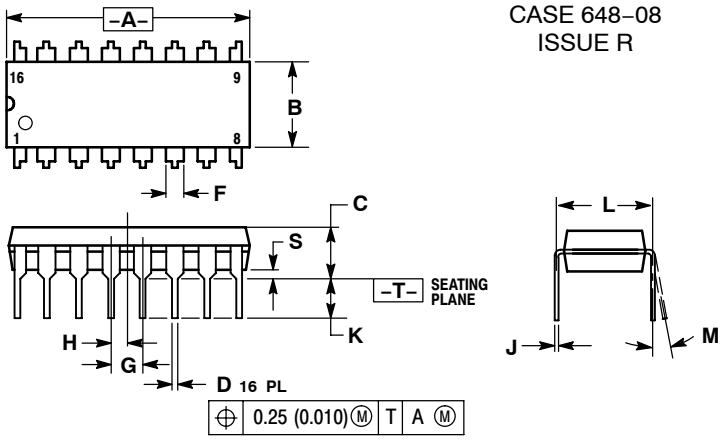


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5 THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620−10.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

PDIP−16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648−08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

MECL 10K is a trademark of Motorola, Inc.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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MC10H350/D