National Semiconductor

October 26, 2010

DS26C31MQML

CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31 is compatible with EIA standard RS-422; however, one exception in test methodology is taken . This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

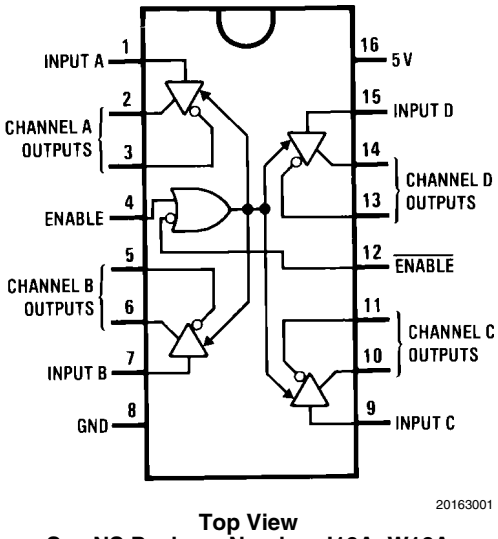
Features

- TTL input compatible
- Outputs will not load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

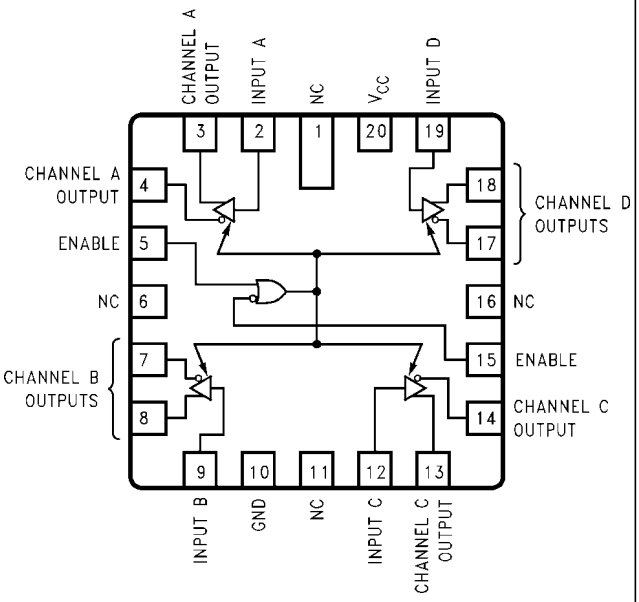
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS26C31ME/883	5962–9163901M2A	E20A	20LD LCC
DS26C31MJ/883	5962–9163901MEA	J16A	16LD Ceramic DIP
DS26C31MW/883	5962–9163901MFA	W16A	16LD Ceramic Flatpack

Connection Diagrams



Top View
See NS Package Number J16A, W16A



Top View
20-Lead Ceramic Leadless Chip Carrier (E)
See NS Package Number E20A

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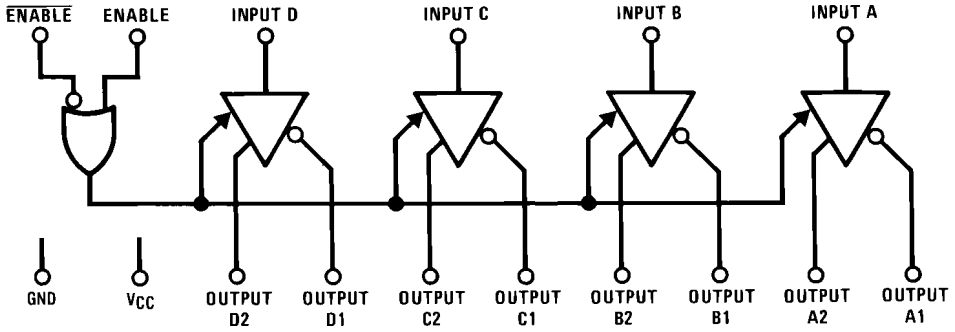
Logic Diagram



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (*Note 1*, *Note 2*)

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_I)	−1.5V to V_{CC} +0.5V
DC Output Voltage (V_O)	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_O)	±150 mA
DC V_{CC} or Gnd Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +150°C
Lead Temperature (T_L) Soldering, 4 sec.	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_I, V_O)	0	V_{CC}	V
Operating Temperature Range (T_A)	−55	+125	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS26C31M Electrical Characteristics

DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IH}	Logical "1" Input Voltage			2.0		V	1, 2, 3
V_{IL}	Logical "0" Input Voltage				0.8	V	1, 2, 3
V_{OH}	Logical "1" Output Voltage	$V_I = V_{IH}$ or V_{IL}, $V_{CC} = 4.5V$, $I_O = -20mA$		2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$V_I = V_{IH}$ or V_{IL}, $I_O = 20mA$, $V_{CC} = 4.5V$			0.5	V	1, 2, 3
V_T	Differential Output Voltage	$R_L = 100\Omega$, $V_{CC} = 4.5V$	(*Note 4*)	2.0		V	1, 2, 3
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output	$R_L = 100\Omega$, $V_{CC} = 4.5V$	(*Note 4*)		0.4	V	1, 2, 3
V_{OS}	Common Mode Output Voltage	$R_L = 100\Omega$, $V_{CC} = 5.5V$	(*Note 4*)		3.0	V	1, 2, 3
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Diff in Common Mode Output	$R_L = 100\Omega$, $V_{CC} = 5.5V$	(*Note 4*)		0.4	V	1, 2, 3
I_I	Input Current	$V_I = V_{CC}$, Gnd, V_{IH}, or V_{IL}, $V_{CC} = 5.5V$			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	$I_O = 0\mu A$, $V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(*Note 5*)		500	µA	1, 2, 3
		$I_O = 0\mu A$, $V_I = 2.4V$ or $0.5V$, $V_{CC} = 5.5V$	(*Note 5*)		2.1	mA	1, 2, 3
I_{OZ}	TRI-STATEOutput Leakage Current	$V_O = V_{CC}$ or Gnd, Enable = V_{IL}, $V_{CC} = 5.5V$, $\overline{\text{Enable}} = V_{IH}$			±5.0	µA	1, 2, 3
I_{SC}	Output Short Circuit Current	$V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(*Note 4*), (*Note 6*)	-30	-150	mA	1, 2, 3
I_{Off}	Output Leakage Current "Power Off"	$V_{CC} = 0V$, $V_O = 6V$			100	µA	1, 2, 3
		$V_{CC} = 0V$, $V_O = 0V$			-100	µA	1, 2, 3

AC Parameters - Propagation Delay Time *Figure 1*

The following conditions apply, unless otherwise specified. $V_{CC} = 5V$, $t_R \leq 6ns$, $t_F \leq 6ns$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}	Input to Output Prop Delay	*Figure 2*			14	ns	9, 10, 11
t_{PHL}	Input to Output Prop Dalay	*Figure 2*			14	ns	9, 10, 11
	Skew		(*Note 7*)		3.0	ns	9, 10, 11
t_{TLH}	Output Rise Time	*Figure 4*			14	ns	9, 10, 11
t_{THL}	Output Fall Time	*Figure 4*			14	ns	9, 10, 11
t_{PZH}	Output Enable Time	*Figure 3*			22	ns	9, 10, 11
t_{PZL}	Output Enable Time	*Figure 3*			28	ns	9, 10, 11
t_{PHZ}	Output Disable Time	*Figure 3*	(*Note 8*)		12	ns	9, 10, 11
t_{PLZ}	Output Disable Time	*Figure 3*	(*Note 8*)		14	ns	9, 10, 11

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Unless otherwise specified, min/max limits apply across the recommended operating temperature range.

Note 4: See EIA Specification RS-422 for exact test conditions.

Note 5: Measured per input. All other inputs at V_{CC} or GND.

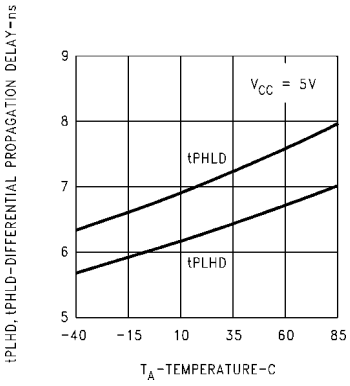
Note 6: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Note 7: Skew is defined as the difference in propagation delays between complimentary outputs at the 50% point.

Note 8: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off.

Typical Performance Characteristics

Differential Propagation Delay vs Temperature



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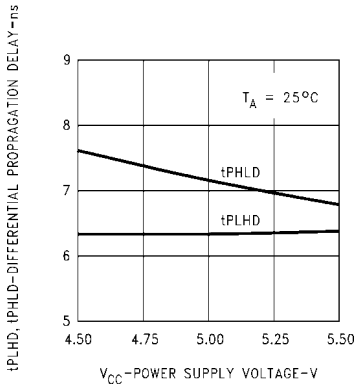
Differential Propagation Delay vs Power Supply Voltage



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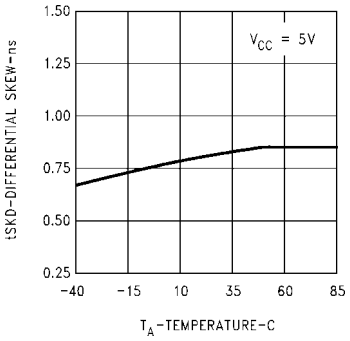
Differential Skew vs Temperature



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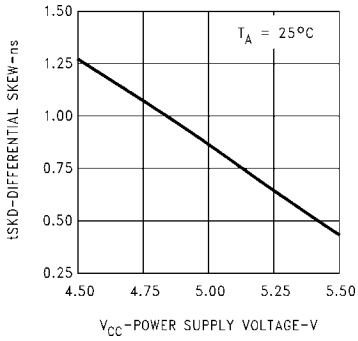
Differential Skew vs Power Supply Voltage



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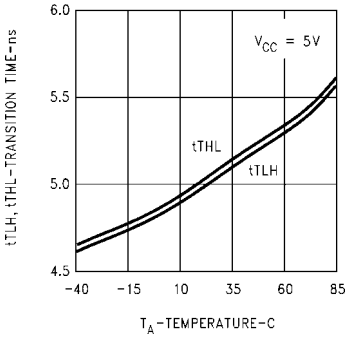
Differential Transition Time vs Temperature



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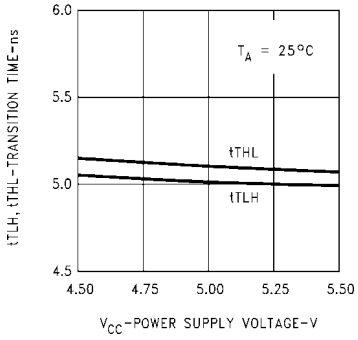
Differential Transition Time vs Power Supply Voltage



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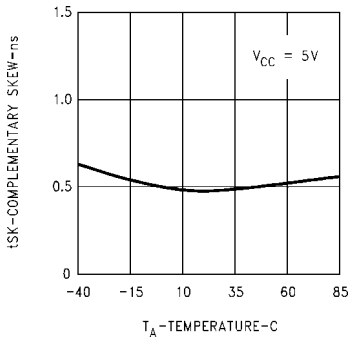
Complementary Skew vs Temperature



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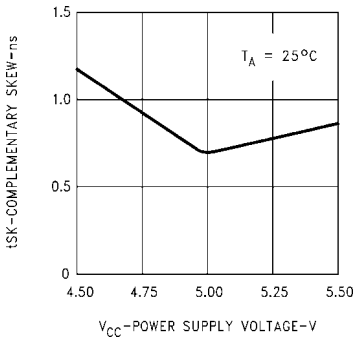
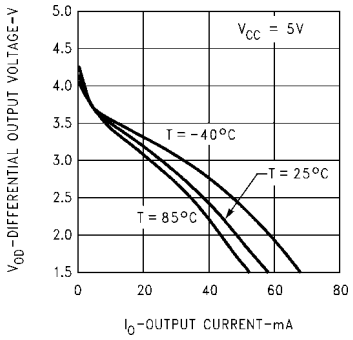
Complementary Skew vs Power Supply Voltage



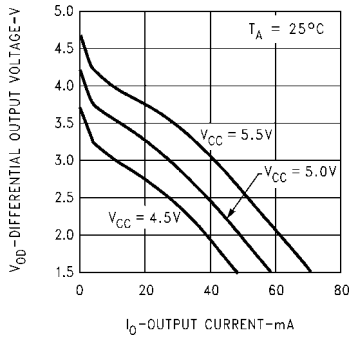
20163021

Differential Output Voltage vs Output Current



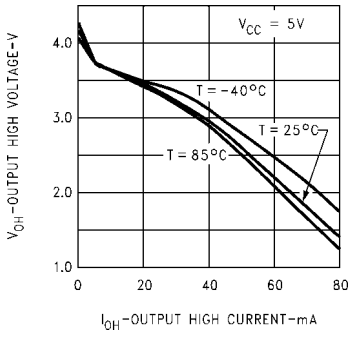
20163022

Differential Output Voltage vs Output Current



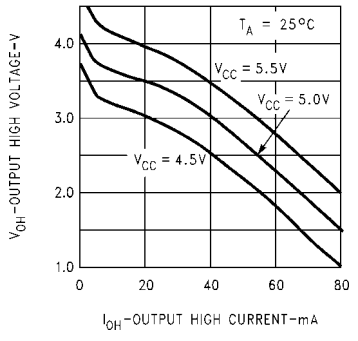
20163023

Output High Voltage vs Output High Current



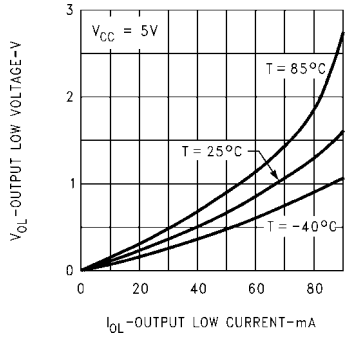
20163024

Output High Voltage vs Output High Current



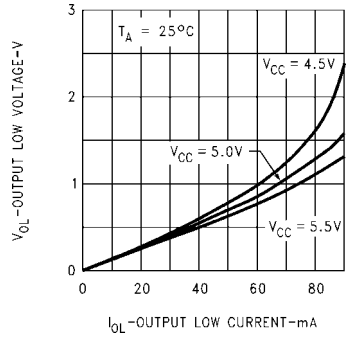
20163025

Output Low Voltage vs Output Low Current



20163026

Output Low Voltage vs Output Low Current



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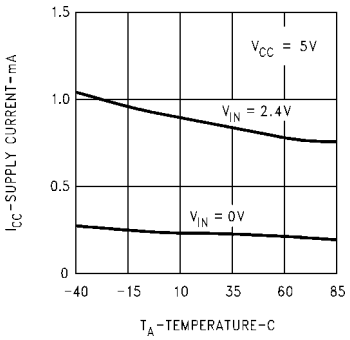
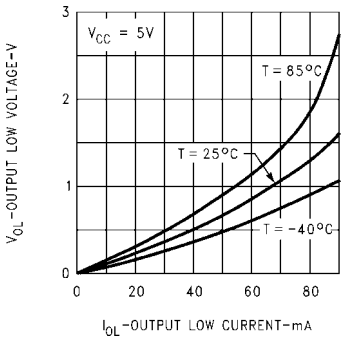
Supply Current vs Temperature



20163028

Output Low Voltage vs Output Low Current



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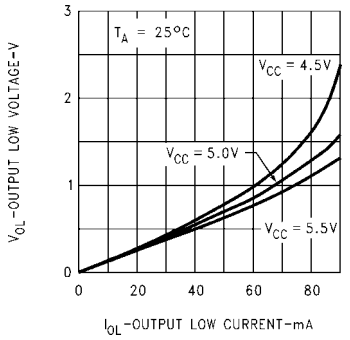
Output Low Voltage vs Output Low Current



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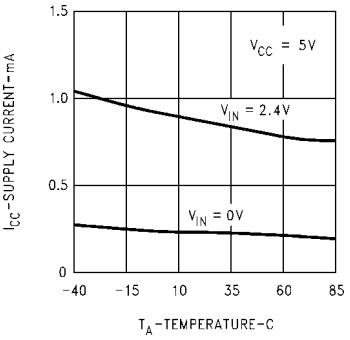
Supply Current vs Temperature



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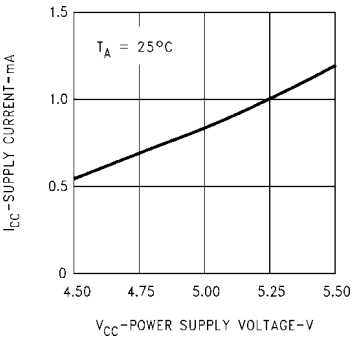
Supply Current vs Power Supply Voltage



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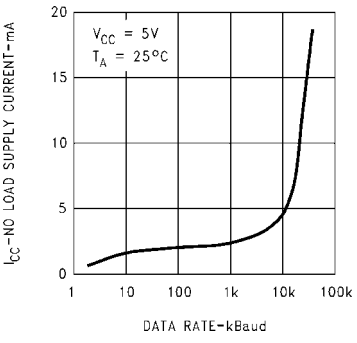
No Load Supply Current vs Data Rate



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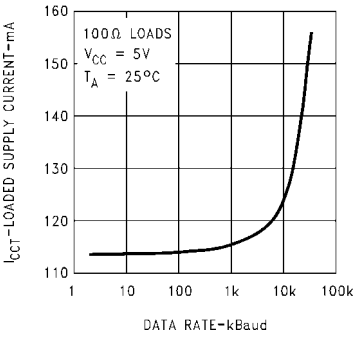
Loaded Supply Current vs Data Rate



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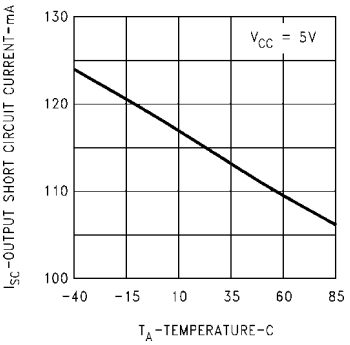
Output Short Circuit Current vs Temperature



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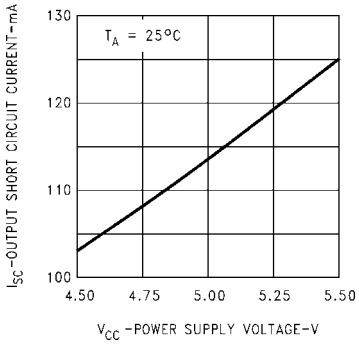
Output Short Circuit Current vs Power Supply Voltage



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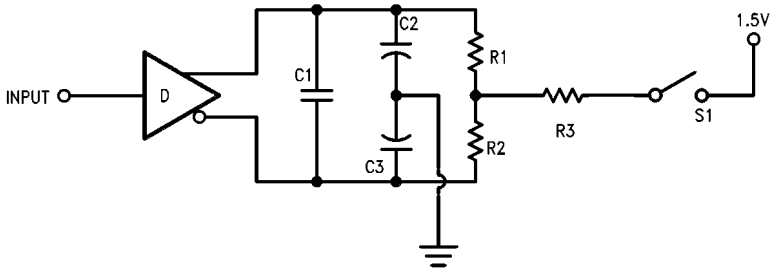
AC Test Circuit and Switching Time Waveforms



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Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit

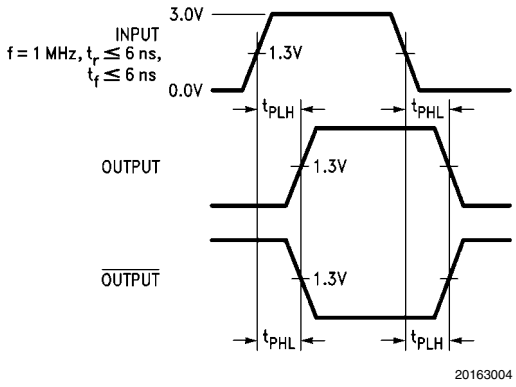

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FIGURE 2. Propagation Delays

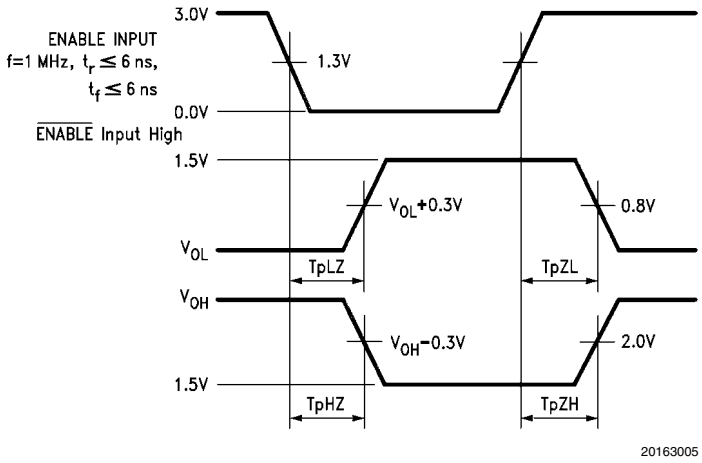
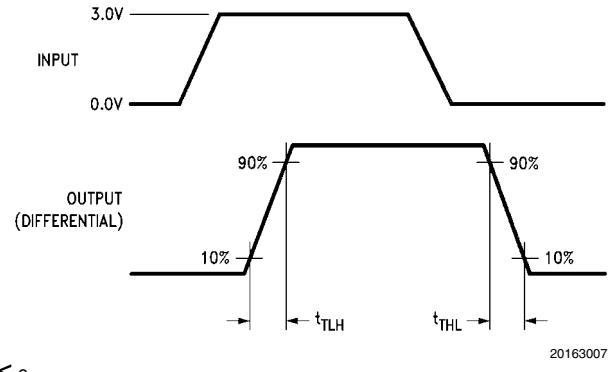


FIGURE 3. Enable and Disable Times

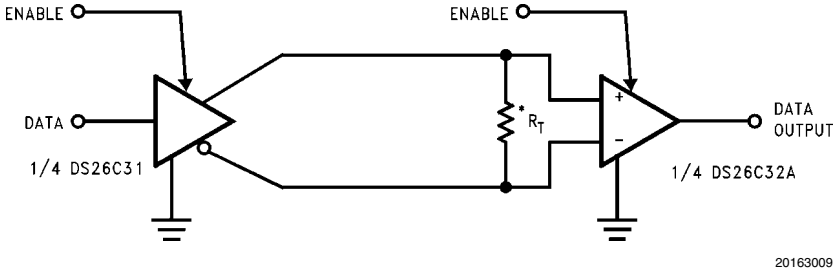


Input pulse; f = 1 MHz, 50%; $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

Typical Applications

Two-Wire Balanced System, RS-422

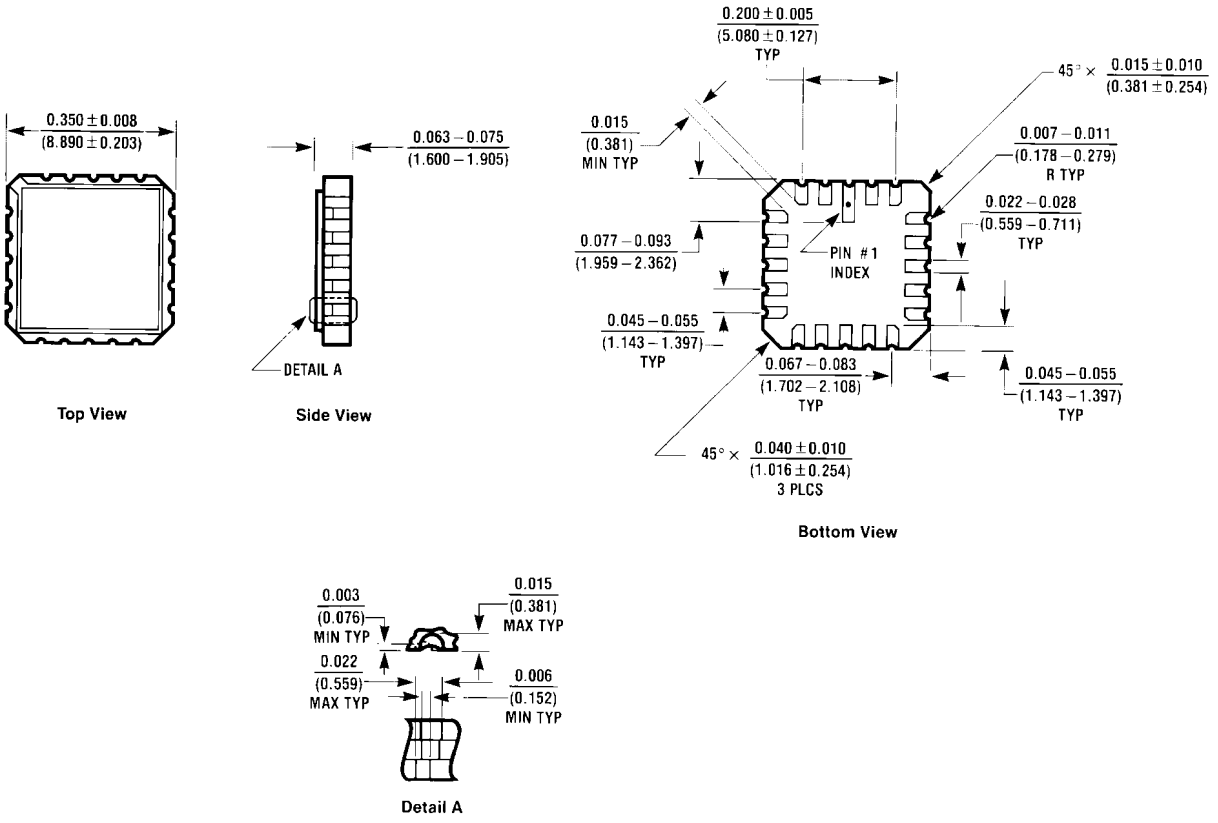


*R_T is optional although highly recommended to reduce reflection.

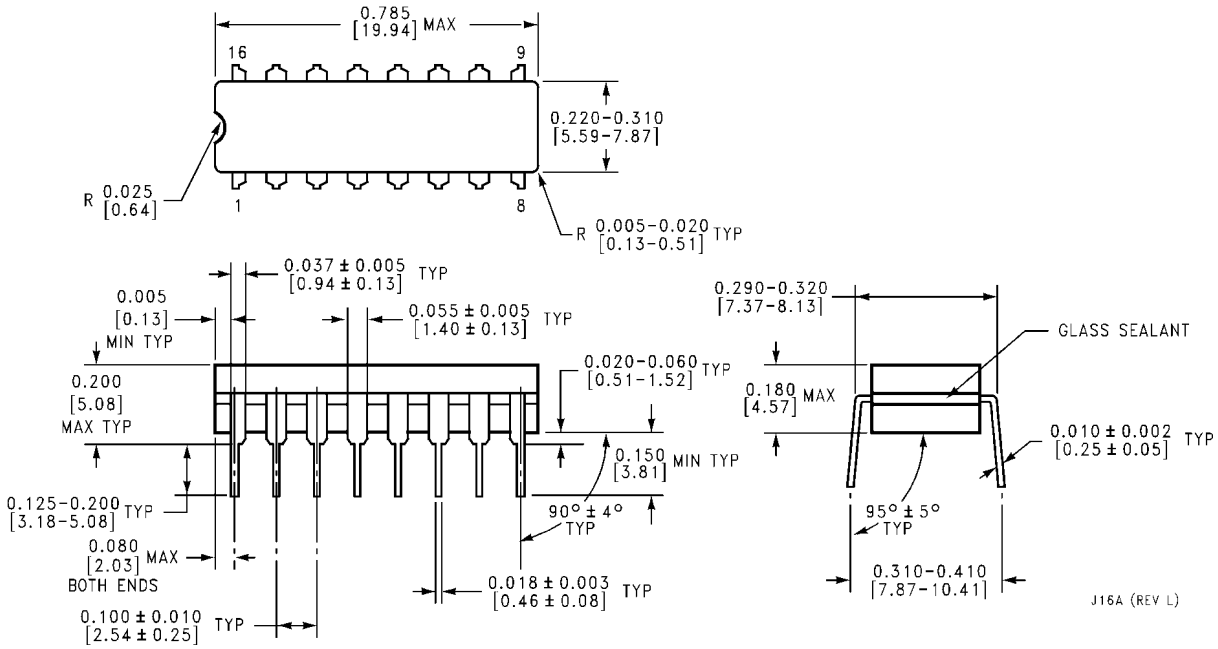
Revision History

Released	Revision	Section	Changes
10/26/2010	A	New Release, Corporate format	1 MDS data sheets converted into one Corp. data sheet format. MNDS26C31M-X Rev 0B0 will be archived.

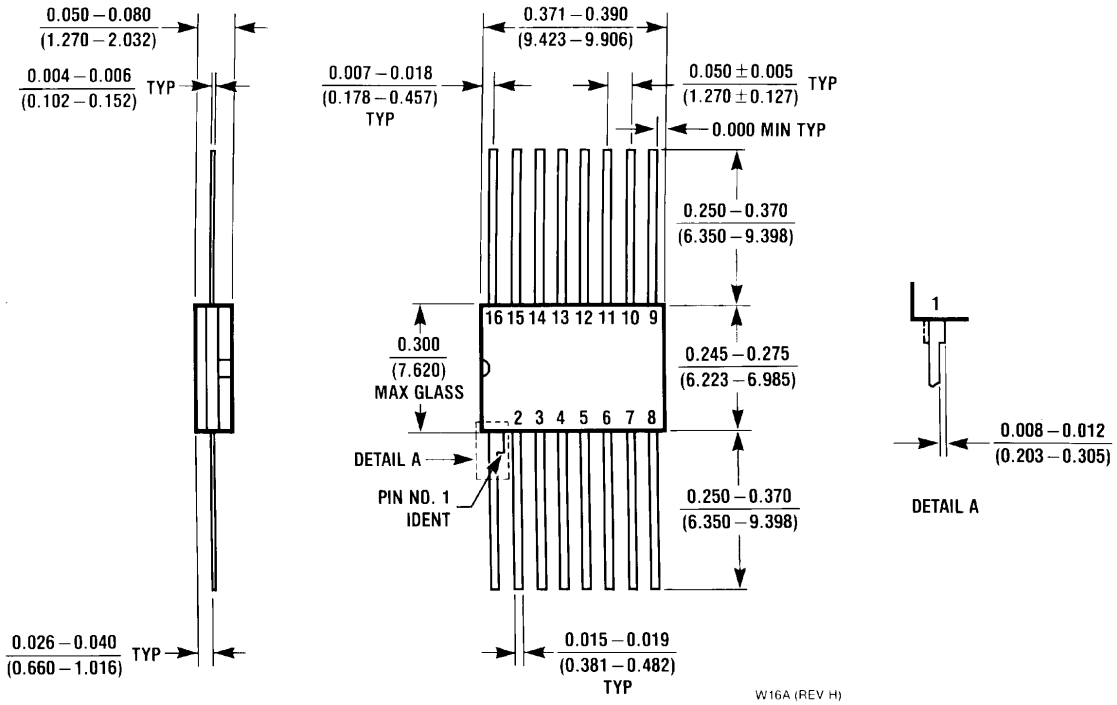
Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Ceramic Leadless Chip Carrier (E)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



16-Lead Ceramic Flatpak Package (W)
NS Package Number W16A

Notes

Notes

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Products		Design Support	
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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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