National Semiconductor

DS96F173MQML/ DS96F175MQML

April 28, 2011

EIA-485/EIA-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Features

- Meets EIA-485, EIA-422A, EIA-423A standards
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Lower power version
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS96F173ME/883	5962-9076602M2A	E20A	20LD Leadless Chip Carrier
DS96F173MJ/883	5962-9076602MEA	J16A	16LD Ceramic Dip
DS96F175ME/883	5962-9076601M2A	E20A	20LD Leadless Chip Carrier
DS96F175MJ-QMLV	5962-9076601VEA	J16A	16LD Ceramic Dip

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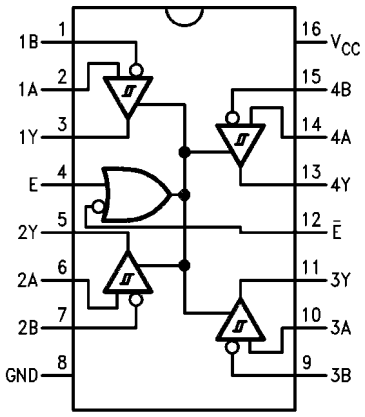
Connection Diagrams

16-Lead Ceramic Dual-In-Line Package (NS Package Number J16A)

DS96F173



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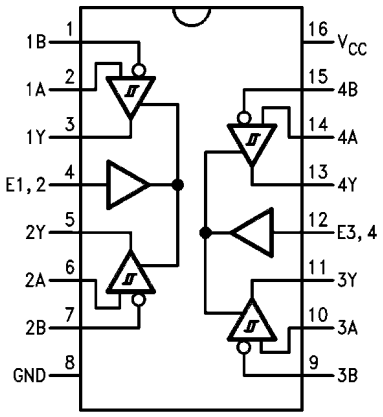
Top View

DS96F175



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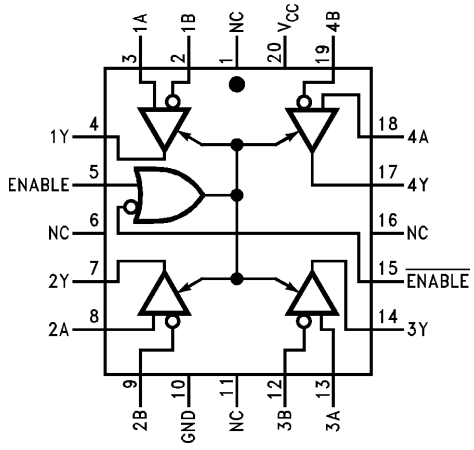
Top View

20-Lead Ceramic Leadless Chip Carrier (NS Package Number E20A)



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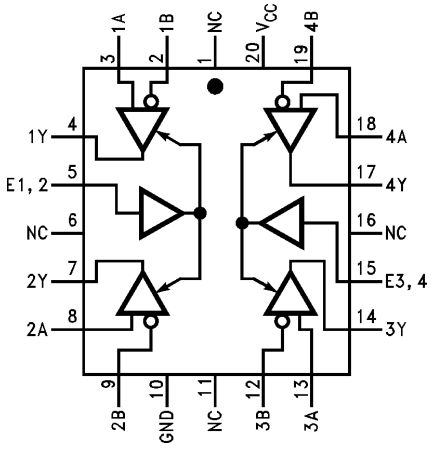
*NC—No Connection

Top View



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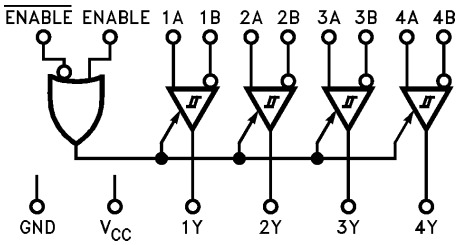
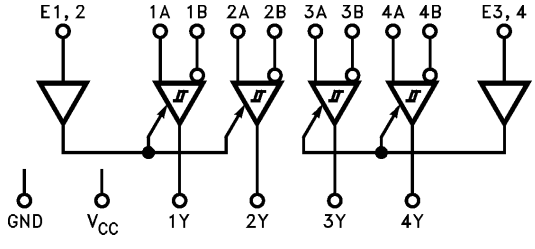
Top View

Logic Diagrams



DS96F173



DS96F175

Function Tables

(Each Receiver) DS96F173

Differential Inputs A–B	Enable E	Enable $\overline{E}$	Output Y
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

(Each Receiver) DS96F175

Differential Inputs A–B	Enable E	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

Absolute Maximum Ratings (*Note 1*)

Storage Temperature Range (T_{Stg})	$-65°C \leq T_A \leq +175°C$
Lead Temperature (Soldering, 60 sec.)	300°C
Max. Package Power Dissipation at 25°C (*Note 2*)	
Ceramic DIP (J)	1,500 mW
Ceramic Flatpak (W)	1,034 mW
Ceramic LCC (E)	1,500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Common Mode Input Voltage (V_{CM})	−7	+12	V
Differential Input Voltage (V_{ID})	−7	+12	V
Output Current HIGH (I_{OH})		−400	µA
Output Current LOW (I_{OL})		16	mA
Operating Temperature (T_A)	−55	125	°C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = 5.0V, Outputs Enabled

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Supply Current	V_{CC} = 5.5V, V_{ID} = 2V	(*Note 3*)		50	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{OH} = -400µA, V_{ID} = 0.2V	(*Note 4*)	2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OL} = 8mA, V_{ID} = -0.2V	(*Note 4*)		0.45	V	1, 2, 3
V_{TH}	Differential-Input High Threshold Voltage	V_{CC} = 4.5V & 5.5V, V_{CM} = 0V, V_O = 2.5V, I_O = -400µA			0.20	V	1, 2, 3
		V_{CC} = 4.5V & 5.5V, V_{CM} = -12V, V_O = 2.5V, I_O = -400µA			0.20	V	1, 2, 3
		V_{CC} = 4.5V & 5.5V, V_{CM} = 12V, V_O = 2.5V, I_O = -400µA			0.20	V	1, 2, 3
V_{TL}	Differential-Input Low Threshold Voltage	V_{CC} = 4.5V & 5.5V, V_{CM} = 0V, V_O = 0.5V, I_O = 16mA		-0.20		V	1, 2, 3
		V_{CC} = 4.5V & 5.5V, V_{CM} = -12V, V_O = 0.5V, I_O = 16mA		-0.20		V	1, 2, 3
		V_{CC} = 4.5V & 5.5V, V_{CM} = 12V, V_O = 0.5V, I_O = 16mA		-0.20		V	1, 2, 3
I_I	Input Line Current	V_{CC} = 4.5V, V_I = 12V, Untested Inputs are 0V			1.0	mA	1, 2, 3
		V_{CC} = 5.5V, V_I = -7V, Untested Inputs are 0V		-0.8		mA	1, 2, 3
I_{IH}	Logical "1" Enable Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V			10	µA	1, 2, 3
I_{IL}	Logical "0" Enable Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V		-100		µA	1, 2, 3
I_{OS}	Output Short Circuit Current	V_{CC} = 4.5V, V_O = 0V	(*Note 8*)	-85	-15	mA	1, 2, 3
		V_{CC} = 5.5V, V_O = 0V		-85	-15	mA	1, 2, 3
V_{IK}	Enable Input Clamp Voltage	V_{CC} = 4.5V, I_I = -18mA		-1.5		V	1, 2, 3
I_{OZ}	High Impedance Output Current	V_{CC} = 5.5V, V_{En} = 0.8V, V_O = 0.4V, Outputs disabled		-20	20	µA	1, 2, 3
		V_{CC} = 5.5V, V_{En} = 0.8V, V_O = 2.4V, Outputs disabled		-20	20	µA	1, 2, 3
V_{IH}	Logical "1" Enable Input Voltage		(*Note 5*)	2.0		V	1, 2, 3
V_{IL}	Logical "0" Enable Input Voltage		(*Note 6*)		0.8	V	1, 2, 3
R_I	Input Resistance			10		kΩ	1, 2, 3

AC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = 5.0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHL}	Propagation Delay	C_L = 15pF			22	ns	1
					30	ns	2, 3
t_{PLH}	Propagation Delay	C_L = 15pF			22	ns	1
					30	ns	2, 3
t_{PZH}	Propagation Delay	C_L = 15pF			16	ns	1
					27	ns	2, 3
t_{PZL}	Propagation Delay	C_L = 15pF			18	ns	1
					27	ns	2, 3
t_{PHZ}	Propagation Delay	C_L = 5pF	(*Note 7*)		20	ns	1
					27	ns	2, 3
		C_L = 20pF			30	ns	1
					37	ns	2, 3
t_{PLZ}	Propagation Delay	C_L = 5pF			18	ns	1
					30	ns	2, 3
t_{PW}	Propagation Delay				3.0	ns	1
					8.0	ns	2
					5.0	ns	3

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Above T_A = 25°C derate J package 10 mW/°C, W package 6.90 mW/°C, E package 11.11 mW/°C.

Note 3: I_{CC} is tested with outputs disabled (worst case), I_{CC} enabled is guaranteed by this test.

Note 4: V_{OH} & V_{OL} are tested over common mode voltage range of +/−12V via the V_{TH} / V_{TL} tests.

Note 5: Guaranteed by V_{OL} & V_{OH} tests.

Note 6: Guaranteed by I_{OZ} test.

Note 7: Testing at 20pF assures conformance to spec at 5pF.

Note 8: Only one output at a time should be shorted.

Parameter Measurement Information

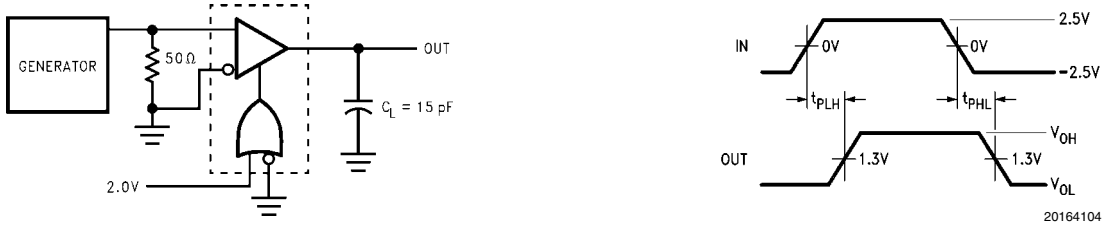


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FIGURE 1. t_{PLH}, t_{PHL} (*Note 9*, *Note 10*)

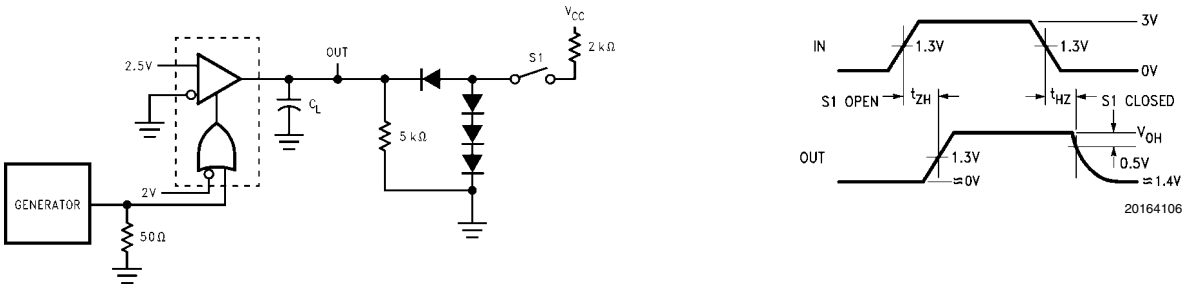

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FIGURE 2. t_{HZ}, t_{ZH} (*Note 9*, *Note 10*, *Note 12*, *Note 13*)

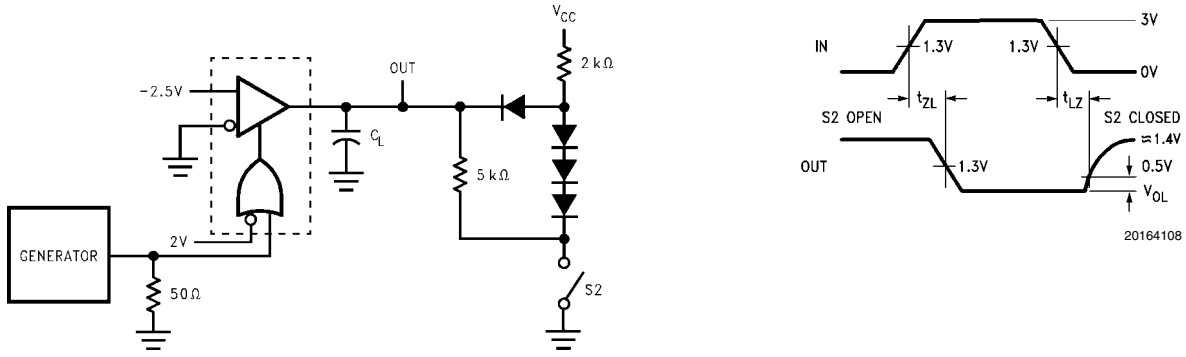

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FIGURE 3. t_{ZL}, t_{LZ} (*Note 9*, *Note 10*, *Note 12*, *Note 13*)

Note 9: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 10: C_L includes probe and stray capacitance.

Note 11: DS96F173 with active high and active low Enables are shown. DS96F175 has active high Enable only.

Note 12: All diodes are 1N916 or equivalent.

Note 13: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

Typical Application

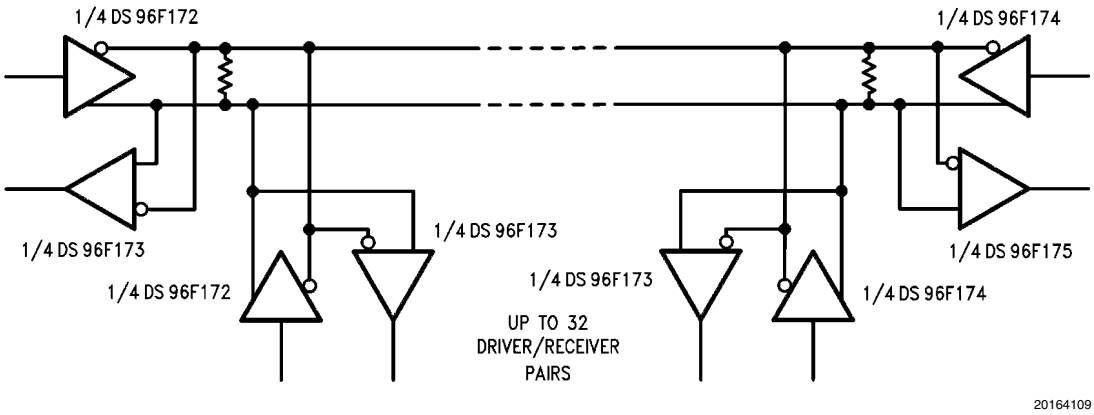


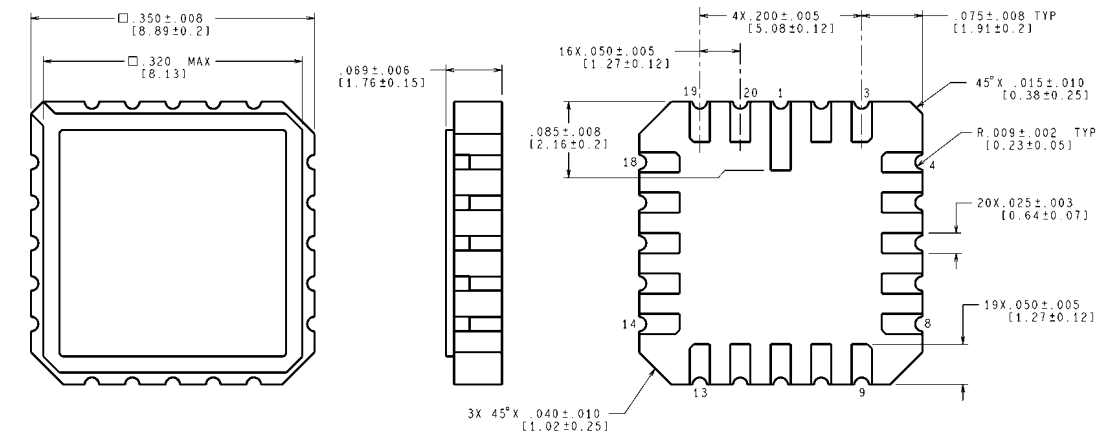
FIGURE 4.

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible .

Revision History

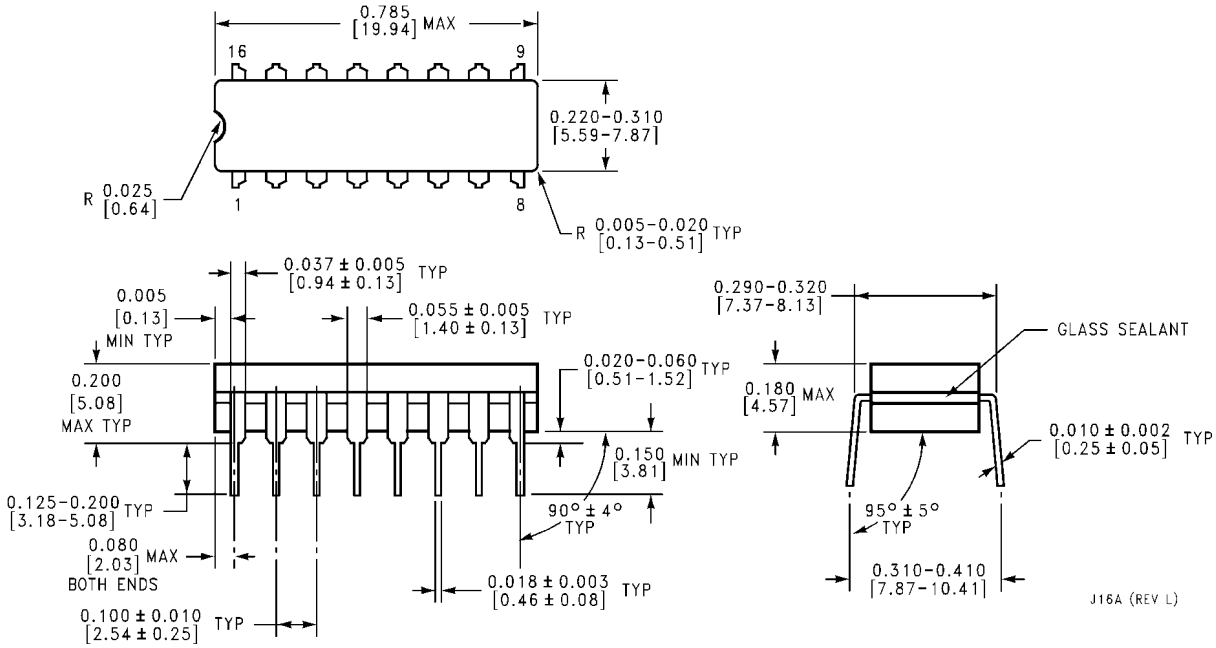
Released	Revision	Section	Changes
28–Apr-11	A	New Release, Corporate format	2 MDS data sheets converted into one Corp. data sheet format. MNDS96F173M-X Rev 0A0 & MNDS96F175M-X Rev 0B0 will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted

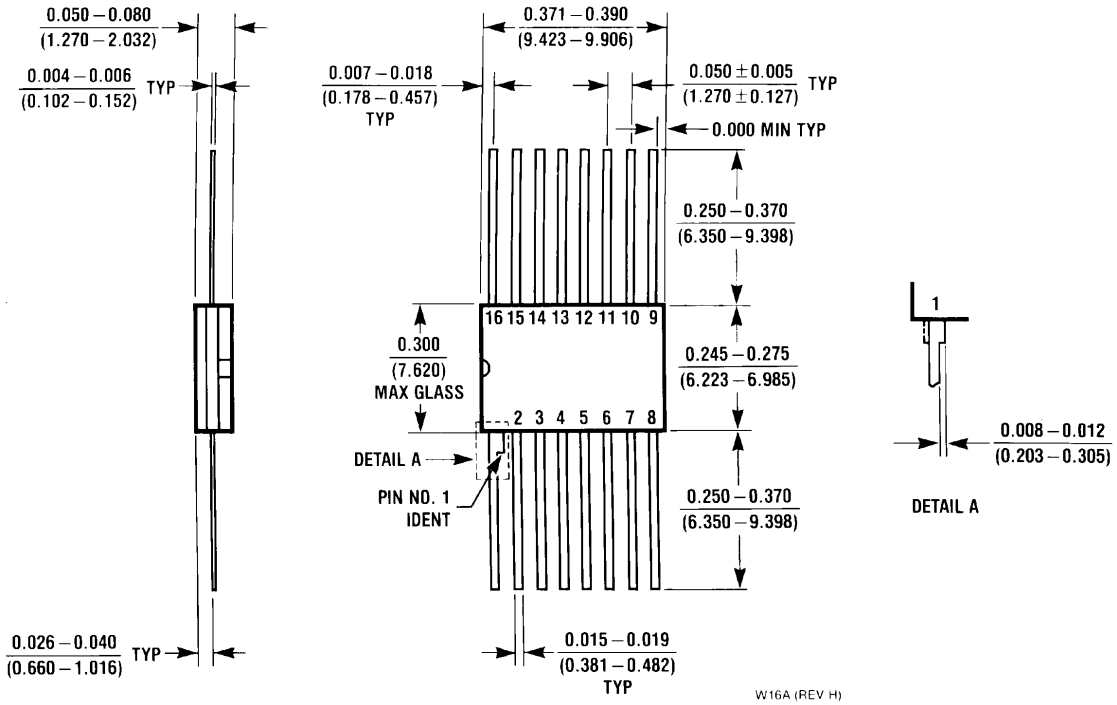


E20A (Rev F)

20-Lead Ceramic Leadless Chip Carrier (E)
NS Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



16-Lead Ceramic FlatPak (W)
NS Package Number W16A

Notes

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