National Semiconductor

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# LMC7101
# Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

## General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/6484 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

## Features

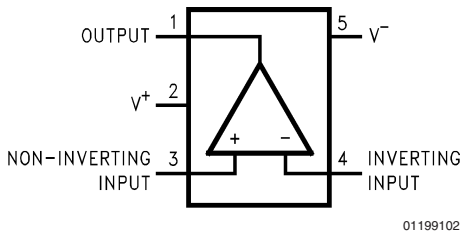
- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/6484
- Rail-to-rail input and output

## Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

## Connection Diagram

**5-Pin SOT23**




**Top View**

## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 5-Pin SOT23 | LMC7101AIM5 | A00A | 1k Units on Tape and Reel | MF05A |
| | LMC7101AIM5X | A00A | 3k Units Tape and Reel | |
| | LMC7101BIM5 | A00B | 1k Units on Tape and Reel | |
| | LMC7101BIM5X | A00B | 3k Units Tape and Reel | |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance (Note 2) | 2000V |
| Difference Input Voltage | ±Supply Voltage |
| Voltage at Input/Output Pin | $(V^+)$ + 0.3V, $(V^-)$ − 0.3V |
| Supply Voltage $(V^+ - V^-)$ | 16V |
| Current at Input Pin | ±5 mA |
| Current at Output Pin (Note 3) | ±35 mA |
| Current at Power Supply Pin | 35 mA |
| Lead Temp. (Soldering, 10 sec.) | 260˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Junction Temperature (Note 4) | 150˚C |

## Recommended Operating Conditions (Note 1)

| | |
|---|---|
| Supply Voltage | $2.7V \le V^+ \le 15.5V$ |
| Temperature Range | |
| LMC7101AI, LMC7101BI | −40˚C to +85˚C |
| Thermal Resistance ($\theta_{JA}$) | |
| 5-Pin STO23 | 325˚C/W |

## 2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$ and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V^+$ = 2.7V | 0.11 | 6 | 9 | mV max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 1 | | | µV/˚C |
| $I_B$ | Input Bias Current | | 1.0 | **64** | **64** | pA max |
| $I_{OS}$ | Input Offset Current | | 0.5 | **32** | **32** | pA max |
| $R_{IN}$ | Input Resistance | | >1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | $0V \le V_{CM} \le 2.7V$<br>$V^+$ = 2.7V | 70 | 55 | 50 | dB min |
| $V_{CM}$ | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | 0.0 | 0.0 | 0.0 | V min |
| | | | 3.0 | 2.7 | 2.7 | V max |
| PSRR | Power Supply Rejection Ratio | $V^+$ = 1.35V to 1.65V<br>$V^-$ = −1.35V to −1.65V<br>$V_{CM}$ = 0 | 60 | 50 | 45 | dB min |
| $C_{IN}$ | Common-Mode Input Capacitance | | 3 | | | pF |
| $V_O$ | Output Swing | $R_L$ = 2 kΩ | 2.45 | 2.15 | 2.15 | V min |
| | | | 0.25 | 0.5 | 0.5 | V max |
| | | $R_L$ = 10 kΩ | 2.68 | 2.64 | 2.64 | V min |
| | | | 0.025 | 0.06 | 0.06 | V max |
| $I_S$ | Supply Current | | 0.5 | 0.81<br>**0.95** | 0.81<br>**0.95** | mA max |
| SR | Slew Rate (Note 8) | | 0.7 | | | V/µs |
| GBW | Gain-Bandwidth Product | | 0.6 | | | MHz |

## 3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 3V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = $V^+$/2 and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | 0.11 | 4<br>**6** | 7<br>**9** | mV<br>max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 1 | | | µV/˚C |
| $I_B$ | Input Current | | 1.0 | **64** | **64** | pA max |
| $I_{OS}$ | Input Offset Current | | 0.5 | **32** | **32** | pA max |
| $R_{IN}$ | Input Resistance | | >1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 3V<br>$V^+$ = 3V | 74 | 64 | 60 | db<br>min |
| $V_{CM}$ | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | 0.0 | 0.0 | 0.0 | V<br>min |
| | | | 3.3 | 3.0 | 3.0 | V<br>max |
| PSRR | Power Supply Rejection Ratio | $V^+$ = 1.5V to 7.5V<br>$V^-$ = –1.5V to –7.5V<br>$V_O$ = $V_{CM}$ = 0 | 80 | 68 | 60 | dB<br>min |
| $C_{IN}$ | Common-Mode Input Capacitance | | 3 | | | pF |
| $V_O$ | Output Swing | $R_L$ = 2 kΩ | 2.8 | 2.6 | 2.6 | V min |
| | | | 0.2 | 0.4 | 0.4 | V max |
| | | $R_L$ = 600Ω | 2.7 | 2.5 | 2.5 | V min |
| | | | 0.37 | 0.6 | 0.6 | V max |
| $I_S$ | Supply Current | | 0.5 | 0.81<br>**0.95** | 0.81<br>**0.95** | mA<br>max |

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = $V^+$/2 and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V^+$ = 5V | | 0.11 | 3<br>**5** | 7<br>**9** | mV<br>max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | | 1.0 | | | µV/˚C |
| $I_B$ | Input Current | | | 1 | **64** | **64** | pA max |
| $I_{OS}$ | Input Offset Current | | | 0.5 | **32** | **32** | pA max |
| $R_{IN}$ | Input Resistance | | | >1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 5V | | 82 | 65<br>**60** | 60<br>**55** | db<br>min |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+$ = 5V to 15V<br>$V^-$ = 0V, $V_O$ = 1.5V | | 82 | 70<br>**65** | 65<br>**62** | dB<br>min |
| –PSRR | Negative Power Supply Rejection Ratio | $V^-$ = –5V to –15V<br>$V^+$ = 0V, $V_O$ = –1.5V | | 82 | 70<br>**65** | 65<br>**62** | dB<br>min |
| $V_{CM}$ | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | | –0.3 | –0.20<br>**0.00** | –0.20<br>**0.00** | V<br>min |
| | | | | 5.3 | 5.20<br>**5.00** | 5.20<br>**5.00** | V<br>max |
| $C_{IN}$ | Common-Mode Input Capacitance | | | 3 | | | pF |
| $V_O$ | Output Swing | $R_L$ = 2 kΩ | | 4.9 | 4.7<br>**4.6** | 4.7<br>**4.6** | V<br>min |
| | | | | 0.1 | 0.18<br>**0.24** | 0.18<br>**0.24** | V<br>max |
| | | $R_L$ = 600Ω | | 4.7 | 4.5<br>**4.24** | 4.5<br>**4.24** | V<br>min |
| | | | | 0.3 | 0.5<br>**0.65** | 0.5<br>**0.65** | V<br>max |
| $I_{SC}$ | Output Short Circuit Current | $V_O$ = 0V | Sourcing | 24 | 16<br>**11** | 16<br>**11** | mA<br>min |
| | | $V_O$ = 5V | Sinking | 19 | 11<br>**7.5** | 11<br>**7.5** | mA<br>min |
| $I_S$ | Supply Current | | | 0.5 | 0.85<br>**1.0** | 0.85<br>**1.0** | mA<br>max |

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = $V^+$/2 and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|
| THD | Total Harmonic Distortion | F = 10 kHz, $A_V$ = –2<br>$R_L$ = 10 kΩ, $V_O$ = 4.0 $V_{PP}$ | 0.01 | | | % |
| SR | Slew Rate | | 1.0 | | | V/µs |
| GBW | Gain Bandwidth Product | | 1.0 | | | MHz |

## 15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 15V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = $V^+$/2 and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | 0.11 | | | mV max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | | 1.0 | | | µV/˚C |
| $I_B$ | Input Current | | | 1.0 | **64** | **64** | pA max |
| $I_{OS}$ | Input Offset Current | | | 0.5 | **32** | **32** | pA max |
| $R_{IN}$ | Input Resistance | | | >1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 15V | | 82 | 70<br>**65** | 65<br>**60** | dB<br>min |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+$ = 5V to 15V<br>$V^-$ = 0V, $V_O$ = 1.5V | | 82 | 70<br>**65** | 65<br>**62** | dB<br>min |
| −PSRR | Negative Power Supply Rejection Ratio | $V^-$ = −5V to −15V<br>$V^+$ = 0V, $V_O$ = −1.5V | | 82 | 70<br>**65** | 65<br>**62** | dB<br>min |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+$ = 5V<br>For CMRR ≥ 50 dB | | −0.3 | −0.20<br>**0.00** | −0.20<br>**0.00** | V<br>min |
| | | | | 15.3 | 15.20<br>**15.00** | 15.20<br>**15.00** | V<br>max |
| $A_V$ | Large Signal Voltage Gain (Note 7) | $R_L$ = 2 kΩ | Sourcing | 340 | 80<br>**40** | 80<br>**40** | V/mV |
| | | | Sinking | 24 | 15<br>**10** | 15<br>**10** | |
| | | $R_L$ = 600Ω | Sourcing | 300 | 34 | 34 | |
| | | | Sinking | 15 | 6 | 6 | |
| $C_{IN}$ | Input Capacitance | | | 3 | | | pF |
| $V_O$ | Output Swing | $V^+$ = 15V<br>$R_L$ = 2 kΩ | | 14.7 | 14.4<br>**14.2** | 14.4<br>**14.2** | V<br>min |
| | | | | 0.16 | 0.32<br>**0.45** | 0.32<br>**0.45** | V<br>max |
| | | $V^+$ = 15V<br>$R_L$ = 600Ω | | 14.1 | 13.4<br>**13.0** | 13.4<br>**13.0** | V<br>min |
| | | | | 0.5 | 1.0<br>**1.3** | 1.0<br>**1.3** | V<br>max |
| $I_{SC}$ | Output Short Circuit Current (Note 9) | $V_O$ = 0V | Sourcing | 50 | 30<br>**20** | 30<br>**20** | mA<br>min |
| | | $V_O$ = 12V | Sinking | 50 | 30<br>**20** | 30<br>**20** | |
| $I_S$ | Supply Current | | | 0.8 | 1.50<br>**1.71** | 1.50<br>**1.71** | mA<br>max |

## 15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 15V, $V^-$ = 0V, $V_{CM}$ = 1.5V, $V_O$ = $V^+$/2 and $R_L$ = 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|---|---|---|---|---|---|---|
| SR | Slew Rate (Note 8) | $V^+$ = 15V | 1.1 | 0.5<br>**0.4** | 0.5<br>**0.4** | V/µs<br>min |
| GBW | Gain-Bandwidth Product | $V^+$ = 15V | 1.1 | | | MHz |
| $\phi_m$ | Phase Margin | | 45 | | | deg |
| $G_m$ | Gain Margin | | 10 | | | dB |
| $e_n$ | Input-Referred Voltage Noise | f = 1 kHz, $V_{CM}$ = 1V | 37 | | | $\frac{nV}{\sqrt{Hz}}$ |
| $i_n$ | Input-Referred Current Noise | f = 1 kHz | 1.5 | | | $\frac{fA}{\sqrt{Hz}}$ |
| THD | Total Harmonic Distortion | f = 10 kHz, $A_V$ = –2<br>$R_L$ = 10 kΩ, $V_O$ = 8.5 $V_{PP}$ | 0.01 | | | % |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human Body Model is 1.5 kΩ in series with 100 pF.

**Note 3:** Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150˚C.

**Note 4:** The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$ and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

**Note 5:** Typical Values represent the most likely parametric norm.

**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:** $V^+$ = 15V, $V_{CM}$ = 1.5V and $R_L$ connect to 7.5V. For sourcing tests, 7.5V ≤ $V_O$ ≤ 12.5V. For sinking tests, 2.5V ≤ $V_O$ ≤ 7.5V.

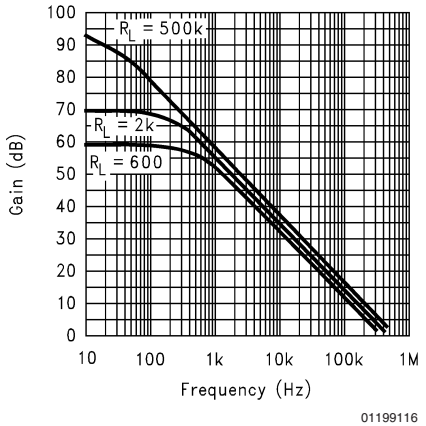
**Note 8:** $V^+$ = 15V. Connected as a voltage follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. $R_L$ = 100 kΩ connected to 7.5V. Amp excited with 1 kHz to produce $V_O$ = 10 $V_{PP}$.

**Note 9:** Do not short circuit output to $V^+$ when $V^+$ is greater than 12V or reliability will be adversely affected.

## 2.7V Typical Performance Characteristics

$V^+$ = 2.7V, $V^-$ = 0V, $T_A$ = 25˚C, unless otherwise specified.

**Open Loop Frequency Response**

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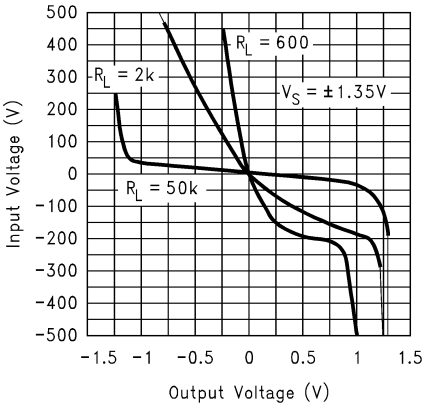
**Input Voltage vs. Output Voltage**

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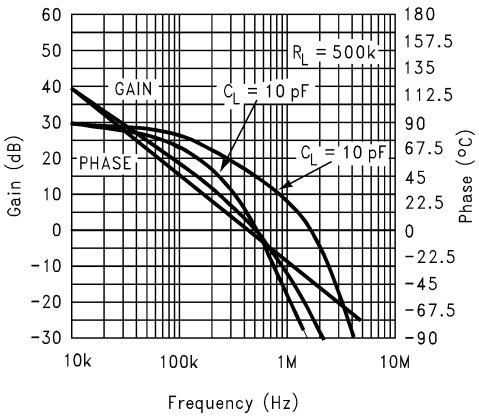
## 2.7V Typical Performance Characteristics $V^+ = 2.7V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Gain and Phase vs. Capacitance Load**

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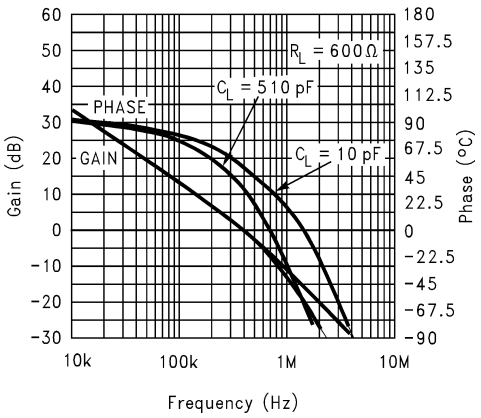
**Gain and Phase vs. Capacitance Load**

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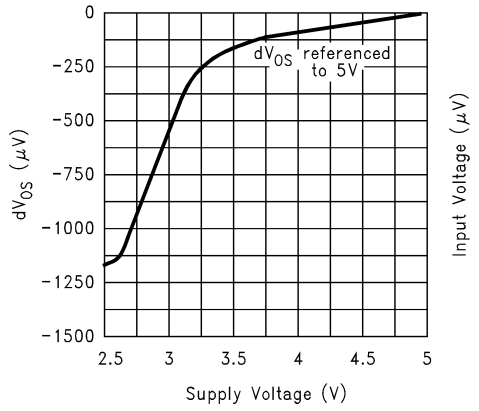
**$dV_{OS}$ vs. Supply Voltage**

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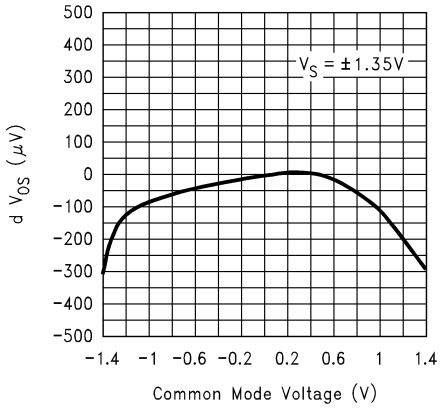
**$dV_{OS}$ vs. Common Mode Voltage**

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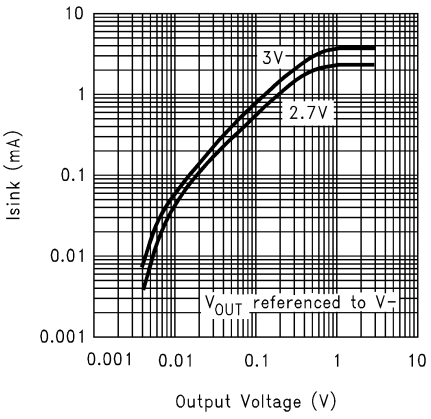
**Sinking Current vs. Output Voltage**

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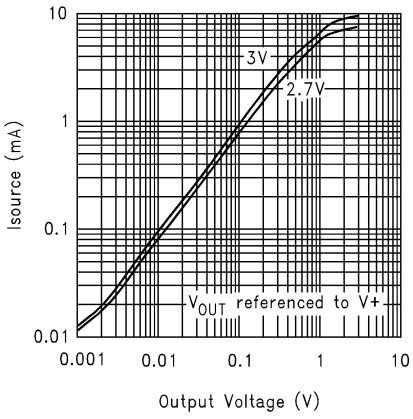
**Sourcing Current vs. Output Voltage**

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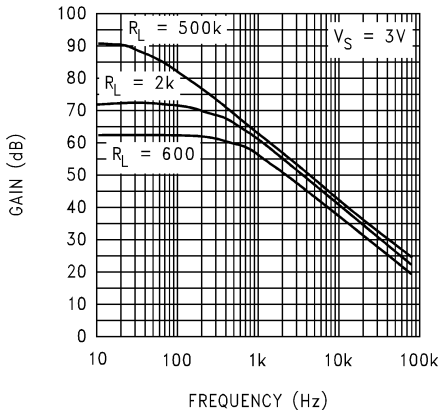
## 3V Typical Performance Characteristics

$V^+$ = 3V, $V^-$ = 0V, $T_A$ = 25°C, unless otherwise specified.

### Open Loop Frequency Response

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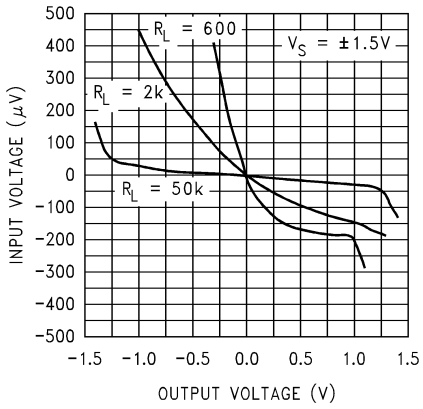
### Input Voltage vs. Output Voltage

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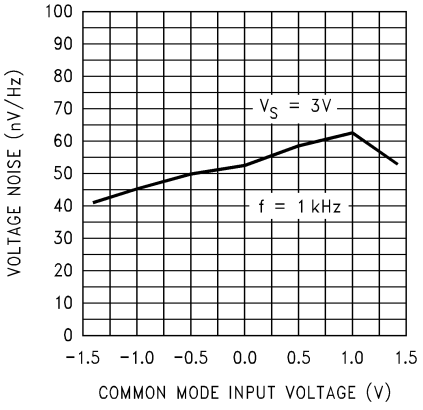
### Input Voltage Noise vs. Input Voltage

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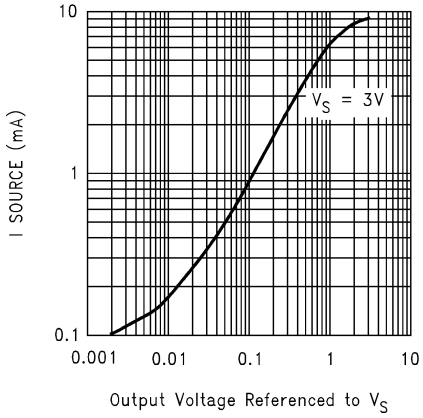
### Sourcing Current vs. Output Voltage

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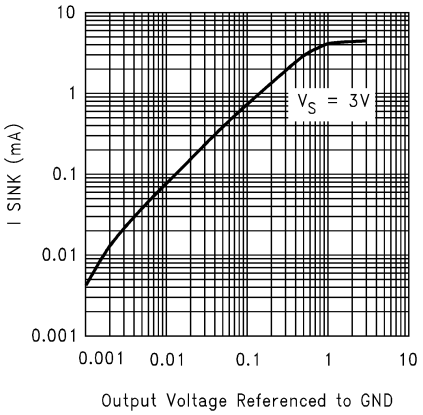
### Sinking Current vs. Output Voltage

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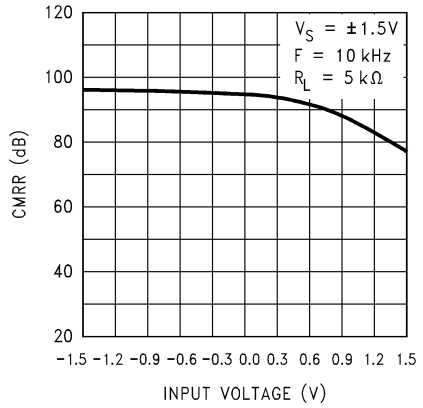
### CMRR vs. Input Voltage

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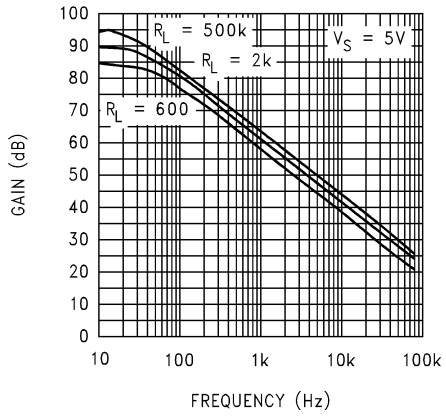
## 5V Typical Performance Characteristics

$V^+ = 5V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified.

### Open Loop Frequency Response

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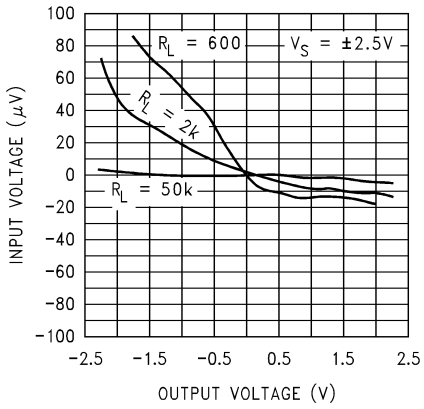
### Input Voltage vs. Output Voltage

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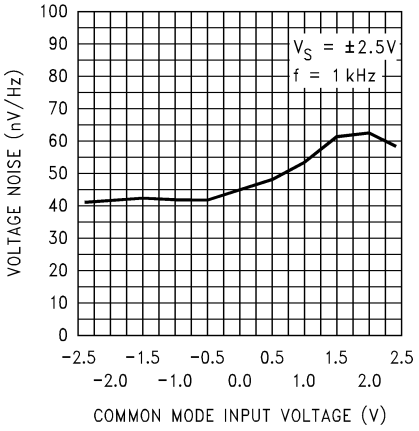
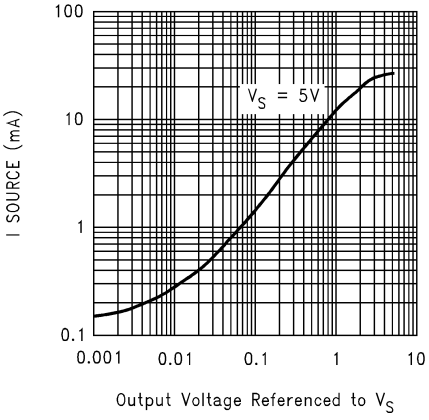
### Input Voltage Noise vs. Input Voltage



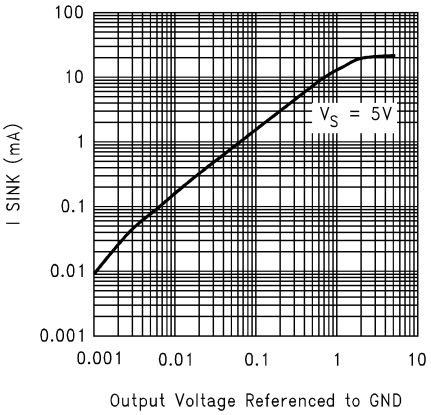

01199132

### Sourcing Current vs, Output Voltage



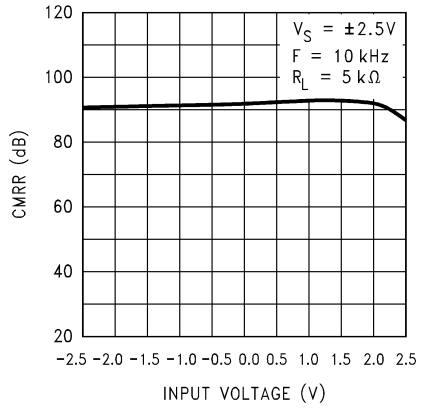

01199133

### Sinking Current vs. Output Voltage




01199134

### CMRR vs. Input Voltage

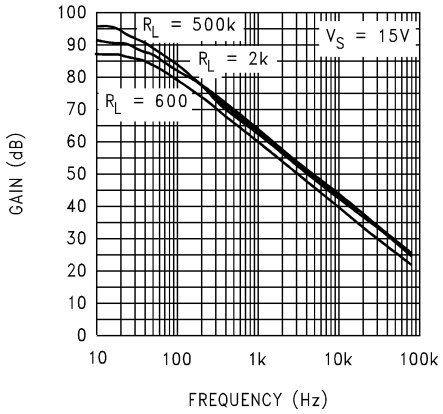



01199135

## 15V Typical Performance Characteristics

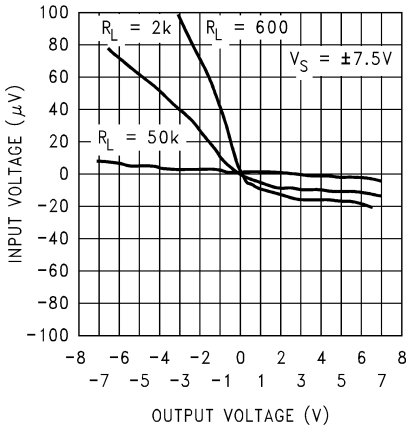
$V^+$ = +15V, $V^-$ = 0V, $T_A$ = 25˚C, unless otherwise specified.

### Open Loop Frequency Response



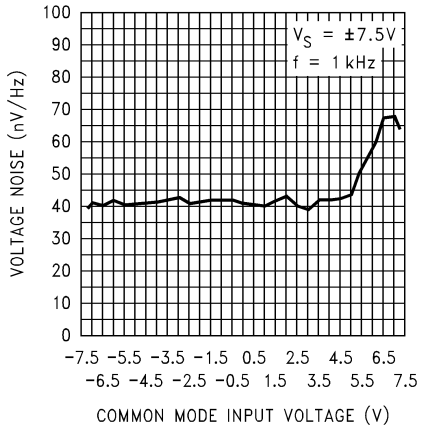

01199136

### Input Voltage vs. Output Voltage



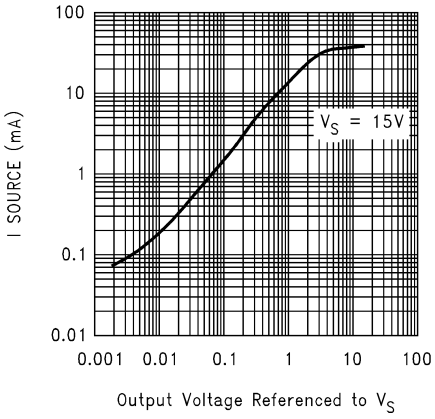

01199137

### Input Voltage Noise vs. Input Voltage



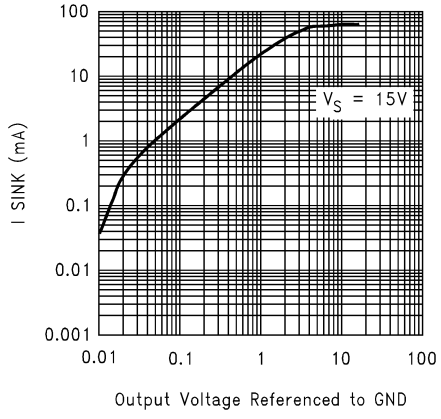

01199138

### Sourcing Current vs. Output Voltage



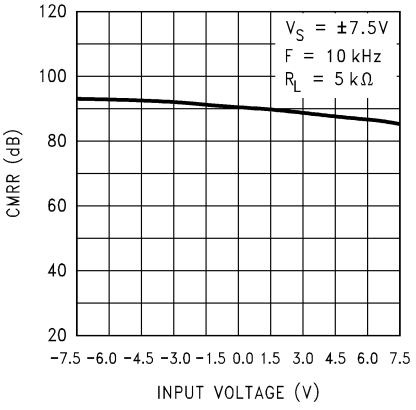

01199139

### Sinking Current vs. Output Voltage




01199140

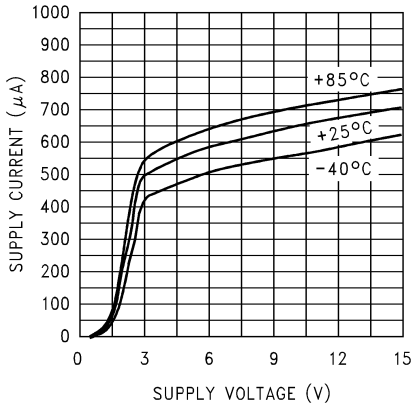
### CMRR vs. Input Voltage




01199141

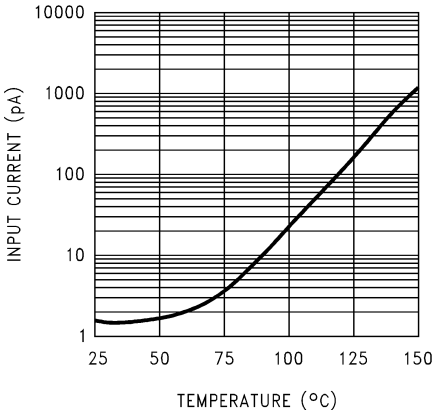
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Supply Current vs. Supply Voltage**



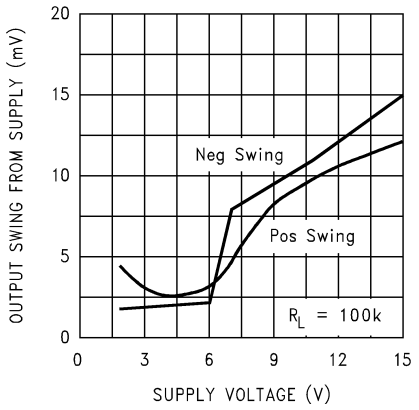

01199142

**Input Current vs. Temperature**



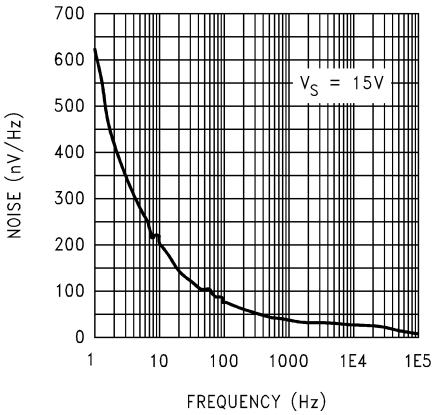

01199143

**Output Voltage Swing vs. Supply Voltage**



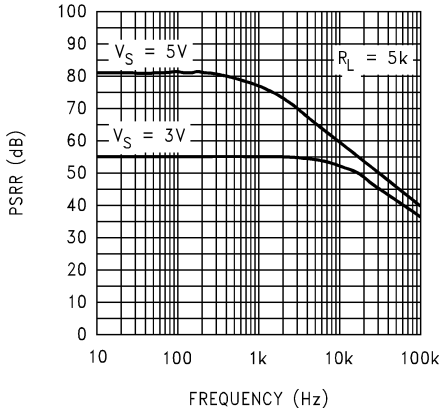

01199144

**Input Voltage Noise vs. Frequency**



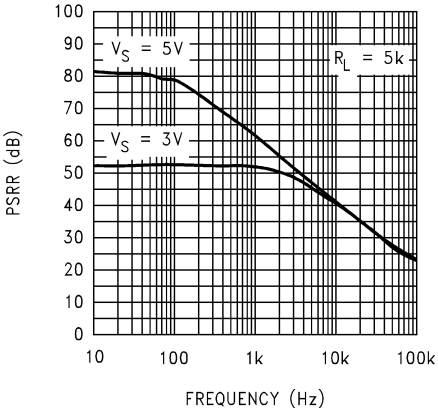

01199145

**Positive PSRR vs. Frequency**




01199146

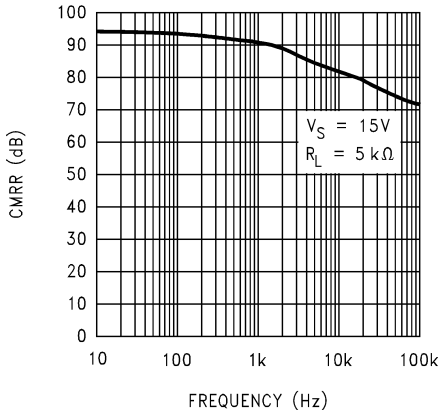
**Negative PSRR vs. Frequency**




01199147

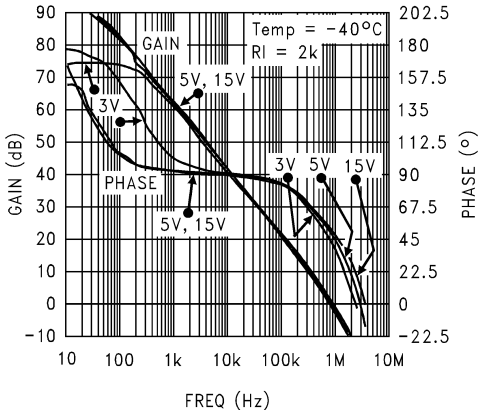
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**CMRR vs. Frequency**



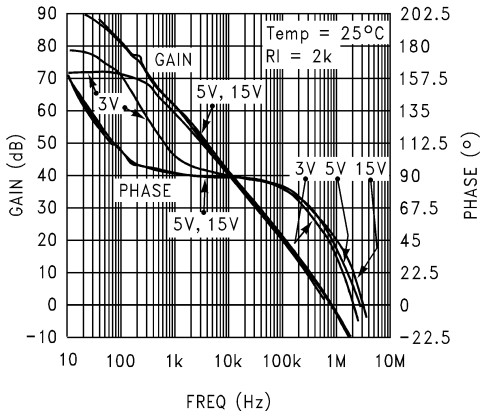

01199148

**Open Loop Frequency Response @ −40˚C**



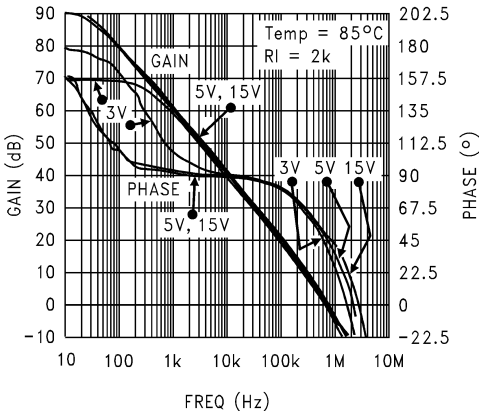

01199149

**Open Loop Frequency Response @ 25˚C**



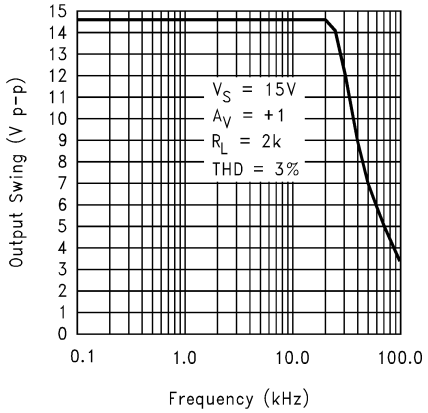

01199150

**Open Loop Frequency Response @ 85˚C**



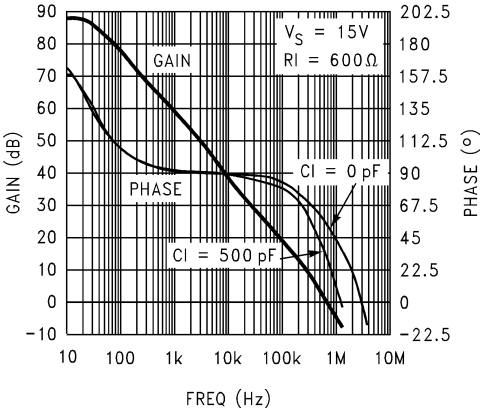

01199151

**Maximum Output Swing vs. Frequency**




01199152

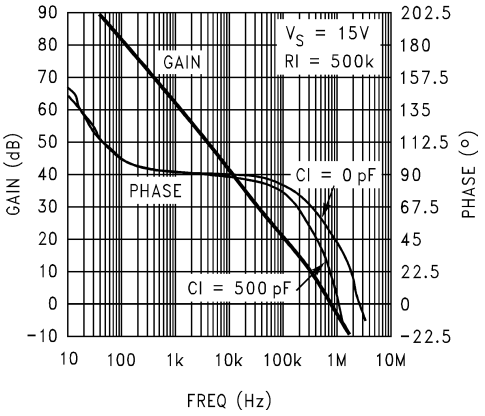
**Gain and Phase vs. Capacitive Load**




01199153

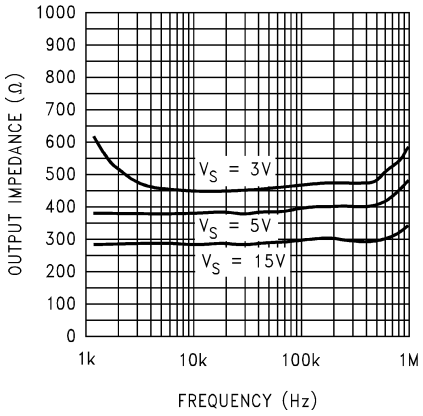
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Gain and Phase vs. Capacitive Load**



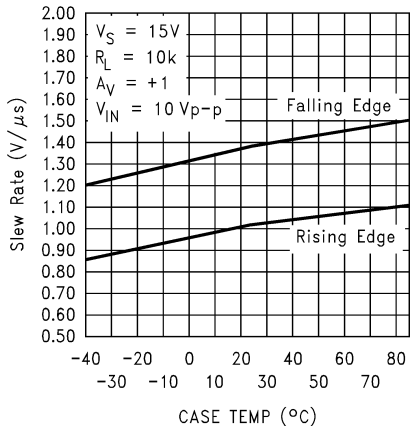

01199154

**Output Impedance vs. Frequency**



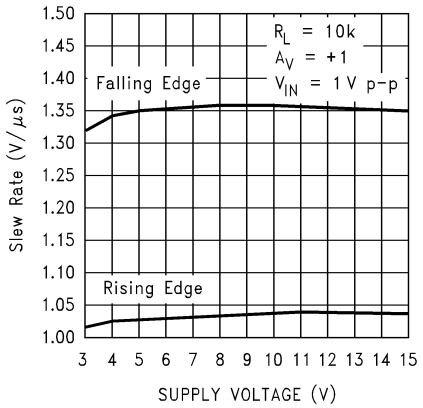

01199155

**Slew Rate vs. Temperature**



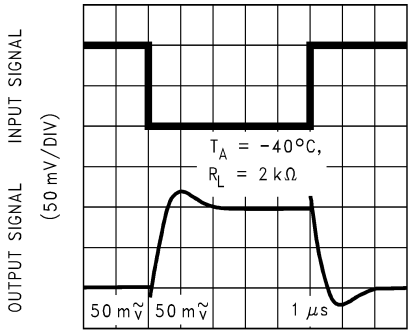

01199156

**Slew Rate vs. Supply Voltage**



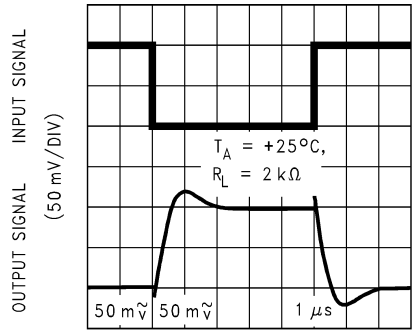

01199157

**Inverting Small Signal Pulse Response**




01199158

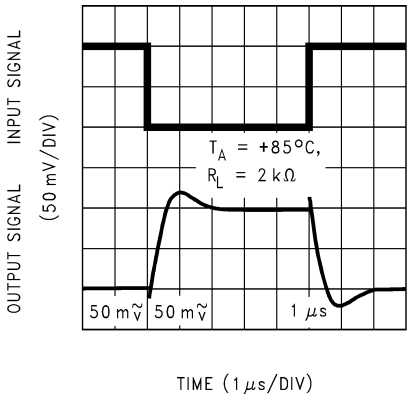
**Inverting Small Signal Pulse Response**




01199159

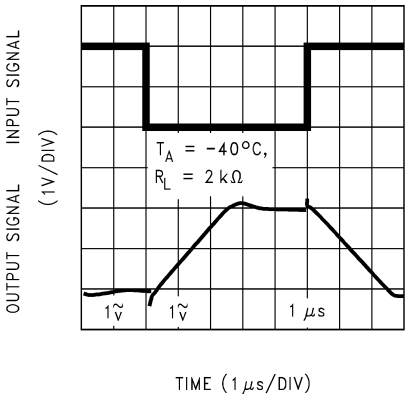
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Inverting Small Signal Pulse Response**



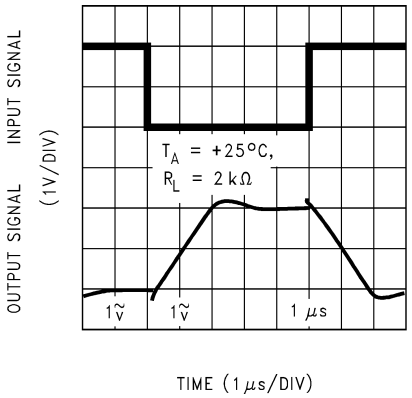

01199160

**Inverting Large Signal Pulse Response**



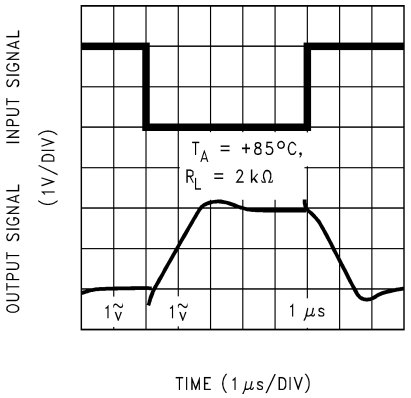

01199161

**Inverting Large Signal Pulse Response**



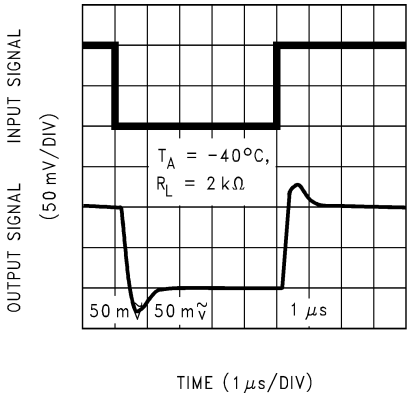

01199162

**Inverting Large Signal Pulse Response**



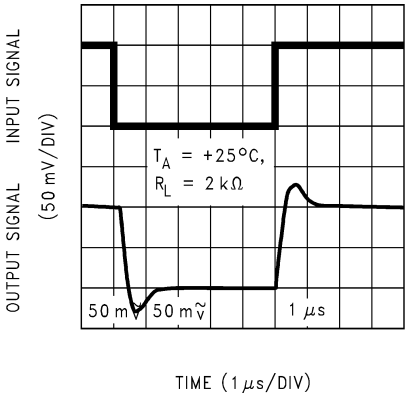

01199163

**Non-Inverting Small Signal Pulse Response**




01199164

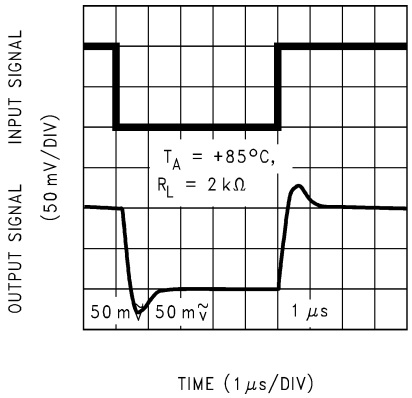
**Non-Inverting Small Signal Pulse Response**




01199165

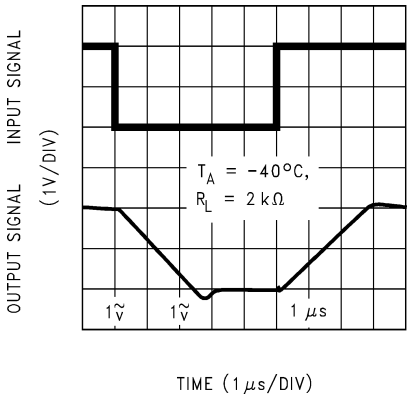
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Non-Inverting Small Signal Pulse Response**



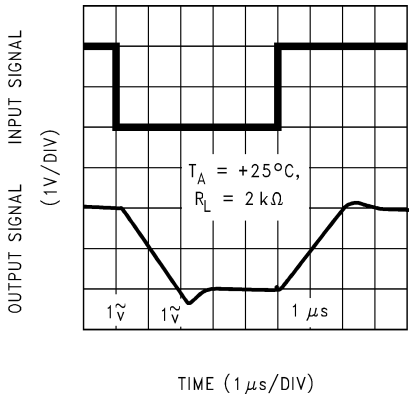

01199166

**Non-Inverting Large Signal Pulse Response**



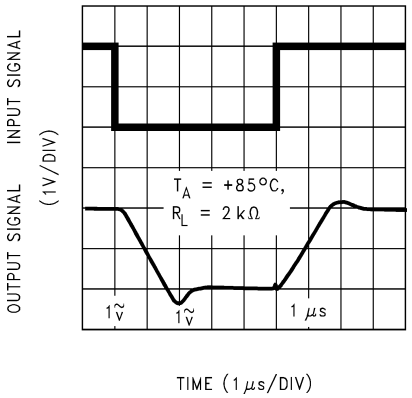

01199167

**Non-Inverting Large Signal Pulse Response**



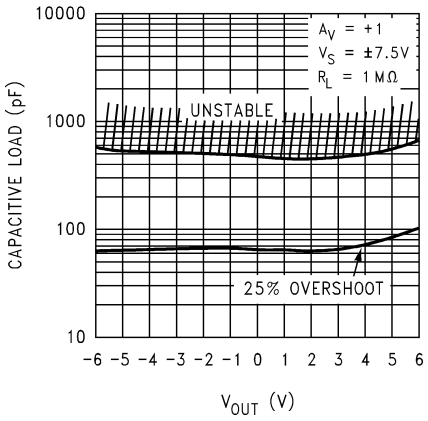

01199168

**Non-Inverting Large Signal Pulse Response**



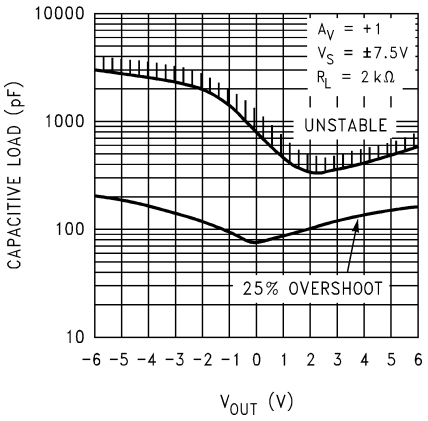

01199169

**Stability vs. Capacitive Load**




01199170

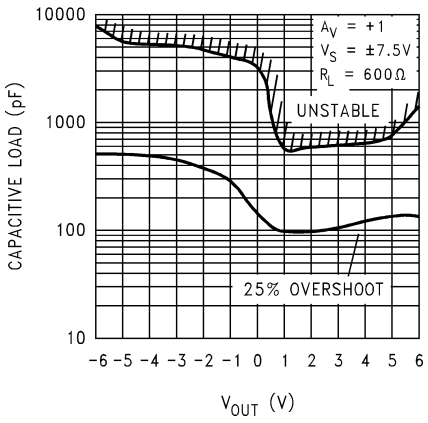
**Stability vs. Capacitive Load**




01199171

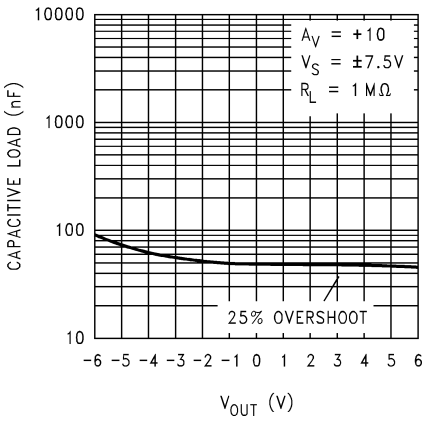
## 15V Typical Performance Characteristics $V^+ = +15V$, $V^- = 0V$, $T_A = 25^\circ C$, unless otherwise specified. (Continued)

**Stability vs. Capacitive Load**



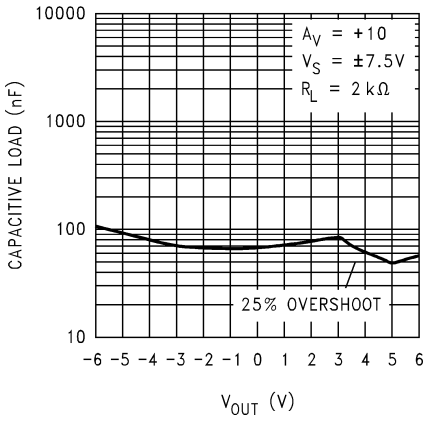

01199175

**Stability vs. Capacitive Load**



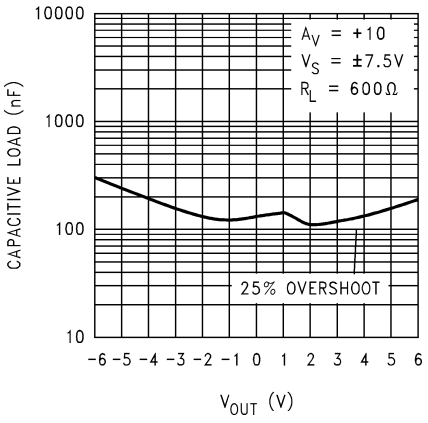

01199176

**Stability vs. Capacitive Load**




01199177

**Stability vs. Capacitive Load**




01199178

# Application Information

### 1.0 BENEFITS OF THE LMC7101 TINY AMP

#### Size

The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

#### Height

The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

#### Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

#### Simplified Board Layout

The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

#### Low THD

The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion — typically 0.01% at 10 kHz with a 10 kΩ load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

#### Low Supply Current

The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

#### Wide Voltage Range

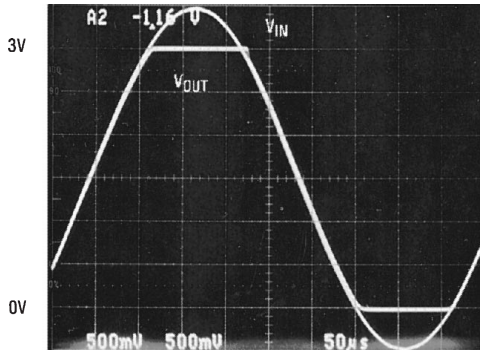
The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

### 2.0 INPUT COMMON MODE

#### Voltage Range

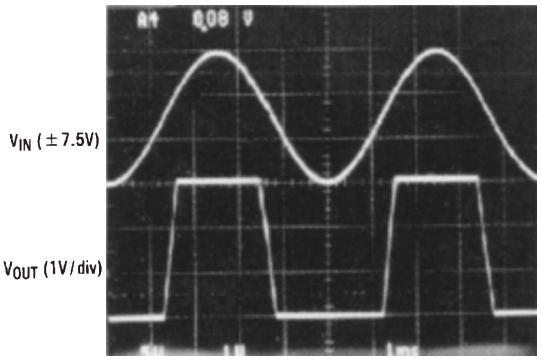
The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins, adversely affecting reliability.




01199108

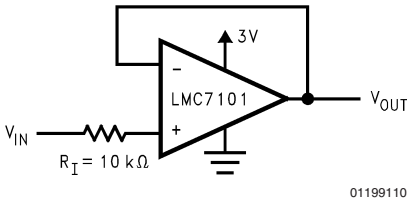
**FIGURE 1. An Input Voltage Signal Exceeds the LMC7101 Power Supply Voltages with No Output Phase Inversion**




01199109

**FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to $R_I$**

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in *Figure 3*.




01199110

**FIGURE 3. $R_I$ Input Current Protection for Voltages Exceeding the Supply Voltage**

### 3.0 RAIL-TO-RAIL OUTPUT

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at $V_S$ = 3V and 110Ω sourcing and 80Ω sinking at $V_S$ = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

## Application Information (Continued)

### 4.0 CAPACITIVE LOAD TOLERANCE

The LMC7101 can typically directly drive a 100 pF load with $V_S$ = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

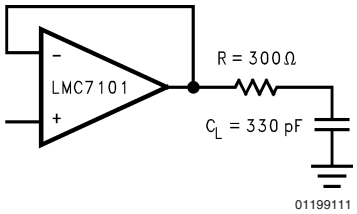



**FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load**

### 5.0 COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 5*), $C_f$ is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_F$ may be different. The values of $C_F$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

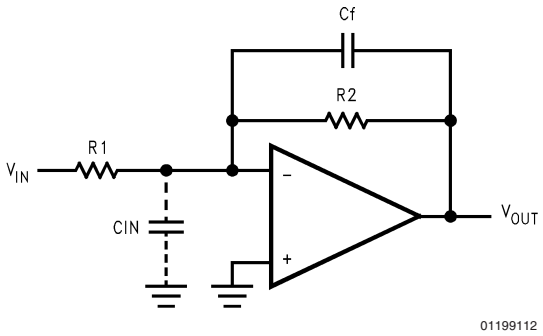



**FIGURE 5. Cancelling the Effect of Input Capacitance**

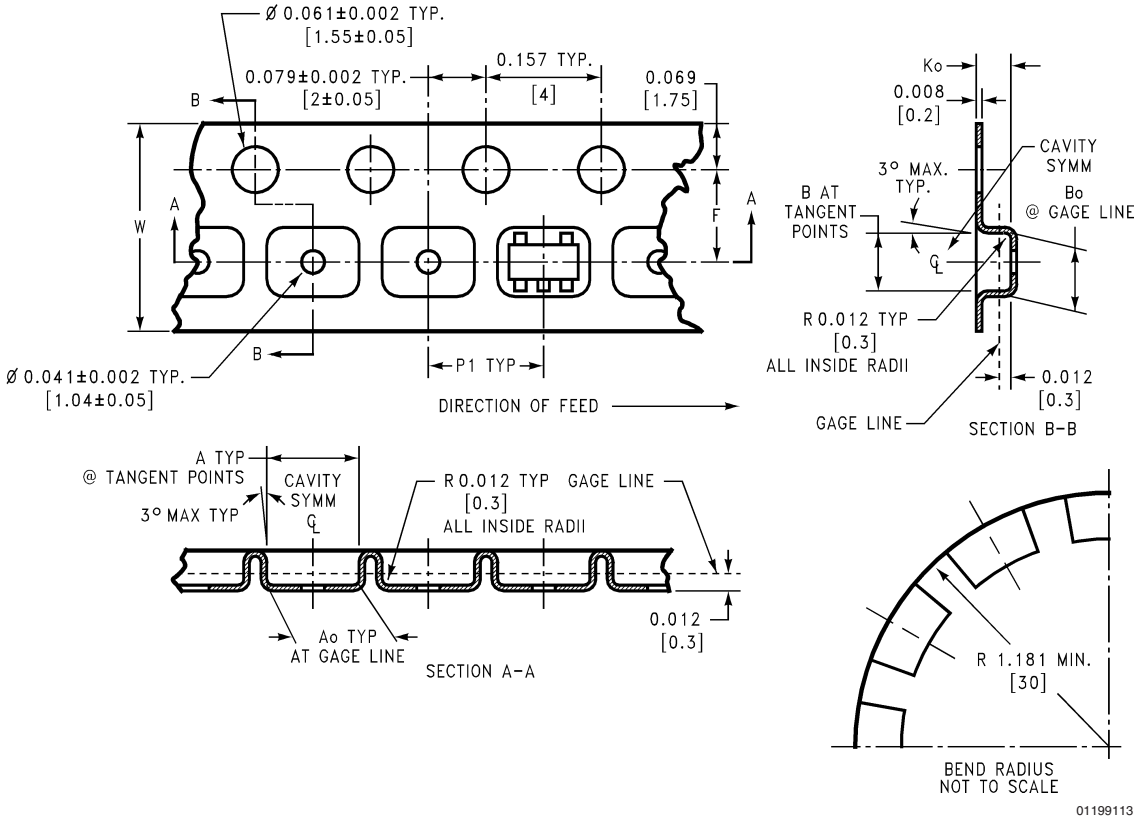
# Application Information (Continued)

## SOT-23-5 TAPE AND REEL SPECIFICATION

### Tape Format

| Tape Section | # Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|
| Leader | 0 (min) | Empty | Sealed |
| (Start End) | 75 (min) | Empty | Sealed |
| Carrier | 3000 | Filled | Sealed |
| | 1000 | Filled | Sealed |
| Trailer | 125 (min) | Empty | Sealed |
| (Hub End) | 0 (min) | Empty | Sealed |

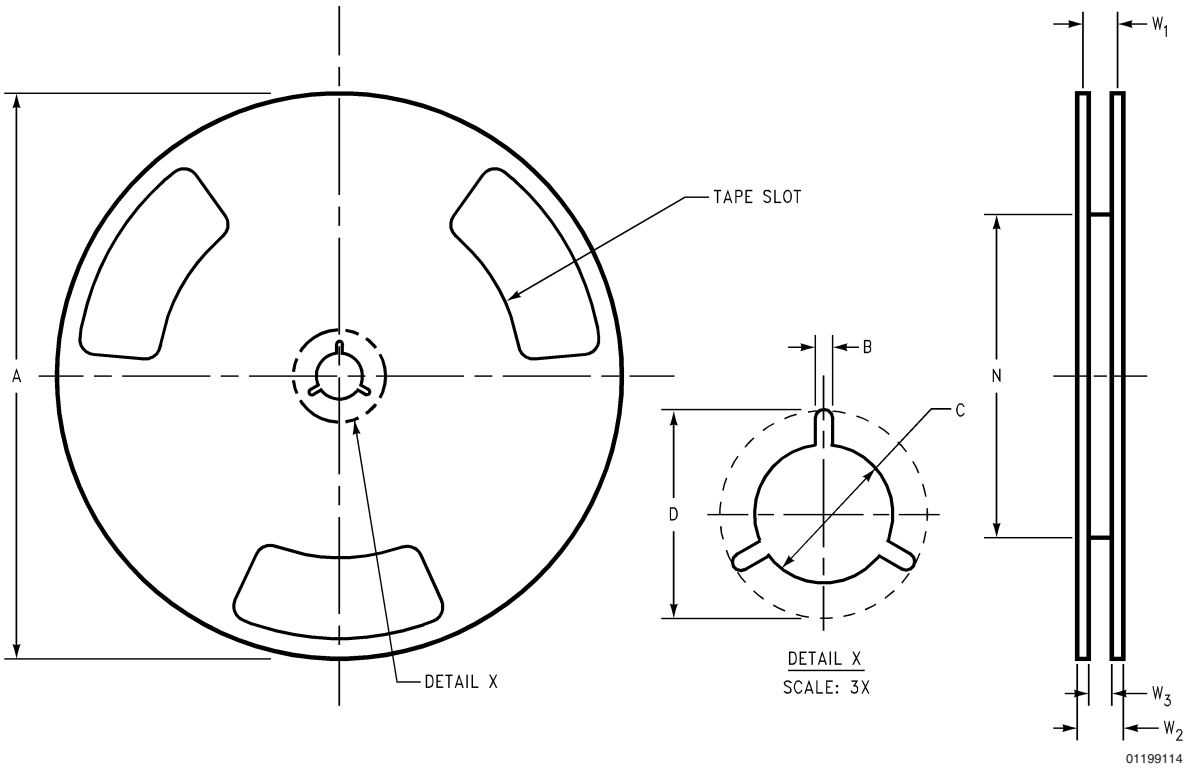
### Tape Dimensions




| 8 mm | 0.130 (3.3) | 0.124 (3.15) | 0.130 (3.3) | 0.126 (3.2) | 0.138 ±0.002 (3.5 ±0.05) | 0.055 ±0.004 (1.4 ±0.11) | 0.157 (4) | 0.315 ±0.012 (8 ±0.3) |
|---|---|---|---|---|---|---|---|---|
| Tape Size | DIM A | DIM Ao | DIM B | DIM Bo | DIM F | DIM Ko | DIM P1 | DIM W |

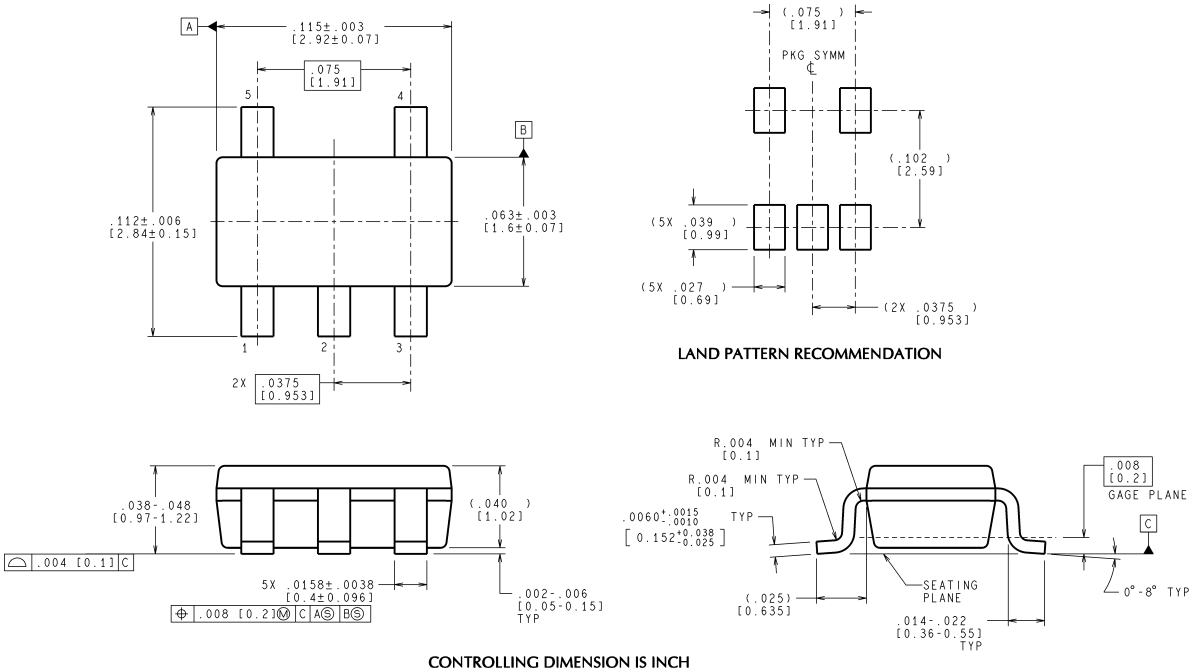
## Application Information (Continued)

**Reel Dimensions**




| 8 mm | 7.00<br>330.00 | 0.059<br>1.50 | 0.512<br>13.00 | 0.795<br>20.20 | 2.165<br>55.00 | 0.331 + 0.059/–0.000<br>8.40 + 1.50/–0.00 | 0.567<br>14.40 | W1+ 0.078/–0.039<br>W1 + 2.00/–1.00 |
|---|---|---|---|---|---|---|---|---|
| Tape Size | A | B | C | D | N | W1 | W2 | W3 |

## Physical Dimensions inches (millimeters) unless otherwise noted




**5-Pin SOT23 Package**
**NS Package Number MF05A**



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