National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM7171AM-X-RH REV 0C0

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Last Major Revision Date: 03/16/00

VERY HIGH SPEED, HIGH OUTPUT CURRENT, VOLTAGE FEEDBACK AMPLIFIER: ALSO AVAILABLE GUARANTEED TO 300K RAD(Si) TESTED TO MIL-STD-883, METHOD 1019.5

General Description

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier; yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as + 2 or -1. It provides a very high slew rate at 2000V/uS (Minimum) and a wide gain-bandwidth product of 170MHz (Minimum) while consuming only 6.5mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100mA output current, the LM7171 can be used for video distribution, as a transformer driver, or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 is ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on National's advanced VIP(TM)III(Vertically integrated PNP) complementary bipolar process.

Industry Part Number

LM7171AM

Prime Die

LM7171

Controlling Document

See Features Section

NS Part Numbers

LM7171AMJ-QML
LM7171AMJ-QMLV
LM7171AMJFQML
LM7171AMJFQMLV
LM7171AMW-QML
LM7171AMW-QMLV
LM7171AMWFQMLV
LM7171AMWG-QML
LM7171AMWG-QMLV
LM7171AMWGFQML
LM7171AMWGFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Typical)

- Easy to use Voltage Feedback Topology
- Very High Slew Rate 2400V/us
- Wide Unity-Gain Bandwidth 200Mhz
- -3dB Frequency @ Av = +2 220 Mhz
- Low Supply Current 6.5 mA
- High Open Loop Gain 85 dB
- High Output Current 100 mA
- Specified for ±15V and ±5V operation

CONTROLLING DOCUMENTS:

LM7171AMJ-QML	5962-9553601QPA
LM7171AMJ-QMLV	5962-9553601VPA
LM7171AMJFQML	5962F9553601QPA
LM7171AMJFQMLV	5962F9553601VPA
LM7171AMW-QML	5962-9553601QHA
LM7171AMW-QMLV	5962-9553601VHA
LM7171AMWFQMLV	5962F9553601VHA
LM7171AMWG-QML	5962-9553601QXA
LM7171AMWG-QMLV	5962-9553601VXA
LM7171AMWGFQML	5962F9553601QXA
LM7171AMWGFQMLV	5962F9553601VXA

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

APPLICATION NOTES:

PERFORMANCE DISCUSSION: The LM7171 is a very high speed, voltage feedback amplifier. It consumes only 6.5mA supply current while providing a gain-bandwidth product of 170MHz (Minimum) and a slew rate of 2000V/uS (Minumum). It also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFA's) have high impedance nodes. The low impedance inverting input in CFA's and a feedback capacitor create an additional pole that will lead to instability. As a result, CFA's cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators, where a feedback capacitor is required.

Applications (Continued)

CIRCUIT OPERATION: The class AB input stage in the LM7171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM7171 Simplified Schematic, (see AN00006) Q1 through Q4 form the equivalent of the current feedback input buffer, RE the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

SLEW RATE CHARACTERISTIC: The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor RE. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. See the LM7171 Commercial Data Book for slew rate Vs input voltage level curve.

When a very fast, large signal, pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1K Ohm in series with the input of the LM7171, the bandwidth is reduced to help lower the overshoot.

SLEW RATE LIMITATION: If the amplifier's input signal has too large of an amplitude at too high of a frequency, the amplifier is said to be slew rate limited; this can cause ringing in time domain, and peaking in frequency domain, at the output of the amplifier.

In the Commercial Data Book "Typical Performance Characteristics" section, there are several curves of Av = +2 and Av = +4 versus input power levels. For the Av = +4 curves, no peaking is present and the LM7171 responds identically to the different input power levels of 30 mV, 100 mV and 300mV.

For the Av = +2 curves, slight peaking occurs. This peaking at high frequency (>100MHz) is caused by a large input signal at high enough frequency, that it exceeds the amplifier's slew rate. The peaking in frequency response does not limit the pulse response in time domain. The LM7171 is stable with noise gain of $\geq$ +2.

LAYOUT CONSIDERATION: PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS: There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation, and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space must be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES: Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENT SELECTION & FEEDBACK RESISTOR: It is important in high speed applications to keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM7171, a feedback resistor of 510 Ohms gives optimal performance.

COMPENSATION FOR INPUT CAPACITANCE: The combinations of an amplfier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value Cf>(Rg X Cin)/Rf can be used to cancel that pole. For LM7171, a feedback capacitor of 2pF is recommended. AN00003 illustrates the compensation circuit.

POWER SUPPLY BYPASSING: Bypassing the power supply is necessary to maintain low power supply impedance across the frequency spectrum. Both positive and negative power supplies should be bypassed individually by placing 0.01uF ceramic capacitors directly to the power supply pins and 2.2uF tantalum capacitors close to the power supply pins. See AN00004.

TERMINATION: In high frequency applications, reflection occur if signals are not properly terminated. Figure 3, in the Commercial Data Book, shows a properly terminated signal, while Figure 4, in the Commercial Data Book, shows an improperly terminated signal.

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75 Ohm characteristic impedance, and RG58 has 50 Ohm characteristic impedance.

Applications (Continued)

DRIVING CAPACITIVE LOADS: Amplifiers driving capactive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown on AN00005. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends upon the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50 Ohm isolation resistor is recommended for initial evaluation. Figure 6, in the Commercial Data Book, shows the LM7171 driving a 150pF load with the 50 Ohm isolation resistor.

POWER DISSIPATION: The maximum power allowed to dissipate in a device is defined as: Pd = [Tj(max) - TA]/ThetaJA, where Pd (is the power dissipation in a device), Tj(max) (is the maximum junction temperature), TA (is the ambient temperature), ThetaJA (is the thermal resistance of a particular package).

For example, for the LM7171 in a J-8 package, the maximum power dissipation at 25 C ambient temperature is 730mW.

The total power dissipation in a device can be calculated as: Pd = Pq + Pl

Pq is the quiescent power dissipated in a device with no load connected at the output. Pl is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore, Pq = supply current x total supply voltage with no load, Pl = output current x (voltage difference between supply voltage and output voltage of the same side of supply voltage).

For example, the total power dissipated by the LM7171 with Vs = ≤15V and output voltage of 10V into 1K Ohm is:

Pd = Pq + Pl

= (6.5mA)x(30V)+(10mA)x(15V - 10V)

= 195mW + 50mW

= 245mW

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (V+ - V-)		36V
Differential Input Voltage (Note 6)		±10V
Maximum Junction Temperature		150 C
Maximum Power Dissipation (Note 2, 3)		730mW
Output Short Circuit to Ground (Note 4)		Continuous
Operating Temperature Range		-55 C ≤ Ta ≤ +125 C
Thermal Resistance (Note 7)		
ThetaJA		
8-Pin CERAMIC DIP	(Still Air)	106 C/W
	(500LF/Min Air flow)	53 C/W
10-Pin CERPAK	(Still Air)	182 C/W
	(500LF/Min Air flow)	105 C/W
10-Pin CERAMIC SOIC	(Still Air)	182 C/W
	(500LF/Min Air flow)	105 C/W
ThetaJC (Note 3)		
8-Pin CERAMIC DIP		3 C/W
10-Pin CERPAK		5 C/W
10-Pin CERAMIC SOIC		5 C/W
Package Weight (Typical)		
8-Pin CERAMIC DIP		965mg
10-Pin CERPAK		235mg
10-Pin CERAMIC SOIC		230mg
Storage Temperature Range		-65 C ≤ Ta ≤ +150 C
ESD Tolerance (Note 5)		3000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

(Continued)

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.
Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C.
Note 5: Human body model, 1.5k Ohms in series with 100pF.
Note 6: Input differential voltage is measured at Vs = $\pm$15V.
Note 7: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

(Note 1)

Supply Voltage

$5.5V \leq V+ \leq 36V$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS: ±15V (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +15V, V- = -15V, Vcm = 0V, and Rl > 1M Ohm

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					1	mV	1
						7	mV	2, 3
+Iib	Input Bias Current					10	uA	1
						12	uA	2, 3
-Iib	Input Bias Current					10	uA	1
						12	uA	2, 3
Iio	Input Offset Current					4	uA	1
						6	uA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±10V			85		dB	1
					70		dB	2, 3
PSRR	Power Supply Rejection Ratio	Vs = ±15V to ±5V			85		dB	1
					80		dB	2, 3
Av	Large Signal Voltage Gain	Rl = 1K Ohm, Vout = ±5V	1		80		dB	1
			1		75		dB	2, 3
		Rl = 100 Ohms, Vout = ±5V	1		75		dB	1
			1		70		dB	2, 3
Vo	Output Swing	Rl = 1K Ohm			13	-13	V	1
					12.7	-12.7	V	2, 3
		Rl = 100 Ohms			10.5	-9.5	V	1
					9.5	-9	V	2, 3
	Output Current (Open Loop)	Sourcing, Rl = 100 Ohms	2		105		mA	1
			2		95		mA	2, 3
		Sinking, Rl = 100 Ohms	2			-95	mA	1
			2			-90	mA	2, 3
Is	Supply Current					8.5	mA	1
						9.5	mA	2, 3

Electrical Characteristics

AC PARAMETERS: ±15V (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ = +15V, V- = -15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Sr	Slew Rate	Av = 2, Vin = ±2.5V, 3nS Rise & Fall time	3, 4		2000		V/uS	4
Gbw	Unity-Gain Bandwidth		5		170		MHz	4

DC PARAMETERS: ±5V (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +5V, V- = -5V, Vcm = 0V, and Rl > 1M Ohm

Vio	Input Offset Voltage					1.5	mV	1
						7	mV	2, 3
+Iib	Input Bias Current					10	uA	1
						12	uA	2, 3
-Iib	Input Bias Current					10	uA	1
						12	uA	2, 3
Iio	Input Offset Current					4	uA	1
						6	uA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±2.5V			80		dB	1
					70		dB	2, 3
Av	Large Signal Voltage Gain	Rl = 1K Ohm, Vout = ±1V	1		75		dB	1
			1		70		dB	2, 3
		Rl = 100 Ohms, Vout = ±1V	1		72		dB	1
			1		67		dB	2, 3
Vo	Output Swing	Rl = 1K Ohm			3.2	-3.2	V	1
					3.0	-3.0	V	2, 3
		Rl = 100 Ohms			2.9	-2.9	V	1
					2.8	-2.75	V	2, 3
	Output Current (Open Loop)	Sourcing, Rl = 100 Ohms	2		29		mA	1
			2		28		mA	2, 3
		Sinking, Rl = 100 Ohms	2			-29	mA	1
			2			-27.5	mA	2, 3
Is	Supply Current					8	mA	1
						9	mA	2, 3

Electrical Characteristics

DC PARAMETERS: ±15V, DRIFT VALUES (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +15V, V- = -15V, Vcm = 0V, and Rl > 1M Ohm. "Delta calculations performed on JAN S and QMLV devices at Group B, subgroup 5 only."

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-250	250	uV	1
+Ibias	Input Bias Current				-500	500	nA	1
-Ibias	Input Bias Current				-500	500	nA	1

DC PARAMETERS: ±5V, DRIFT VALUES (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +5V, V- = -5V, Vcm = 0V, and Rl > 1M Ohm. "Delta calculations performed on JAN S and QMLV devices at Group B, subgroup 5 only."

Vio	Input Offset Voltage				-250	250	uV	1
+Ibias	Input Bias Current				-500	500	nA	1
-Ibias	Input Bias Current				-500	500	nA	1

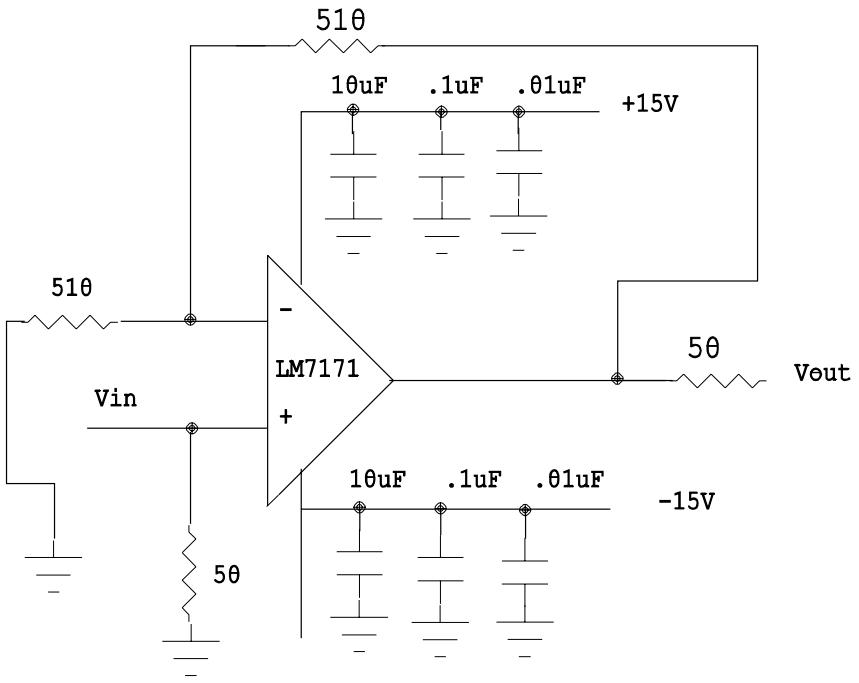
Note 1: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For Vs = ±15V, Vout = ±5V. For Vs = ±5V, Vout = ±1V.
Note 2: The open loop output current is guaranteed, by the measurement of the open loop output voltage swing, using 100 Ohms output load.
Note 3: See AN00001 for Sr test circuit.
Note 4: Slew Rate measured between ±4V.
Note 5: See AN00002 for Gbw test circuit.
Note 6: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05885HRA4	CERDIP (J), 8 LEAD (B/I CKT)
06344HRA1	CERAMIC SOIC (WG, W), 10 LEAD (B/I CKT)
AN00001A	SLEWRATE TEST CKT
AN00002A	CBW TEST CKT
AN00003A	COMPENSATING FOR INPUT CAPACITANCE
AN00004A	POWER SUPPLY BYPASSING
AN00005A	ISOLATION RESISTOR TO DRIVE CAPACITIVE LOAD
AN00006A	SIMPLIFIED SCHEMATIC DIAGRAM
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000029B	CERDIP (J), 8 LEAD (PIN OUT)
P000157A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
P000170A	CERPACK (W), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

LM7171 Slew Rate Test Circuit



Vin = +-2.5V 3nS Rise Time.

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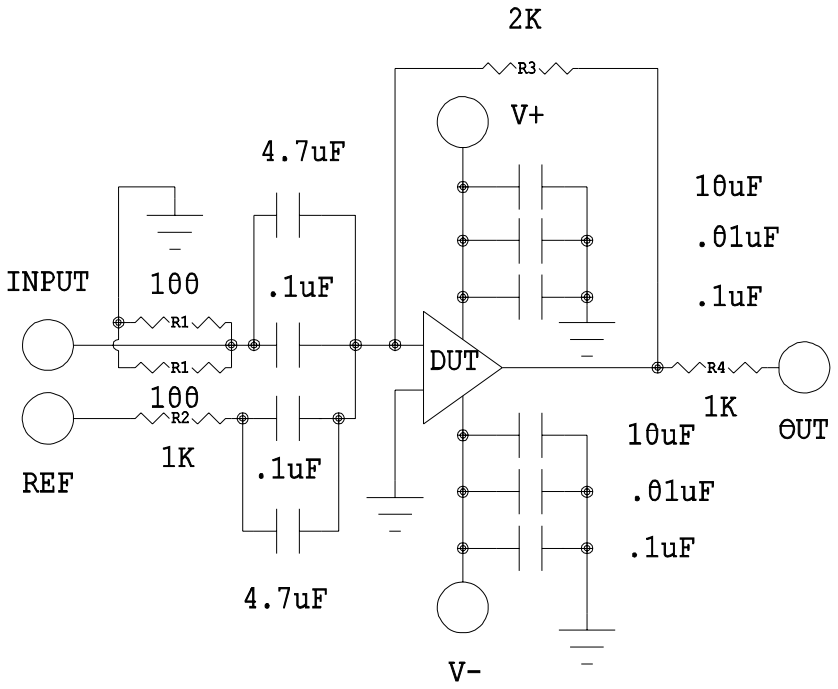
AN00001A

LM7171 GBW Test Circuit



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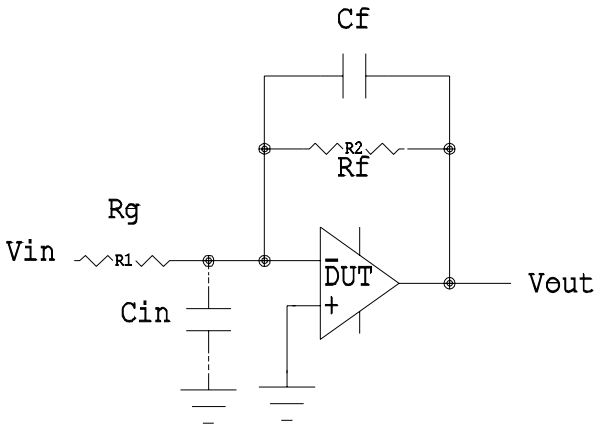
AN00002A



Compensation for Input Capacitance

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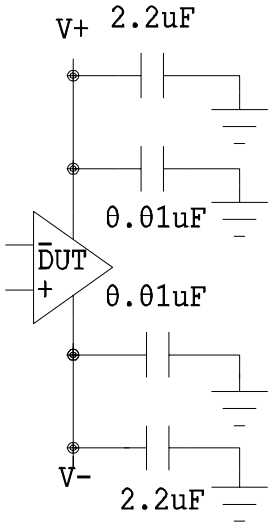
AN00003A



Power Supply Bypassing

AN00004A

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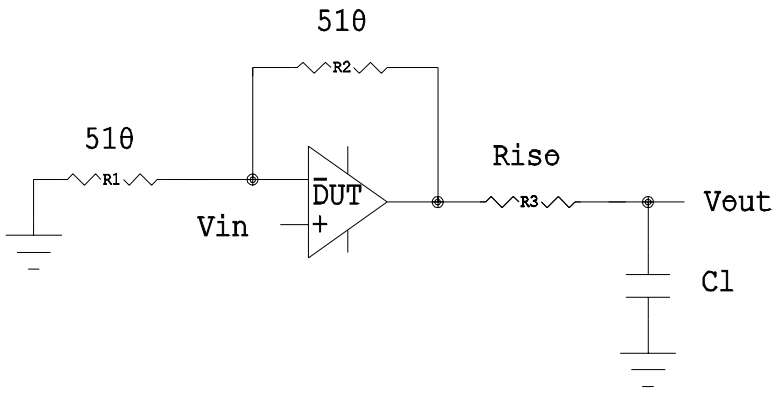

Isolation Resistor Used to Drive Capacitive Load

AN00005A

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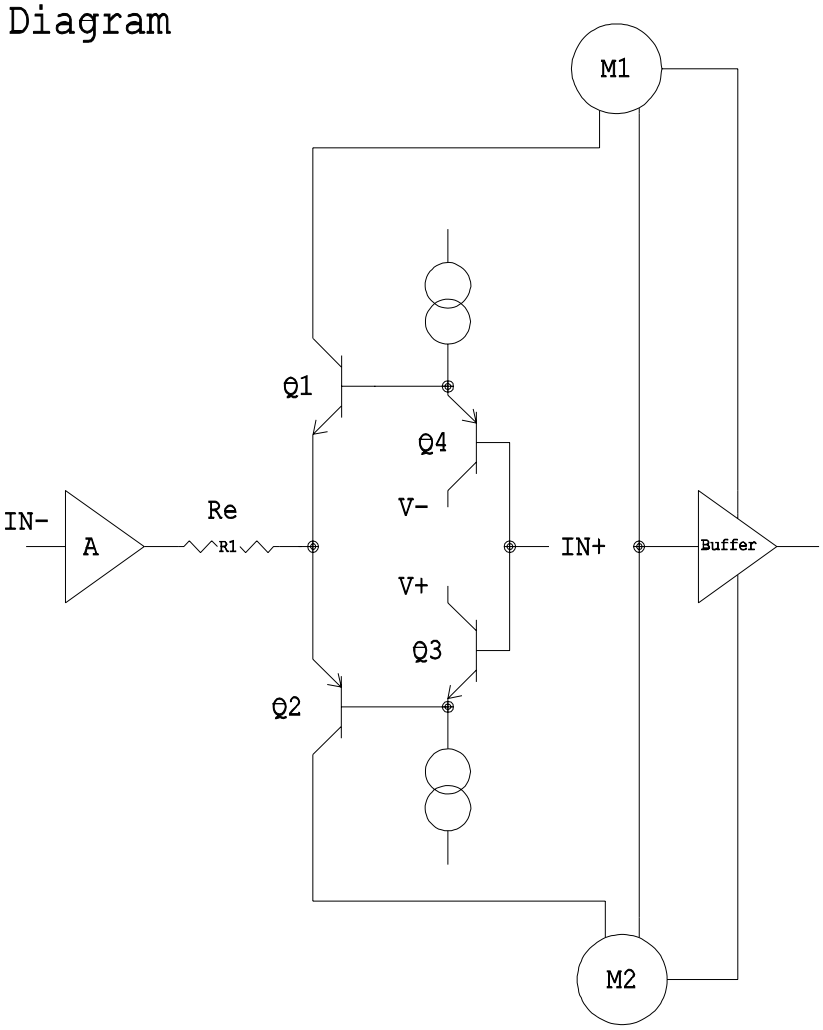
Simplified Schematic Diagram



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AN00006A

REVISIONS				
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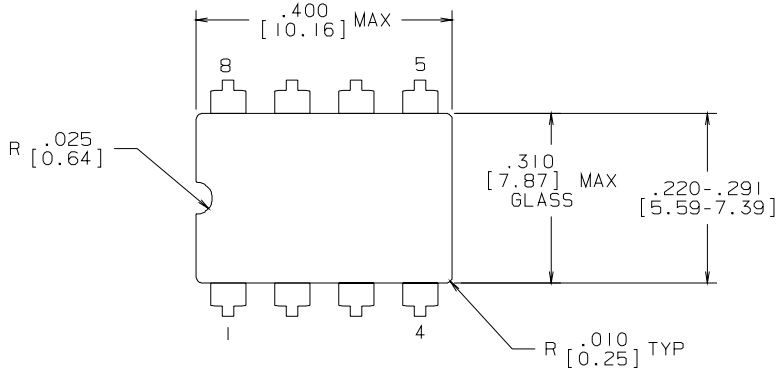
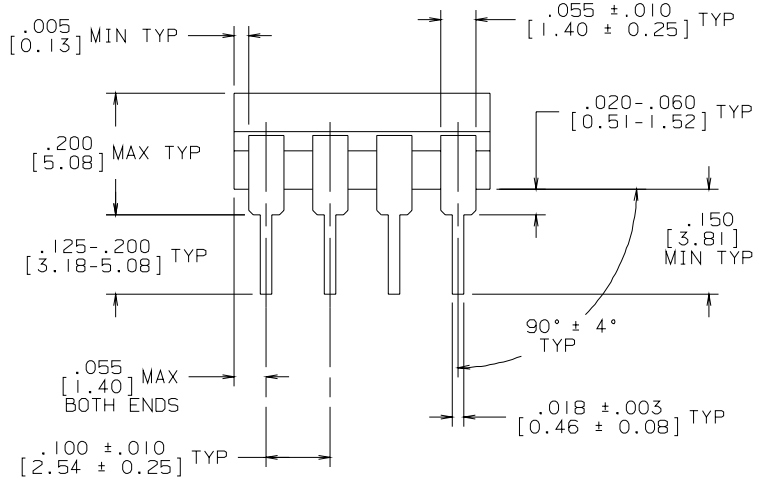
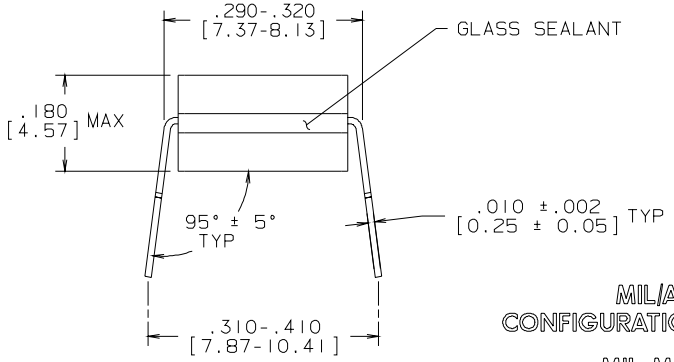
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

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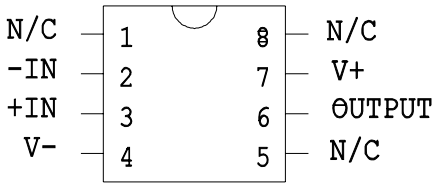
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM7171AMJ-QML

8 - LEAD DIP

CONNECTION DIAGRAM

(TOP VIEW)

P0000298

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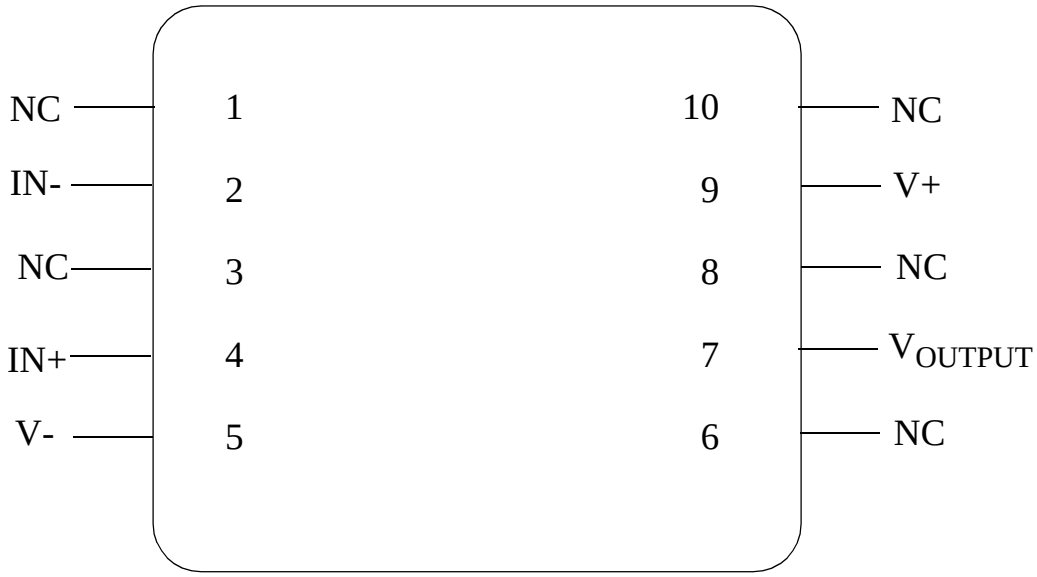

LM7171AMWG

10 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM
TOP VIEW

P000157A

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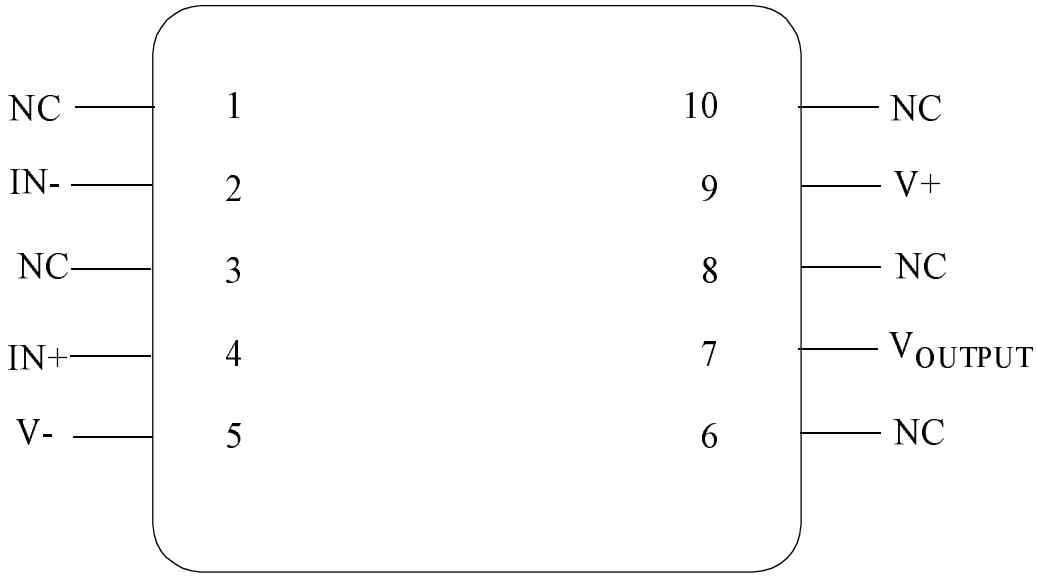
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM7171W-QML

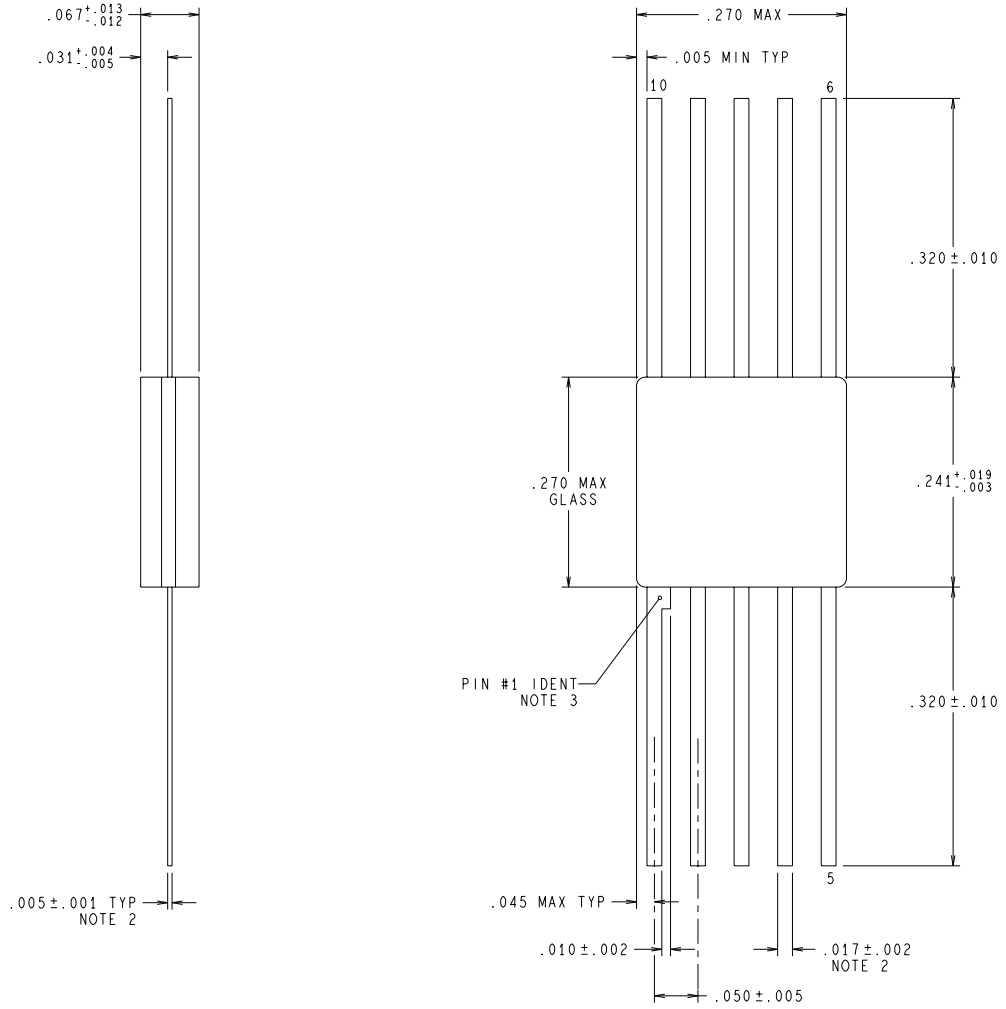
10 - LEAD CERPACK

CONNECTION DIAGRAM
TOP VIEW

P000170A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

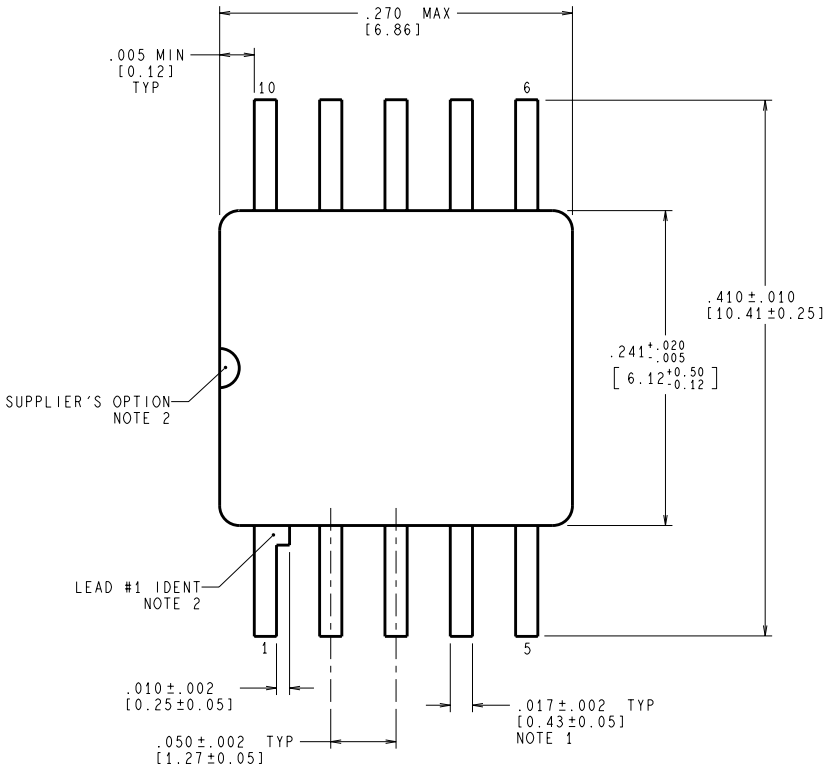
CERPACK, 10 LEAD

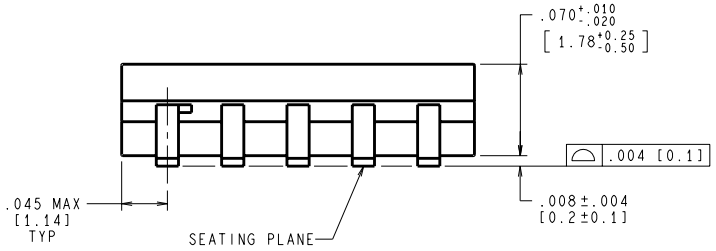
PROJECTION — INCH [MM]

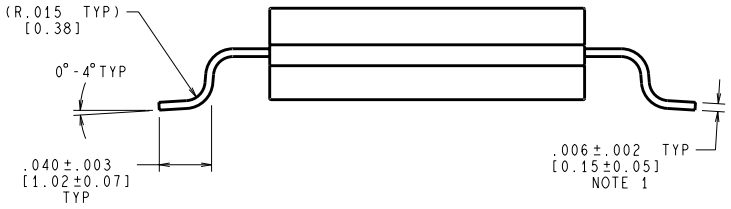
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
10 LEAD,
GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003645	08/31/00	Rose Malone	Initial MDS Release: MNLM7171AM-X-RH, Rev. 0A0
0B0	M0003729	08/02/01	Rose Malone	Update MDS: MNLM7171AM-X-RH, Rev. 0A0 to MNLM7171AM-X-RH, Rev. 0B0. Changed Main Table and Features Section reference to Rad Hard NS Part Numbers and 5962 SMD Drawings for J Pkg and WG Pkg. Changed from RQML, RQMLV, 5962R9553601QPA, VPA, QXA, VXA to FQML, FQMLV, 5962F9553601QPA, VPA, QXA, VXA. Rad Hard Level 100K to 300K.
0C0	M0003819	08/02/01	Rose Malone	Updated MDS: MNLM7171AM-X-RH, Rev. 0B0 to MNLM7171AM-X-RH, Rev. 0C0. Added LM7171AMWFQMLV and SMD reference to Main Table and Features Section.