FAN8038B(KA3038)

4-Channel Motor Drive IC

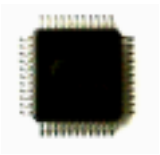
Features

- 4-CH H-Bridge Driver
- Built-in DC/DC Converter Controller Circuit
- Built-in Reset Circuit
- Built-in Battery Charging Circuit
- Built-in Voltage Drop Detector
- Built-in Thermal Shutdown Circuit
- Built-in General OP-AMP
- Low Power Consumption
- Built-in Power Controller Circuit

Description

FAN8038B is monolithic IC for portable CD player.

44-QFP-1010B



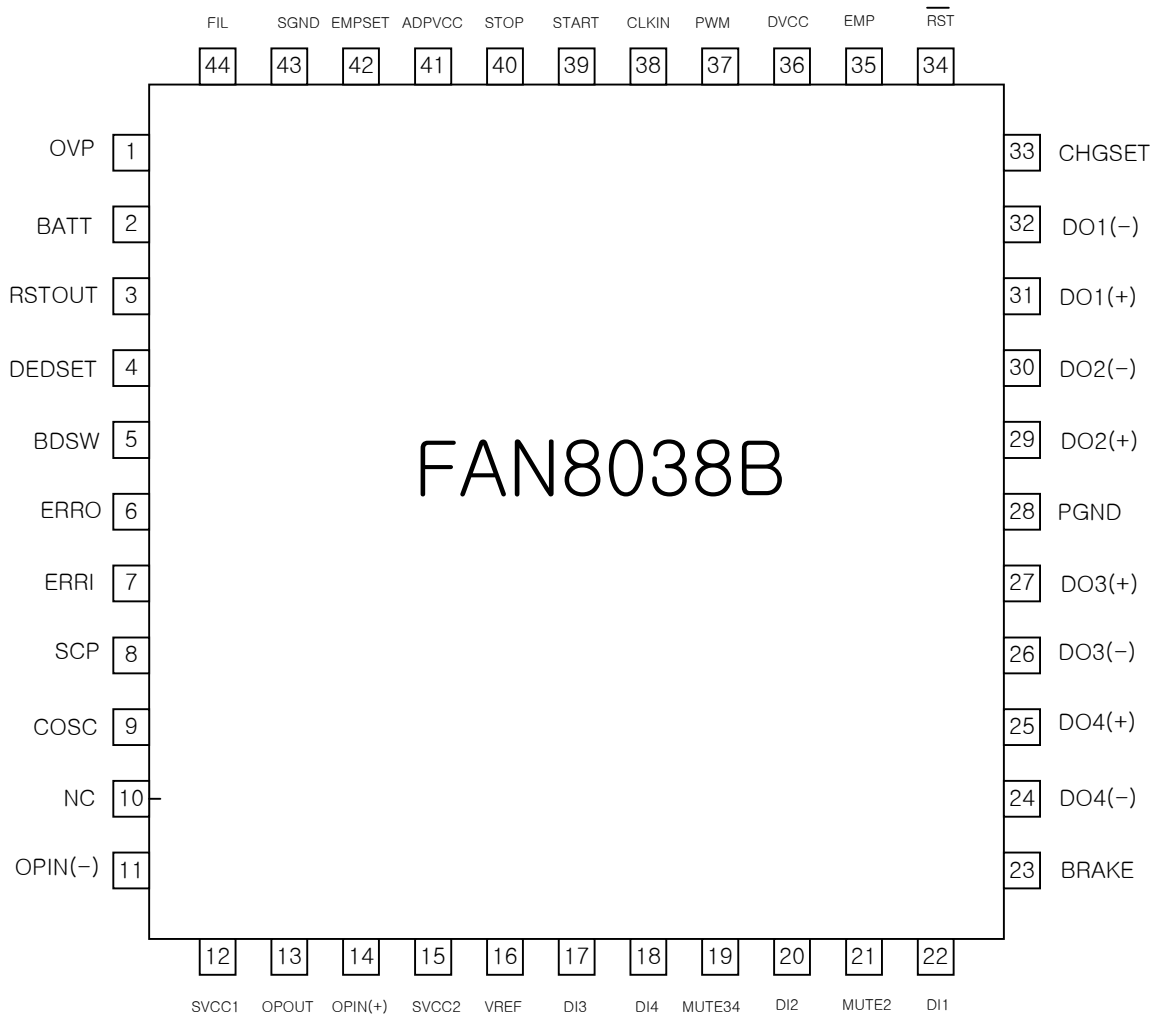
Typical application

- Portable Compact Disk Player (CDP)
- Portable Mini Disk Player (MD)
- Disc-Man
- Other Potable Compact Disk Media

Ordering Information

Device	Package	Operating Temp.
FAN8038B	44-QFP-1010B	-35°C ~ +85°C

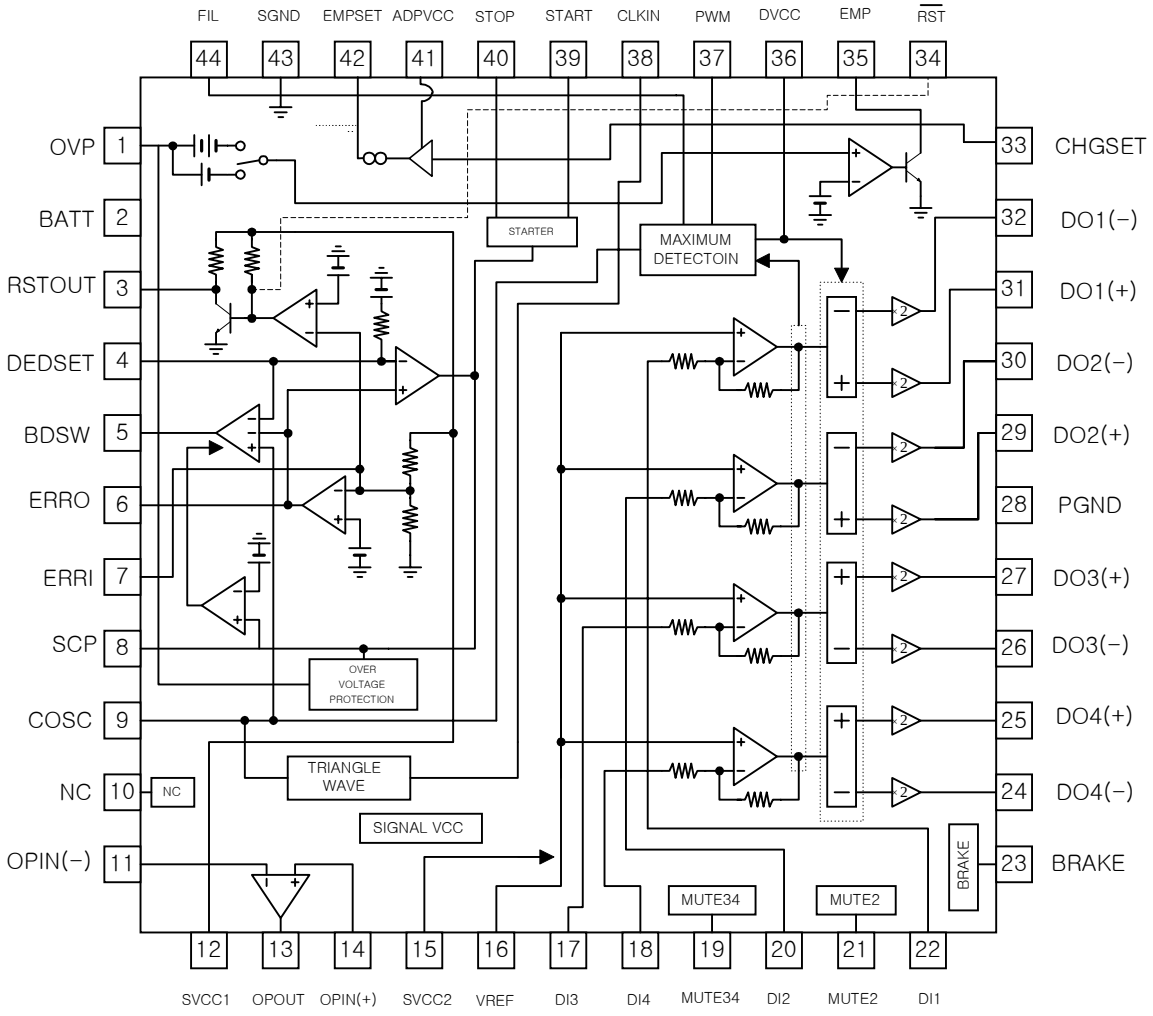
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	OVP	Battery Power Supply Mode
2	BATT	Battery Power Supply
3	RSTOUT	RSTOUT Detection Output
4	DEDSET	DEDSET Time Setting
5	BDSW	Booster Transistor Drive
6	ERRO	Error Amp Output
7	ERRI	Error Amp Input
8	SCP	Short Circuit Protection Setting
9	COSC	Triangular Wave Output
10	N.C	No Connection
11	OPIN(-)	OP-AMP Negative Input
12	SVCC1	Control Circuit Power Supply
13	OPOUT	OP-AMP Output
14	OPIN(+)	OP-AMP Positive Input
15	SVCC2	Pre-Drive Power Supply
16	VREF	Reference Voltage
17	DI3	CH3 Control Signal Input
18	DI4	CH4 Control Signal Input
19	MUTE34	CH3, 4 Mute
20	DI2	CH2 Control Signal Input
21	MUTE2	CH2 Mute
22	DI1	CH1 Control Signal Input
23	BRAKE	CH1 Brake
24	DO4(-)	CH4 Negative Output
25	DO4(+)	CH4 Positive Output
26	DO3(-)	CH3 Negative Output
27	DO3(+)	CH3 Positive Output
28	PGND	Power Unit Power Ground
29	DO2(+)	CH2 Positive Output
30	DO2(-)	CH2 Negative Output
31	DO1(+)	CH1 Positive Output
32	DO1(-)	CH1 Negative Output
33	CHGSET	Charge Current Setting
34	RST	RSTOUT Inverting Output
35	EMP	Empty Detection Output
36	DVCC	H-Bridge Power Supply
37	PWM	PWM Transistor Drive
38	CLKIN	External Clock Input
39	START	Boost DC/DC Converter Starting
40	STOP	Boost DC/DC Converter Off
41	ADPVCC	Charging Circuit Power Supply
42	EMPSET	Empty Dection Level Converting
43	SGND	Signal Ground
44	FIL	PWM Phase Compensation

Internal Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	13.2	V
Maximum Output Current	I_O	500	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{OPR}	-35 ~ +85	°C
Stroage Temperature	T_{STG}	-55 ~ +150	°C

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charging Circuit Power Supply Voltage	ADPVCC	3.0	4.5	8.0	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Control Circuit Power Supply Voltage	SVCC	2.7	3.2	5.5	V
PRE-Driver V_{CC}	SVCC2	2.7	3.2	5.5	V
Output Voltage	VM	-	PWM	BATT	V
Operating Temperature	Ta	-10	25	70	°C

Electrical characteristics

(Ta=25°C, BATT=2.4V, $SV_{CC}1=SV_{CC}2=3.2V$, $V_{REF}=1.6V$, $ADPV_{CC}=0V$, fCLKIN=88.2kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
COMMON SECTION						
BATT Stand-by Current	I_{ST}	BATT=10.5V,SVCC1, 2=VREF=0V	-	-	5	μA
BATT Supply Current (No Load)	I_{BATT}	DVCC=0.45V, MUTE34=3.2V	-	2.5	3.5	mA
SVCC Supply Current (No Load)	I_{SVCC1}	DVCC=0.45V, MUTE34=3.2V, ERRI=0V	-	3.0	3.5	mA
SVCC2 Supply Current (No Load)	I_{SVCC2}	DVCC=0.45V, MUTE34=3.2V	-	3.5	5.0	mA
ADPVCC Supply Current (No Load)	I_{ADPVCC}	ADPVCC=4.5V, ROUT=OPEN	-	0.2	1.0	mA
H-DRIVE PART						
Voltage Gain CH1, 3, 4 CH2	$G_{VC}134$ $G_{VC}2$	-	12 21.5	14 23.5	16 24.5	dB
Gain Error By Polarity	ΔG_{VC}	-	-2	0	2	dB
Input pin Resistance CH1,3,4 CH2	$R_{DI}134$ $R_{DI}2$	IN=1.7 & 1.8V	9 6	11 7.5	13 9	KΩ
Maximum Output Voltage	V_{OUT}	RL=8Ω, DVCC=BATT=4V, IN=0 ~ 3.2V	1.9	2.1	-	V
Saturation Voltage (Lower)	V_{SAT1}	IO= -300mA, IN=0 & 3.2V	-	240	400	mV
Saturation Voltage (Upper)	V_{SAT2}	IO=300mA, IN=0 & 3.2V	-	240	400	mV
Input offset Voltage	V_{IO}	-	-8	0	8	mV
Output Offset Voltage CH1,3,4 CH2	$V_{OO}134$ $V_{OO}2$	VREF=IN=1.6V	-70 -130	0 0	70 130	mV
DEAD Zone	V_{DB}	-	-20	0	20	mV
Brake1 On Voltage	V_{M1ON}	DI1=1.8V	2.0	-	-	V
Brake1 Off Voltage	V_{M1OFF}	DI1=1.8V	-	-	0.8	V
MUTE2 On Voltage	V_{M2ON}	DI2=1.8V	2.0	-	-	V
MUTE2 Off Voltage	V_{M2OFF}	DI2=1.8V	-	-	0.8	V
MUTE34 On Voltage	V_{M34ON}	DI3=DI4=1.8V	-	-	0.8	V
MUTE34 Off Voltage	V_{M34OFF}	DI3=DI4=1.8V	2.0	-	-	V
VREF On Voltage	V_{REFON}	INn=1.8V(N=1, 2, 3, 4)	1.2	-	-	V
VREF Off Voltage	V_{REFOFF}	INn=1.8V(N=1, 2, 3, 4)	-	-	0.8	V
BRAKE1 Brake Current	I_{BRAKE}	Brake Current	4	7	10	mA

*Granteed Design Value

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM POWER SUPPLY DRIVING						
PWM Sink Current	I_{PWM}	DI1=2.1V	10	13	17	mA
*DVCC Level Shift Voltage	V_{SHIF}	DI1=1.8V, DVCC-OUT1F	0.35	0.45	0.55	V
DVCC Leak Current	I_{DLK}	DVCC=9V, SVCC1,2=BATT=0V	-	0	5	μA
*PWM Amp Transfer Gain	G_{PWM}	DI1=1.8V, DVCC=1.2V ~ 1.4V	1/60	1/50	1/40	1/kΩ
DC/DC CONVERTER						
ERROR AMP						
SVCC1 Pin Threshold Voltage	V_{S1TH}	-	3.05	3.20	3.35	V
ERRO Pin Output Voltage H	V_{EOH}	ERRI=0.7V, IO = -100μA	1.4	1.6	-	V
ERRO Pin Output Voltage L	V_{EOL}	ERRI=1.3V, IO = 100μA	-	-	0.3	V
SHORT CIRCUIT PROTECTION						
SCP Pin Voltage	V_{SCP}	ERRI=1.3V	-	0	0.1	V
SCP Pin Current 1	I_{SCP1}	ERRI=0.7V	6	10	16	μA
SCP Pin Current 2	I_{SCP2}	ERRI=1.3V, OFF=0V	12	20	32	μA
SCP Pin Current 3	I_{SCP3}	ERRI=1.3V, BATT=9.5V	12	20	32	μA
*SCP Pin Impedance	R_{SCP}	-	175	220	265	kΩ
SCP Pin Threshold Voltage	V_{SCPTH}	ERRI=0.7V, COSC=470PF	1.10	1.20	1.30	V
Over Voltage Protection Detect	V_{OVP}	OVP Voltage	9.5	10	10.5	V
TRANSISTOR DRIVING						
BDSW Pin Output Voltage 1H	V_{SW1H}	BATT=COSC=1.5V =SVCC2=0V, 10mA	0.78	0.98	1.13	V
BDSW Pin Output Voltage 2H	V_{SW2H}	COSC=0V, I_O = -10mA, ERRI=0.7V SCP=0V	1.0	1.5	-	V
BDSW Pin Output Voltage 2L	V_{SW2L}	CT=2V, IO=1-mA	-	0.3	0.45	V
BDSW Pin Oscillating Reequency1	f_{SW1}	COSC=470pF, =SVCC2=0V	65	80	95	kHz
SW Pin Oscillating Reequency 2	f_{SW2}	COSC=470pF, CLKIN=0V	60	70	82	kHz
BDSW Pin Oscillating Reequency 3	f_{SW3}	COSC=470pF	-	88.2	-	kHz
***BDSW Pin Minimum Pulse Width	T_{SWMIN}	COSC=470pF, ERRO=0.5 → 0.7V	0.01	-	0.6	μs
Pulse Duty Start	D_{SW1}	COSC=470PF, SVSS1,SVCC2=0V	40	50	60	%
MAX. Pulse Duty at Self-Running	D_{SW2}	COSC=470pF, ERR0=0.8V, CLKIN=0V	50	60	70	%
MAX. Pulse Duty at CLKIN Synchronization	D_{SW3}	ERR0=0.8V, COSC=470pF	45	55	65	%

*Granteed Design Value

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DEAD TIME						
*DEDSET Pin Impedance	R_{DEDSET}	-	52	65	78	kΩ
DEDSET Pin Output Voltage	V_{DEDSET}	-	0.78	0.88	0.98	V
INTERFACE						
STOP Pin Threshold Voltage	V_{STOPTH}	ERRI=1.3V	2.0	-	-	V
STOP Pin Bias Current	I_{STOP}	OFF=0V	75	95	115	µA
START Pin On Threshold Voltage	V_{STATH1}	SVCC1,SVCC2=0V, COSC=2V	1.3	-	-	V
START Pin Off Threshold Voltage	V_{STATH2}	SVCC1,SVCC2=0V, COSC=2V	-	-	2.1	V
START Pin Bias Current	I_{START}	START=0V	13	16	19	µA
CLKIN Pin Threshold Voltage H	$V_{CLKINTH H}$	-	2.0	-	-	V
CLKIN Pin Threshold Voltage L	$V_{CLKINTH L}$	-	-	-	0.8	V
CLKIN Pin Bias Current	I_{CLKIN}	CLKIN=3.2V	-	-	10	µA
START CURCUIT						
Starter Switching Voltage	V_{SSV}	SVCC1,SVCC2=0V → 3.2V START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SSHS}	START=0V	130	200	300	mV
Discharge Release Voltage	V_{DIS}	-	1.63	1.83	2.03	V
RESET CIRCUIT						
*SVCC1 RESET Threshold Voltage Ratio	R_{RSTOTH}	-	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}	-	25	50	100	mV
RSTOUT Pin Output Voltage	V_{RSTO}	IO=1mA, SVCC1,SVCC2=2.8V	-	-	0.5	V
RSTOUT Pin Pull Up Resistance	R_{RSTO}	-	72	90	108	kΩ
RST Pin Output Voltage 1	V_{RST1}	IO= -1mA, SVCC1,SVCC2=2.8V	2.0	-	2.4	V
RST Pin Output Voltage 2	V_{RST2}	IO= -1mA, SVCC1,SVCC2=0V	2.0	-	2.4	V
*RST Pin Pull Up Resistance	R_{RST}	-	77	95	113	kΩ

*Granteed Design Value

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OP-AMP						
Input Bias Current	I_{BIAS}	IN(+)=1.6V	-	-	300	nA
Input Offset Voltage	V_{OFOP}	IN(+)=1.6V	-5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	RL=OPEN	2.8	-	-	V
Low Level Output Voltage	V_{OLOP}	RL=OPEN	-	-	0.2	V
Output Drive Current (Source)	V_{SOURCE}	50Ω GND	-	-6.5	-3.0	mA
Output Drive Current (Sink)	V_{SINK}	50Ω SVCC	0.4	0.7	-	mA
*Open Loop Voltage Gain	GVO	VIN= -75dB, F=1kHz	-	70	-	dB
*Slew Rate	SR	-	-	0.5	-	V/µs
BATTERY CHARGING CURCUIT						
CHGSET Pin Bias Voltage	V_{CHGSET}	ADPVCC=4.5V, CHGSET=1.8kΩ	0.71	0.81	0.91	V
*CHGSET Pin Output Resistance	R_{CHGSET}	ADPVCC=4.5V	0.75	0.95	1.20	kΩ
EMPSET Pin Leak Current 1	I_{EMPSET}	ADPVCC=4.5V, CHGSET=OPEN	-	-	1.0	µA
EMPSET Pin Leak Current 2	I_{EMPSET}	ADPVCC = 0.6V, CHGSET = 1.8kΩ	-	-	1.0	µA
EMPSET Pin Saturation Voltage	V_{EMPSET}	ADPVCC = 4.5V, I_O = 300mA, CHGSET = 0Ω	-	0.45	1.0	V
EMPTY DETECTION						
EMP Detection Voltge 1	V_{EMPT1}	V_{EMPSET} = 0V	2.1	2.2	2.3	V
EMP Detection Voltge 2	V_{EMPT2}	I_{EMPSET} = -2µA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	V_{EMPSET} = 0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	I_{EMPSET} = -2µA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	I_O = 1mA, OVP = 1V	-	-	0.5	V
EMP Pin Output Leak Current	I_{EMPLK}	OVP = 2.4V	-	-	1.0	µA
*OVP Pin Input Resistance	R_{OVP}	V_{EMPSET} = 0V	17	23	27	kΩ
OVP Pin Leak Current	I_{OVPLK}	SVCC1 = SVCC2 = 0V, OVP = 4.5V	-	-	1.0	V
EMP_SET Pin Detection Voltage	V_{EMPSET}	V_{EMPSET} = BATT-$_{EMPSET}$, OVP = 2V	1.5	-	-	V
EMP_SET Pin Detection Current	I_{EMPSET}	EMPSET	-2	-	-	µA

*Granteed Design Value

Application Information

1. Mute Function

- When The BRAKE Pin is low is normal opration (high is CH1 mute on).
- When The Mute2 Pin is low is normal opration (high is CH2 mute on).
- When The Mute34 Pin is high is normal opration (low is CH3,4 mute on).

2. Vref Drop Mute (Figure 1)

- When the Voltage of the mute pin is above 1V, the mute circuit is stopped and the output circuit is.

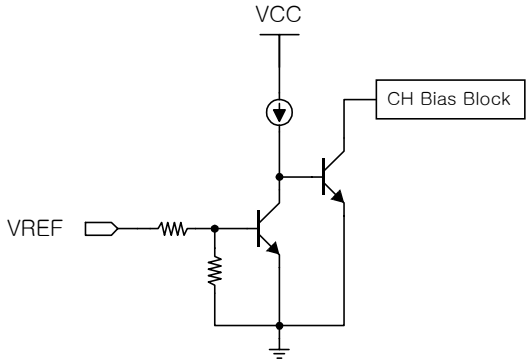


Figure 1. VREF Drop MUTE Circuit

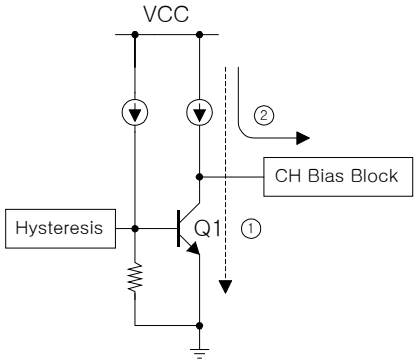


Figure 2. TSD Circuit

3. Thermal Shutdown(Figure 2)

- If the chip temperature rises above 150°C, then the thermal shutdown (TSD) circuit is activated and the output circuit will be mute.

4. H-bridge Driver (4-Channels)

Driver input resistance is 10kΩ of CH1, CH3, CH4 and input resistance of CH2 is 7.5kΩ.

Driver gain can obtain under -mentioned

CH1, 3, 4: $GV = 20\log\left|\frac{55K}{11K + R}\right|$

CH2 $GV = 20\log\left|\frac{110K}{7.5K + R}\right|$

R is External resistance.

5. Switching Regulated Power Supply Drive

- This circuit detects a maximum output value of 4CH drivers and then generates PWM Signal.
- External Component is PNP-Tr, Coil, Schottky Diodeand Capacitor .

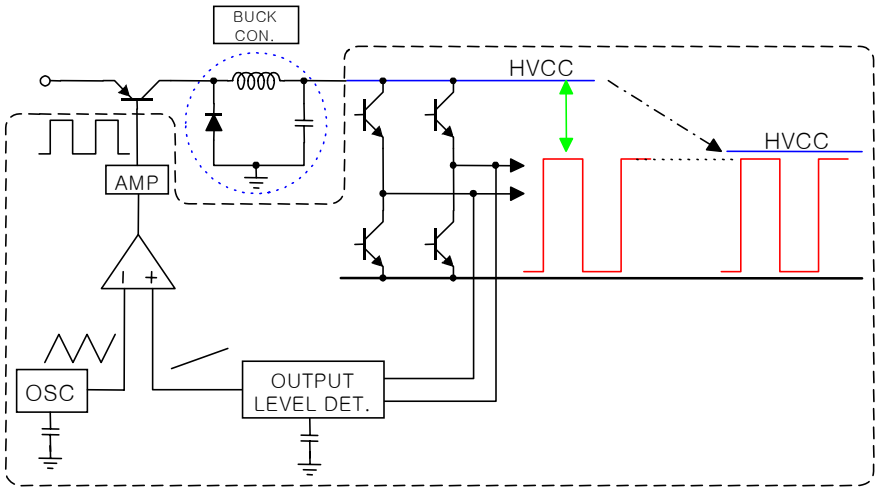


Figure 1. Switching Regulated Power Supply

6. DC/DC Converter Control Circuit

- Booster circuit needs External component. and the voltage() is defined as follows.

$$SVCC1 = 1.267 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}}$$

R1 = Resistor1
R2 = Resistor2
R3 = 30KΩ
R4 = 30.5KΩ

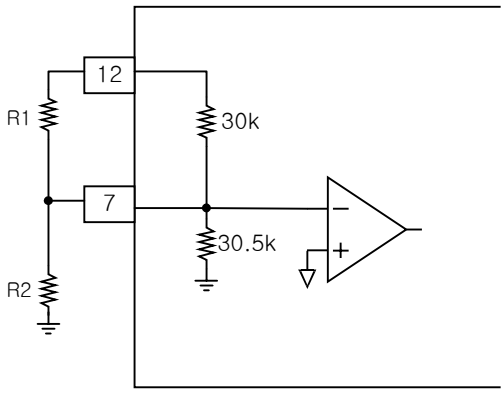


Figure 2. Output Voltage

- Short Circuit Protection function when GND and is short, ERRI become LOW and ERRO HIGH and it makes capacitor charging. fanally AMP3 is OFF.(figure 5)

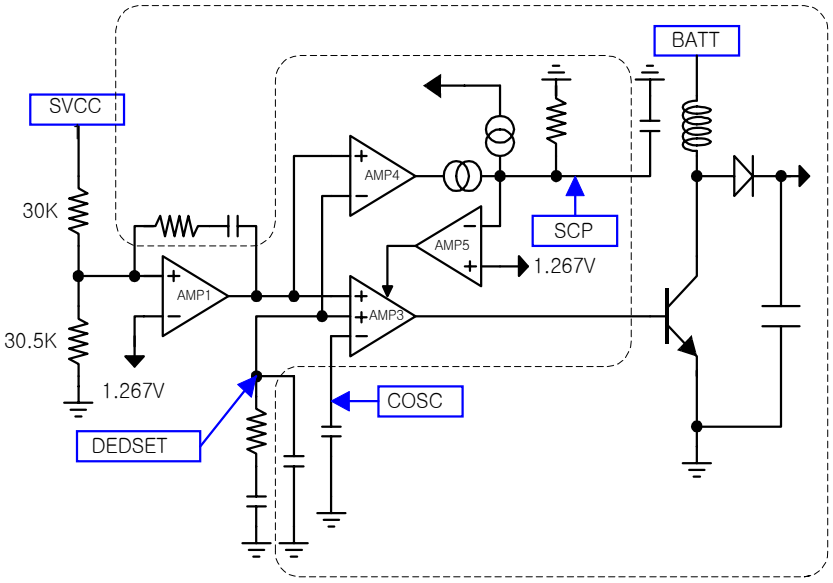


Figure 3. DC/DC Converter Control Circuit

Switching off time depen on a capacitor of the SCP . and the equation is as follow.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{SCP}} \qquad (V_{TH} = 1.25V,\ I_{SPRT} = 10\mu A)$$

- Max Duty can be controlled resistor. the equation is as follow.

$$t = C_{DEDSET} \times R \qquad (R = 65K\Omega)$$

- Capacitor of the SCP terminal can control disable switiching time and it can be calculated by as follow equation.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{STOP}} \qquad (V_{TH} = 1.25V,\ I_{OFF} = 20\mu A)$$

- Over Voltage Protection BATT Voltage is over 9.7V charging SCP terminal Capacitor, it reach to V_{TH} SW terminal signal is OFF the equation is as follow

$$t = C_{SCP} \times \frac{V_{TH}}{I_{HV}} \qquad (V_{TH} = 1.25V,\ I_{HV} = 20\mu A)$$

- If Output Voltage of RSTOUT Circuit DC/DC Conver is over than 90%, RSTOUT terminal turn to HIGH and Hysteresis is 50mV. and RSTOUT stste is ON.

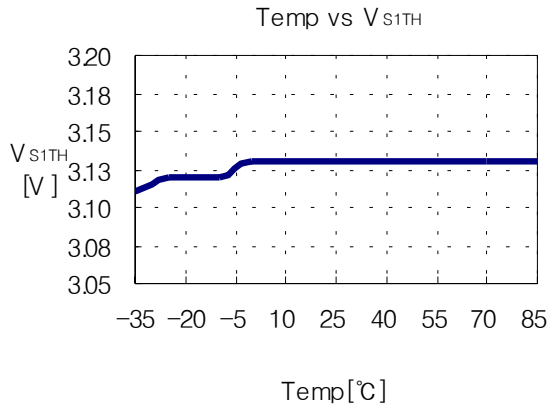
7. Empty Detecting Circuit.

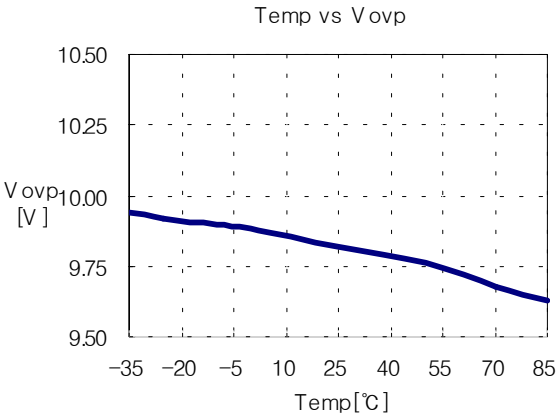
EMPSET	Detect Voltage	Hysteresis	Mode
LOW	2.2V	50mV	Battery Mode
HIGH-Z	1.8V	50mV	Adapter Mode

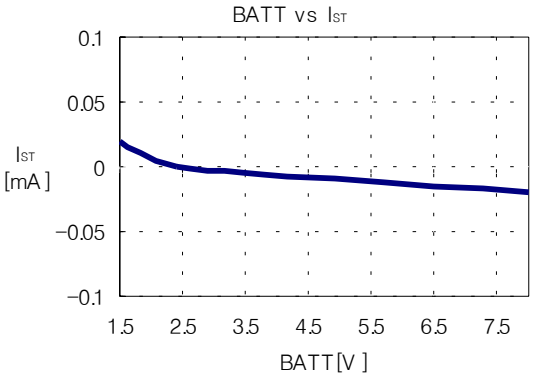
8. Battery Charging Circuit

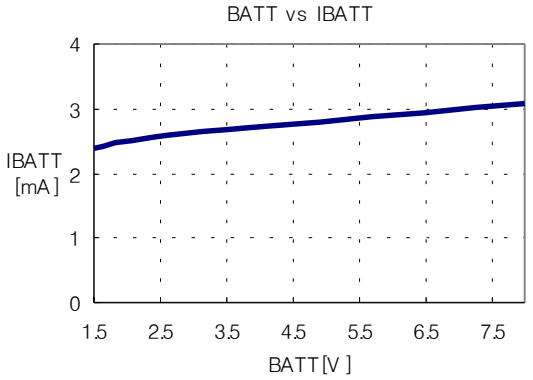
- the battery charger circuit is separated from any other block .
- TSD operate at 150°C. Hysteresis is 30°C

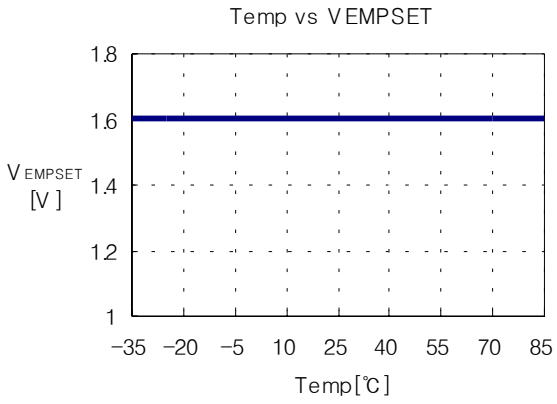
Typical Performance Characteristics

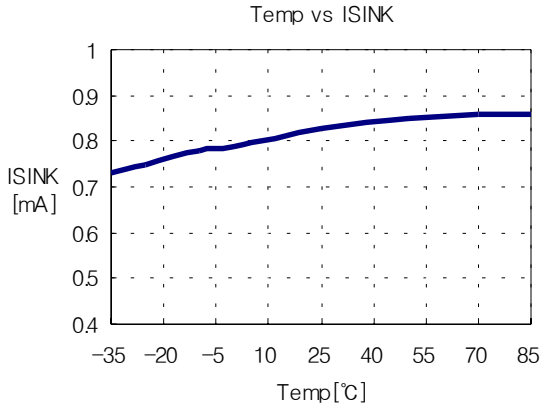




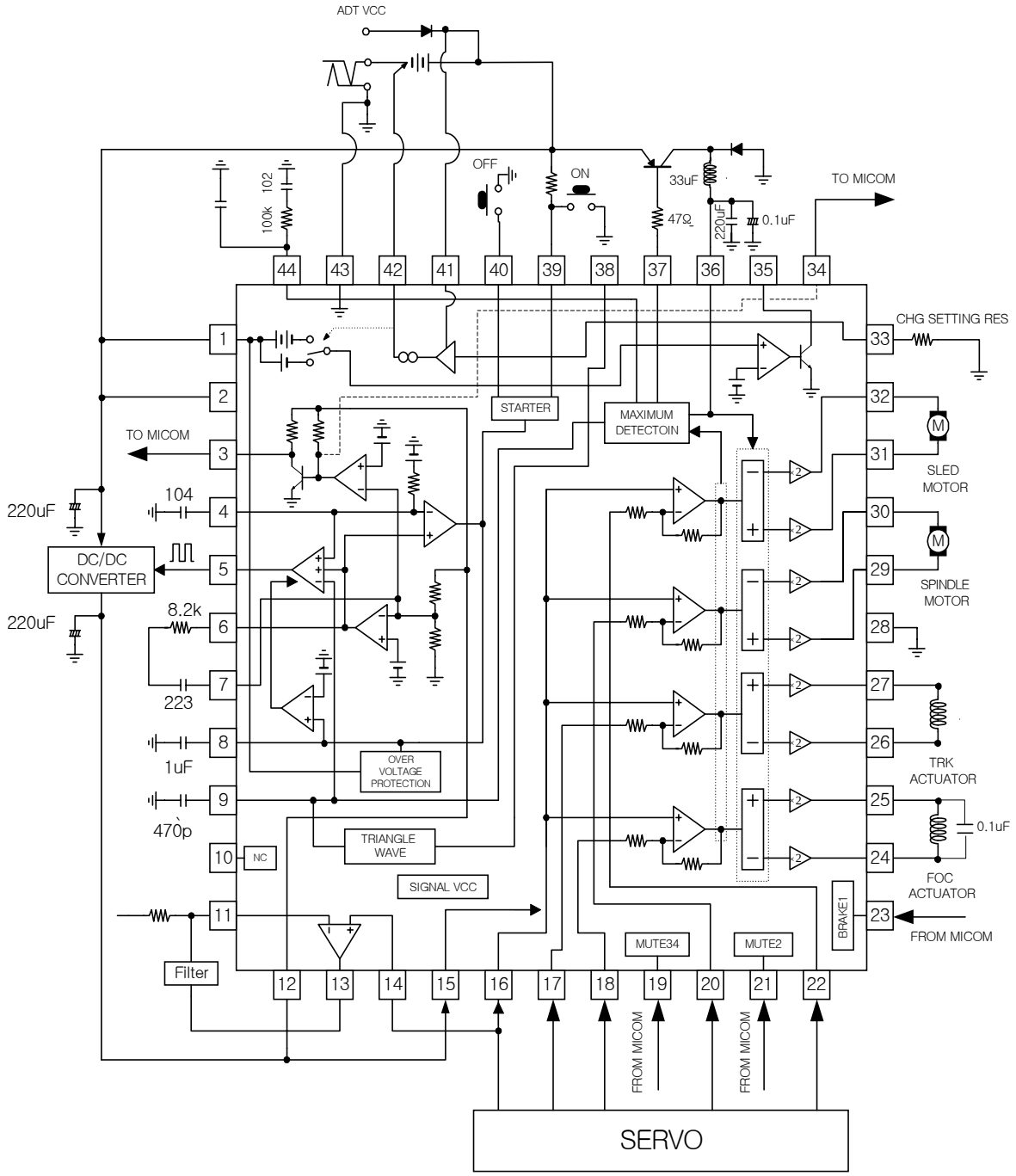








Application Circuits



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