FAIRCHILD SEMICONDUCTOR™

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# MM74C240 • MM74C244
# Inverting • Non-Inverting Octal Buffer and Line Driver with 3-STATE Outputs

## General Description

The MM74C240 and MM74C244 octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with 3-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

## Features

- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 $V_{CC}$ typ)
- Low power consumption
- High capacitive load drive capability
- 3-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

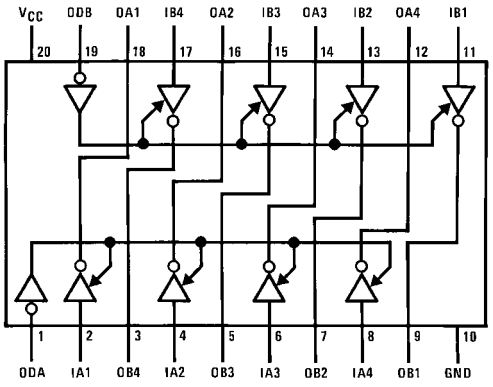
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74C240WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74C240N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| MM74C244WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| MM74C244N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

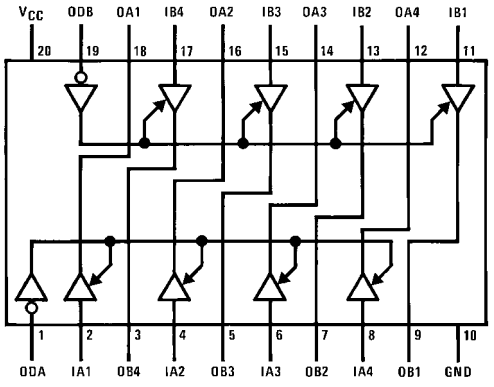
## Connection Diagrams

**MM74C240**




(Top View)

**MM74C244**

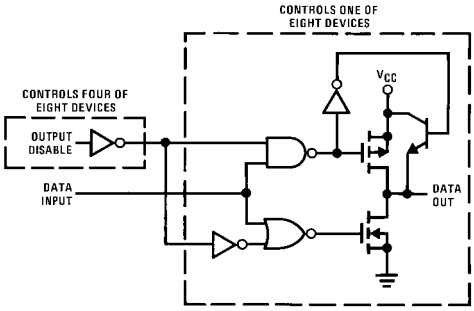



(Top View)

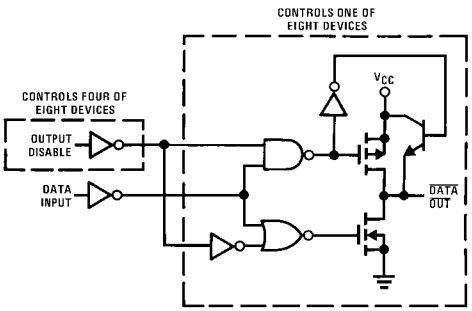
 

## Logic Diagrams

MM74C240




MM74C244




## Truth Tables

MM74C240

| ODA | IA | OA |
|---|---|---|
| 1 | X | Z |
| 1 | X | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

| ODB | IB | OB |
|---|---|---|
| 1 | X | Z |
| 1 | X | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |

1 = HIGH
0 = LOW

MM74C244

| ODA | IA | OA |
|---|---|---|
| 1 | X | Z |
| 1 | X | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |

| ODB | IB | OB |
|---|---|---|
| 1 | X | Z |
| 1 | X | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |

X = Don't Care
Z = 3-STATE

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Voltage at Any Pin | −0.3V to $V_{CC}$ + 0.3V |
| Operating Temperature Range | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Power Dissipation | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3V to 15V |
| Absolute Maximum $V_{CC}$ | 18V |
| Lead Temperature | |
| (Soldering, 10 seconds) | 260°C |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

## DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 5V | 3.5 | | | V |
| | | $V_{CC}$ = 10V | 8.0 | | | |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 5V | | | 1.5 | V |
| | | $V_{CC}$ = 10V | | | 2.0 | |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 5V, $I_O$ = −10 µA | 4.5 | | | V |
| | | $V_{CC}$ = 10V, $I_O$ = −10 µA | 9.0 | | | |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 5V, $I_O$ = 10 µA | | | 0.5 | V |
| | | $V_{CC}$ = 10V, $I_O$ = 10 µA | | | 1.0 | |
| $I_{OZ}$ | 3-STATE Output Current | $V_{CC}$ = 10V, OD = $V_{IH}$ | | | ±10 | µA |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 15V | | 0.005 | 1.0 | µA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 0V | −1.0 | −0.005 | | µA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 15V | | 0.05 | 300 | µA |
| **CMOS/LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 4.75V | $V_{CC}$ − 1.5 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 4.75V | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = −450 µA | $V_{CC}$ − 0.4 | | | V |
| | | $V_{CC}$ = 4.75V, $I_O$ = −2.2 mA | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 2.2 mA | | | 0.4 | V |
| **OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current (P-Channel) | $V_{CC}$ = 5V, $V_{OUT}$ = 0V, $T_A$ = 25°C | −14 | −30 | | mA |
| | | $V_{CC}$ = 10V, $V_{OUT}$ = 0V, $T_A$ = 25°C | −36 | −70 | | mA |
| $I_{SINK}$ | Output Sink Current (N-Channel) | $V_{CC}$ = 5V, $V_{OUT}$ = $V_{CC}$, $T_A$ = 25°C | 12 | 20 | | mA |
| | | $V_{CC}$ = 10V, $V_{OUT}$ = $V_{CC}$, $T_A$ = 25°C | 48 | 70 | | mA |

## AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

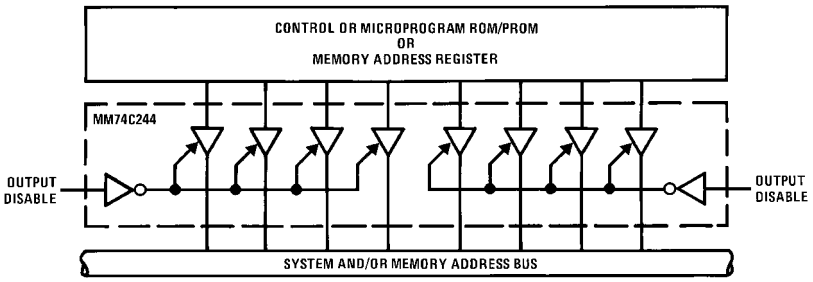
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PD(1)}$, $t_{PD(0)}$ | Propagation Delay (Data In to Out) | | | | | |
| | MM74C240 | $V_{CC} = 5V$, $C_L = 50$ pF | | 60 | 90 | ns |
| | | $V_{CC} = 10V$, $C_L = 50$ pF | | 40 | 70 | |
| | | $V_{CC} = 5V$, $C_L = 150$ pF | | 80 | 110 | |
| | | $V_{CC} = 10V$, $C_L = 150$ pF | | 60 | 90 | |
| | MM74C244 | $V_{CC} = 5V$, $C_L = 50$ pF | | 45 | 70 | ns |
| | | $V_{CC} = 10V$, $C_L = 50$ pF | | 25 | 50 | |
| | | $V_{CC} = 5V$, $C_L = 150$ pF | | 60 | 90 | |
| | | $V_{CC} = 10V$, $C_L = 150$ pF | | 40 | 70 | |
| $t_{1H}$, $t_{0H}$ | Propagation Delay Output Disable to High Impedance State (from a Logic Level) | $R_L = 1k$, $C_L = 50$ pF | | | | ns |
| | | $V_{CC} = 5V$ | | 45 | 80 | |
| | | $V_{CC} = 10V$ | | 35 | 60 | |
| $t_{H1}$, $t_{H0}$ | Propagation Delay Output Disable to Logic Level (from High Impedance State) | $R_L = 1k$, $C_L = 50$ pF | | | | ns |
| | | $V_{CC} = 5V$ | | 50 | 90 | |
| | | $V_{CC} = 10V$ | | 30 | 60 | |
| $t_{T(HL)}$, $t_{T(LH)}$ | Transition Time | $V_{CC} = 5V$, $C_L = 50$ pF | | 45 | 80 | ns |
| | | $V_{CC} = 10V$, $C_L = 50$ pF | | 30 | 60 | |
| | | $V_{CC} = 5V$, $C_L = 150$ pF | | 75 | 140 | |
| | | $V_{CC} = 10V$, $C_L = 150$ pF | | 50 | 100 | |
| $C_{PD}$ | Power Dissipation Capacitance (Output Enabled per Buffer) | (Note 3) | | | | |
| | MM74C240 | | | 100 | | pF |
| | MM74C244 | | | 100 | | |
| | (Output Disabled per Buffer) | | | | | |
| | MM74C240 | | | 10 | | pF |
| | MM74C244 | | | 0 | | |
| $C_{IN}$ | Input Capacitance (Note 4) (Any Input) | $V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$ | | 10 | | pF |
| $C_O$ | Output Capacitance (Note 4) (Output Disabled) | $V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$ | | 10 | | pF |

**Note 2:** AC Parameters are guaranteed by DC correlated testing.

**Note 3:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note, AN-90.

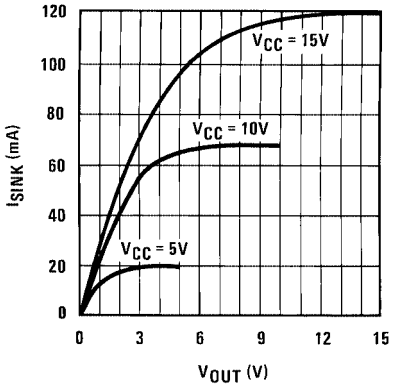
**Note 4:** Capacitance is guaranteed by periodic testing.

## Typical Application

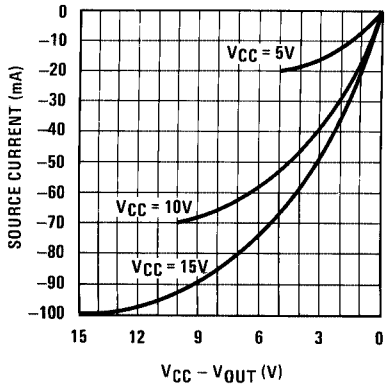



## Typical Performance Characteristics

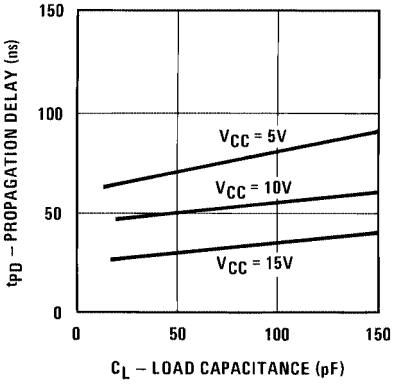
**N-Channel Output Drive at 25°C**



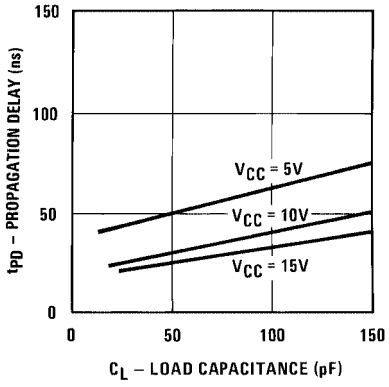

**P-Channel Output Drive at 25°C**




**MM74C240**
**Propagation Delay vs. Load Capacitance**

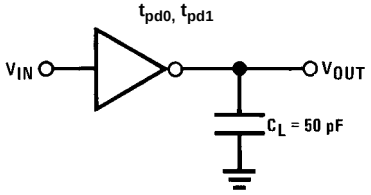



**MM74C244**
**Propagation Delay vs. Load Capacitance**

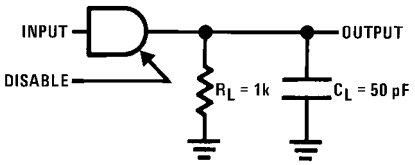


## AC Test Circuits and Switching Time Waveforms

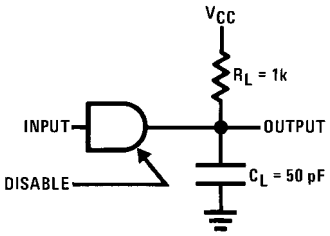
$t_{pd0}$, $t_{pd1}$




$t_{1H}$ and $t_{H1}$

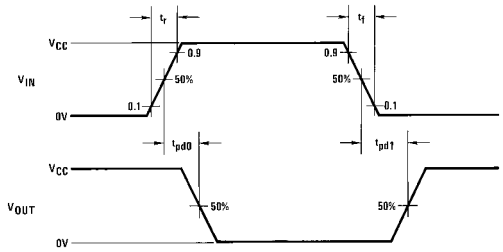



$t_{0H}$ and $t_{H0}$

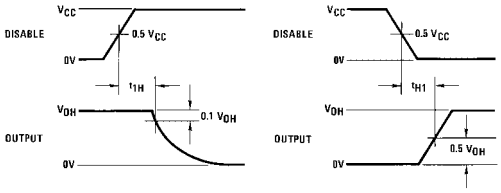



**Note:** Delays measured with input $t_r$, $t_f \leq 20$ ns.

CMOS to CMOS

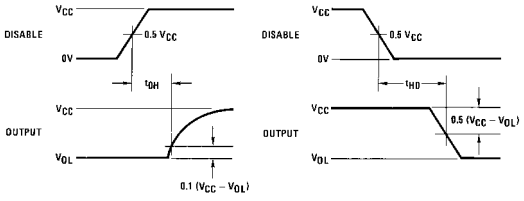



$t_{1H}$ and $t_{H1}$



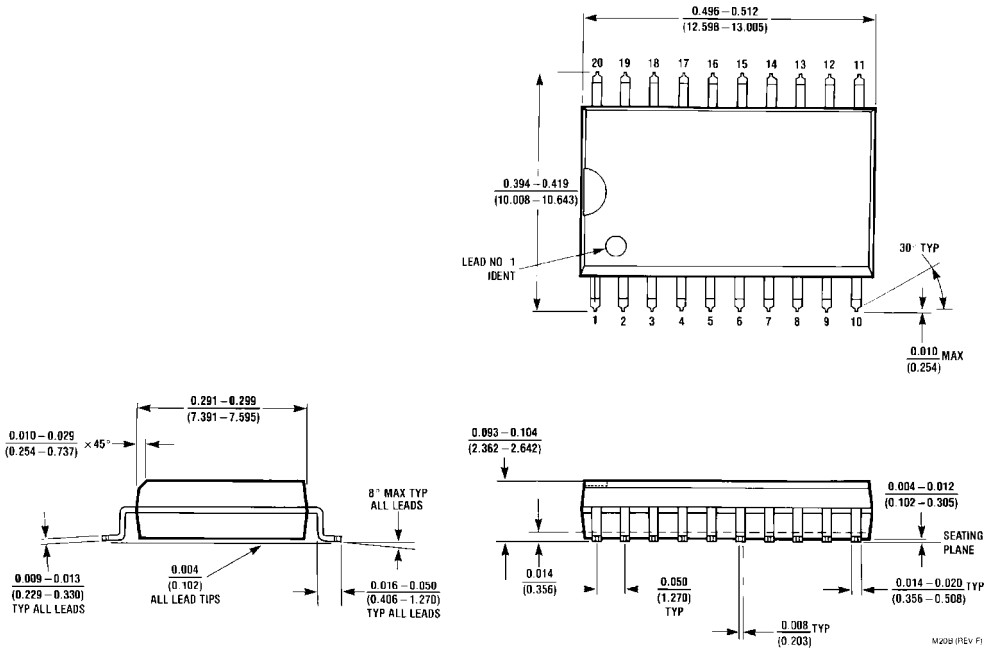

**Note:** $V_{OH}$ is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

$t_{0H}$ and $t_{H0}$



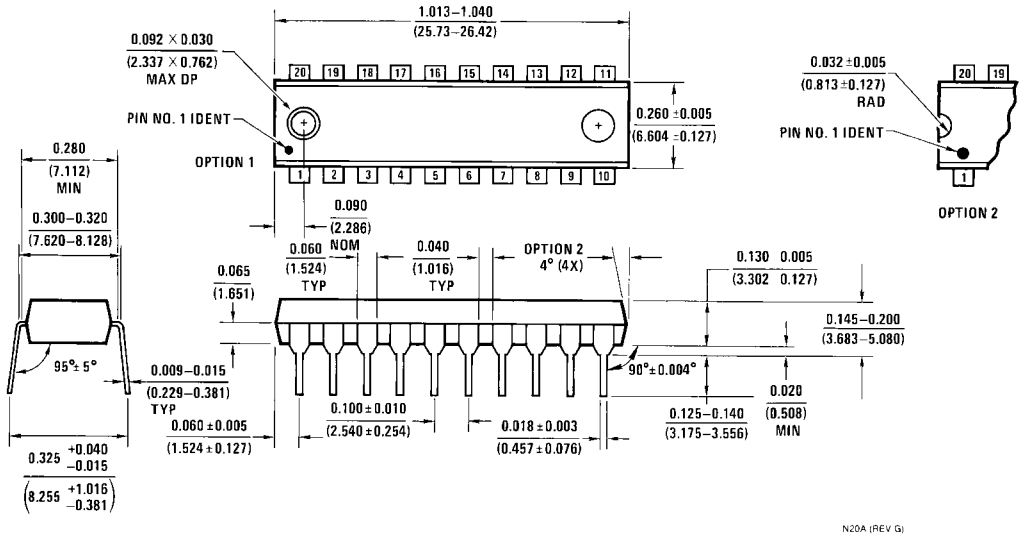

**Note:** $V_{OL}$ is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to $V_{CC}$.

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N20A**



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