National Semiconductor

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DS90LV031A
3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

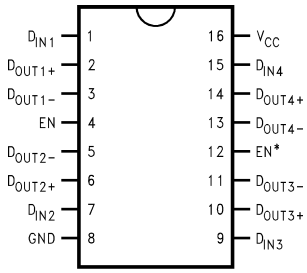
The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns typical differential skew
- 0.4 ns maximum differential skew
- 2.0 ns maximum propagation delay
- 3.3V power supply design
- ±350 mV differential signaling
- Low power dissipation (13mW at 3.3V static)
- Interoperable with existing 5V LVDS devices
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard
- Industrial and Military operating temperature range
- Available in SOIC, TSSOP and Cerpack surface mount packaging
- Standard Microcircuit Drawing (SMD) 5962-9865201

Connection Diagram

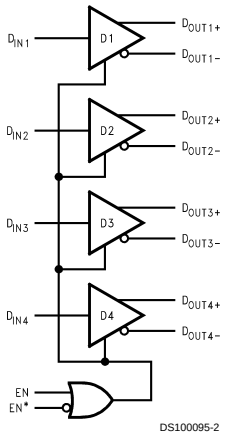
Dual-In-Line



DS100095-1

Order Number DS90LV031ATM
or DS90LV031ATMTC
or DS90LV031AW
See NS Package Number M16A or MTC16 or W16A

Functional Diagram



DS100095-2

Truth Table

DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})	−0.3V to +3.9V
Short Circuit Duration (D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation @ +25˚C	
M Package	1088 mW
MTC Package	866 mW
W Package	845 mW
Derate M Package	8.5 mW/˚C above +25˚C
Derate MTC Package	6.9 mW/˚C above +25˚C
Derate W Package	6.8 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating (Note 10)	
(HBM, 1.5 kΩ, 100 pF)	≥ 6 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)				
Industrial	−40	+25	+85	˚C
Military	-55	+25	+125	˚C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3, 4)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	D_{OUT-} D_{OUT+}	250	350	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High				1.38	1.6	V
V_{OL}	Output Voltage Low			0.90	1.03		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_{IH}	Input Current	V_{IN} = V_{CC} or 2.5V		−10	±1	+10	µA
I_{IL}	Input Current	V_{IN} = GND or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	ENABLED, (Note 11) D_{IN} = V_{CC}, D_{OUT+} = 0V or D_{IN} = GND, D_{OUT-} = 0V	D_{OUT-} D_{OUT+}		−6.0	−9.0	mA
I_{OSD}	Differential Output Short Circuit Current	ENABLED, V_{OD} = 0V (Note 11)			−6.0	−9.0	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0V or 3.6V, V_{CC} = 0V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		5.0	8.0	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels, D_{IN} = V_{CC} or GND (all inputs)			23	30	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.6	6.0	mA

Switching Characteristics - Industrial

V_{CC} = +3.3V ±10%, T_A = −40˚C to +85˚C (Notes 3, 9, 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	0.8	1.18	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.8	1.25	2.0	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 5)		0	0.07	0.4	ns
t_{SKD2}	Channel-to-Channel Skew (Note 6)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (Note 7)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 8)		0		1.2	ns
t_{TLH}	Rise Time			0.38	1.5	ns
t_{THL}	Fall Time			0.40	1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (*Figure 4* and *Figure 5*)			5	ns
t_{PLZ}	Disable Time Low to Z				5	ns
t_{PZH}	Enable Time Z to High				7	ns
t_{PZL}	Enable Time Z to Low				7	ns
f_{MAX}	Maximum Operating Frequency (Note 14)		200	250		MHz

Switching Characteristics - Military

V_{CC} = +3.3V ±10%, T_A = −55˚C to +125˚C (Notes 9, 12)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	0.8	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.8	2.0	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 5)		0	0.4	ns
t_{SKD2}	Channel-to-Channel Skew (Note 6)		0	0.5	ns
t_{SKD3}	Differential Part to Part Skew (Note 7)		0	1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 8)		0	1.2	ns
t_{TLH}	Rise Time			1.5	ns
t_{THL}	Fall Time			1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (*Figure 4* and *Figure 5*)		5	ns
t_{PLZ}	Disable Time Low to Z			5	ns
t_{PZH}	Enable Time Z to High			7	ns
t_{PZL}	Enable Time Z to Low			7	ns
f_{MAX}	Maximum Operating Frequency (Note 14)		200		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: V_{CC} = +3.3V, T_A = +25˚C.

Note 4: The DS90LV031A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90Ω to 110Ω)

Note 5: t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 6: t_{SKD2} is the Differential Channel-to-Channel Skew of any event on the same device.

Note 7: t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5˚C of each other within the operating temperature range.

Note 8: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

Note 9: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, $t_r \le 1$ ns, and $t_f \le 1$ ns.

Note 10: ESD Ratings:

HBM (1.5 kΩ, 100 pF) ≥ 6 kV

Note 11: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 12: C_L includes probe and jig capacitance.

Note 13: All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.

Note 14: f_{MAX} generator input conditions: $t_r = t_f < 1$ns, (0% to 100%), 50% duty cycle, 0V to 3V. Output Criteria: duty cycle = 45%/55%, VOD > 250mV, all channels switching.

Parameter Measurement Information

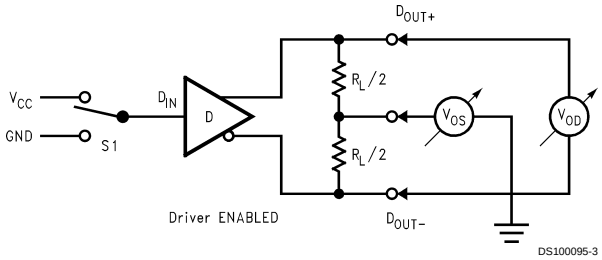


FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

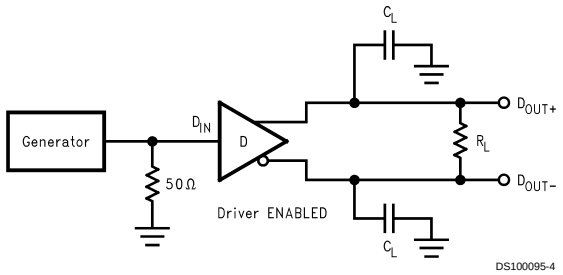


FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

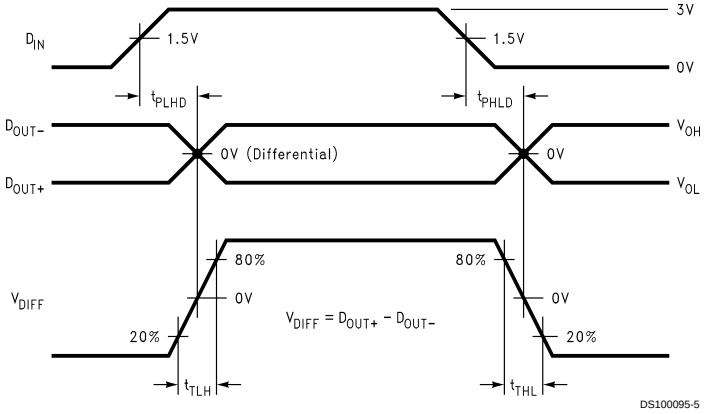


FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

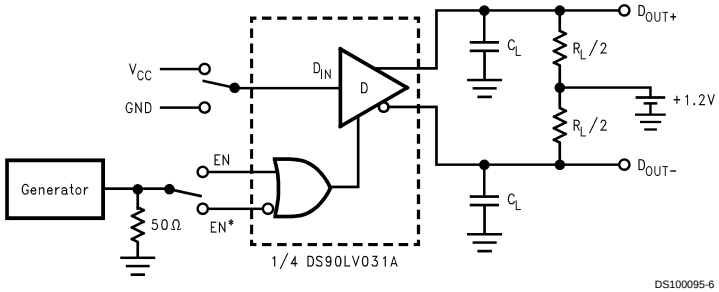


FIGURE 4. Driver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)

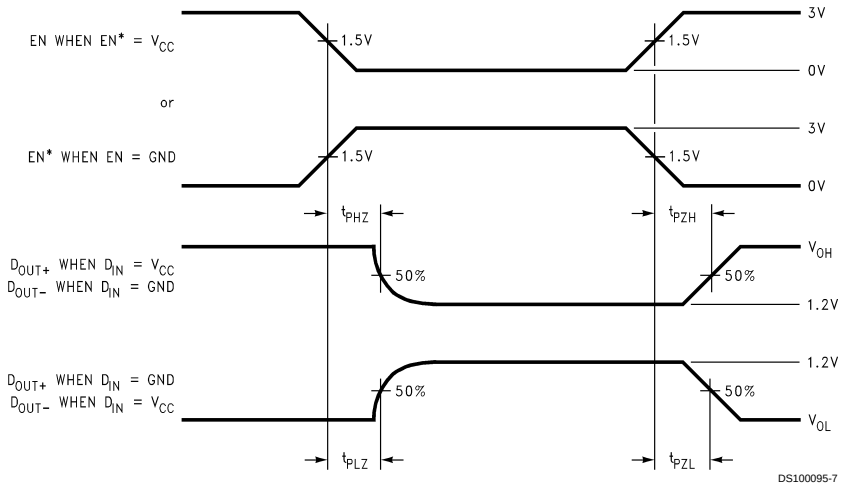


FIGURE 5. Driver TRI-STATE Delay Waveform

Typical Application

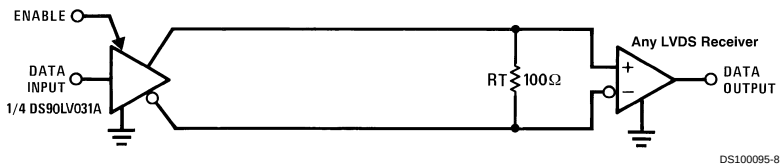


FIGURE 6. Point-to-Point Application

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-001), AN808, AN1035, AN977, AN971, AN916, AN805, AN903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 6*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV031A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 6*. AC or unterminated configurations are not allowed. The 3.5 mA loop current will develop a differential voltage of 350 mV across the 100Ω termination resistor which the receiver detects with a 250 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV – 100 mV = 250 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 7*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

Applications Information (Continued)

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90LV031A is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver and is a step down replacement for the 5V DS90C031 Quad Driver.

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations:

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces:

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be $<$ 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90˚ turns (these cause impedance discontinuities). Use arcs or 45˚ bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination:

Use a resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be $<$ 10mm (12mm MAX).

Probing LVDS Transmission Lines:

Always use high impedance ($>$ 100kΩ), low capacitance ($<$ 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments:

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver. For cable distances $<$ 0.5M, most cables can be made to work effectively. For distances 0.5M $\leq$ d $\leq$ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV032A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.

Applications Information (Continued)

3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

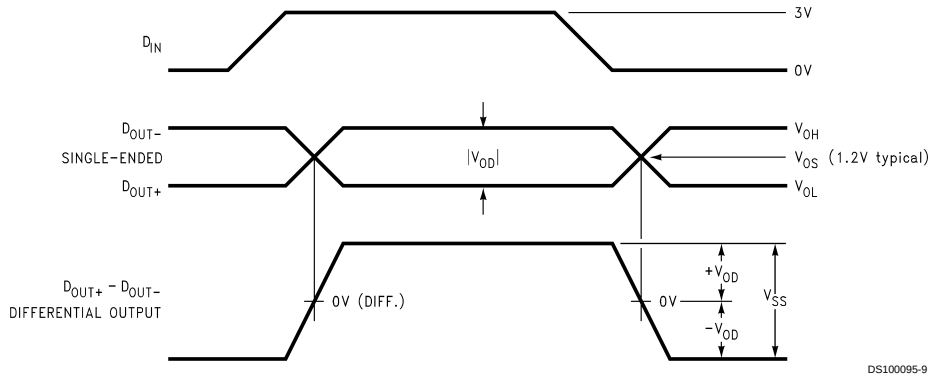


FIGURE 7. Driver Output Levels

Pin Descriptions

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M16A	DS90LV031ATM
−40˚C to +85˚C	TSSOP/MTC16	DS90LV031ATMTC
-55˚C to +125˚C	Cerpack/W16A	DS90LV031AW-QML

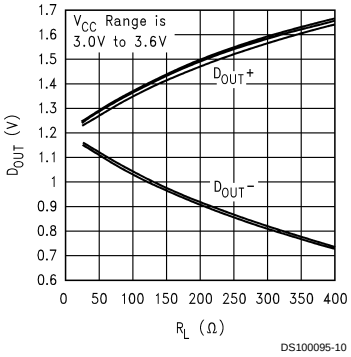


FIGURE 8. Typical DS90LV031A, D_{OUT} (single ended) vs R_L, T_A = 25˚C

Applications Information (Continued)

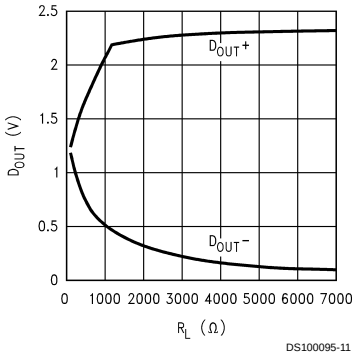
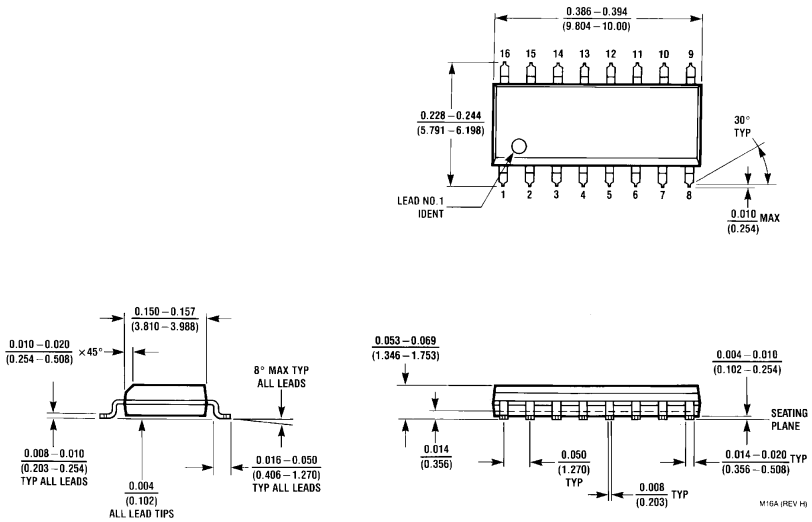


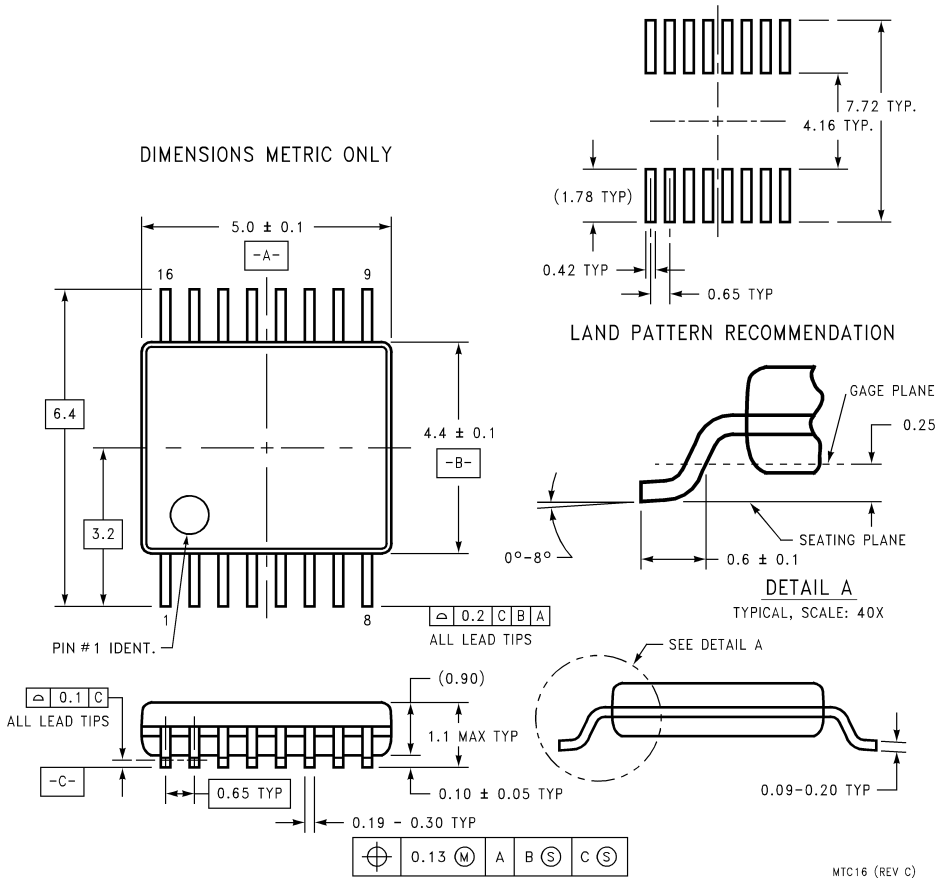
FIGURE 9. Typical DS90LV031A, D_{OUT} vs R_L, V_{CC} = 3.3V, T_A = 25°C

Physical Dimensions inches (millimeters) unless otherwise noted



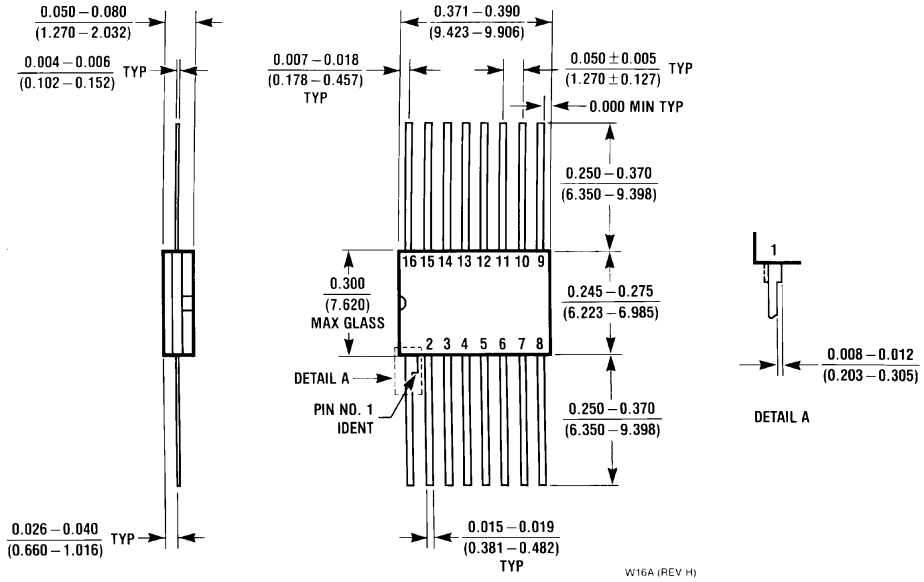
16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV031ATM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.100" Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV031ATMTC
NS Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Cerpack
Order Number DS90LV031AW-QML
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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