MN3101

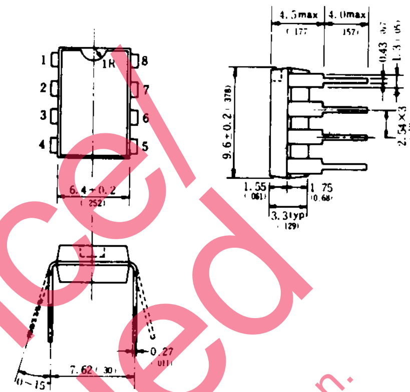
CLOCK GENERATOR/DRIVER CMOS LSI FOR BBD

■ Description

The MN3101 is a CMOS LSI generating two phase clock signal of low output impedance to drive MN3000 series BBD. Built-in V_{GG} power supply circuit for the MN3000 series BBD* provides most suitable V_{GG} voltage for the BBD when the MN3101 is used with the same power source as BBD. Oscillation is abled by external resistors and capacitors, and also oscillation drive is possible by the separate excitation oscillation.
Clock signal frequency is 1/2 of oscillation frequency.

* MN3000 series BBDs
MN3001, MN3002, MN3003, MN3004, MN3005, MN3006 MN3007, MN3008, MN3009, MN3010, MN3011, MN3012.
Note) Clock signal generator is built-in the MN3003 and MN3012.

Unit: mm (inch)



8-Lead Dual-In-Line Plastic Package

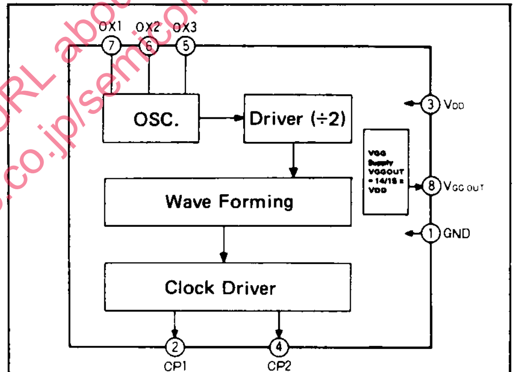
■ Features

- BBD direct driving capability of up to two MN3005s (equivalent to 8192-stages).
- Self and separate oscillations.
- Two phase clock output (Duty: 1/2).
- V_{GG} voltage generator is built-in for the BBD.
- Single power supply: −8 ~ −16V.
- 8-Lead Dual-In-Line Plastic Package.

■ Applications

- BBD clock generator/driver.

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Drain Supply Voltage	V_{DD}	−18～+0.3	V	GND=0V
Input Terminal Voltage	V_I	V_{DD}−0.3～+0.3	V	GND=0V
Output Terminal Voltage	V_O	V_{DD}−0.3～+0.3	V	GND=0V
Power Dissipation	P_D	200	mW	
Operating Ambient Temperature	Topr	−10～+70	℃	
Storage Temperature	Tstg	−30～+125	℃	

■ Operating Condition (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	GND= 0 V	−8	−15	−16	V

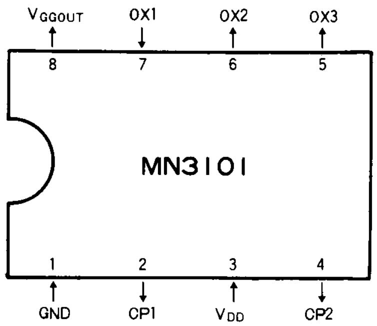
■ Electrical Characteristics (Ta = 25°C, V_{DD} = −15V, GND = 0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input drain current	I_{DD}	No loard		3		mA
Total Power Dissipation	P_{tot}	Clock output 40kHz		45		mW
OX1 Input Terminal						
Voltage "H" Level	V_{IH}		0		−1	V
Voltage "L" Level	V_{IL}		V_{DD}+1		V_{DD}	V
Input Leakage Current	I_{LK}	V_I=0～−15V			30	μA
OX2 Output Terminal						
Output Current "H" Level	I_{OH1}	V_O=−1 V	0.6			mA
Output Current "L" Level	I_{OL1}	V_O=−14V	0.5			mA
Output Leakage Current	I_{LOL1}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH1}	V_O=GND			30	μA
OX3 Output Temrinal						
Output Current "H" Level	I_{OH2}	V_O=−1 V	1.5			mA
Output Current "L" Level	I_{OL2}	V_O=−14V	2			mA
Output Leakage Current	I_{LOL2}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH2}	V_O=GND			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	I_{OH3}	V_O=−1V	10			mA
Output Current "L" Level	I_{OL3}	V_O=−14V	10			mA
Output Leakage Current	I_{LOL3}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH3}	V_O=GND			30	μA
$V_{GG\ OUT}$ Output Terminal (*)						
Output Voltage	$V_{GG\ OUT}$			−14		V

(*) This terminal generates V_{GG} voltage exclusively applied for BBD manufactured by Matsushita Electronics Corporation, therefore, some times it might not be applicable for the device other than the V_{GG} voltage of MEC's BBD. $V_{GG\ OUT}$ changes by following formula depending on the value of V_{DD}.

$$V_{GG\ OUT} \fallingdotseq \frac{14}{15} V_{DD}$$

Terminal Assignments

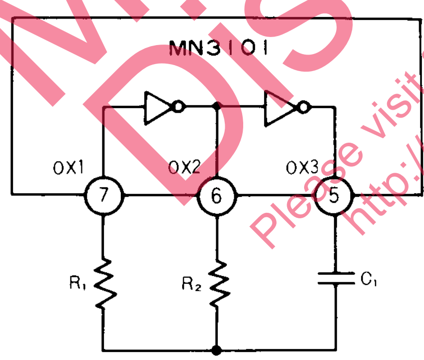


(Top View)

Terminal Description

Terminal No.	Symbol	I/O	Terminal Name	Description	
1	GND	Power supply	Ground	Connected to GND of the circuit.	
2	CP1	0	Clock output 1	This terminal outputs clock signal that is a revers phase of CP2 with Duty 1/2, 1/2 frequency of oscillation frequency	
3	V_{DD}	Power supply	V_{DD} apply	−15V is applied.	
4	CP 2	0	Clock output 2	This terminal outputs clock signal that is a reverse phase of CP 1.	
5	OX 3	0	C and R is connected.	C, R are connected in case of selfoscillation. (Refer to oscillation circuit).	In case of separate excitation, OX3 and OX2 are opened and OX1 is set to OSC input.
6	OX 2	0			
7	OX 1	1			
8	$V_{GG\ OUT}$	0	V_{GG} voltage output.	−14V is output. (V_{DD} = −15V) $V_{GG\ OUT}$ = 14/15V_{DD}.	

Example of Oscillation Generation Circuit

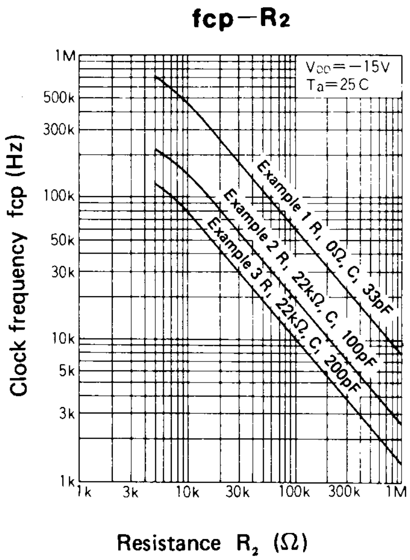


Oscillation circuit of the MN3101 is composed of 2-stage inverter and oscillation frequency is defined by the time constant of C1 and R2 shown left.

Following is an example of C1, R1 and R2.
Figure 1 shows f_{cp}* −R2 characteristics.

Example \ Constant	R_1 (Ω)	R_2 (Ω)	C_1 (pF)	f_{osc}** (kHz)	f_{CP}* (kHz)
Example ①	0	5 k~1 M	33	15~1500	7.5~750
Example ②	22k	5 k~1 M	100	5.2~440	2.6~220
Example ③	22k	5 k~1 M	200	1.4~280	0.7~140

* Clock output frequency of CP1 or CP2 terminals.
** Oscillation frequency of OX1, OX2 and OX3.



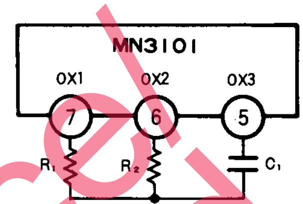


Figure 1 Example of characteristics of clock oscillation frequency.

■ The maximum clock frequency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption.

The permissible dissipation for this LSI is = P_D = 200mW.

If the clock frequency on the load capacitance is increased, the power consumption will be increased. (Refer to Figure 2.)

Accordingly, in order to utilize the MN3101 with dissipation less than the permissible value, it is necessary to select adequate values for the clock frequency and load capacitance.

Figure 3 shows an example of the dependence of the maximum clock frequency on the load capacitance in P_D = 150mW.

By connecting a resistance to the clock output terminal, it is made possible to increase the value of the maximum clock frequency without increasing dissipation. (Refer to Figures 2 and 3.)

It is because the dissipation on the LSI side is lessened, as a part of the power consumption required for driving the load capacitance is consumed by the series resistance.

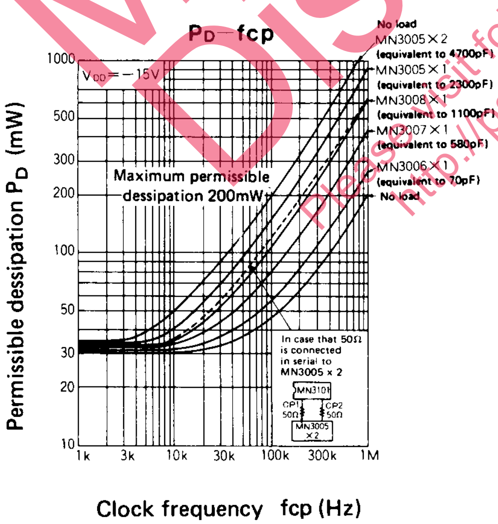


Figure 2 Example of the dependence of power consumption on the clock frequency.

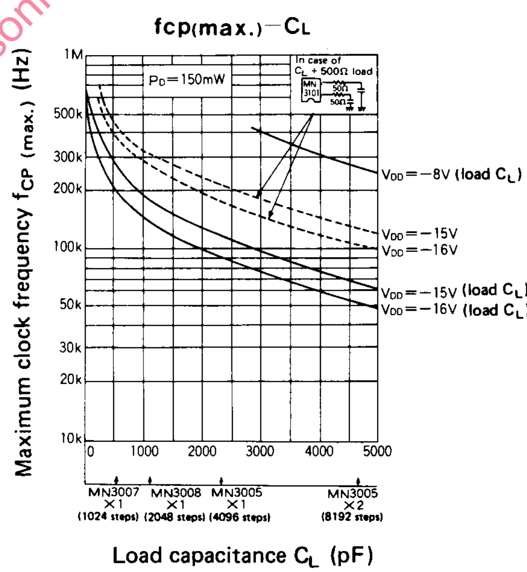


Figure 3 Example of the load capacitance characteristic of the maximum clock frequency in the power consumption of 150mW.

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