MN3005

4096-STAGE LONG DELAY BBD

■ General description

The MN3005 is a world's first 4096-stage long delay BBD, 8 times longer than 512-stage BBD manufactured by using a P-channel low noise silicon gate process.

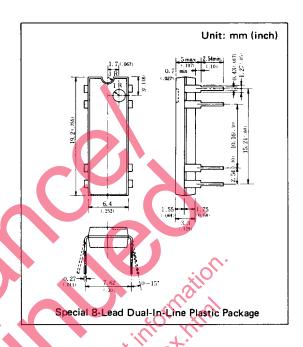
Long signal delay time 205ms can be obtained at clock frequency 10KHz. S/N is 75dB. S/N has been improved by more than 20dB in comparting with 8-connected 512-stage BBD's. The MN3005 is suitably used for reverberation and echo effects in electronic musical instruments such as electronic organ, guitar amplifier and music synthesizer which need long delay time.

Features

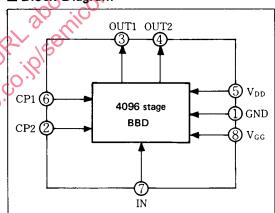
- 1 chip 4096 stage and wide range of variable delay times: 20.48 ~ 204.8ms.
- High S/N in spite of multi-stage and wide dynamic range; $S/N \simeq 75dB \text{ typ.}$
- No insertion loss since the loss occuring in the signal transfer is corrected by the MOS capacity of input and output. $L_i = 0dB$.
- High integration and high reliability by using P channel low noise silicon gate process.
- Special 8 lead dual-in-line plastic package.

Applications

- Reverberation and echo effects in echo microphone and stereo equipment.
- Chorus effect in electronic musical instruments.
- Please visit to loan asonic Telephone time compression and delay line for voice communication systems, etc.



Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V _{DD} , V _{GG}	-15, V _{DD} +1	V
Signal Delay Time	t _D	20.48~204.8	ms
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V _{DD} , V _{GG} , V _{CP} , V _I	−18~+0.3	٧
Output Voltage	Vo	−18~+0.3	V
Operating Temperature	Topr	−20~+60	°C
Storage Temperature	Tstg	<i>−</i> 55∼+125	c

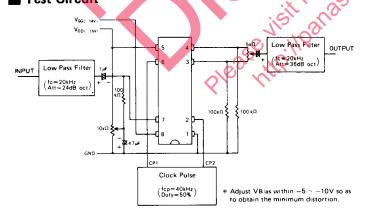
Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Drain Supply Voltage	V _{DD}		-14	—15	-16	V
Gate Supply Voltage	V _{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V _{CPH}		0		-1	V
Clock Voltage "L" Level	V _{CPL}			V _{DD}		V
Clock Input Capacitance	C _{CP}			A	2800	рF
Clock Frequency	f _{CP}		10		100	kHz
Clock Pulse Width *2	t _{cpw}	Test Circuit			0.5T*2	
Clock Rise Time *2	t _{cpr}	Test Circuit			500	ns
Clock Fall Time *2	t _{cpf}	Test Circuit			500	ns
Clock Cross Point	V _X		0	3	3	٧
Input DC Bias Voltage	V _{Bias}		- 5	W.C	_10	٧

■ Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 100kΩ$)

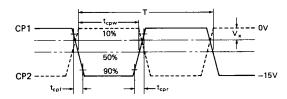
Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Signal Delay Time	t _D		20.48		204.8	ms
Input Signal Frequency	fi	$f_{ep} = 40 \text{kHz}$, $V_i = 1.0 \text{Vrms}$, Output Attenuation $\leq 3 \text{dB}$ (0dB at $f_i = 1 \text{kHz}$)	01/10			kHz
Input Signal Swing	۷i	f_{CP} =40kHz, $f_i = 1$ kHz, THD=2.5%	1.0			Vrms
Insertion Loss	Li	f_{CP} =40kHz, $f_i = 1$ kHz, $V_i = 1.0$ Vrms	-4	0	4	dB
Total Harmonic Distortion	THD	f_{CP} =40kHz, $f_i = 1$ kHz, $V_i = 0.78$ Vrms		1	2.5	%
Noise Voltage	V _{no}	f _{cp} = 100kHz Weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio	S/N	W. C.		75		dB





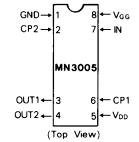
*1 Clock Pulse Waveforms

-0 01'T1③

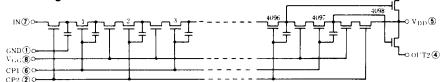


*2 T = 1/fcp

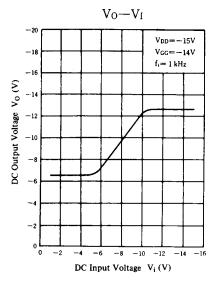
■ Terminal Assignments

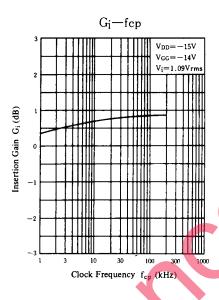


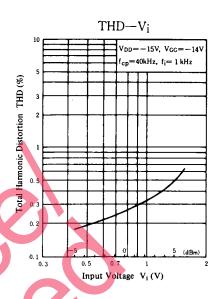
■ Circuit Diagram

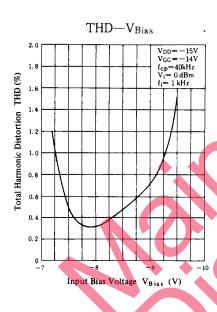


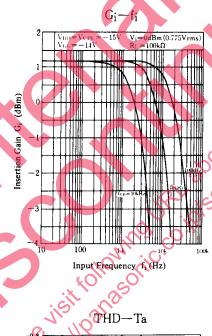
Typical Electrical Characteristic Curves

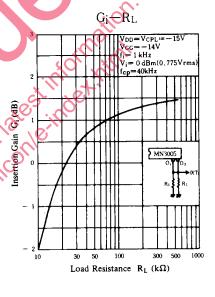




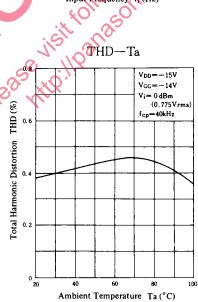






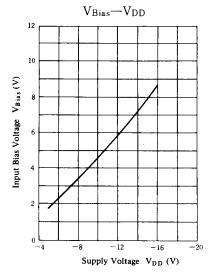


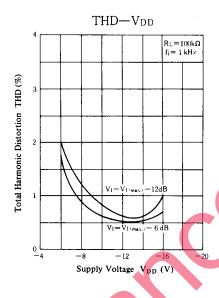


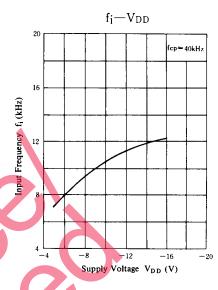


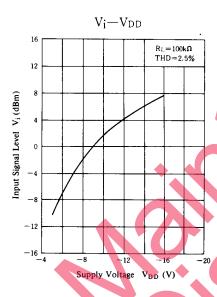
MN3000 Series MN3005

■ Supply Voltage Characteristics

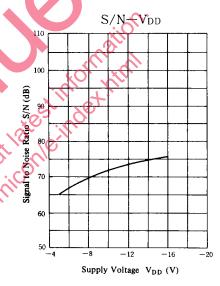






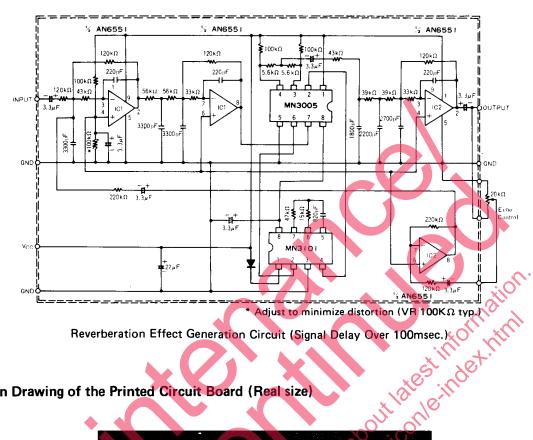






MN3000 Series MN3005

■ Application Circuit



Pattern Drawing of the Printed Circuit Board (Real size)



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