



Integrated Device Technology, Inc.

FAST CMOS 12-BIT TRI-PORT BUS EXCHANGER

IDT54/74FCT16260AT/CT/ET
IDT54/74FCT162260AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
 - Extended commercial range of -40°C to +85°C
 - VCC = 5V $\pm 10\%$
- **Features for FCT16260AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C
- **Features for FCT162260AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

DESCRIPTION:

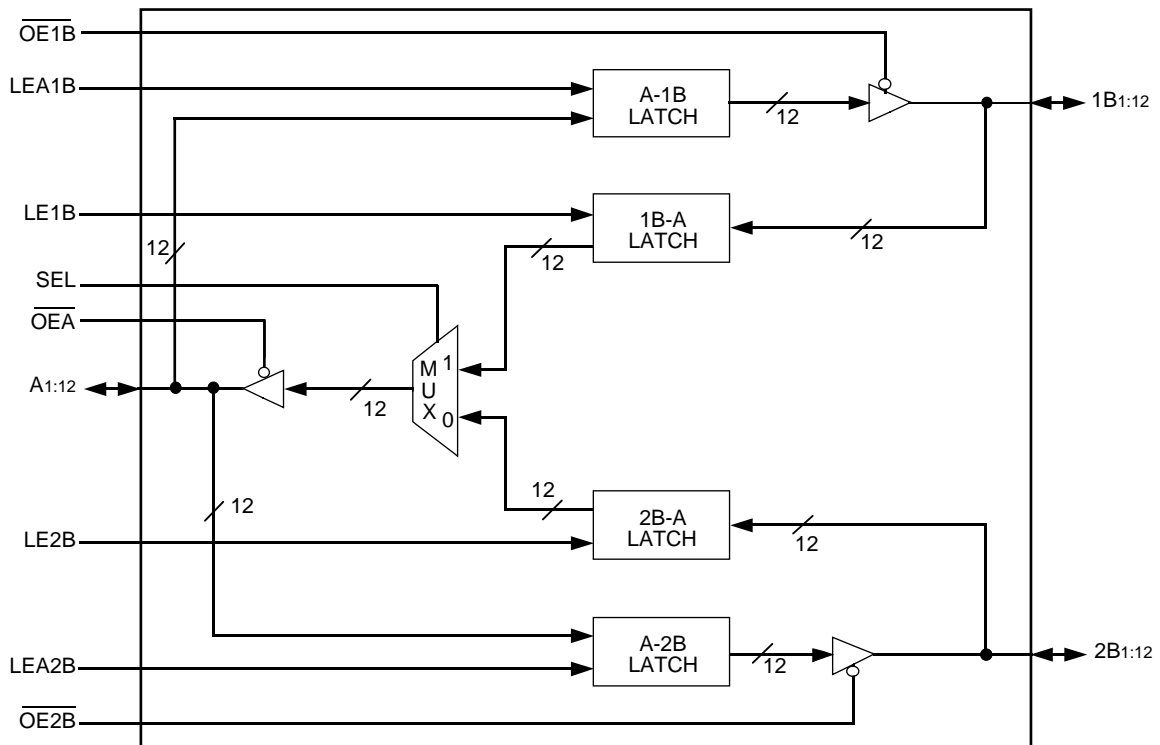
The FCT16260AT/CT/ET and the FCT162260AT/CT/ET Tri-Port Bus Exchangers are high-speed 12-bit latched bus multiplexers/transceivers for use in high-speed microprocessor applications. These Bus Exchangers support memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

The Tri-Port Bus Exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is HIGH, the latch is transparent. When a latch-enable input is LOW, the data at the input is latched and remains latched until the latch enable input is returned HIGH. Independent output enables ($\overline{\text{OE1B}}$ and $\overline{\text{OE2B}}$) allow reading from one port while writing to the other port.

The FCT16260AT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162260AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times - reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



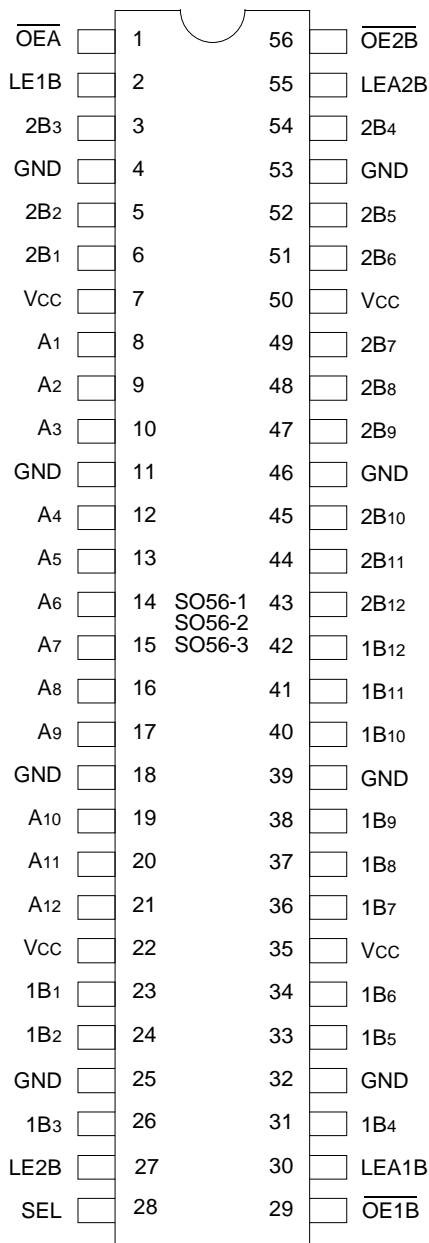
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

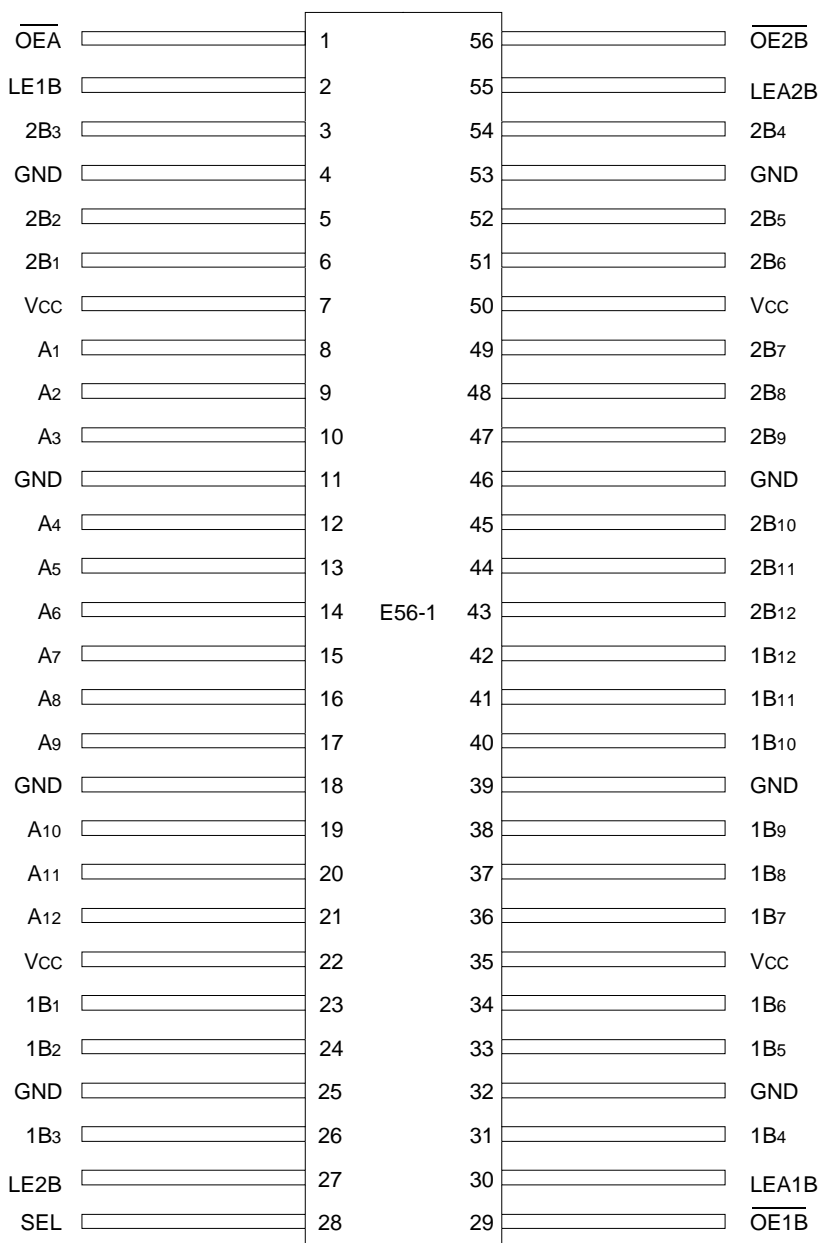
AUGUST 1996

PIN CONFIGURATIONS



**SSOP/
 TSSOP/TVSOP
 TOP VIEW**

3032 drw 02



**CERPACK
 TOP VIEW**

3032 drw 03

PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.
1B(1:12)	I/O	Bidirectional Data Port 1B. Connected to the even path or even bank of memory.
2B(1:12)	I/O	Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory.
LEA1B	I	Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B.
LEA2B	I	Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-Port is latched on the HIGH to LOW transition of LEA2B.
LE1B	I	Latch Enable Input for the 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B.
LE2B	I	Latch Enable Input for the 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B.
SEL	I	1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port.
$\overline{OE}A$	I	Output Enable for A Port (Active LOW).
$\overline{OE}1B$	I	Output Enable for 1B Port (Active LOW).
$\overline{OE}2B$	I	Output Enable for 2B Port (Active LOW).

3032 tbl 01

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

3032 tbl 02

- NOTES:**
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 - All device terminals except FCT162XXXT Output and I/O terminals.
 - Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

3032 tbl 03

- NOTE:**
- This parameter is measured at characterization but not tested.

FUNCTION TABLES⁽²⁾

Inputs						Output
1B	2B	SEL	LE1B	LE2B	$\overline{OE}A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ⁽¹⁾
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ⁽¹⁾
X	X	X	X	X	H	Z

3032 tbl 04

Inputs					Outputs	
A	LEA1B	LEA2B	$\overline{OE}1B$	$\overline{OE}2B$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	B ⁽¹⁾
L	H	L	L	L	L	B ⁽¹⁾
H	L	H	L	L	B ⁽¹⁾	H
L	L	H	L	L	B ⁽¹⁾	L
X	L	L	L	L	B ⁽¹⁾	B ⁽¹⁾
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

NOTES:

3032 tbl 05

- Output level before the indicated steady-state input conditions were established.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

3032 tbl 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT16260T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}^{(4)}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

3032 tbl 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT162260T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	1.5	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open One Output Port Enabled $LE_{xx} = V_{CC}$ One Input Bit Toggling One Output Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	60	100 $\mu A/$ MHz	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle One Output Port Enabled $LE_{xx} = V_{CC}$ One Input Bit Toggling One Output Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	1.5	mA
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle One Output Port Enabled $LE_{xx} = V_{CC}$ Twelve Input Bits Toggling Twelve Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.8	3.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	0.9	2.3	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	4.8	12.5 ⁽⁵⁾	

NOTES:

3032 tbl 09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16260AT/162260AT				FCT16260CT/162260CT				FCT16260ET/162260ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	3.6	—	—	ns
tPHL	Ax to 1Bx or Ax to 2Bx														
tPLH	Propagation Delay		1.5	5.6	1.5	5.9	1.5	5.0	1.5	5.4	1.5	3.6	—	—	ns
tPHL	1Bx to Ax or 2Bx to Ax														
tPLH	Propagation Delay		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	4.0	—	—	ns
tPHL	LExB to Ax														
tPLH	Propagation Delay		1.5	4.7	1.5	5.2	1.5	4.4	1.5	4.8	1.5	4.0	—	—	ns
tPHL	LEA1B to 1Bx or LEA2B to 2Bx														
tPLH	Propagation Delay		1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	1.5	4.0	—	—	ns
tPHL	SEL to Ax														
tPZH	Output Enable Time		1.5	5.7	1.5	6.1	1.5	5.1	1.5	5.4	1.5	4.4	—	—	ns
tPZL	OE \bar{A} to Ax, OE $\bar{1B}$ to 1Bx, or OE $\bar{2B}$ to 2Bx														
tPHZ	Output Disable Time	1.5	4.4	1.5	4.8	1.5	4.0	1.5	4.4	1.5	4.0	—	—	ns	
tPLZ	OE \bar{A} to Ax, OE $\bar{1B}$ to 1Bx, or OE $\bar{2B}$ to 2Bx														
tsu	Set-Up Time, HIGH or LOW Data to Latch	1.5	—	1.5	—	1.0	—	1.0	—	1.0	—	—	—	ns	
th	Hold Time, Latch to Data	1.0	—	1.5	—	1.0	—	1.5	—	1.0	—	—	—	ns	
tw	Pulse Width, Latch HIGH ⁽⁴⁾	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns	
tsk(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns	

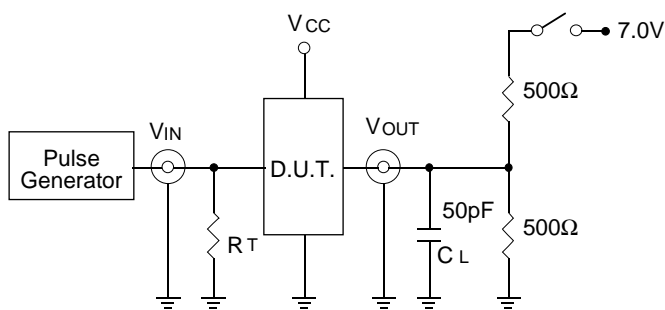
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

3032 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3032 Ink 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

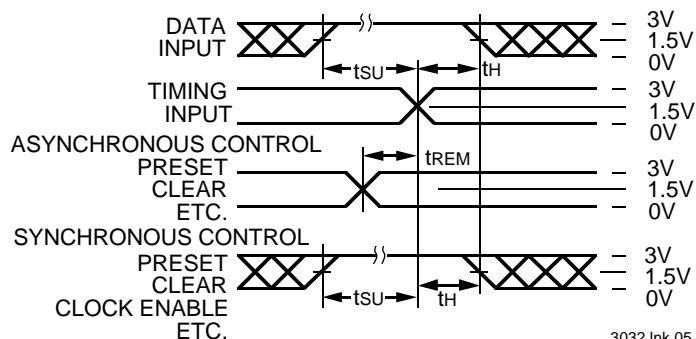
3032 Ink 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

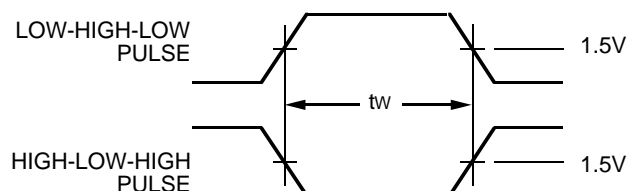
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



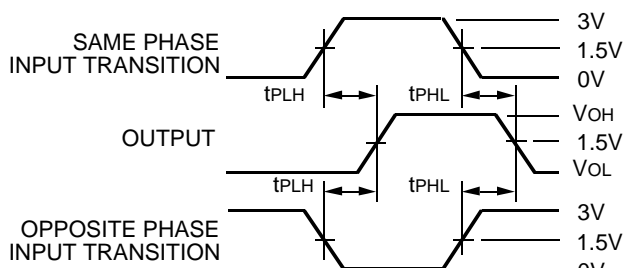
3032 Ink 05

PULSE WIDTH



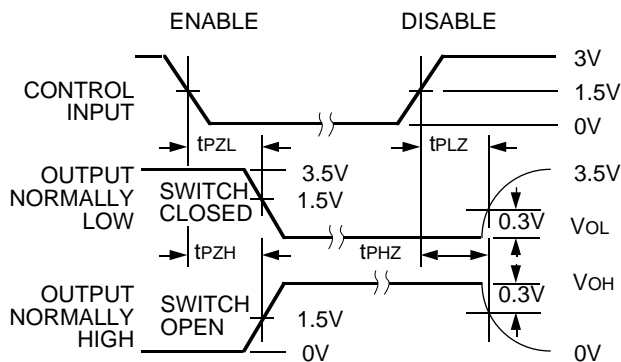
3032 Ink 06

PROPAGATION DELAY



3032 Ink 07

ENABLE AND DISABLE TIMES

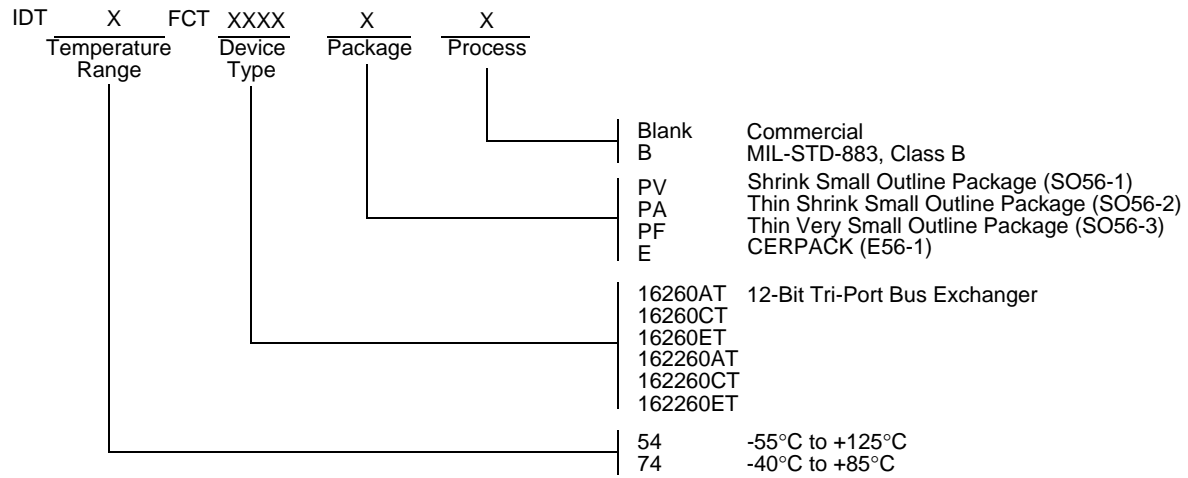


3032 Ink 08

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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