

# MN3004

## 512-STAGE LOW NOISE BBD

### General Description

The MN3004 is a 512-stage high performance low noise BBD that provides a 85dB of signal to noise ratio (S/N) by increasing a capacity of capacitors with the same chip area, which is enabled by the improvement of silicon materials and process. There are many features for this device such as low insertion loss and no back gate bias voltage  $V_{BB}$ , etc.

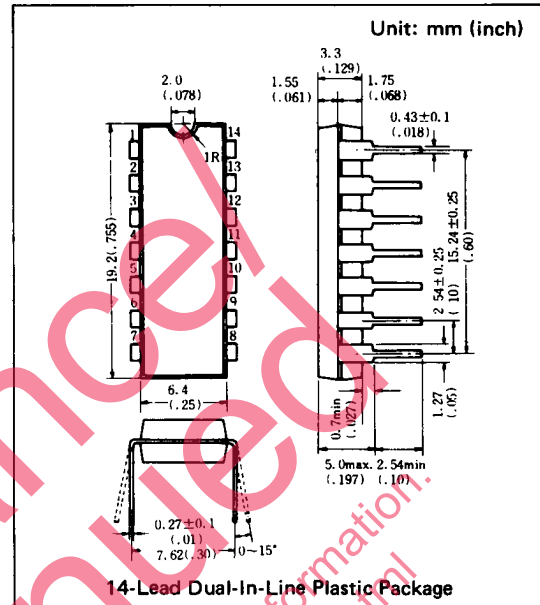
The MN3004 can delay analog signal of the audio band in the range of 2.56ms ~ 25.6ms by adjusting a clock frequency.

### Features

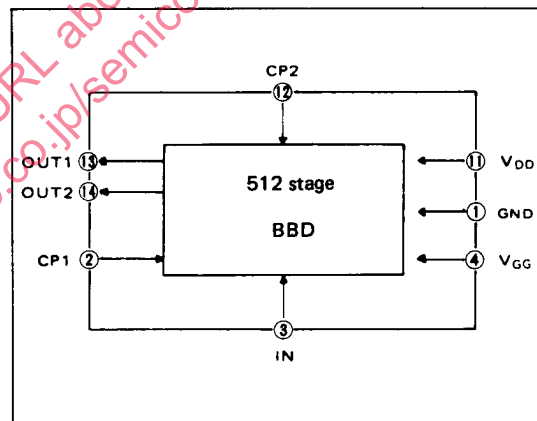
- Variable delay of audio signal: 2.56ms ~ 25.6ms
- Clock component cancellation capability.
- Low insertion loss:  $L_i = 1/5\text{dB}$  typ.
- Wide dynamic range:  $S/N \approx 85\text{dB}$  typ.
- Wide frequency response:  $f_i \leq 0.3 \times f_{cp}$
- Clock frequency range: 10 ~ 100KHz
- Low noise:  $V_{NO} = 0.21\text{mVrms}$  max.
- Low distortion: THD = 0.4% typ.

### Applications

- Variable playback speed of tape recorder.
- Reverberation and echo effects of audio equipments such as stereo.
- Tremolo, vibrato and chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems.
- Others.



### Block Diagram



### Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	$V_{DD}, V_{GG}$	-15, $V_{DD} + 1$	V
Signal Delay Time	$t_D$	2.56~25.6	ms
Total Harmonic Distortion	THD	0.4	%
Signal to Noise Ratio	S/N	85	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V <sub>DD</sub> , V <sub>GG</sub> , V <sub>CP</sub> , V <sub>i</sub>	-18~+0.3	V
Output Voltage	V <sub>O</sub>	-18~+0.3	V
Operating Temperature	T <sub>opr</sub>	-20~+60	°C
Storage Temperature	T <sub>stg</sub>	-55~+125	°C

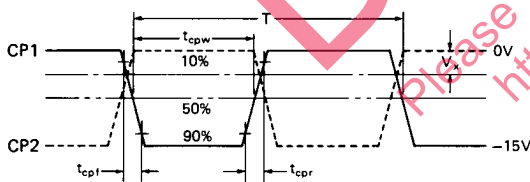
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V <sub>DD</sub>		-14	-15	-16	V
Gate Supply Voltage	V <sub>GG</sub>			V <sub>DD</sub> + 1		V
Clock Voltage "H" Level	V <sub>CPH</sub>		0		-1	V
Clock Voltage "L" Level	V <sub>OPL</sub>			V <sub>DD</sub>		V
Clock Input Capacitance	C <sub>CP</sub>				350	pF
Clock Frequency	f <sub>CP</sub>		10		100	kHz
Clock Pulse Width *1	t <sub>cpw</sub>				0.5T*2	
Clock Rise Time *1	t <sub>cpr</sub>				500	ns
Clock Fall Time *1	t <sub>cpf</sub>				500	ns
Clock Cross Point	V <sub>X</sub>		0		-3	V
Input DC Bias	V <sub>Bias</sub>		-5		-10	V

■ Electrical Characteristics (Ta = 25°C, V<sub>DD</sub> = V<sub>CPL</sub> = -5V, V<sub>CPH</sub> = 0V, V<sub>GG</sub> = -14V, R<sub>L</sub> = KΩ)

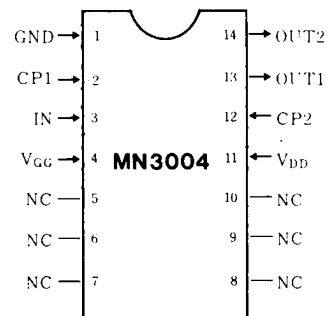
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t <sub>d</sub>		2.56		25.6	ms
Input Signal Frequency	f <sub>i</sub>	f <sub>CP</sub> = 40kHz, V <sub>i</sub> = 1.8Vrms, 3dB down (0 dB at f <sub>i</sub> = 1kHz)	12			kHz
Input Signal Swing	V <sub>i</sub>	f <sub>CP</sub> = 40kHz, f <sub>i</sub> = 1 kHz, THD ≤ 2.5%	1.8			Vrms
Insertion Loss	L <sub>i</sub>	f <sub>CP</sub> = 40kHz, f <sub>i</sub> = 1 kHz, V <sub>i</sub> = 1.8Vrms	-4	1.5	4	dB
Total Harmonic Distortion	THD	f <sub>CP</sub> = 40kHz, f <sub>i</sub> = 1 kHz, V <sub>i</sub> = 1 Vrms		0.4	2.5	%
Noise Voltage	V <sub>no</sub>	f <sub>CP</sub> = 100kHz Weighted by "A" curve			0.21	mVrms
Signal to Noise Ratio	S/N			85		dB

\*1 Clock Pulse Waveforms



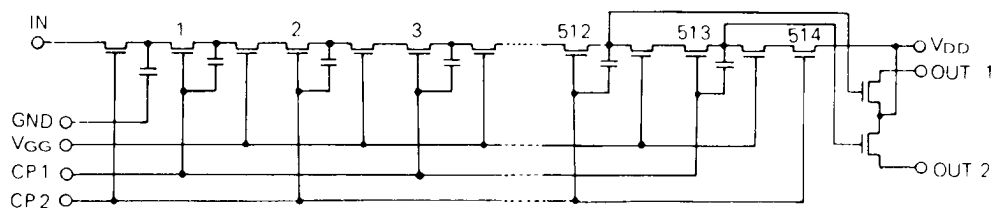
\*2 T = 1/f<sub>cp</sub> (Clock Period)

■ Terminal Assignments

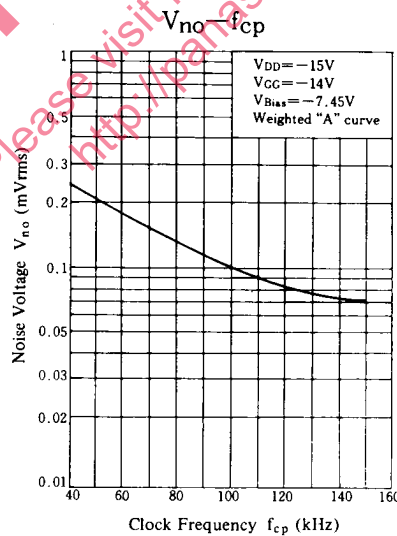
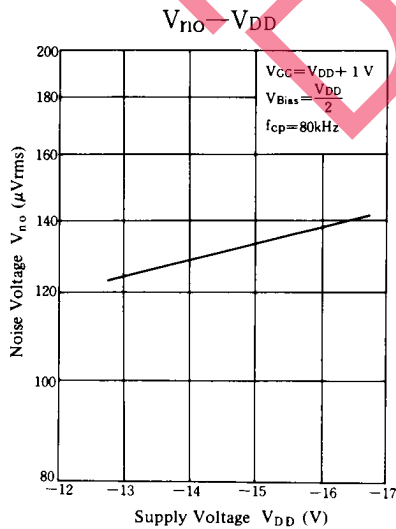
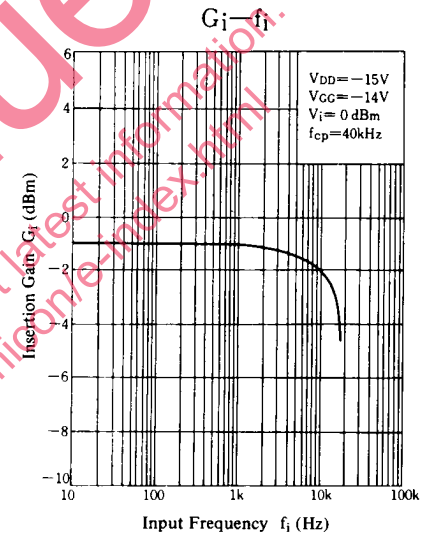
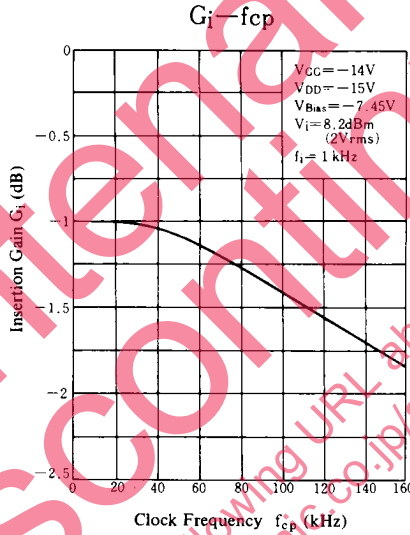
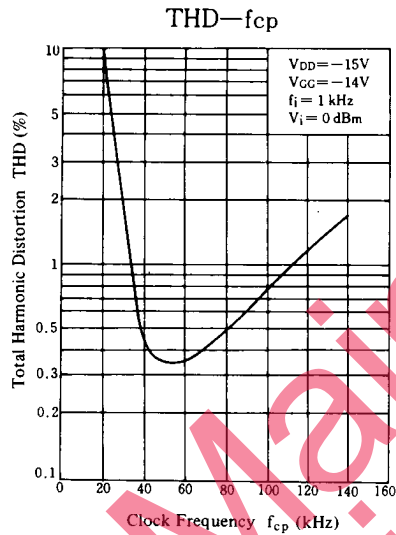
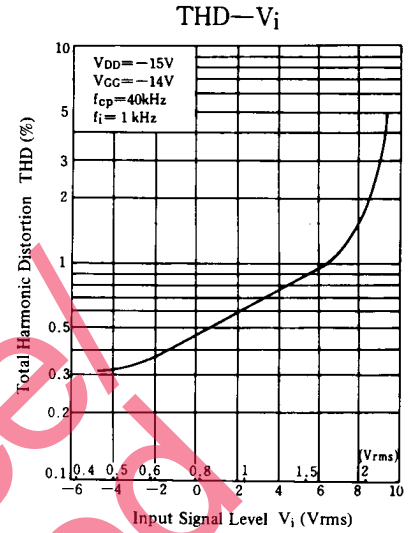
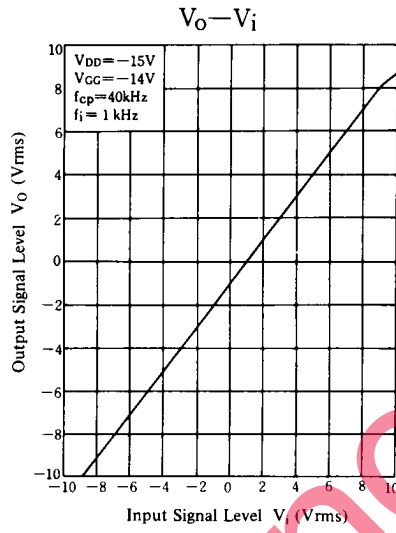
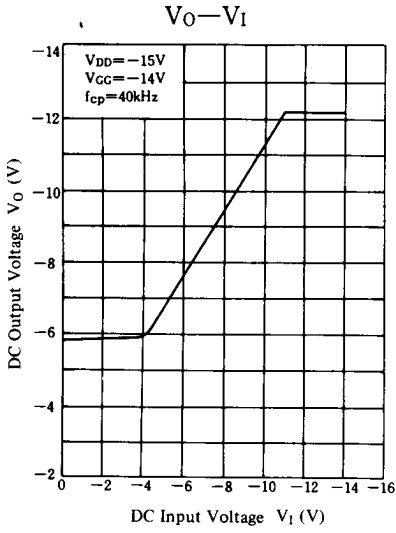


(Top View)

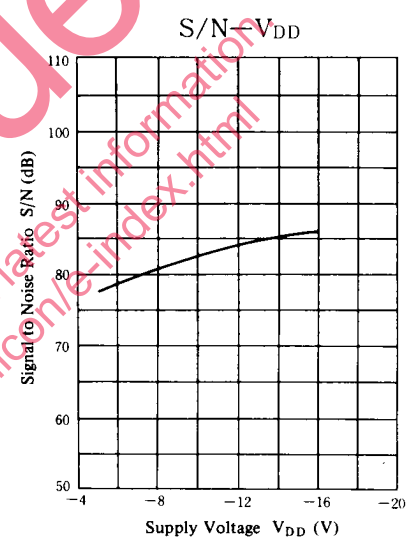
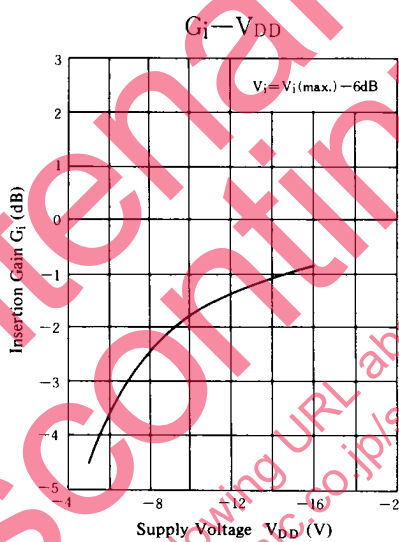
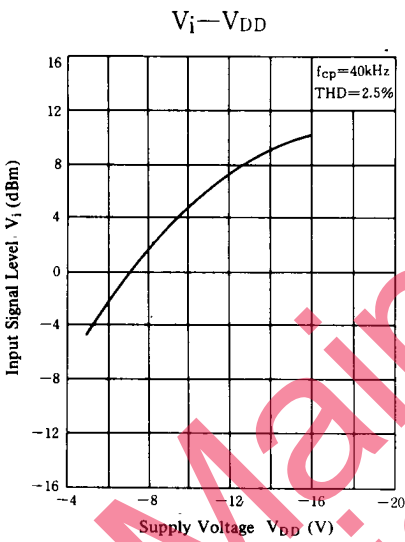
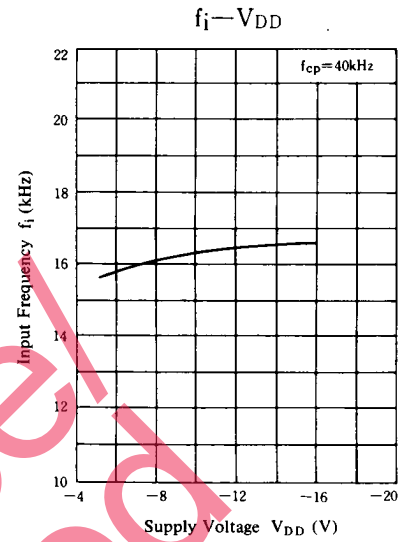
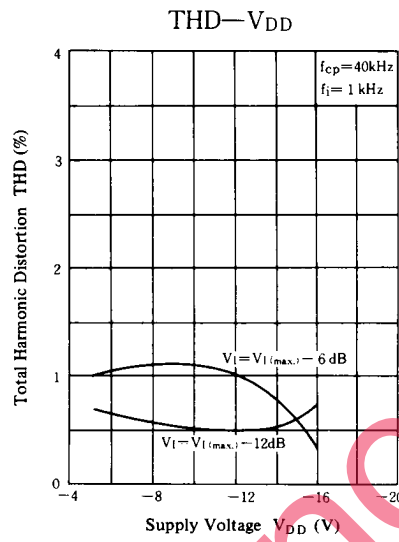
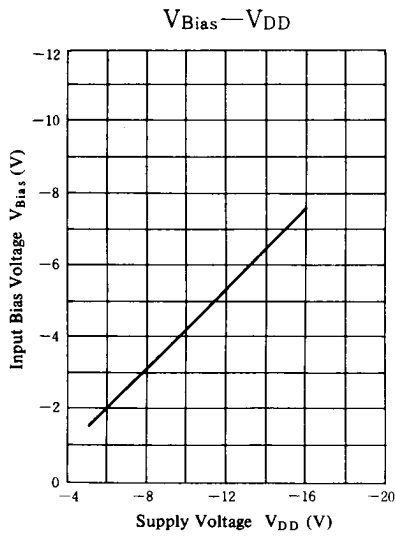
■ Circuit Diagram



Typical Electrical Characteristic Curves

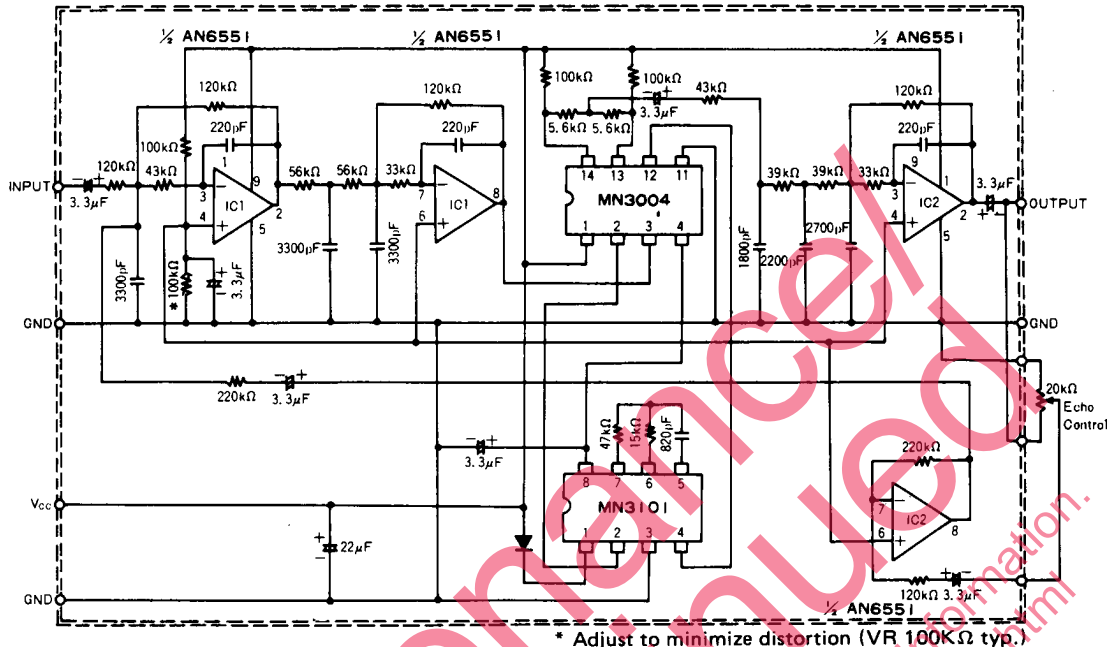


Supply Voltage Characteristics



Maintenance  
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Application Circuit



\* Adjust to minimize distortion (VR 100KΩ typ.)

Echo Effect Generation Circuit (Signal Delay Over 10msec.)

Maintentance  
 Discontinued  
 Please visit following URL about latest information.  
<http://panasonic.co.jp/semicon/e-index.html>

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